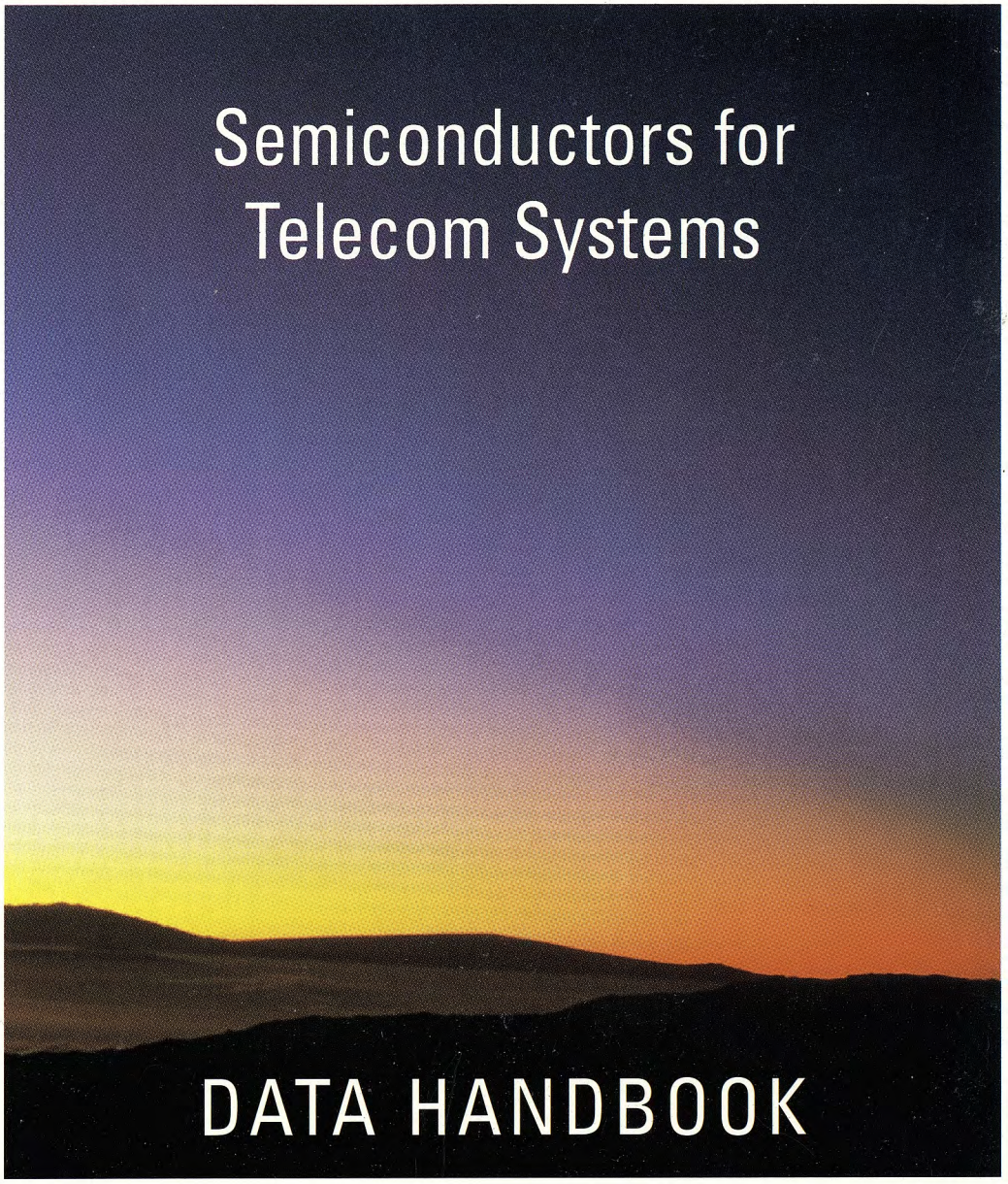
INTEGRATED CIRCUITS

Semiconductors for Telecom Systems



DATA HANDBOOK

BOOK IC03 1995

Philips Semiconductors

PHILIPS

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Semiconductors for Telecom Systems

CONTENTS

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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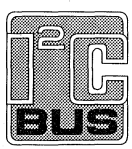
PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

SELECTION GUIDE

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LOW-VOLTAGE RF POWER TRANSISTORS

RF POWER MODULES

BATTERY MANAGEMENT

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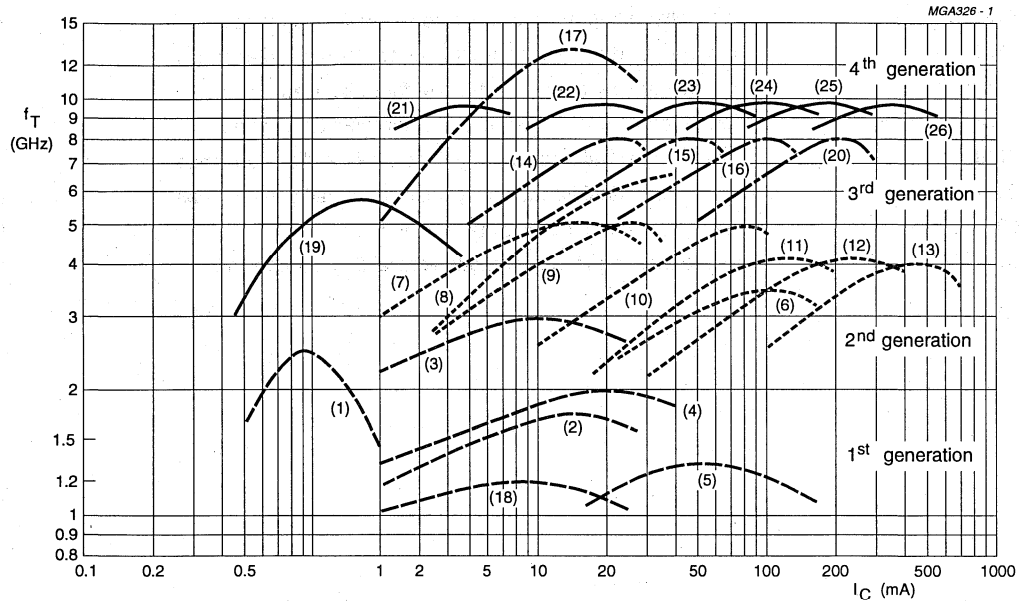
GENERAL

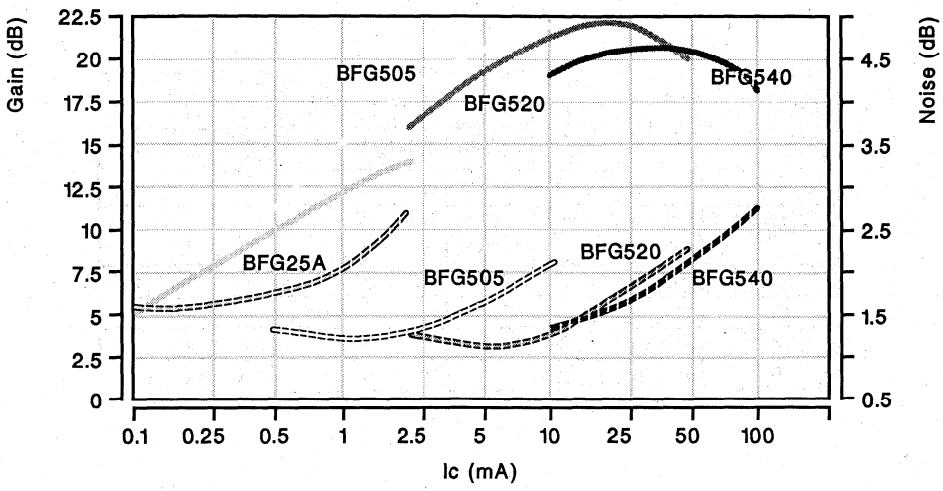
For further information, refer to Data Handbook SC08a *"RF Bipolar transistors"*, to Data Handbook SC09 *"RF Power Modules"* and to Data Handbook SC14 *"RF Wideband Transistors, Video Transistors and Modules"*.

RF WIDEBAND TRANSISTORS



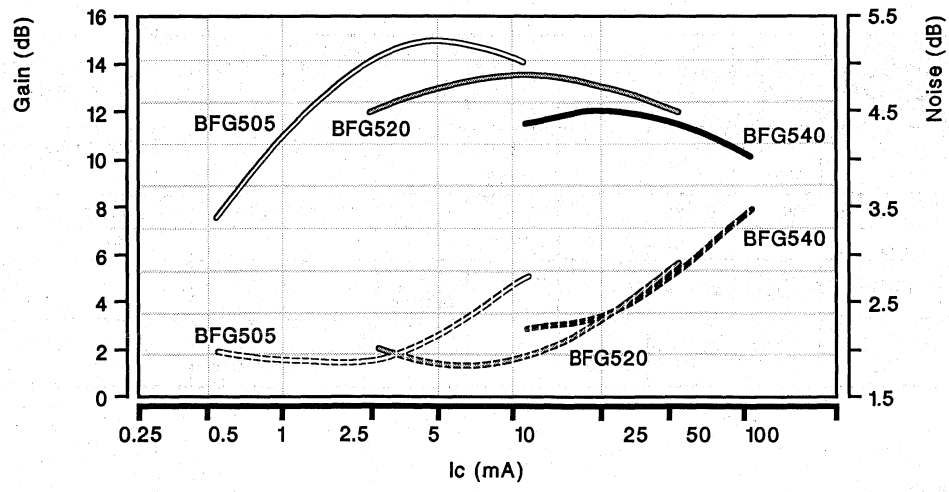
For numbers in parenthesis see Figs 4, 5, 6 and 7.

Fig.1 Transition frequency (f_T) curves as a function of collector current (I_C) for the four generations of RF bipolar transistors.



At 900 MHz.

Fig.2 Gain and noise as a function of collector current.



At 1.9 GHz.

Fig.3 Gain and noise as a function of collector current.

f_T/I_C curve	I_C (mA)	V_{CE} (V)	Surface Mount Package				
			SOT23	SOT89	SOT143	SOT223	SOT323
(1)	0.1 - 2	3 - 5	BFT25				
(18)	3 - 20	3 -20	BF547 BF747				BF547W
(2)	3 - 20	3 - 12	BFS17				BSF17W
(3)	3 - 20	3 - 12	BFS17A		BFG17A		
(4)	10 - 40	3 - 7	BFR53				
(5)	20 - 150	5 - 20		BFQ17		BFG16A	

f_T up to 3.5 GHz.
See Fig.1 for the f_T/I_C curves.

Fig.4 First generation NPN wideband transistors.

f_T/I_C curve	Polarity	I_C (mA)	V_{CE} (V)	Surface Mount package					
				SOT23	SOT89	SOT143*	SOT223	SOT323	SOT343*
(7)	NPN PNP	3 - 20	3 - 12	BFR92(A) BFT92		BFG92A		BFR92AW BFT92W	BFG92AW
(8)	NPN	5 - 30	3 - 10	BFR93(A)		BFG93A	BFG94	BFR93AW	BFG93AW
(9)	PNP	5 - 30	3 - 12	BFT93				BFT93W	
(10)	NPN PNP	20 - 80	5 - 12	BFR106	BFQ19 BFQ149		BFG97 BFG31		
(11)	NPN PNP	40 - 120	5 - 15		BFQ18A		BFG35 BFG55		

f_T up to 6 GHz.
* Also available /X and /XR versions.
See Fig.1 for the f_T/I_C curves.

Fig.5 Second generation NPN wideband transistors.

f_T/I_C curve	Surface Mount package						
	I_C (mA)	V_{CE} (V)	SOT23	SOT143*	SOT223	SOT323	SOT343*
(14)	3 - 25	2 - 8	BFQ67	BFG67		BFQ67W	BFG67W
(15)	10 - 70	2 - 8		BFG197	BFG198		
(16)	20 - 130	5 - 12			BFG135		
(17)	1 -20	2 -7		BFG33			

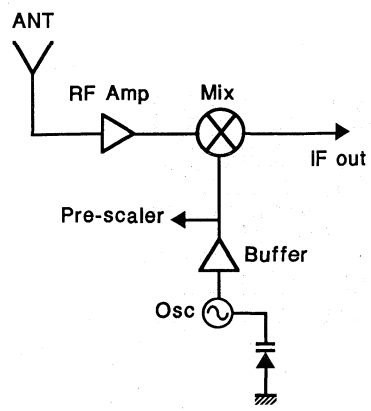
f_T up to 8 GHz.
* Also available /X and /XR versions.
See Fig.1 for the f_T/I_C curves.

Fig.6 Third generation NPN wideband transistors.

f_T/I_C curve	I_C (mA)	V_{CE} (V)	Surface Mount Package						
			SOT23	SOT143	SOT223	SOT323	SOT343	SOT353@	SOT363@
(19)	0.1 - 2	1 - 5	BFT25A	BFG25A/X		BFS25A	BFG25AW*		
(21)	2 - 10	1 - 12	BFR505	BFG505*		BFS505	BFG505W*	BFC505 BFE505	BFM505/X
(22)	3 - 30	3 - 12	BFLR520	BFG520*		BFS520	BFG520W*	BFC520 BFE520	BFM520/X
(23)	10 - 60	3 - 12	BFR540	BFG540*	BFG541	BFS540	BFG540W*	BFC540 BFE540	BFM540/X
(24)	30 - 100	5 - 12		BFG590*	BFG591		BFG590W*		
	#	3 - 10		BFG10/X			BFG10W@		
	#	3 - 10		BFG11/X			BFG10W@		

f_T up to 9.5 GHz.
* Also available /X and /XR versions.
# Class A/B bias for pulsed power amplifier.
@ In development.
See Fig.1 for the f_T/I_C curves.

Fig.7 Fourth generation NPN wideband transistors.



Socket	Transistor *	Remark
RF Amp	BFT25A	Lowest current (0.2 mA)
	BFR505	Higher gain Lower noise (1mA)
	BFC505	Higher gain, lower noise high isolation (0.3 mA)
OSC, Mix or buffer	BFR92A	Choice of transistor determined by available current and required performance
	BFQ67	
	BFT25A	
	BFR505	

Equivalent types available in SOT23, SOT143, SOT323 or SOT343 packages.

Fig.8 Line-up for pager front end.

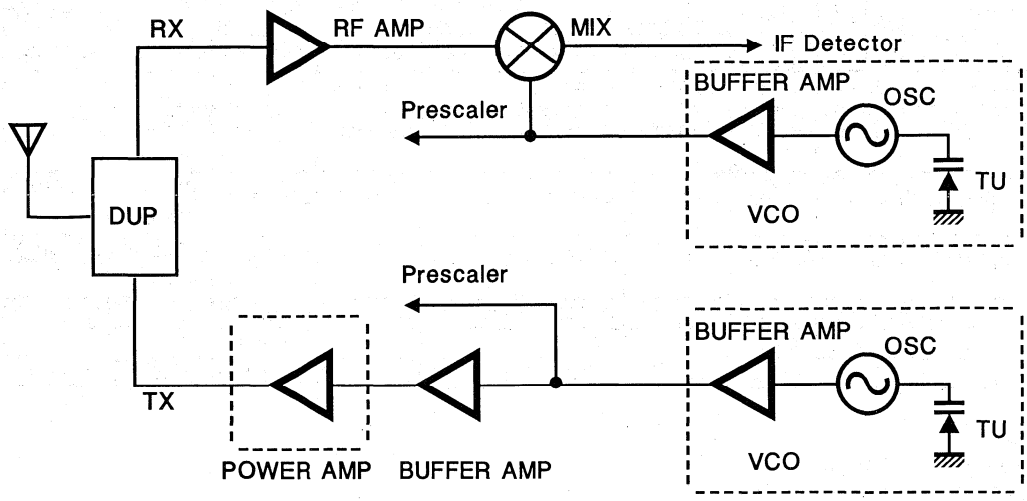


Fig.9 Principle circuit diagram for (Discrete) RF part in cordless and cellular telephones.

Socket	Type	System Freq. (MHz)	Remark
LNA	BFC505	1900	High isolation gain, Low noise current
	BFR505	900 & 1900	Good performance at low current (1 mA)
	BFR520	900 & 1900	Higher gain, Lower noise (10 mA)
Mixer	BFR93A	900	Low cost, acceptable performance
	BFG505	900 & 1900	Good performance, Low current
	BFG520	900 & 1900	Higher power to IF (10 mA)
	BFE505	900 & 1900	Balanced mixer in one SOT353 package
Buffer & VCO	BFR92A	900	Excellent VCO, Good buffer, Low cost
	BFR93A	900	Excellent VCO, Good buffer, Low cost
	BFQ67	900	Third generation, good performance
	BFR505	900 & 1900	Good VCO, High gain buffer, Low current
	BFR520	900 & 1900	Good VCO, Higher output power
	BFC505	1900	Buffer and VCO in one SOT353 package
IF	BFS17A	40 .. 100	Any first or second generation transistor

Fig.10 Types for receiver side (selection considerations).

Socket	System Freq. (MHz)	SOT23	SOT323	SOT143*	SOT343*	SOT353#	SOT363#
LNA	900 & 1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505/X
	900 & 1900	BFR520	BFS520	BFG520	BFG520W	BFC520	BFM520/X
Mixer	900	BFR93A	BFR93AW	BFG93A	BFG93AW		
	900 & 1900	BFR505	BFS505	BFG505	BFG505W	BFE505	BFM505/X
	900 & 1900	BFR520	BFS520	BFG520	BFG520W	BFE520	BFM520/X
Buffer & VCO	900	BFR92A	BFR92AW	BFG92A	BFG92AW		
	900	BFR93A	BFR93AW	BFG93A	BFG93AW		
	900	BFQ67	BFQ67W	BFG67	BFG67W		
	900 & 1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505/X
	900 & 1900	BFR520	BFS520	BFG520	BFG520W	BFC520	BFM520/X
IF	40 .. 100	BF547	BF547W				
		BFS17	BFS17W	BFG17A			
		BFR92A	BFR92AW	BFG92A	BFG92AW		

Fig.11 Overview of types for receiver side.

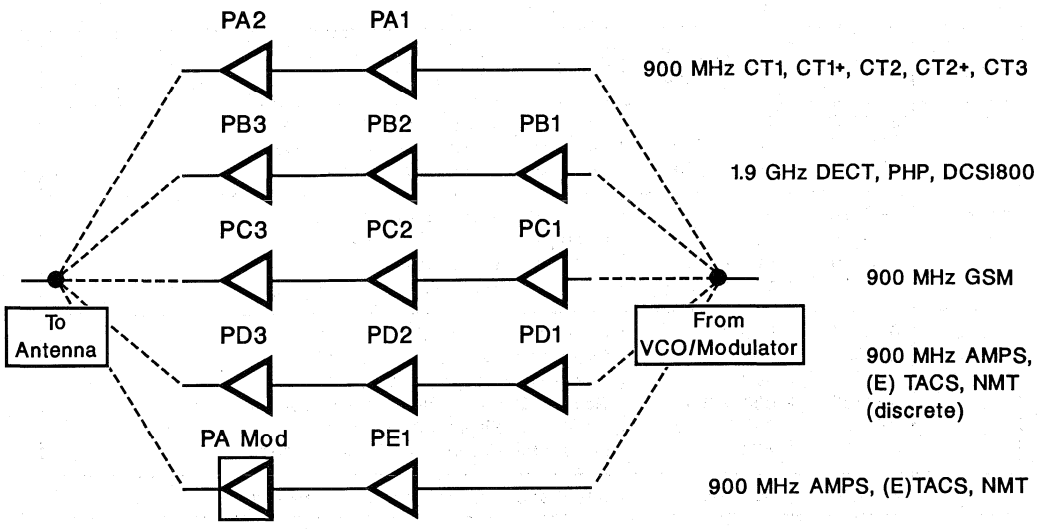


Fig.12 Power amplifier in cordless and cellular

System	Voltage	Pout	SOT143	SOT343
CT1, CT1+, CT2, CT2+ CT3	3.3 V	(Driver for PA2)	BFG67 BFG505 BFG520	BFG67W BFG505W BFG520W
		15 mW 20 mW 40 mW	BFG67 BFG520 BFG540	BFG67W BFG520W BFG540W
DECT, PHP	3.3 V	400 mW	BFG540/X BFG10/X BFG11/X	BFG540W/X BFG10W/X* BFG11W/X*

* In development.

Fig.13 Line-up for pagers in cordless.

RF POWER MODULES

- Private Mobile Radio (PMR) - VHF / UHF / SHF
  - Mobile and handportable
- Analog Cellular - 450 MHz / 900 MHz
  - AMPS, (E)TACS, NMT
  - Mobile and handportable
- Digital Cellular - 900 MHz / 1800 MHz
  - GSM, DCS1800
  - Mobile and handportable

Fig.14 Application areas.

Type	Frequency (MHz)	Pl (W)	Pd (mW)	min. Eff (%)
BGY132	68 - 88	18	100	38
BGY133	80 - 108	18	100	38
BGY135	132 - 156	18	150	38
BGY136	148 - 174	18	150	38
BGY143	146 - 174	13	150	40
BGY145A	68 - 88	29	150	37
BGY145B	146 - 174	28	300	40

VHF: 68 to 174 MHz.

Fig.15 Modules for mobile equipment.

Type	Frequency (MHz)	Vs (V)	Pl (W)	Pd (mW)	min. Eff (%)
BGY46A	400 - 440	9.6	1.4	45	40
BGY46B	430 - 470	9.6	1.4	45	40
BGY47A	400 - 470	9.6 / 7.5	3.2 / 2.0	50	40
BGY47B	460 - 520	9.6 / 7.5	3.2 / 2.0	50	40
BGY113A	400 - 440	7.5	7.0	1	40
BGY113B	430 - 470	7.5	7.0	1	40
BGY113C	470 - 520	7.5	7.0	1	35

UHF: 400 to 520 MHz.

Fig.16 Modules for portable equipment.

Type	Frequency (MHz)	Vs (V)	Pl (W)	Pd (mW)	min. Eff (%)
BGY116D	800 - 870	12.5	6	1	33
BGY116E	890 - 950	12.5	6	1	33

UHF: 800 to 950 MHz.

Fig.17 Modules for mobile equipment.

Type	Frequency (MHz)	Vs (V)	Pl (W)	Pd (mW)	min. Eff (%)	Package Volume (cm^3)
BGY115A	824 - 849	6.0	1.2	2	45	0.9
BGY115B	872 - 905	6.0	1.2	2	45	0.9
BGY115C	890 - 915	6.0	1.6	2	45	0.9
BGY115D	902 - 928	6.0	1.2	2	45	0.9
BGY118A	824 - 849	4.8	1.2	2	50	0.9
BGY118B	872 - 905	4.8	1.2	2	50	0.9
BGY118D	898 - 928	4.8	1.2	2	50	0.9

Analog cellular radio.

Fig.18 Modules for portable equipment (1).

Type	Frequency (MHz)	Vs (V)	Pl (W)	Pd (mW)	min. Eff (%)	Package Volume (cm^3)
BGY119A	824 - 849	4.8	1.2	2	50	0.6
BGY119B	872 - 905	4.8	1.2	2	50	0.6
BGY119D	898 - 928	4.8	1.2	2	50	0.6
BGY120A*	824 - 849	3.6	1.2	2	50	0.4
BGY120B*	872 - 905	3.6	1.2	2	50	0.4

Analog cellular radio.

* In development.

Fig.19 Modules for portable equipment (2).

Type	Vs (V)	Pl (W)	Pd (mW)	min. Eff (%)	Package volume (cm^3)
BGY201	12.5	14.0	1	35	5
BGY203	6	3.5	1	40	1.7
BGY205	6	3.5	2	40	0.9
BGY204	4.8	3.5	2	40	0.9
BGY206	4.8	3.0	5	40	0.6
BGY202	6.0	1.4	2	45	0.9
BGY207	4.8	1.2	2	50	0.6

Digital cellular radio.

Fig.20 Modules for GSM (890 to 915 MHz).

Type	Frequency (MHz)	Pl (W)	Pd (mW)	min. Eff (%)
BGY114A	824 - 849	6	1	35
BGY114B	872 - 905	6	1	35
BGY114C	890 - 915	8	1	35

Analog cellular radio.

Fig.21 Modules for mobile equipment.

LOW VOLTAGE RF POWER MODULES

- Private Mobile Radio (PMR) - VHF / UHF / SHF
  - Mobile and handportable
- Analog Cellular - 450 MHz / 900 MHz
  - AMPS, (E)TACS, NMT
  - Mobile and handportable
- Digital Cellular - 900 MHz / 1800 MHz
  - GSM, DCS1800
  - Mobile and handportable

Fig.22 Application areas.

Type	PI (W)	min. Gp (dB)	Outline
BFQ42	2	11.0	SOT5
BFQ43	4	12.0	SOT5
BLV10	8	9.0	SOT123
BLV11	15	7.5	SOT123
BLV12	30	9.0	SOT123
BLV13	40	8.5	SOT123
BLW29	15	10.0	SOT120
BLW30	30	10.0	SOT120
BLW40	40	10.0	SOT120
BLV75/12	75	6.5	SOT119

VHF: 175 MHz.

Fig.23 Transistors for mobile equipment (12.5 V).

Type	V_S (V)	Pl (W)	min. Gp (dB)	Outline
BLT50	7.5	1.2	10	SOT223
BLU99/SL	7.5	2.5	10	SOT122D
BLT53	7.5	8.0	6	SOT122D

UHF: 470 MHz.

Fig.24 Transistors for portable equipment.

Type	Pl (W)	min. Gp (dB)	Outline
BLU56	1	12.0	SOT223
BLW79	2	9.0	SOT122
BLW80	4	8.0	SOT122
BLU99	5	10.5	SOT122
BLU97	7	8.5	SOT122
BLU10/12	10	8.0	SOT122
BLU15/12	15	7.8	SOT122
BLU20/12	20	6.5	SOT122
BLU30/12	30	6.0	SOT119
BLU45/12	45	4.8	SOT119
BLU60/12	60	4.4	SOT119

UHF: 470 MHz.

Fig.25 Transistors for mobile equipment (12.5 V).

Type	V_S (V)	Pl (W)	min Gp (dB)	Outline
BLT80	6.0	0.8	6	SOT223
BLT81	6.0	1.2	6	SOT223
BLT70	4.8	0.6	6	SOT223
BLT71	4.8	1.2	6	SOT223
BFG10W/X	3.6	0.2	10	SOT343
BLT61*	3.6	1.2	8	SO8

Analog cellular radio (900 MHz).
* In development.

Fig.26 Transistors for portable equipment.

Type	Pl (W)	min. Gp (dB)	Outline
BLU98	0.5	8.0	SOT103
BLU86	1.0	7.0	SOT223
BLV91	2.0	6.5	SOT172
BLV92	4.0	7.5	SOT171
BLV193	12	6.5	SOT171
BLV194	16	6.0	SOT171

UHF: 900 MHz.

Fig.27 Transistors for mobile equipment (12.5 V).

Type	Freq. (MHz)	Vs (V)	Pl (W)	min. Gp (dB)	Outline
BLT82	900	6.0	3.5	8.0	SO8
BLT72*	900	4.8	3.0	8.0	SO8
BFG10W/X	900	6.0	0.65	10.0	SOT343
BFG10W/X	1800	6.0	0.65	5.0	SOT343
BLT13*	1800	6.0	2.0	6.0	SO8
BLT14*	1800	4.8	1.6	6.0	SO8

Digital cellular radio (GSM and PCS).
* In development.

Fig.28 Transistors for portable equipment.

Application	Vs (V)	Pl (W)	1-st stage	2-nd stage	3-rd stage
Analog	6.0	1.2	BFG540	BLT80	BLT81*
	4.8	1.2	BFG540	BLT70	BLT71
	3.6	1.2	BFG520	BFG10W/X	BLT61
GSM	6.0	3.5	BFG520	BFG10W/X	BLT82
	4.8	3.0	BFG520	BFG10W/X	BLT72
PCN / DCS1800	6.0	2.0	BFG540	BFG10W/X	BLT13
	4.8	1.6	BFG540	BFG10W/X	BLT14

* Application note and demo-board available.

Fig.29 Recommended line-ups for cellular radio.

DIALLERS

Table 1 Dialler feature reference matrix

TYPE NUMBER	PULSE	DTMF	REDIAL	REP. DIAL	RINGER
PCD3310 family	x	x	x	–	–
PCD332X family	x	–	x	–	–
PCD3330-1	x	x	x	x	x
PCD3332-1	x	x	x	x	x
PCD3332-2 (S)	x	x	x	x	x

Table 2 PSD matrix

TYPE NUMBER	PLD INPUTS/ PROD. TERMS	PORTS	EPROM SIZE	SRAM SIZE	CONFIGURATION 8 bits/16 bits	MEMORY PAGING
Field-programmable microcontroller peripherals						
PSD301	14/40	19	256 kbyte	16 kbyte	8 or 16	N
PSD311	14/40	19	256 kbyte	16 kbyte	8	N
PSD302	18/40	19	512 kbyte	16 kbyte	8 or 16	Y
PSD312	18/40	19	512 kbyte	16 kbyte	8	Y
PSD303	18/40	19	1 Mbyte	16 kbyte	8 or 16	Y
PSD313	18/40	19	1 Mbyte	16 kbyte	8	Y
3-volt single chip field-programmable microcontroller peripherals						
PSD301L	14/40	19	256 kbyte	16 kbyte	8 or 16	N
PSD311L	14/40	19	256 kbyte	16 kbyte	8	N
PSD302L	18/40	19	512 kbyte	16 kbyte	8 or 16	Y
PSD312L	18/40	19	512 kbyte	16 kbyte	8	Y
PSD303L	18/40	19	1 Mbyte	16 kbyte	8 or 16	Y
PSD313L	18/40	19	1 Mbyte	16 kbyte	8	Y

Table 3 Preferred telephone set /microcontroller selection matrix

TYPE NUMBERS	TEL. SETS	ANSWERING MACHINE	CORDLESS CT0/CT1	DIGITAL CORDLESS	ANALOG CELLULAR	PAGERS	PERIPHERAL CONTROLLER
PCD3315A	x	–	–	–	–	–	x
PCD3343A	x	–	–	–	–	–	x
PCD3344A	x	x	–	–	–	–	–
PCD3346	x	–	–	–	–	–	–
PCD3347	x	–	–	–	–	–	–
PCD3348A	x	x	–	–	–	–	x
PCD3349A	x	x	x	–	–	–	–
PCD3350A	x	x	x	–	–	–	x
PCD3351A	x	–	–	–	–	–	x
PCD3352A	x	–	–	–	–	–	x
PCD3353A	x	x	x	–	–	–	x
PCD3354A	x	x	x	–	–	–	x
PCF84CXXA	x	x	x	–	–	–	x
P80CL31/51	x	x	x	–	–	x	x
P80/83CL410	x	x	x	–	–	x	x
P83C550	–	–	–	–	x	–	–
P83C552-5	–	–	–	–	x	–	–
P83C562	–	–	–	–	–	–	–
P80/83CL580	–	–	x	–	x	x	x
P83C652	–	–	x	–	–	–	–
P83C654	–	–	x	x	x	–	–
P83CL781	x	x	x	–	–	x	x
P83CL782	x	x	x	x	–	x	x
P83C851	–	–	–	–	x	–	–
P90CL301/302	–	–	–	–	–	–	x

GENERAL

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A Germanium or other material with a band gap of 0.6 to 1 eV

B Silicon or other material with a band gap of 1 to 1.3 eV

C Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A Diode; signal, low power

B Diode; variable capacitance

C Transistor; low power, audio frequency

D Transistor; power, audio frequency

E Diode; tunnel

F Transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under "Serial number/special third letter"

H Diode; magnetic sensitive

L Transistor; power, high frequency

N Photocoupler

P Radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q Radiation generator; e.g. LED, laser; with special third letter

R Control or switching device; e.g. thyristor, low power; with special third letter

S Transistor; low power, switching

T Control and switching device; e.g. thyristor, power; with special third letter

U Transistor; power, switching

W Surface acoustic wave device

X Diode; multiplier, e.g. varactor, step recovery

Y Diode; rectifying, booster

Z Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A For triacs, after second letter 'R' or 'T'

F For emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L For lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O For opto-triacs, after second letter 'R'

T For 3-state bicolour LEDs, after second letter 'Q'

W For transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112	Germanium, low power signal diode (consumer type)
ACY32	Germanium, low power AF transistor (industrial type)
BD232	Silicon, power AF transistor (consumer type)
CQY17	GaAs, light-emitting diode (industrial type)
RPY84	CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%

B 2%

C 5%

D 10%

E 20%.

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C −55 to +125 °C

D −25 to + 70 °C

E −25 to + 85 °C

F −40 to + 85 °C

G −55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

SECOND LETTER (MATERIAL)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

Examples

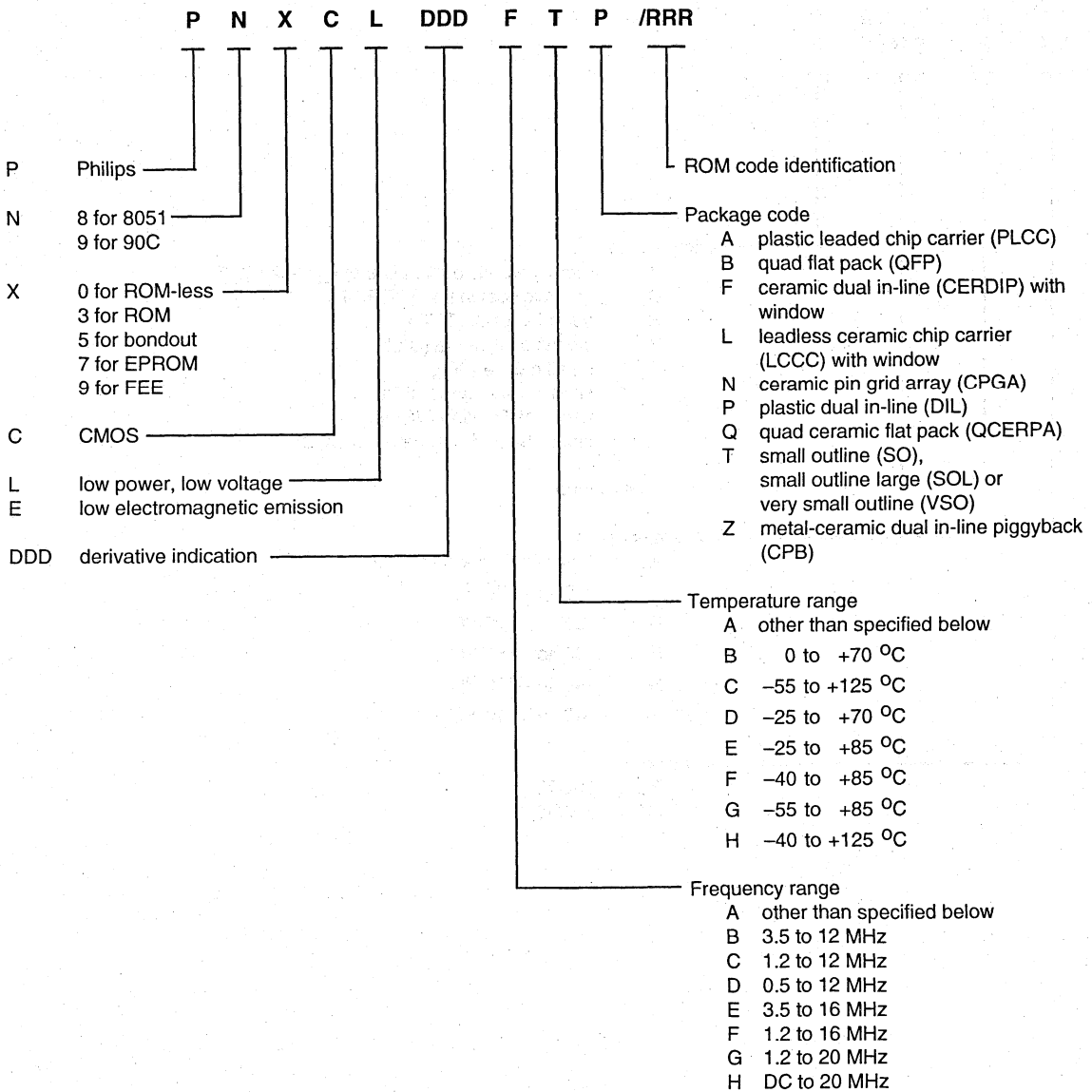
PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

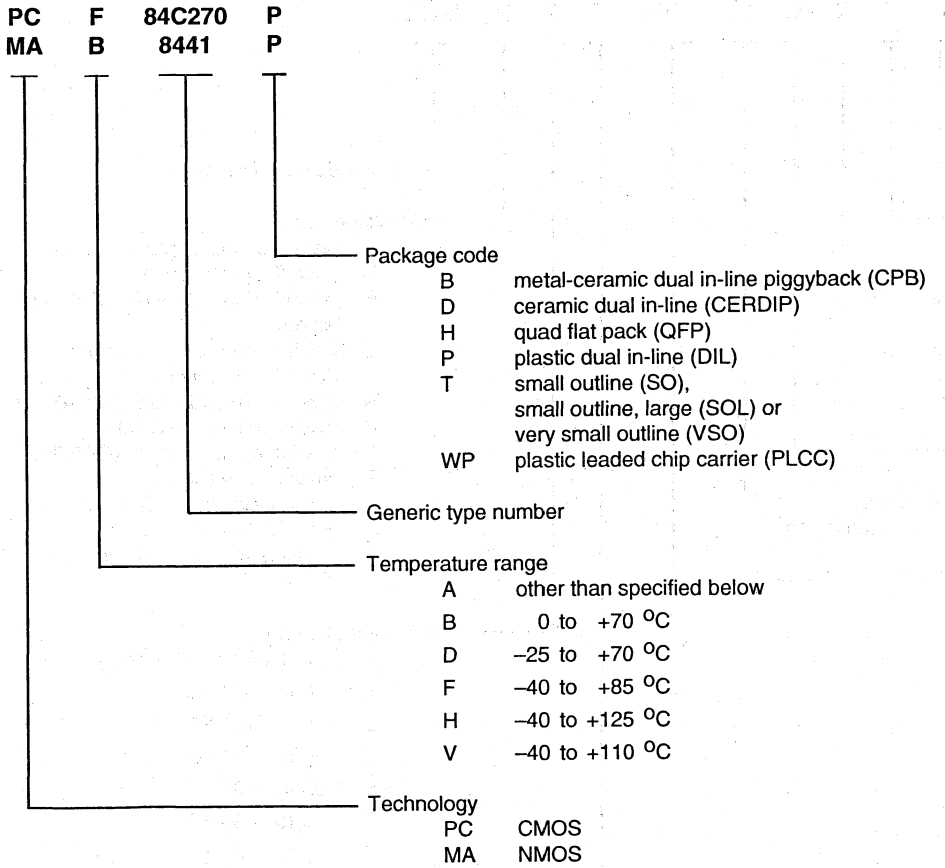
TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

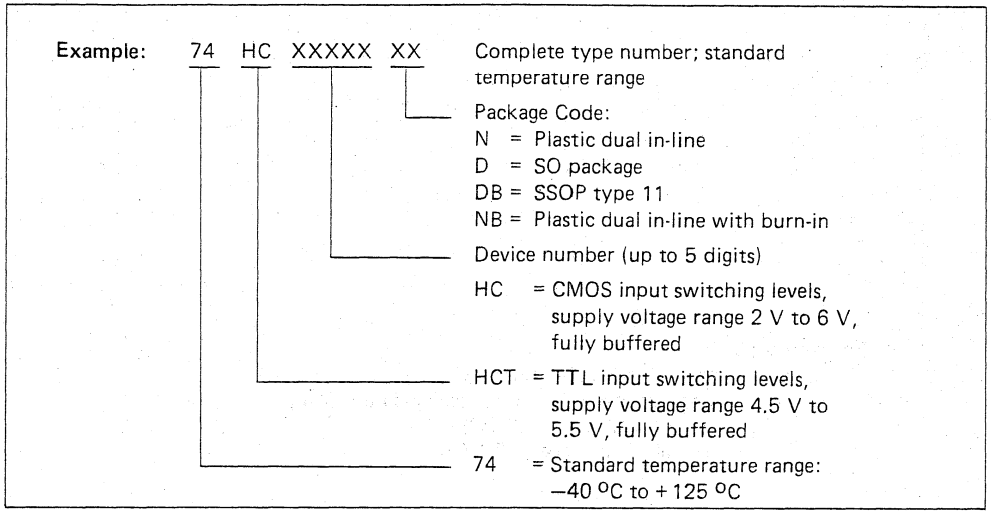
TYPE NUMBERING OF 8051 AND 90C MICROCONTROLLER DERIVATIVES



TYPE NUMBERING OF 8048 MICROCONTROLLER DERIVATIVES



TYPE NUMBERING OF HCMOS INTEGRATED CIRCUITS

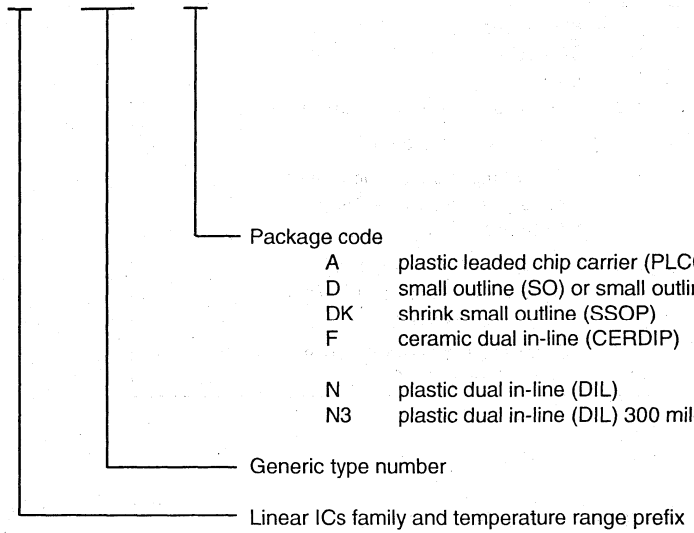


ORDERING

When ordering, please state:
- the quantity required;
- the package code (N = plastic DIL, D = plastic SO mini-pack, DB = SSOP type 11);
- screening class (B) if burn-in option is required (only applicable for NB package).

TYPE NUMBERING OF LINEAR AND MEMORY DEVICES

NE 567 N
SA 604A D



Package code

A	plastic leaded chip carrier (PLCC)
D	small outline (SO) or small outline large (SOL)
DK	shrink small outline (SSOP)
F	ceramic dual in-line (CERDIP)
N	plastic dual in-line (DIL)
N3	plastic dual in-line (DIL) 300 mil-wide

Generic type number

Linear ICs family and temperature range prefix

MC	0 to +70 °C
N	0 to +70 °C
NE	0 to +70 °C
S	−55 to +125 °C
SE	−55 to +125 °C
SA	−40 to +85 °C

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental

conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor
- All mains-powered electrical equipment should be connected via an earth leakage switch
- Equipment cases should be earthed
- Relative humidity should be maintained between 50 and 65%
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

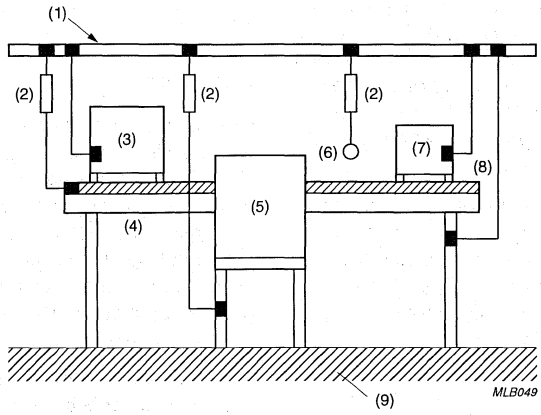
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.

Fig.1 Protected work station.

DEVICE DATA

Single-chip 8-bit microcontroller — 80C552/83C552

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

Single-chip 8-bit microcontroller with 10-bit A/D, capture/compare timer, high-speed outputs, PWM

DESCRIPTION

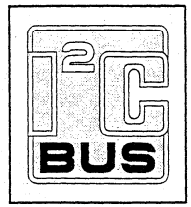
The 80C552/83C552 (hereafter generically referred to as 8XC552) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC552 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C552—8k bytes mask programmable ROM
- 80C552—ROMless version of the 83C552
- 87C552—8k bytes EPROM (described in a separate chapter)

The 8XC552 contains a non-volatile 8k × 8 read-only program memory (83C552), a volatile 256 × 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC552 can be expanded using standard TTL compatible memories and logic.

In addition, the 8XC552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

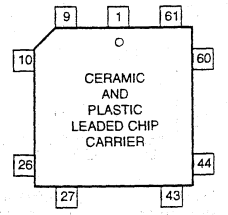
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16MHz (24MHz) crystal, 58% of the instructions are executed in 0.75µs (0.5µs) and 40% in 1.5µs (1µs). Multiply and divide instructions require 3µs (2µs).



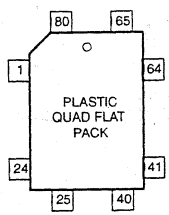
FEATURES

- 80C51 central processing unit
- 8k × 8 ROM expandable externally to 64k bytes
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256 × 8 RAM, expandable externally to 64k bytes
- Capable of producing eight synchronized, timed outputs
- A 10-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three speed ranges:
  - 1.2 to 16MHz
  - 1.2 to 24MHz (ROM, ROMless only)
  - 1.2 to 30MHz (ROM, ROMless only)
- Three operating ambient temperature ranges:
  - PCB83C552–5: 0°C to +70°C
  - PCF83C552–5: –40°C to +85°C (XTAL frequency max. 24 MHz)
  - PCA83C552–5: –40°C to +125°C (XTAL frequency max. 16 MHz)

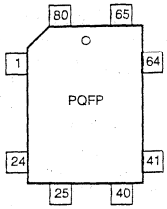
PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	P5.0/ADC0	35	XTAL1
2	V_{DD}	36	V_{SS}
3	STADC	37	V_{SS}
4	$\overline{PWM0}$	38	NC
5	$\overline{PWM1}$	39	P2.0/A08
6	$\overline{EW}$	40	P2.1/A09
7	P4.0/CMSR0	41	P2.2/A10
8	P4.1/CMSR1	42	P2.3/A11
9	P4.2/CMSR2	43	P2.4/A12
10	P4.3/CMSR3	44	P2.5/A13
11	P4.4/CMSR4	45	P2.6/A14
12	P4.5/CMSR5	46	P2.7/A15
13	P4.6/CMT0	47	$\overline{PSEN}$
14	P4.7/CMT1	48	ALE
15	RST	49	$\overline{EA}$
16	P1.0/CT0I	50	P0.7/AD7
17	P1.1/CT1I	51	P0.6/AD6
18	P1.2/CT2I	52	P0.5/AD5
19	P1.3/CT3I	53	P0.4/AD4
20	P1.4/T2	54	P0.3/AD3
21	P1.5/RT2	55	P0.2/AD2
22	P1.6/SCL	56	P0.1/AD1
23	P1.7/SDA	57	P0.0/AD0
24	P3.0/RxD	58	AVref–
25	P3.1/TxD	59	AVref+
26	P3.2/$\overline{INT0}$	60	AV_{SS}
27	P3.3/$\overline{INT1}$	61	AV_{DD}
28	P3.4/T0	62	P5.7/ADC7
29	P3.5/T1	63	P5.6/ADC6
30	P3.6/$\overline{WR}$	64	P5.5/ADC5
31	P3.7/$\overline{RD}$	65	P5.4/ADC4
32	NC	66	P5.3/ADC3
33	NC	67	P5.2/ADC2
34	XTAL2	68	P5.1/ADC1



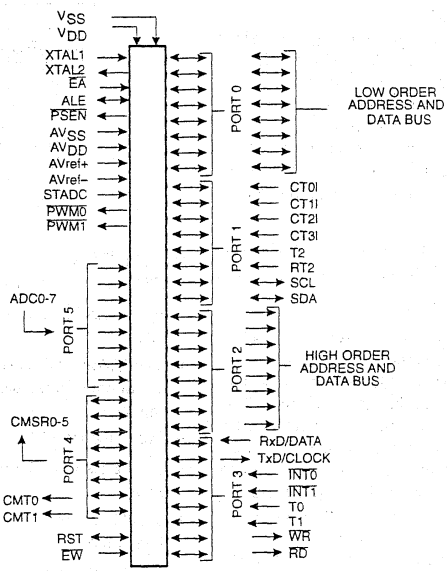
PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P4.1/CMSR1	41	P2.3/A11
2	P4.2/CMSR2	42	P2.4/A12
3	NC	43	NC
4	P4.3/CMSR3	44	NC
5	P4.4/CMSR4	45	P2.5/A13
6	P4.5/CMSR5	46	P2.6/A14
7	P4.6/CMT0	47	P2.7/A15
8	P4.7/CMT1	48	$\overline{PSEN}$
9	RST	49	ALE
10	P1.0/CT0I	50	$\overline{EA}$
11	P1.1/CT1I	51	P0.7/AD7
12	P1.2/CT2I	52	P0.6/AD6
13	P1.3/CT3I	53	P0.5/AD5
14	P1.4/T2	54	P0.4/AD4
15	P1.5/RT2	55	P0.3/AD3
16	P1.6/SCL	56	P0.2/AD2
17	P1.7/SDA	57	P0.1/AD1
18	P3.0/RxD	58	P0.0/AD0
19	P3.1/TxD	59	AVref–
20	P3.2/$\overline{INT0}$	60	AVref+
21	NC	61	AV_{SS}
22	NC	62	NC
23	P3.3/$\overline{INT1}$	63	AV_{DD}
24	P3.4/T0	64	P5.7/ADC7
25	P3.5/T1	65	P5.6/ADC6
26	P3.6/$\overline{WR}$	66	P5.5/ADC5
27	P3.7/$\overline{RD}$	67	P5.4/ADC4
28	NC	68	P5.3/ADC3
29	NC	69	P5.2/ADC2
30	NC	70	P5.1/ADC1
31	XTAL2	71	P5.0/ADC0
32	XTAL1	72	V_{DD}
33	IC	73	IC
34	V_{SS}	74	STADC
35	V_{SS}	75	$\overline{PWM0}$
36	V_{SS}	76	$\overline{PWM1}$
37	NC	77	$\overline{EW}$
38	P2.0/A08	78	NC
39	P2.1/A09	79	NC
40	P2.2/A10	80	P4.0/CMSR0

NC = not connected
IC = internally connected (do not use)

LOGIC SYMBOL



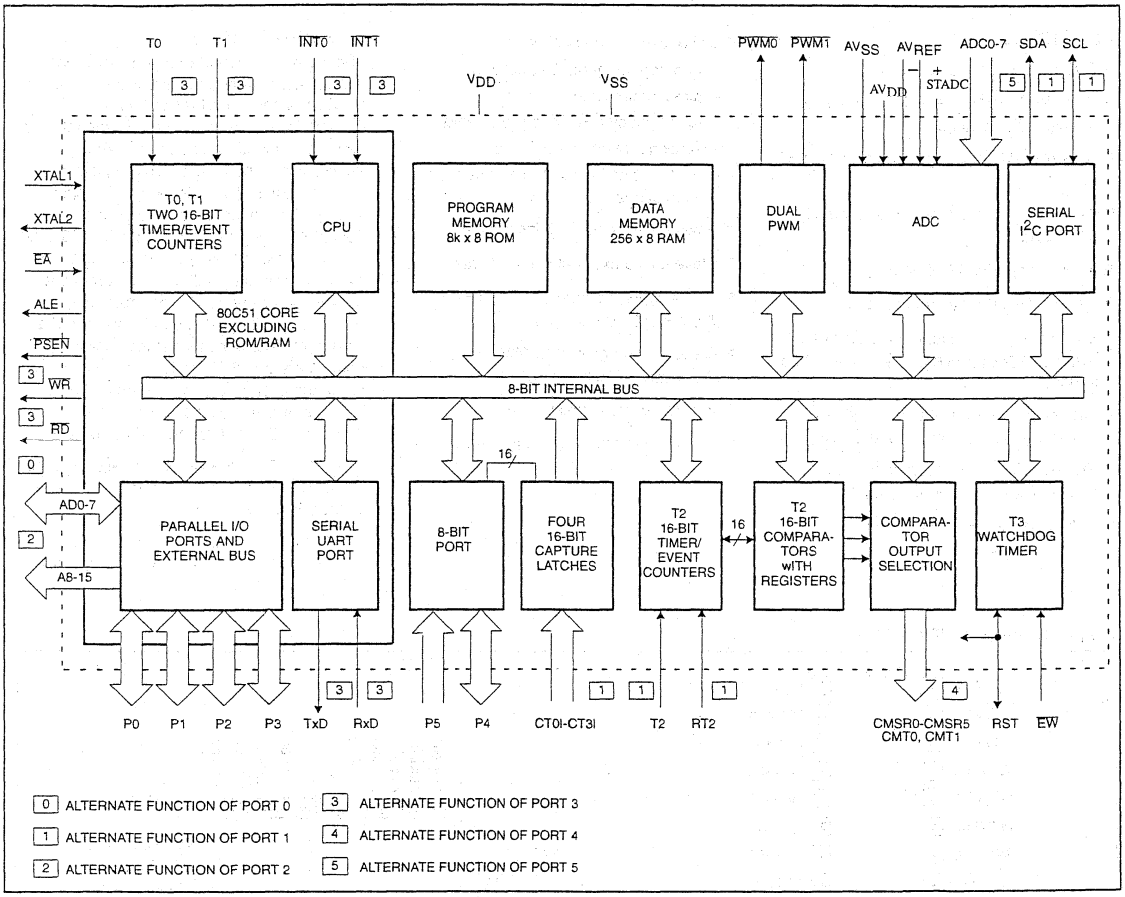
ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		NORTH AMERICA PHILIPS PART ORDER NUMBER		DRAWING	TEMPERATURE °C	FREQ
ROMless	ROM	ROMless	ROM	NUMBER	AND PACKAGE	MHz
PCB80C552-5-16WP	PCB83C552-5WP/xxx	S80C552-4A68	S83C552-4A68	SOT188	0 to +70, Plastic Leaded Chip Carrier	16
PCB80C552-5-16H	PCB83C552-5H/xxx	S80C552-4B	S83C552-4B	SOT318	0 to +70, Plastic Quad Flat Pack	16
PCF80C552-5-16WP	PCF83C552-5WP/xxx	S80C552-5A68	S83C552-5A68	SOT188	–40 to +85, Plastic Leaded Chip Carrier	16
PCF80C552-5-16H	PCF83C552-5H/xxx	S80C552-5B	S83C552-5B	SOT318	–40 to +85, Plastic Quad Flat Pack	16
PCA80C552-5-16WP	PCA83C552-5WP/xxx	S80C552-6A68	S83C552-6A68	SOT188	–40 to +125, Plastic Leaded Chip Carrier	16
PCA80C552-5-16H	PCA83C552-5H/xxx	S80C552-6B	S83C552-6B	SOT318	–40 to +125, Plastic Quad Flat Pack	16
PCB80C552-5-24WP	PCB83C552-5WP/xxx	S80C552-AA68	S83C552-AA68	SOT188	0 to +70, Plastic Leaded Chip Carrier	24
PCB80C552-5-24H	PCB83C552-5H/xxx	S80C552-AB	S83C552-AB	SOT318	0 to +70, Plastic Quad Flat Pack	24
PCF80C552-5-24WP	PCF83C552-5WP/xxx	S80C552-BA68	S83C552-BA68	SOT188	–40 to +85, Plastic Leaded Chip Carrier	24
PCF80C552-5-24H	PCF83C552-5H/xxx	S80C552-BB	S83C552-BB	SOT318	–40 to +85, Plastic Quad Flat Pack	24
PCB80C552-5-30WP	PCB83C552-5WP/xxx	S80C552-CA68	S83C552-CA68	SOT188	0 to +70, Plastic Leaded Chip Carrier	30
PCB80C552-5-30H	PCB83C552-5H/xxx	S80C552-CB	S83C552-CB	SOT318	0 to +70, Plastic Quad Flat Pack	30

NOTE:
1. xxx denotes the ROM code number.

EPROM	DRAWING NUMBER	TEMPERATURE °C AND PACKAGE	FREQ MHz
S87C552-4A68	0398E	0 to +70, Plastic Leaded Chip Carrier	16
S87C552-4K68	1473A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
S87C552-4B	SOT318	0 to +70, Plastic Quad Flat Pack	16
S87C552-5A68	0398E	–40 to +85, Plastic Leaded Chip Carrier	16
S87C552-5K68	1473A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	16
S87C552-5B	SOT318	–40 to +85, Plastic Quad Flat Pack	16

BLOCK DIAGRAM



Low-voltage single-chip 8-bit microcontrollers

80CL31/80CL51

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, 1/0 in a single 40-lead DIL / mini-pack
- 4K x 8 ROM, expandable externally to 64K bytes
- 128 bytes RAM, expandable externally to 64K bytes
- Four 8-bit ports, 321/0 lines
- Two 16-bit timer / event counters
- External memory expandable up to 128K, external ROM up to 64K and / or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Thirteen source, thirteen vector interrupt structure with two priority levels
- Full duplex serial port (UART)
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight byte RAM register banks
  - stack depth up to 128 bytes
  - multiply, divide, subtract and compare instructions
- Power-Down and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8V to 6.0V (5.0V ±10% for P80C51)
- Frequency range of 0 to 16MHz (3.5MHz to 16MHz for P80C51)
- Very low current consumption
- Operating temperature range: -40 to +85°C

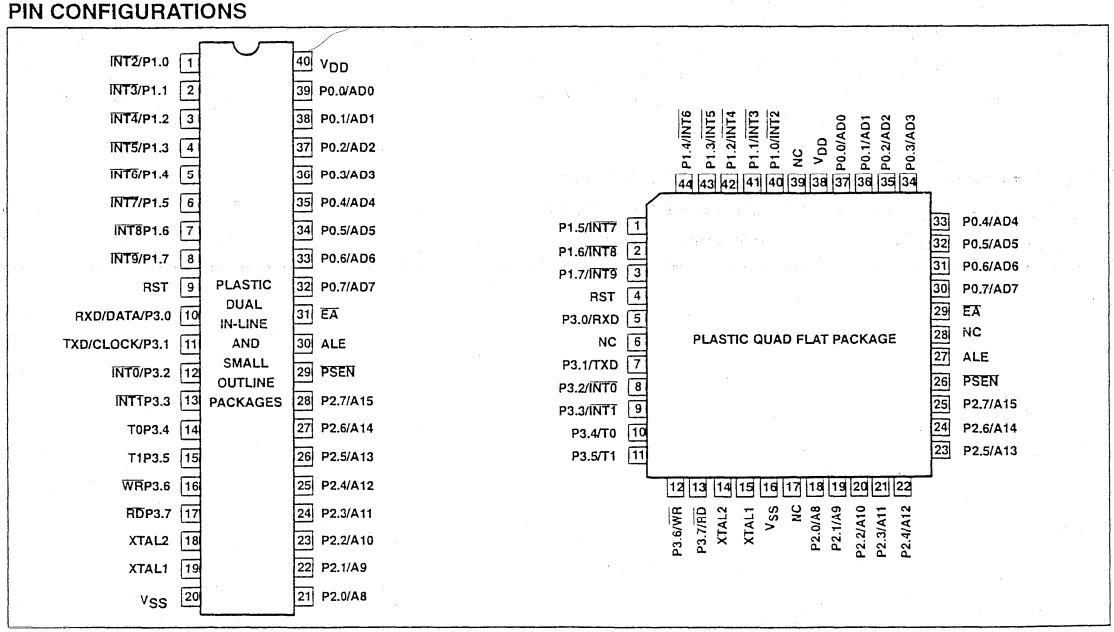
DESCRIPTION

The 80CL51 is manufactured in an advanced CMOS technology. The instruction set of the 80CL51 is based on that of the 8051. The 80CL51 is a general purpose microcontroller especially suited for battery-powered applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the 85CL000 (Piggy-back version) with 256 bytes of RAM is recommended. The 80CL51 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The 80CL51 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

The P80CL31 is the ROMless version of the P80CL51. P80C51 is a 5V version of the low voltage P80CL51.

The P80CL31 is the ROMless version of the P80CL51. P80C51 is a 5V version of the low voltage P80CL51.

PIN CONFIGURATIONS

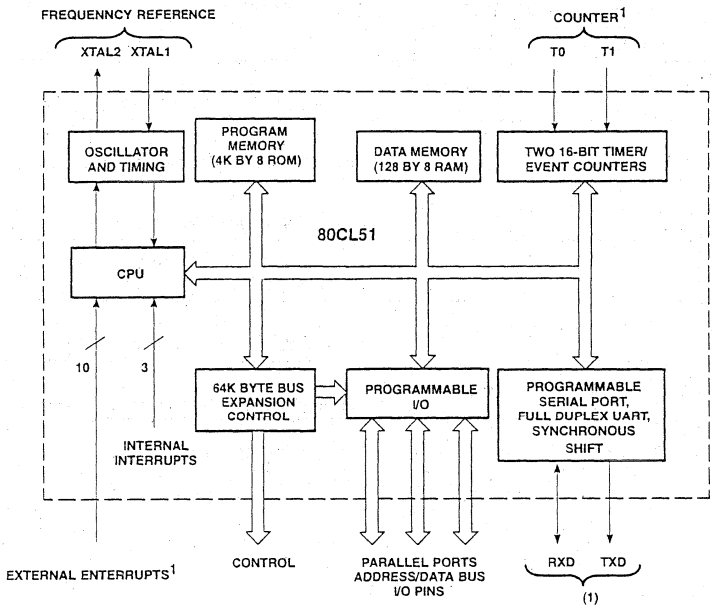


ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA [1] PART ORDER NUMBER		TEMPERATURE RANGE °C AND PACKAGE	DRAWING NUMBER
ROMless	ROM	ROMless	ROM		
P80CL31HFP	P80CL51HFP	P80CL31HFP N	P80CL51HFP N	–40 to +85; 40-lead Plastic Dual In-line Package (1.8V to 6V)	SOT129
P80CL31HFT	P80CL51HFT	P80CL31HFT D	P80CL51HFT D	–40 to +85; 40-lead Plastic Small Outline Package (1.8V to 6V)	SOT158A
	P80CL51HFH	P80CL41HFH B	P80CL51HFH B	–40 to +85; 44-lead Plastic Quad Flat Package (1.8V to 6V)	SOT307
	P80C51HFP		P80C51HFP N	–40 to +85; 40-lead Plastic Dual In-line Package (5.0V ±10%)	SOT129
	P80C51HFT		P80C51HFT D	–40 to +85; 40-lead Plastic Small Outline Package (5.0V ±10%)	SOT158A
	P80C51HFH		P80C51HFH B	–40 to +85; 44-lead Plastic Quad Flat Package (5.0V ±10%)	SOT307

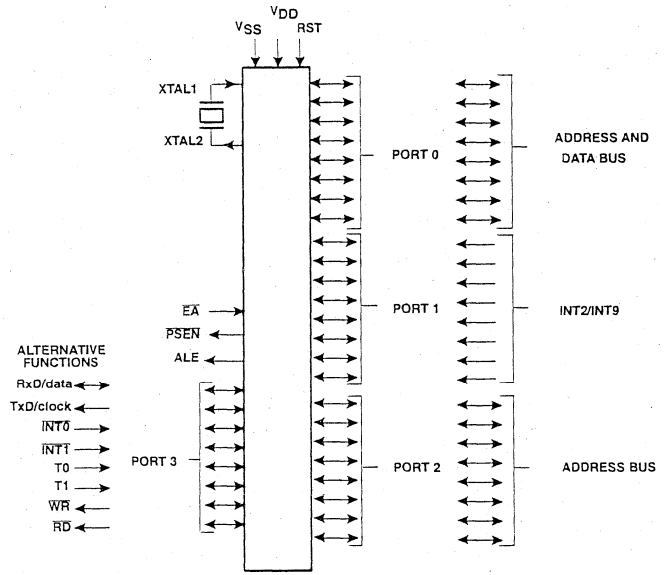
NOTE:
1. Parts ordered by the Philips North America part number will be marked with the Philips part marking.

BLOCK DIAGRAM



1. Pins shared with parallels ports pins.

FUNCTIONAL DIAGRAM



Low voltage /low power single-chip 8-bit microcontroller with I²C

80CL410/83CL410

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

DESCRIPTION

The 80CL410/83CL410 (hereafter generically referred to as 8XCL410) is manufactured in an advanced CMOS process that allows the part to operate at supply voltages down to 1.8V and oscillator frequencies down to DC. The 8XCL410 has the same instruction set as the 80C51.

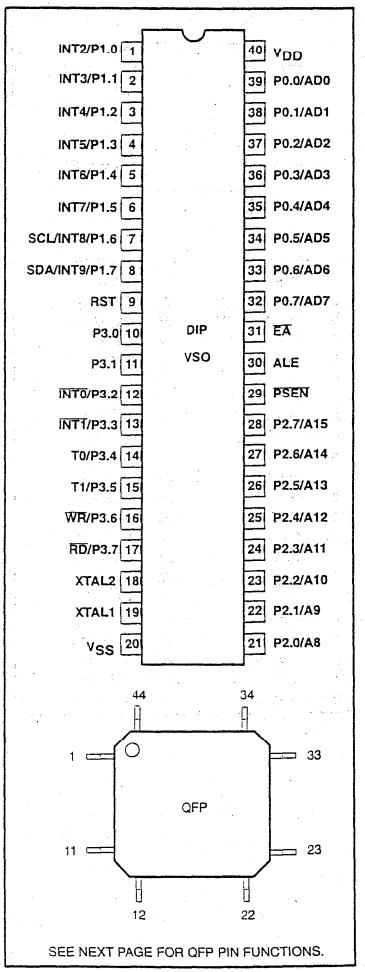
The 8XCL410 features a 4k byte ROM (83CL410), 128 bytes RAM (both ROM and RAM are externally expandable to 64k bytes), four 8-bit ports, two 16-bit timer/counters, an I²C serial interface, a thirteen source, two priority level nested interrupt structure, and on-chip oscillator circuitry suitable for quartz crystal, ceramic resonator, RC, or LC.

The 8XCL410 has two reduced power modes that are the same as those on the standard 80C51. The special reduced power feature of this part is that it can be stopped and then restarted. Running from an external clock source, the clock can be stopped and after a period of time restarted. The 8XCL410 will resume operation from where it was when the code stopped with no loss of internal state, RAM contents, or Special Function Register contents. If the internal oscillator is used the part cannot be stopped and started, but the power-down mode, which can be terminated via an interrupt, can be used to achieve similar power savings and then restart without loss of on-chip RAM and Special Function Register values.

FEATURES

- Single supply voltage 1.8V to 6.0V
- Frequency from DC to 12MHz
- 80C51 based architecture
  - 4k x 8 ROM (64k external)
  - 128 x 8 RAM (64k external)
  - Four 8-bit I/O ports
  - Two 16-bit timer/counters
  - A thirteen-source, two-level, nested priority interrupt structure
  - 10 external interrupts
- Fully static 80C51 CPU
- I²C Serial Interface
- Two power control modes
  - Idle mode
  - Power-down mode – can be terminated by reset or external interrupt
- Wake-up via external interrupts at port 1
- Single supply voltage 1.8V to 6.0V
- Frequency range of DC to 12MHz
- On-chip oscillator (quartz crystal, ceramic resonator, RC, LC)
- Very low power consumption
- Operating temperature range: –40 to +85°C

PIN CONFIGURATION



SEE NEXT PAGE FOR QFP PIN FUNCTIONS.

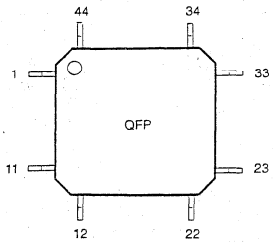
For emulation purposes, the P85CL000 (Piggyback version) with 256 bytes of RAM is recommended.

ORDERING CODE

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER[1]		TEMPERATURE °C AND PACKAGE	FREQUENCY	Drawing Number
ROMless	ROM	ROMless	ROM			
P80CL410HFP	P83CL410HFP	P80CL410HF N	P83CL410HF N	–40 to +85, 40-Pin Plastic Dual In-line Package	32kHZ to 12MHz	SOT129
P80CL410HFT	P83CL410HFT	P80CL410HF D	P83CL410HF D	–40 to +85, 40-Pin Plastic Very Small Outline Package	32kHZ to 12MHz	SOT158A
	P83CL410HFH			–40 to +85, 44-Pin Plastic Quad Flat Pack	32kHZ to 12MHz	SOT307B

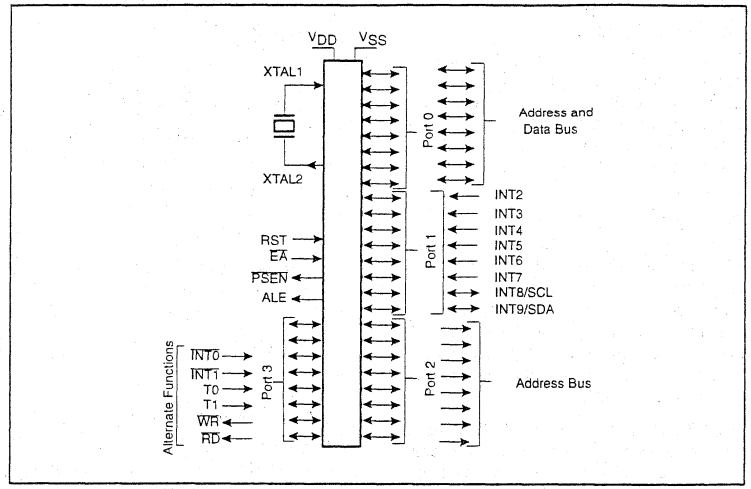
NOTE:
1. Parts ordered by the Philips North America part number will be marked with the Philips part marking.

PLASTIC QUAD FLAT PACK PIN FUNCTIONS

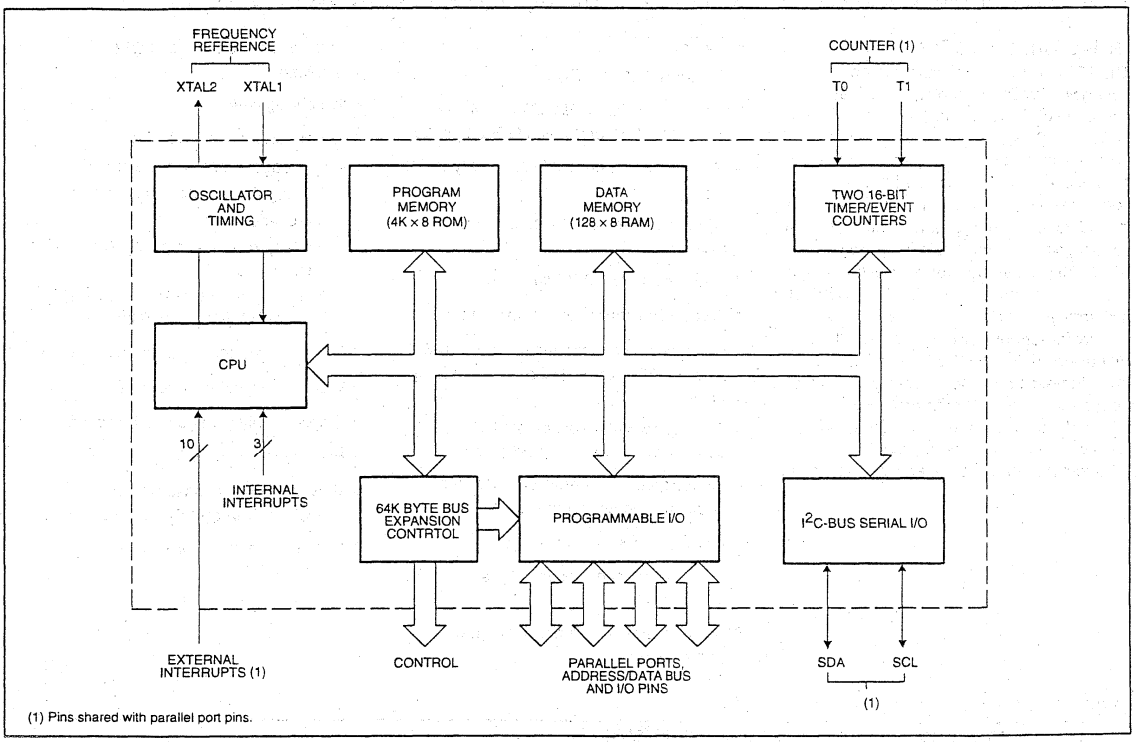


Pin	Function	Pin	Function
1	P1.5/INT7	23	P2.5/A13
2	P1.6/INT8/SCL	24	P2.6/A14
3	P1.7/INT9/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0	27	ALE
6	NC	28	NC
7	P3.1	29	$\overline{EA}$
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS}	38	V_{DD}
17	NC	39	NC
18	P2.0/A8	40	P1.0/INT2
19	P2.1/A9	41	P1.1/INT3
20	P2.2/A10	42	P1.2/INT4
21	P2.3/A11	43	P1.3/INT5
22	P2.4/A12	44	P1.4/INT6

LOGIC SYMBOL



BLOCK DIAGRAM



(1) Pins shared with parallel port pins.

Low-voltage single-chip 8-bit microcontroller

80CL580/83CL580

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

GENERAL DESCRIPTION

The 83CL580 is manufactured in an advanced CMOS technology. The instruction set of the 83CL580 is based on that of the 8051. The 83CL580 is an 8-bit general purpose microcontroller especially suited for cordless telephones and mobile communication applications. The device has low power consumption and a wide range of supply voltages. For emulation purposes, the 85CL580 (Piggy-back version) with 256 bytes of RAM is recommended. The 83CL580 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The 83CL580 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions:
49 one-byte, 46 two-byte, and 16 three-byte.

FEATURES

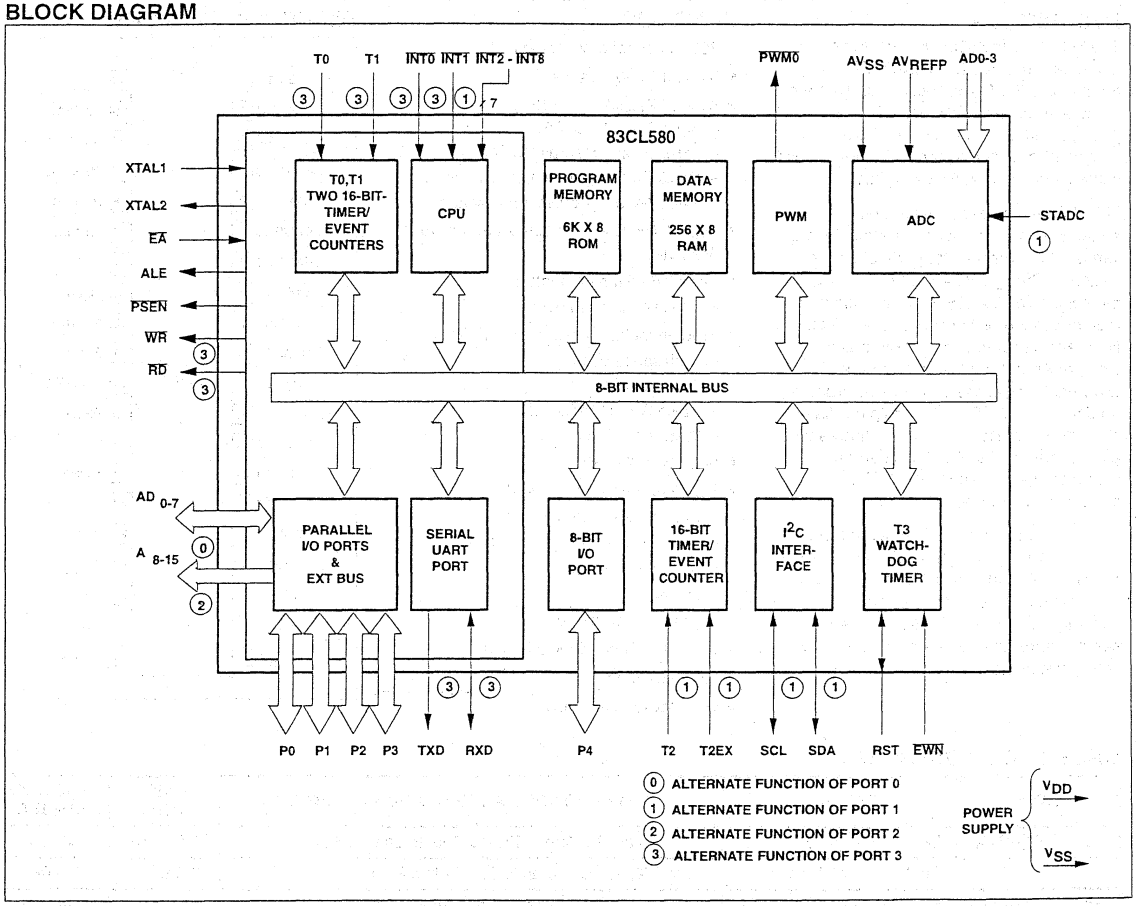
- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a single 56-lead VSO56 or 64-lead QFP64 package
- 6K x 8 ROM, expandable externally to 64K bytes
- 256 bytes RAM, expandable externally to 64K bytes
- Five 8-bit ports, 40 I/O lines
- Three 16-bit timer / event counters
- External memory expandable up to 128K, external ROM up to 64K and / or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector interrupt structure with two priority levels
- Full duplex serial UART
- I^2C-bus interface for serial transfer on two lines
- A/D converter with power-down mode (8-bit, 4 inputs)
- Pulse width modulated output (8-bit resolution)
- Watchdog timer
- Enhanced architecture with:
  - non-page oriented instructions
  - four eight byte RAM register banks
  - direct addressing
  - multiply, divide, subtract and compare instructions
  - stack depth limited only by available internal RAM (max. 256 bytes)
- Power-Down and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 2.5V to 6.0V
- Frequency range of 0 to 12MHz
- Very low current consumption: typically 4.5mA at 2.5V / 8MHz
- Operating temperature range: –40 to +85°C

ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA [1] PART ORDER NUMBER		TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
ROMless	ROM	ROMless	ROM			
P80CL580HFT	P83CL580HFT	P80CL580HF D	P83CL580HF D	–40 to +85 56-Lead Plastic VSO (Very Small Outline) Dual In-line Package	32KHz to 12MHz	SOT190
P80CL580HFH	P83CL580HFH	P80CL580HF B	P83CL580HF B	–40 to +85 64-Lead Plastic Quad Flat Pack	32KHz to 12MHz	SOT319

NOTE:
1. Parts ordered by the Philips North America part number will be marked with the Philips part marking.

BLOCK DIAGRAM



CMOS single-chip 3.0V 8-bit microcontroller

83L51FA/87L51FA

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

DESCRIPTION

The 87L51FA and 83L51FA (hereafter generically referred to as 8XL51FA) Single-Chip 3.0V 8-Bit Microcontrollers are manufactured in an advanced CMOS process and are derivatives of the 80C51 microcontroller family. The 8XL51FA has the same instruction set as the 80C51.

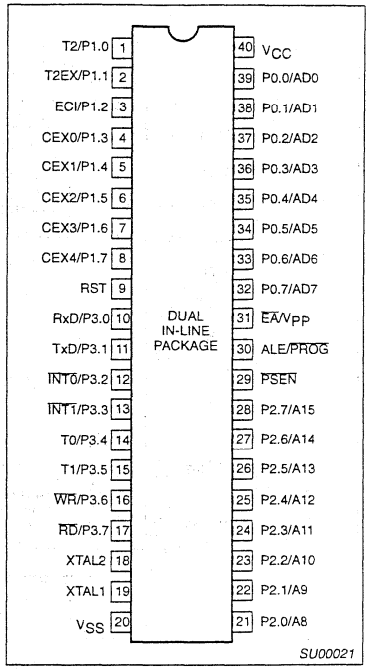
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 8XL51FA contains 8k × 8 memory, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, three 16-bit timer/event counters, a Programmable Counter Array (PCA), a multi-source, two-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XL51FA can be expanded using standard 3.3V TTL compatible memories and logic.

Its added features make it an even more powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multiprocessor communications.

FEATURES

- 80C51 central processing unit
- 3.0 to 4.5V V_{CC} range
- 8k × 8 EPROM (87L51FA)
  8k × 8 ROM (83L51FA)
  - expandable externally to 64k bytes
  - Quick Pulse programming algorithm
  - Two level program security system
- 256 × 8 RAM, expandable externally to 64k bytes
- Three 16-bit timer/counters
  - T2 is an up/down counter
- Programmable Counter Array (PCA)
  - High speed output
  - Capture/compare
  - Pulse Width Modulator
  - Watchdog Timer
- Four 8-bit I/O ports
- Full-duplex enhanced UART
  - Framing error detection
  - Automatic address recognition
- Power control modes
  - Idle mode
  - Power-down mode
- Once (On Circuit Emulation) Mode
- Five package styles
- OTP package available

PIN CONFIGURATIONS

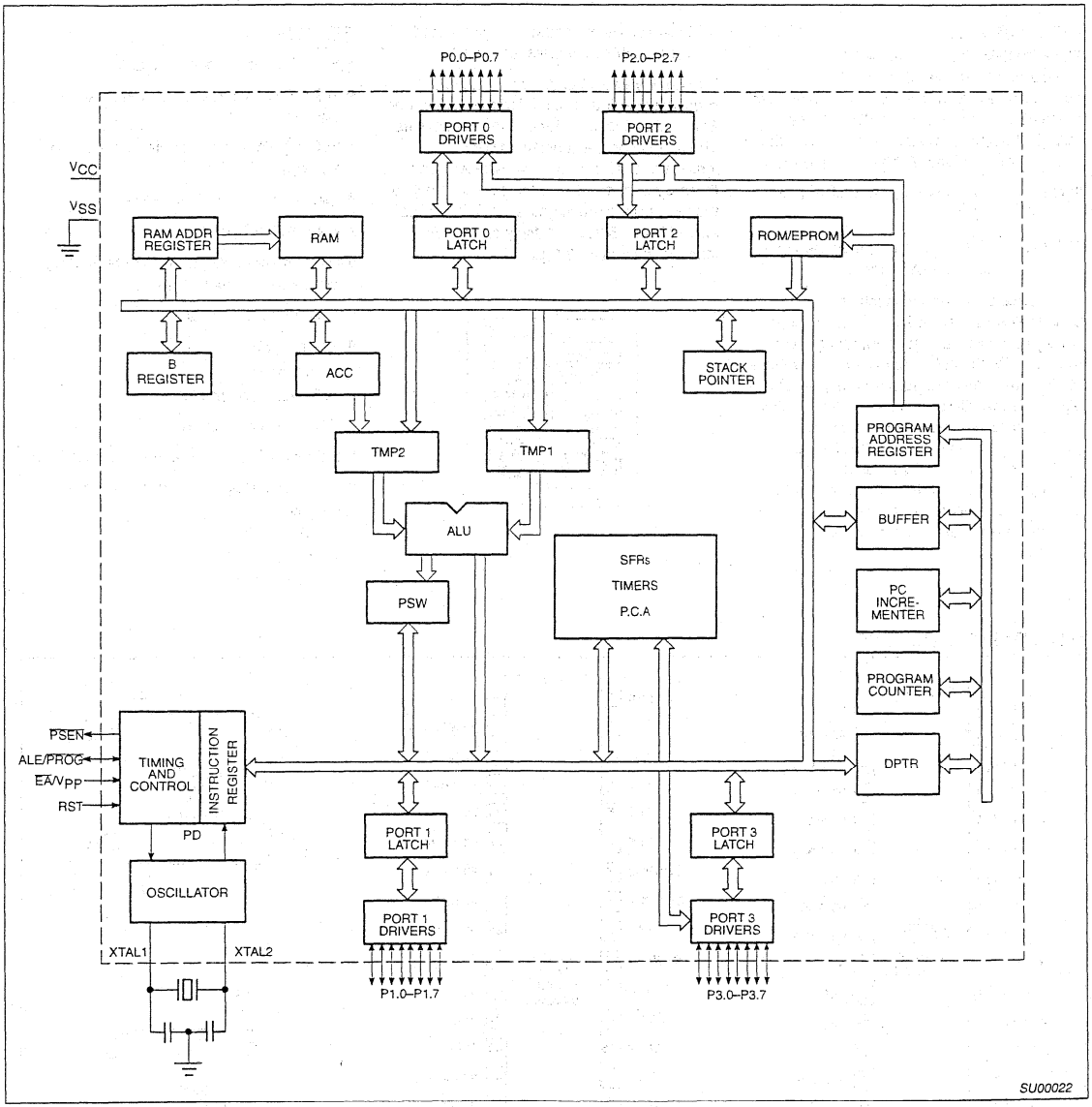


ORDERING INFORMATION

ROM	EPROM[1]		TEMPERATURE RANGE °C AND PACKAGE	FREQ. (MHz)	DRAWING NUMBER
S83L51FA–4N40	S87L51FA–4N40	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	3.5 to 16	0415C
	S87L51FA–4F40	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 16	0590B
S83L51FA–4A44	S87L51FA–4A44	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	3.5 to 16	0403G
	S87L51FA–4K44	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 16	1472A
S83L51FA–4B44	S87L51FA–4B44	OTP	0 to +70, 44-Pin Plastic Quad Flat Pack	3.5 to 16	1118D
S83L51FA–5N40	S87L51FA–5N40	OTP	–40 to +85, 40-Pin Plastic Dual In-line Package	3.5 to 16	0415C
	S87L51FA–5F40	UV	–40 to +85, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 16	0590B
S83L51FA–5A44	S87L51FA–5A44	OTP	–40 to +85, 44-Pin Plastic Leaded Chip Carrier	3.5 to 16	0403G
	S87L51FA–5K44	UV	–40 to +85, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 16	1472A
S83L51FA–5B44	S87L51FA–5B44	OTP	–40 to +85, 44-Pin Plastic Quad Flat Pack	3.5 to 16	1118D
S83L51FA–7N40	S87L51FA–7N40	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	3.5 to 20	0415C
	S87L51FA–7F40	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 20	0590B
S83L51FA–7A44	S87L51FA–7A44	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	3.5 to 20	0403G
	S87L51FA–7K44	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 20	1472A
S83L51FA–8N40	S87L51FA–8N40	OTP	–40 to +85, 40-Pin Plastic Dual In-line Package	3.5 to 20	0415C
	S87L51FA–8F40	UV	–40 to +85, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 20	0590B
S83L51FA–8A44	S87L51FA–8A44	OTP	–40 to +85, 44-Pin Plastic Leaded Chip Carrier	3.5 to 20	0403G
	S87L51FA–8K44	UV	–40 to +85, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 20	1472A

NOTE:
1. OTP = One Time Programmable EPROM. UV = Erasable EPROM.

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller 83C654

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

DESCRIPTION

The P83C654 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C654 has the same instruction set as the 80C51. Two versions of the derivative exist:

83C654 — 16k bytes mask programmable ROM

87C654 — EPROM version (described in a separate data sheet)

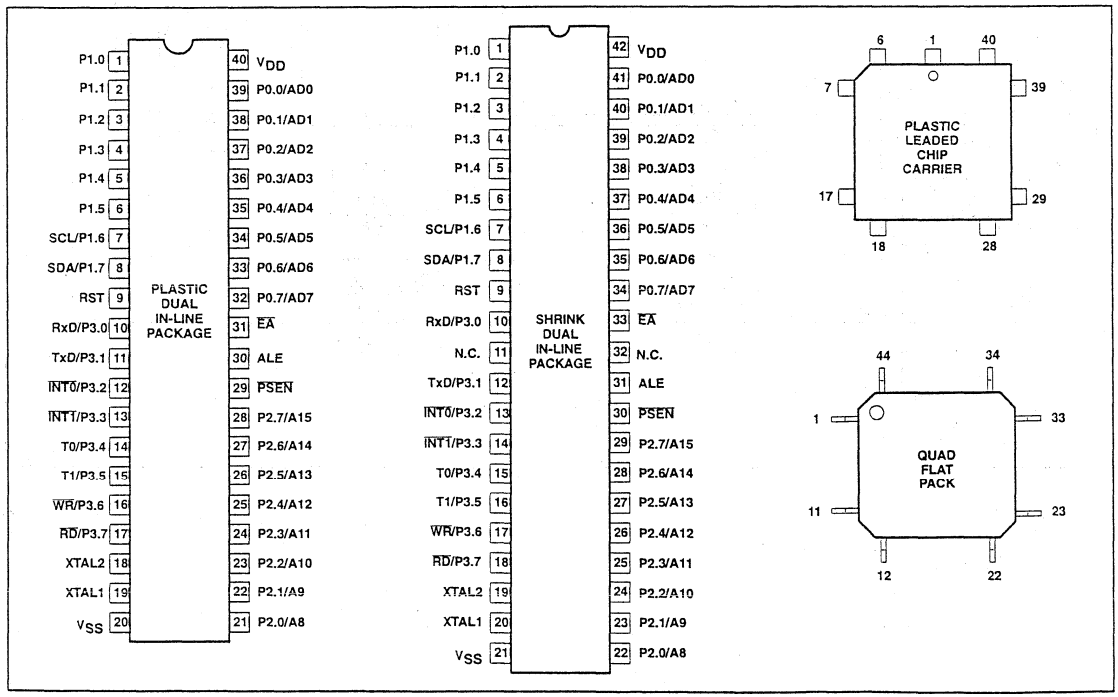
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 83C654 contains a non-volatile 16k × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I²C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC654 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16(24)MHz crystal, 58% of the instructions are executed in 0.75(0.5)µs and 40% in 1.5(1)µs. Multiply and divide instructions require 3(2)µs.

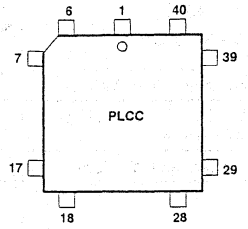
FEATURES

- 80C51 central processing unit
- 16k × 8 ROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- ROM code protection
- Extended frequency range: 1.2 to 24 MHz
- Three operating ambient temperature ranges:
  - 0 to +70°C
  - –40 to +85°C
  - –40 to +125°C

PIN CONFIGURATIONS

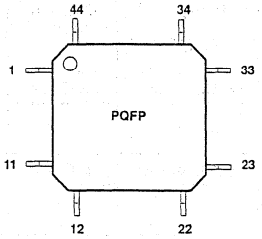


PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	P2.0/A8
3	P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6/SCL	30	P2.6/A14
9	P1.7/SDA	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RxD	33	ALE
12	NC	34	NC
13	P3.1/TxD	35	$\overline{EA}$
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{DD}

PLASTIC QUAD FLAT PACK PIN FUNCTIONS

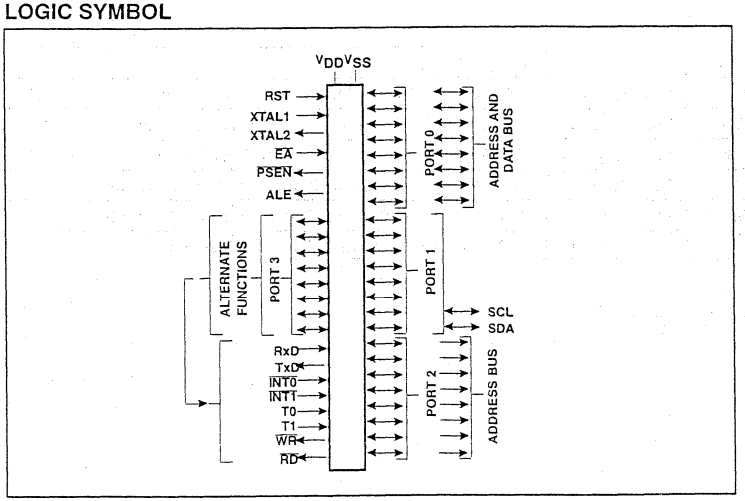


Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6/SCL	24	P2.6/A14
3	P1.7/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE
6	V_{SS4}	28	V_{SS2}
7	P3.1/TxD	29	$\overline{EA}$/V_{PP}
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS1}	38	V_{DD}
17	NC	39	V_{SS3}
18	P2.0/A8	40	P1.0
19	P2.1/A9	41	P1.1
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

NOTES TO QFP ONLY:

1. Due to EMC improvements, all V_{SS} pins (6, 16, 28, 39) must be connected to V_{SS} on the 80C652/83C654.

LOGIC SYMBOL



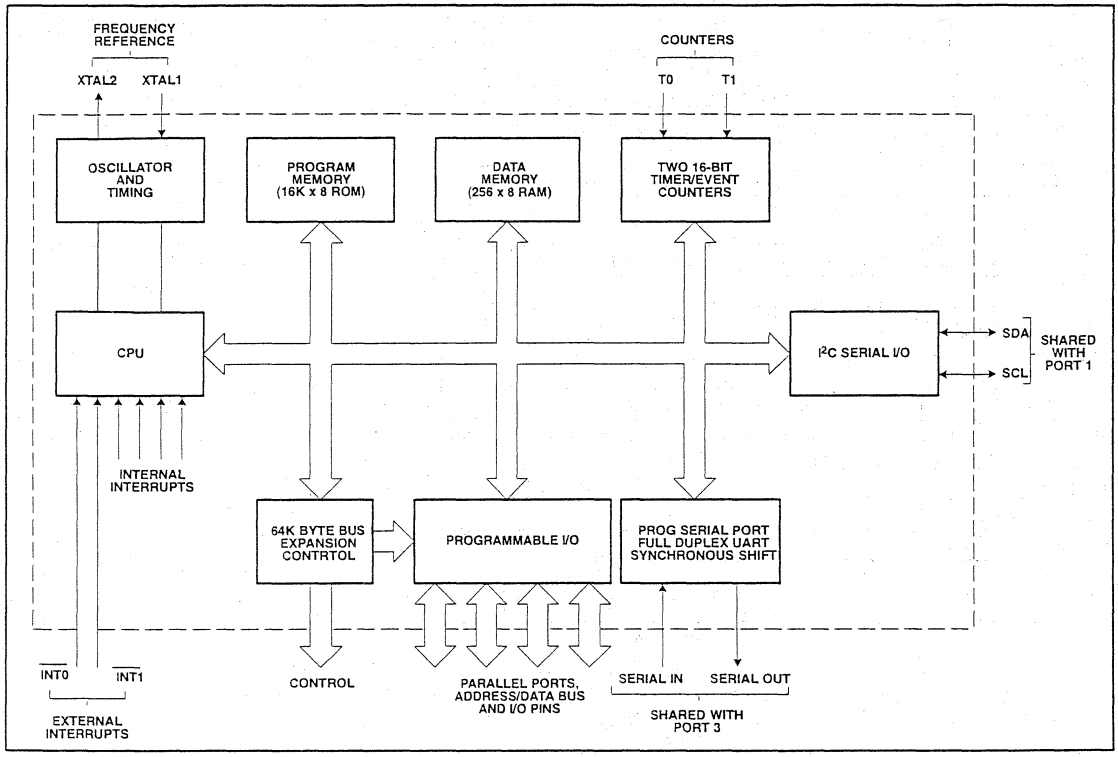
ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER		Drawing Number	TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz[2,3]
ROMless[1]	ROM	ROMless[1]	ROM			
P80C652FBP	P83C654FBP/xxx	P80C652FBPN	P83C654FBPN	SOT129	0 to +70, Plastic Dual In-line Package	16
					0 to +70, Ceramic Dual In-line Package w/Window	16
P80C652FBA	P83C654FBA/xxx	P80C652FBAA	P83C654FBAA	SOT187	0 to +70, Plastic Leaded Chip Carrier	16
P80C652FBB	P83C654FBB/xxx	P80C652FBBB	P83C654FBBB	SOT307-2[5]	0 to +70, Plastic Quad Flat Pack	16
	P83C654FBR/xxx			SOT270	0 to +70, Plastic Shrink Dual In-Line Package	
P80C652FFP	P83C654FFP/xxx	P80C652FFPN	P83C654FFPN	SOT129	–40 to +85, Plastic Dual In-line Package	16
P80C652FFA	P83C654FFA/xxx	P80C652FFAA	P83C654FFAA	SOT187	–40 to +85, Plastic Leaded Chip Carrier	16
P80C652FFB	P83C654FFB/xxx	P80C652FFBB	P83C654FFBB	SOT307-2[5]	–40 to +85, Plastic Quad Flat Pack	16
P80C652FHP	P83C654FHP/xxx	P80C652FHPN	P83C654FHPN	SOT129	–40 to +125, Plastic Dual In-line Package	16
P80C652FHA	P83C654FHA/xxx	P80C652FHAA	P83C654FHAA	SOT187	–40 to +125, Plastic Leaded Chip Carrier	16
P80C652FHB	P83C654FHB/xxx	P80C652FHBB	P83C654FHBB	SOT307-2[5]	–40 to +125, Plastic Quad Flat Pack	16
P80C652IBP	P83C654IBP/xxx	P80C652IBPN	P83C654IBPN	SOT129	0 to +70, Plastic Dual In-line Package	24
P80C652IBA	P83C654IBA/xxx	P80C652IBAA	P83C654IBAA	SOT187	0 to +70, Plastic Leaded Chip Carrier	24
P80C652IBB	P83C654IBB/xxx	P80C652IBBB	P83C654IBBB	SOT307-2[5]	0 to +70, Plastic Quad Flat Pack	24
P80C652IFP	P83C654IFP/xxx	P80C652IFPN	P83C654IFPN	SOT129	–40 to +85, Plastic Dual In-line Package	24
P80C652IFA	P83C654IFA/xxx	P80C652IFAA	P83C654IFAA	SOT187	–40 to +85, Plastic Leaded Chip Carrier	24
P80C652IFB	P83C654IFB/xxx	P80C652IFBB	P83C654IFBB	SOT307-2[5]	–40 to +85, Plastic Quad Flat Pack	24

NOTES:
1. For full specification, see the 80C652/83C652 data sheet.
2. 83C654 frequency range is 1.2MHz – 16MHz or 1.2MHz – 24MHz.
3. For specification of the EPROM version, see the 87C654 data sheet.
4. xxx denotes the ROM code number.
5. SOT311 replaced by SOT307-2.

EPROM[3]	Drawing Number	TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz[2,3]
S87C654-4N40	0415C	0 to +70, Plastic Dual In-line Package	16
S87C654-4F40	0590B	0 to +70, Ceramic Dual In-line Package w/Window	16
S87C654-4A44	0403G	0 to +70, Plastic Leaded Chip Carrier	16
S87C654-4K44	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
S87C654–4B44	1118D	0 to +70, PlasticQuad Flat Pack	16
S87C654-5N40	0415C	–40 to +85, Plastic Dual In-line Package	16
S87C654-5F40	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	16
S87C654-5A44	0403G	–40 to +85, Plastic Leaded Chip Carrier	16
S87C654–5K44	1472A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	16
S87C654-5B44	1118D	–40 to +85, Plastic Quad Flat Pack	16
S87C654–7N40	0415C	0 to +70, Plastic Dual In-line Package	20
S87C654–7F40	0590B	0 to +70, Ceramic Dual In-line Package w/Window	20
S87C654–7A44	0403G	0 to +70, Plastic Leaded Chip Carrier	20
S87C654–7K44	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	20
S87C654–8N40	0415C	–40 to +85, Plastic Dual In-line Package	20
S87C654–8F40	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	20
S87C654–8A44	0403G	–40 to +85, Plastic Leaded Chip Carrier	20

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller with on-chip EEPROM

80C851/83C851

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

DESCRIPTION

The Philips 80C851/83C851 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The 80C851/83C851 has the same instruction set as the 80C51. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. The Philips epitaxial substrate minimizes latch-up sensitivity.

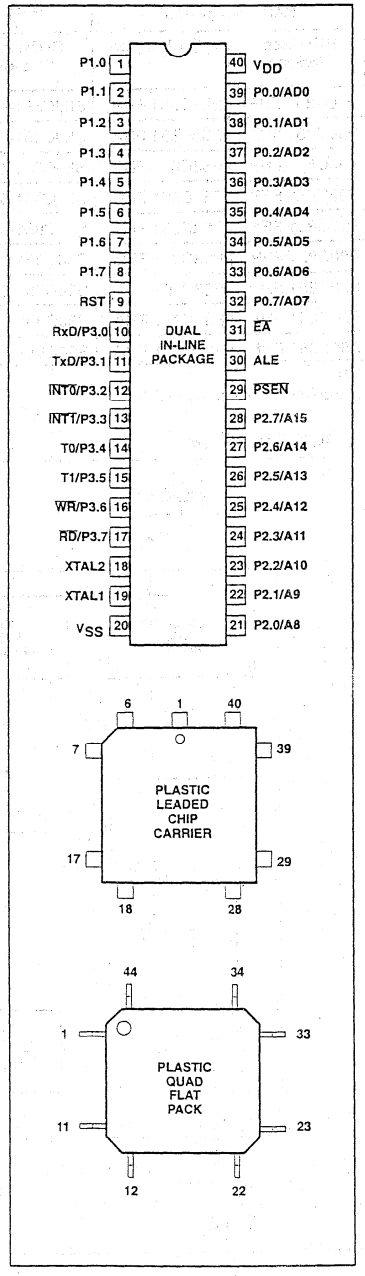
The 80C851/83C851 contains a 4k × 8 ROM with mask-programmable ROM code protection, a 128 × 8 RAM, 256 × 8 EEPROM, 32 I/O lines, two 16-bit counter/timers, a seven-source, five vector, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 80C851/83C851 has two software selectable modes of power reduction — idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM and EEPROM contents but freezes the oscillator, causing all other chip functions to be inoperative.

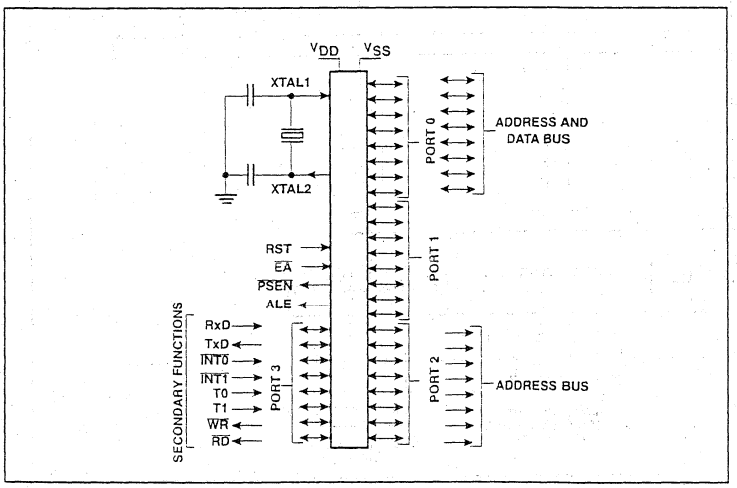
FEATURES

- 80C51 based architecture
  - 4k × 8 ROM
  - 128 × 8 RAM
  - Two 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Non-volatile 256 × 8-bit EEPROM (electrically erasable programmable read only memory)
  - On-chip voltage multiplier for erase/write
  - 50,000 erase/write cycles per byte
  - 10 years non-volatile data retention
  - Infinite number of read cycles
  - User selectable security mode
  - Block erase capability
- Mask-programmable ROM code protection
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- 1.2 to 16MHz
- Three package styles
- Three temperature ranges
- ROM code protection

PIN CONFIGURATIONS



LOGIC SYMBOL

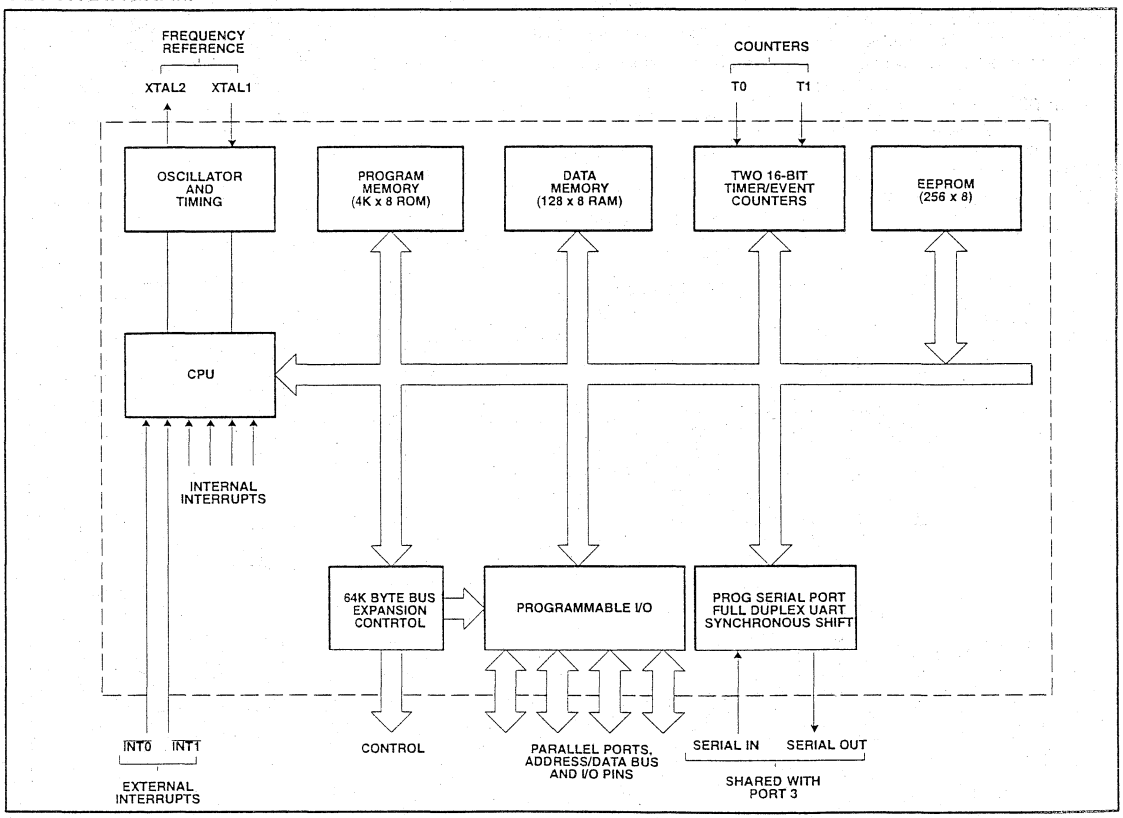


ORDERING INFORMATION

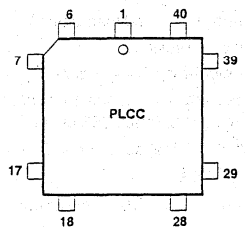
PHILIPS PART ORDER NUMBER PART MARKING		NORTH AMERICA PHILIPS PART ORDER NUMBER		TEMPERATURE RANGE °C AND PACKAGE	FREQ. (MHz)	DRAWING NUMBER
ROMless Version	ROM Version	ROMless Version	ROM Version			
P80C851 FBP	P83C851 FBP	S80C851-4N40	S83C851-4N40	0 to +70, Plastic Dual In-line Package	1.2 to 16	SOT129
P80C851 FBA	P83C851 FBA	S80C851-4A44	S83C851-4A44	0 to +70, Plastic Leaded Chip Carrier	1.2 to 16	SOT187
P80C851 FBB	P83C851 FBB	S80C851-4B44	S83C851-4B44	0 to +70, Plastic Quad Flat Pack	1.2 to 16	SOT307-2 [1]
P80C851 FFP	P83C851 FFP	S80C851-5N40	S83C851-5N40	–40 to +85, Plastic Dual In-line Package	1.2 to 16	SOT129
P80C851 FFA	P83C851 FFA	S80C851-5A44	S83C851-5A44	–40 to +85, Plastic Leaded Chip Carrier	1.2 to 16	SOT187
P80C851 FFB	P83C851 FFB	S80C851-5B44	S83C851-5B44	–40 to +85, Plastic Quad Flat Pack	1.2 to 16	SOT307-2 [1]
P80C851 FHP	P83C851 FHP	S80C851-6N40	S83C851-6N40	–40 to +125, Plastic Dual In-line Package	1.2 to 16	SOT129
P80C851 FHA	P83C851 FHA	S80C851-6A44	S83C851-6A44	–40 to +125, Plastic Leaded Chip Carrier	1.2 to 16	SOT187
P80C851 FHB	P83C851 FHB	S80C851-6B44	S83C851-6B44	–40 to +125, Plastic Quad Flat Pack	1.2 to 16	SOT307-2 [1]

NOTE:
1. SOT311 replaced by SOT307-2.

BLOCK DIAGRAM

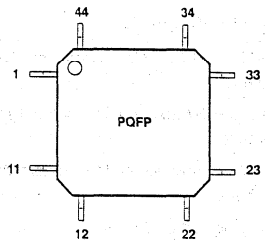


PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	P2.0/A8
3	P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6	30	P2.6/A14
9	P1.7	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RxD	33	ALE
12	NC	34	NC
13	P3.1/TxD	35	$\overline{EA}$
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{DD}

PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6	24	P2.6/A14
3	P1.7	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE
6	NC	28	NC
7	P3.1/TxD	29	$\overline{EA}$
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS}	38	V_{DD}
17	NC	39	V_{SS}
18	P2.0/A8	40	P1.0
19	P2.1/A9	41	P1.1
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

Low-voltage single-chip 8-bit microcontrollers

83CL781/83CL782

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

GENERAL DESCRIPTION

The 83CL781 and 83CL782 are manufactured in an advanced CMOS technology. The instruction set of the 83CL781/83CL782 is based on that of the 8051. The 83CL781/83CL782 is an 8-bit general purpose microcontroller especially suited for cordless telephone applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the 85CL782 (Piggy-back version) with 256 bytes of RAM is recommended. The 83CL781/83CL782 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The 83CL781/83CL782 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

The 83CL782 is a faster version of the 83CL781 with a maximum speed of 12MHz at $V_{DD} \geq 3.1V$.

FEATURES

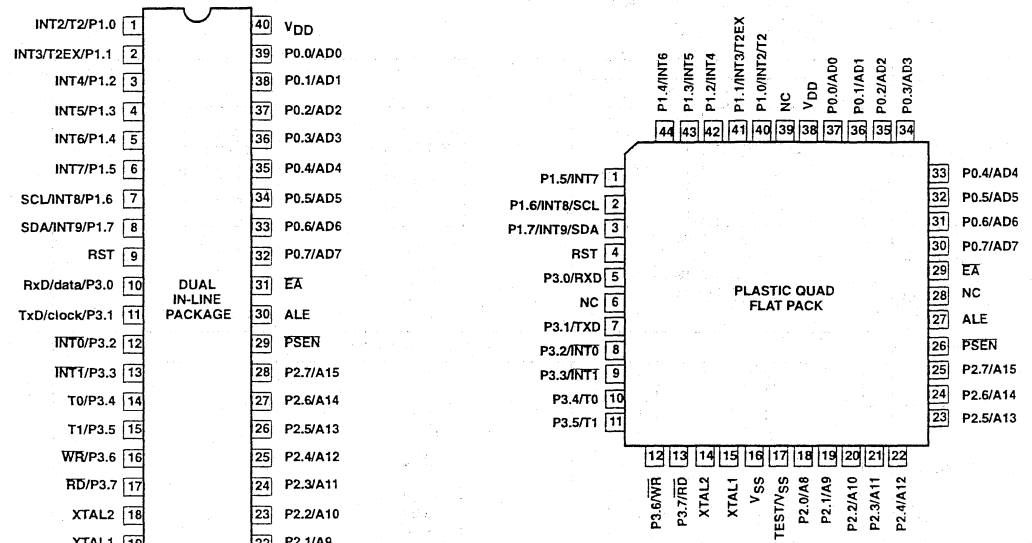
- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a single package
- 16K × 8 ROM, expandable externally to 64K bytes
- 256 bytes RAM, expandable externally to 64K bytes
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- External memory expandable up to 128K, external ROM up to 64K and/or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector interrupt structure with two priority levels
- Full duplex serial UART
- I^2C bus interface for serial transfer on two lines.
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight-byte RAM register banks
  - stack depth limited only by available internal RAM (max. 256 bytes)
  - multiply, divide, subtract and compare instructions
- Power-down and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8V to 6.0V
- Frequency range of DC to 12MHz
- 12MHz operation at 3.1V (8XCL782)
- Very low current consumption, typ 8mA at 12MHz/3.1V
- Operating temperature range:
  - 83CL781: -40 to +85°C
  - 83CL782: -25 to +55°C

ORDERING INFORMATION

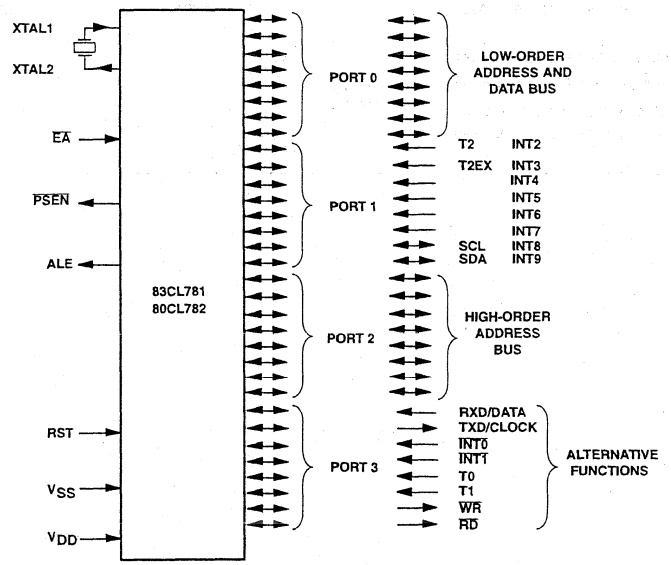
PHILIPS PART ORDER NUMBER PART MARKING	PHILIPS NORTH AMERICA[3] PART ORDER NUMBER	TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
ROM	ROM			
P83CL781HFP	P83CL781HF N	–40 to +85; 40-Pin Plastic DIP[1]	DC to 12MHz	SOT129
P83CL781HFH	P83CL781HF B	–40 to +85; 44-Pin Plastic QFP[2]	DC to 12MHz	SOT205
P83CL781HFH	P83CL781HF B	–40 to +85; 44-Pin Plastic QFP[2]	DC to 12MHz	SOT307
P83CL782HDP	P83CL782HD N	–25 to +55 40-Pin Plastic DIP[1]	DC to 12MHz	SOT129
P83CL782HDH	P83CL782HD B	–25 to +55 44-Pin Plastic QFP[2]	DC to 12MHz	SOT205
P83CL782HDH	P83CL782HD B	–25 to +55 44-Pin Plastic QFP[2]	DC to 12MHz	SOT307

NOTES:
1. DIP = Dual In-line Package
2. QFP = Quad Flat Pack.
   Two body sizes are available: SOT205 – 14mm × 14mm and SOT307 – 10mm × 10mm. See package dimension section for details.
3. Parts ordered by the Philips North America part number will be marked with the Philips part marking.

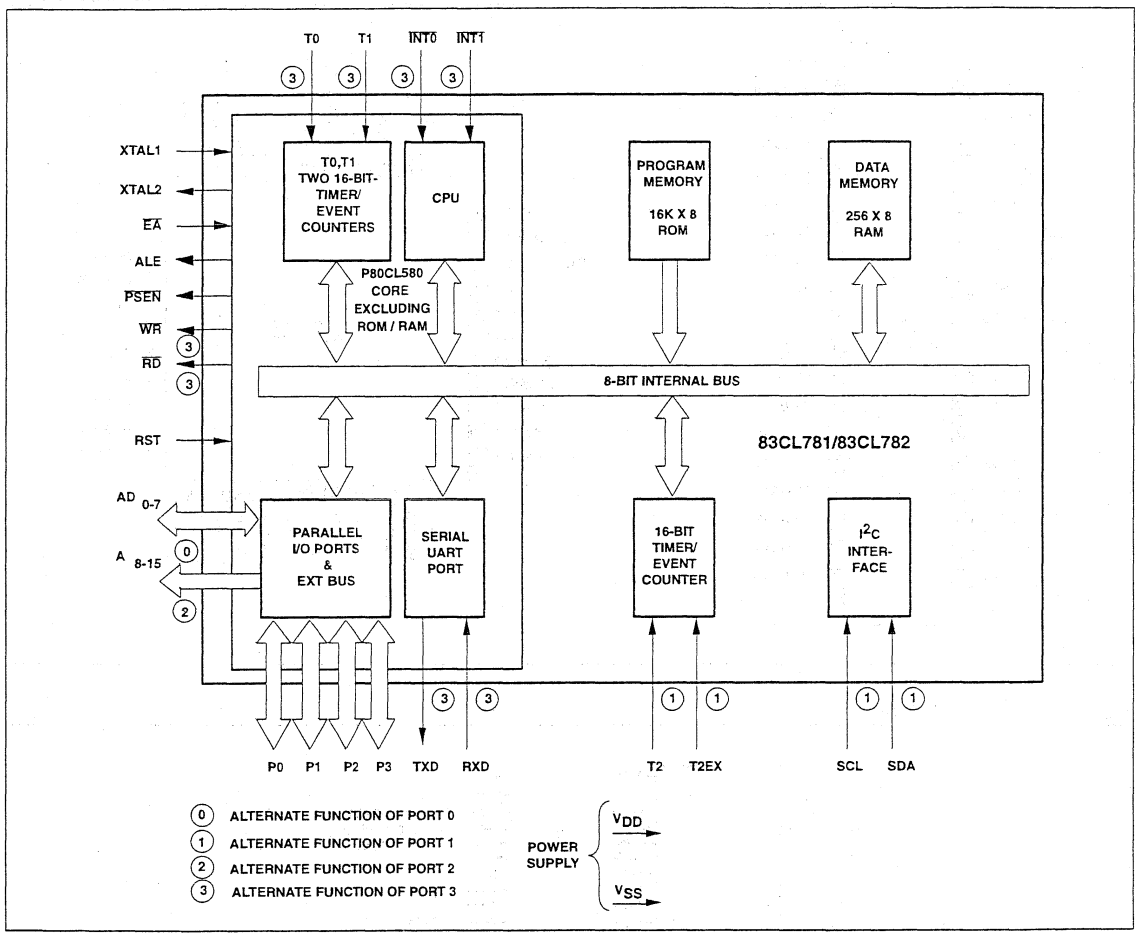
PIN CONFIGURATIONS



FUNCTIONAL DIAGRAM



BLOCK DIAGRAM



Digital phase-locked-loop filter

74HC/HCT297

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC06 OR DATA SHEET

FEATURES

- Digital design avoids analog compensation errors
- Easily cascadable for higher order loops
- Useful frequency range:
  DC to 55 MHz typical (K-clock)
  DC to 35 MHz typical (I/D-clock)
- Dynamically variable bandwidth
- Very narrow bandwidth attainable
- Power-on reset
- Output capability: standard/bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT297 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT297 are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-n counter, to build first order phase-locked-loops.

Both EXCLUSIVE-OR (XORPD) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lock-range.

Proper partioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Fig. 7) or to cascade to higher order phase-locked-loops.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay I/D_{CP} to I/D_{OUT} ϕA_1, ϕB to $XORPD_{OUT}$ ϕB, ϕA_2 to $ECPD_{OUT}$	C_L = 15 pF V_{CC} = 5 V	 15 13 19	 18 13 19	ns
f_{max}	maximum clock frequency K_{CP} I/D_{CP}		 63 41	 68 40	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	18	19	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16L; SOT162A).

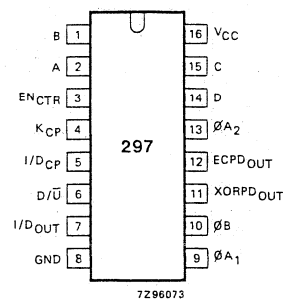


Fig. 1 Pin configuration.

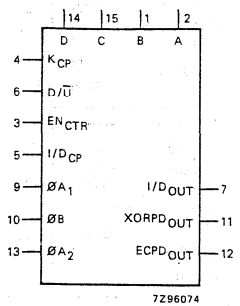


Fig. 2 Logic symbol.

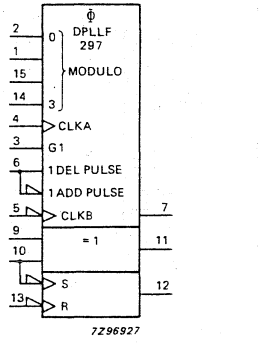


Fig. 3 IEC logic symbol.

Phase-locked-loop with VCO | 74HC/HCT4046A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC06 OR DATA SHEET

FEATURES

- Low power consumption
- Centre frequency of up to 17 MHz (typ.) at V_{CC} = 4.5 V
- Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operating power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- I_{CC} category: MSI

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_o	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ V_{CC} = 5 V	19	19	MHz
C_I	input capacitance (pin 5)		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

GND = 0 V; T_{amb} = 25 °C

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections see Figs 22, 23 and 24.

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).
16-lead mini-pack; plastic (SO16; SOT109A).

GENERAL DESCRIPTION

The 74HC/HCT4046A are high-speed Si-gate CMOS devices and are pin compatible with the "4046" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4046A are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "4046A" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

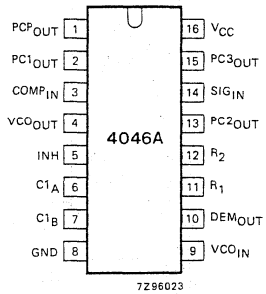


Fig. 1 Pin configuration.

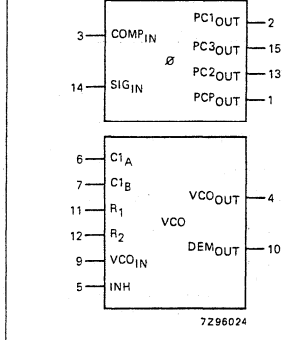


Fig. 2 Logic symbol.

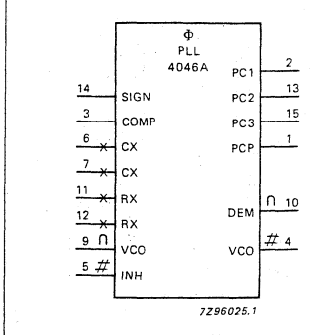


Fig. 3 IEC logic symbol.

Phase-locked-loop with lock detector 74HC/HCT7046A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC06 OR DATA SHEET

FEATURES

- Low power consumption
- Centre frequency up to 17 MHz (typ.) at V_{CC} = 4.5 V
- Choice of two phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop;
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operation power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- I_{CC} category: MSI

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_o	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ V_{CC} = 5 V	19	19	MHz
C_I	input capacitance (pin 5)		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

GND = 0 V; T_{amb} = 25 °C

Notes

1. Applies to the phase comparator section only (VCO disabled).
   For power dissipation of VCO and demodulator sections see Figs 20, 21 and 22.
2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38CP).
16-lead mini-pack; plastic (SO16; SOT109A).

GENERAL DESCRIPTION

The 74HC/HCT7046 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT7046 are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input.

A lock detector is provided and this gives a HIGH level at pin 1 (LD) when the PLL is locked. The lock detector capacitor must be connected between pin 15 (C_{LD}) and pin 8 (GND). The value of the C_{LD} capacitor can be determined, using information supplied in Fig. 32

The input signal can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "7046" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

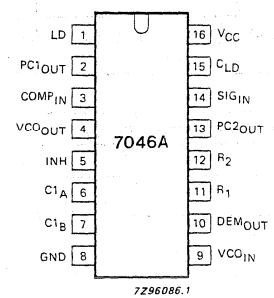


Fig. 1 Pin configuration.

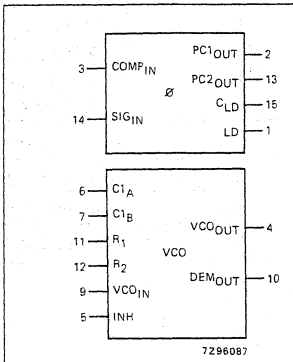


Fig. 2 Logic symbol.

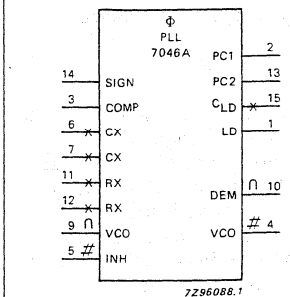


Fig. 3 IEC logic symbol.

Timer for NiCd and NiMH chargers — 74LV4799

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC24 OR DATA SHEET

FEATURES

- Wide supply voltage range of 0.9 V to 6 V allows 1 to 4-cell applications
- 10 V allowed on special inputs
- Supports virtually all battery chargers, including switched-mode power supplies
- On-chip timer calculates the actual capacity of the battery by measuring the charge time, discharge time and self-discharge time
- Automatic switch-over to trickle charge after completion of the charge time
- Can be adjusted for use with different types of batteries:
  - Charge time: 4 to 16 hours
  - Discharge time: 15 minutes to 4.7 hours
  - Self-discharge time: 50 to 100 days
- Battery status indication included:
  - $\overline{\text{LED}}$ output for charging/full indication
  - $\overline{\text{MOLLI}}$ output for battery-low indication
- LED mode select allows two different methods of indication
- Automatic power-ON reset
- Low power consumption
- Requires only a few peripheral components
- Very accurate on-chip oscillator
- Scan test facilities included
- I_{CC} category: non-standard.

APPLICATIONS

- Time-controlled NiCd and NiMH low-current chargers
- Domestic appliances such as rechargeable battery shavers, electric toothbrushes etc.
- Portable equipment such as notebook PCs, laptop PCs, camera flash units etc.
- Personal communications like cordless telephones, personal mobile radios, pagers etc.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage		0.9	–	6.0	V
I_{CC}	operating supply current	V_{CC} = 3.3 V; self-discharge mode; R_S = 100 kΩ; C_1 = 220 nF	–	36	–	µA
Δf	oscillator frequency tolerance	V_{CC} = 1 to 6 V	–	–	7	%

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4799N	16	DIL16	plastic	SOT38Z
74LV4799D	16	SO16	plastic	SOT109A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{LED}}$	LED driver output pin (active LOW)
2	EN	enable output (active HIGH)
3	$\overline{\text{EN}}$	enable output (active LOW)
4	V_{in}	external supply input
5	PWRS	power sense input
6	$\overline{\text{MOLLI}}$/SCO	more-or-less-low-indication output (active LOW)/scan test output
7	SEL	LED mode select input
8	GND	ground (0 V)
9	$\overline{\text{DIS}}$	discharge input (active LOW)
10	R_C	external resistor pin 3-state oscillator output (charge)
11	R_D	external resistor pin 3-state oscillator output (discharge)
12	R_S	external resistor pin 3-state oscillator output (self-discharge)
13	I_{OSC}	oscillator input
14	SCAN	scan test mode select input (active HIGH)
15	SCI	scan test input
16	V_{CC}	positive supply voltage

Timer for NiCd and NiMH chargers 74LV4799

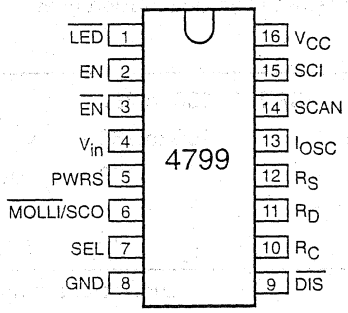


Fig.1 Pin configuration.

GENERAL DESCRIPTION

The 74LV4799 is a low-voltage Si-gate CMOS control IC for battery management. It consists of:

- 17-stage divider
- 10-stage up/down counter
- Control logic
- Integrated precision oscillator (using external timing components)
- Automatic power-ON reset
- Scan test facilities
- Battery charging/full indication output ($\overline{LED}$)
- Battery-low indication output ($\overline{MOLLI}$)
- Open-drain-N outputs for driving the load transistor.

Battery management with the 74LV4799 is based on the principle of time measurement. It measures the charge time, discharge time and self-discharge time by means of a very accurate on-chip oscillator, a divider and an up/down counter.

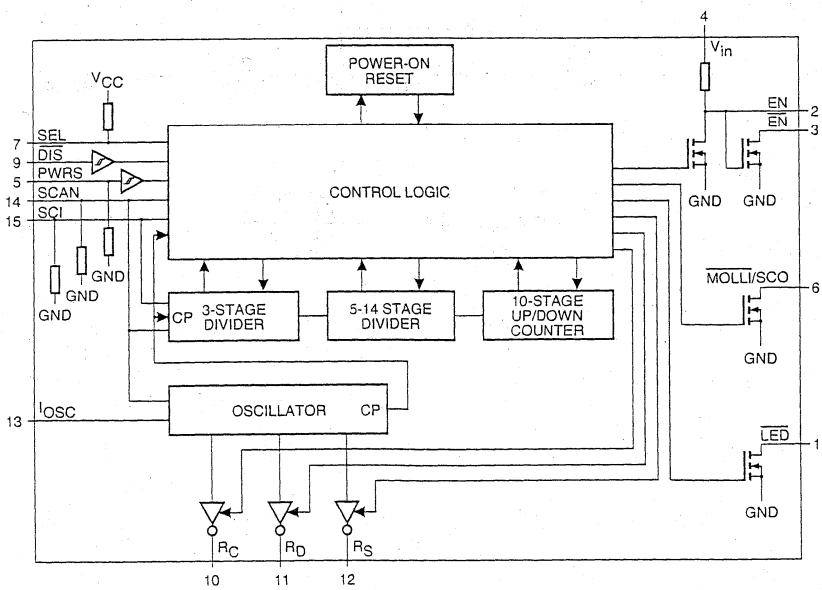


Fig.2 Functional diagram.

Breakover diodes BR211 series

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC02 OR DATA SHEET

A range of bidirectional diodes in hermetically sealed axial-leaded implosion-diode glass outlines with a +/– 12% tolerance of breakover voltage. These devices feature controlled breakover voltage and high holding current together with a good peak current handling capability. Typical applications include transient overvoltage in telephony equipment, data transmission and remote instrumentation lines.

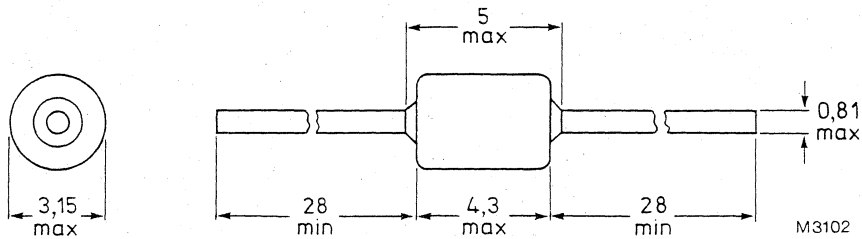
QUICK REFERENCE DATA

			BR211–100 to 280	
Breakover voltage	$V_{(BO)}$	nom.	100 to 280	V
Holding current	I_H	>	150	mA
Transient peak current (10/320 μs impulse)	I_{TSM}	max.	40	A

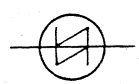
MECHANICAL DATA

Dimensions in mm

Fig.1 SOD-84.



Circuit symbol:



Net mass: 0.35 g.

N-channel enhancement mode vertical D-MOS transistor

BS107

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High speed switching
- No secondary breakdown

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

PIN CONFIGURATION

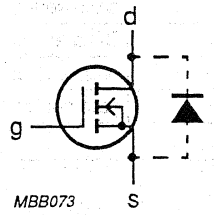


Fig.1 Symbol.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	source
2	gate
3	drain

Note: Other pinnings are available on request.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	drain current	150	mA
$R_{DS(on)}$	drain-source on-resistance	28	Ω
$V_{GS(th)}$	gate threshold voltage	2.4	V

N-channel enhancement mode vertical D-MOS transistor

BS108

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

PINNING

PIN	DESCRIPTION
1	source
2	gate
3	drain

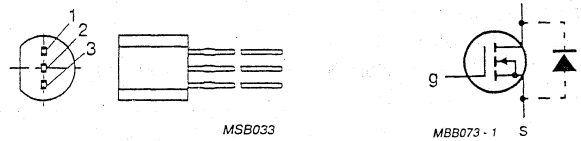


Fig.1 Simplified outline (TO-92 variant) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125 K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 x 10 mm

N-channel vertical D-MOS transistor BS170

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}.
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

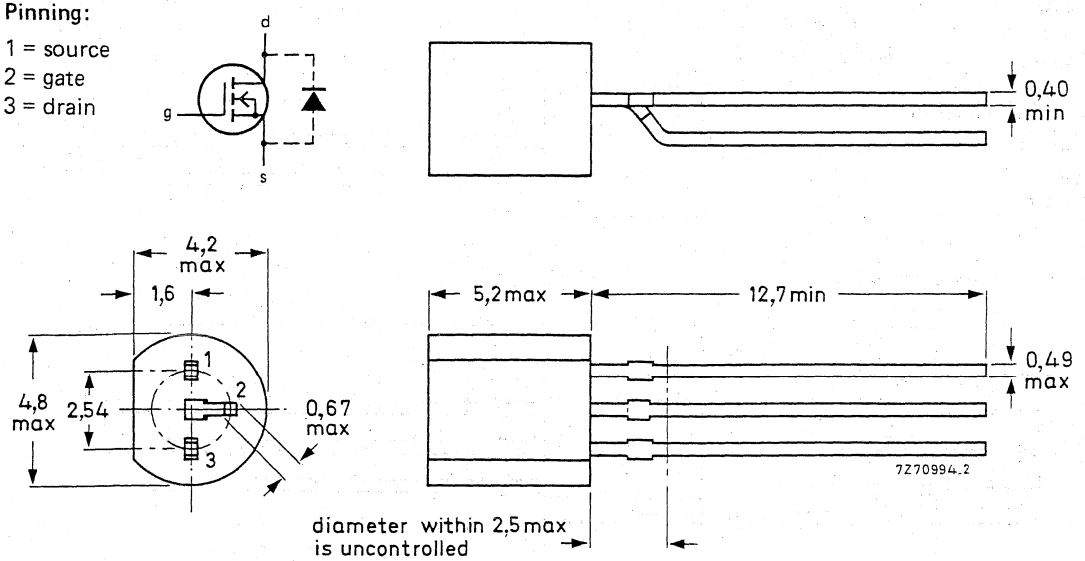
Drain-source voltage	V_{DS}	max.	60 V
Gate-source voltage	V_{GS}	max.	15 V
Drain current (DC)	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830 mW
Junction temperature	T_j	max.	150 °C
Drain-source ON-resistance V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	max.	5 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = source
2 = gate
3 = drain



Note: Various pin configurations available.

N-channel enhancement mode vertical D-MOS transistors

BSN254/A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-channel enhancement mode vertical D-MOS transistors in TO-92 variant envelope and designed for use as line current interrupters in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2 V

MECHANICAL DATA

Dimensions in mm

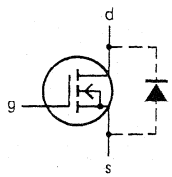
Fig.1 TO-92 variant.

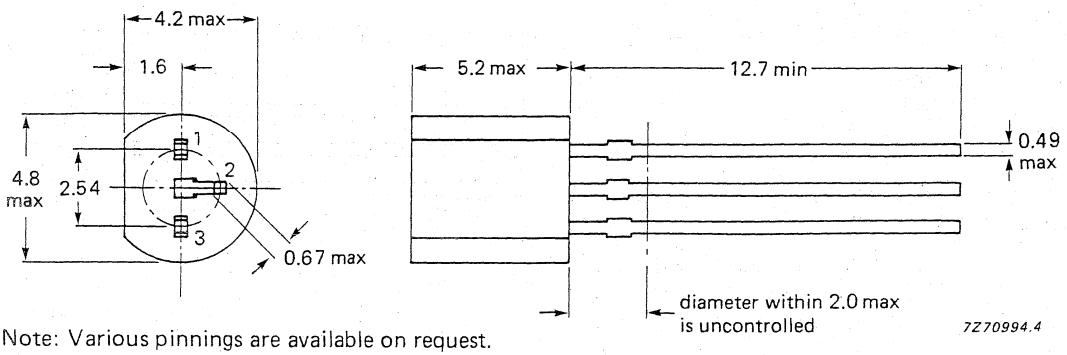
Pinning (BSN254)

1 = gate
2 = drain
3 = source

Pinning (BSN254A)

1 = source
2 = gate
3 = drain





Note: Various pinnings are available on request.

N-channel enhancement mode vertical D-MOS transistor

BSP126

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Drain current (DC)	I_D	max.	350 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5 W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2 V

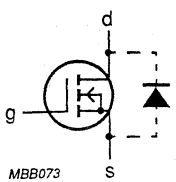
MECHANICAL DATA

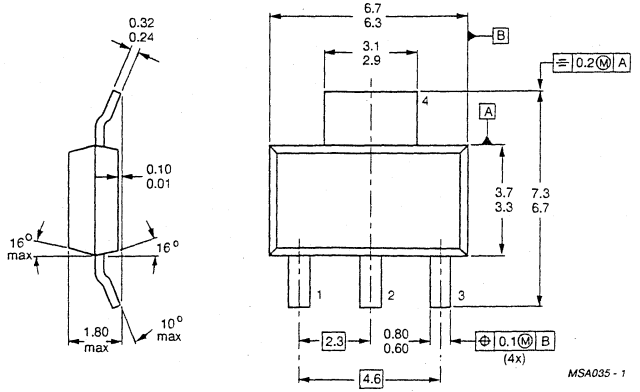
Fig.1 SOT223.

Dimensions in mm

Pinning

1 = gate
2 = drain
3 = source
4 = drain





Marking code

BSP126

P-channel enhancement mode vertical D-MOS transistor

BSP225

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope, intended for use in relay, high-speed and line transformer drivers.

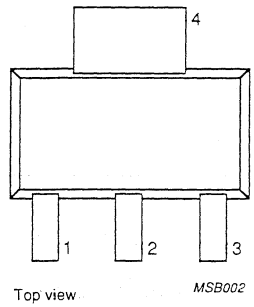
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		250	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	15	Ω
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION



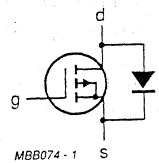


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP254/A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

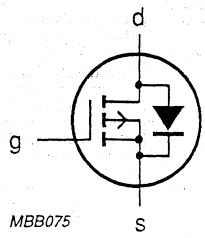


Fig.1 Symbol.

PINNING - TO-92 variant (BSP254)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant (BSP254A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	-	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	-	20	V
$-I_D$	drain-current	DC	-	-	0.2	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	-	1	W
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	-	10	15	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	-	mS

N-channel enhancement mode vertical D-MOS transistor

BSP89

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptors in telephone sets and for application in relay, high speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

PINNING

PIN	DESCRIPTION
Code: BSP89	
1	gate
2	drain
3	source
4	drain

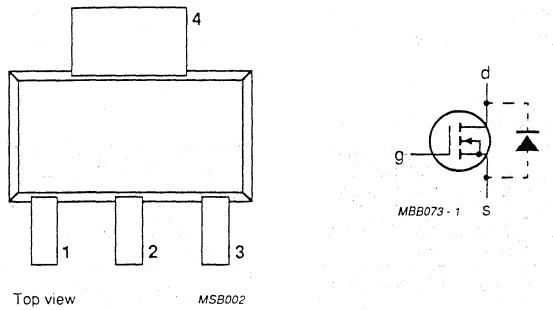


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

P-channel enhancement mode vertical D-MOS transistor

BSP92

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Low threshold voltage $V_{GS(th)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$-V_{DS}$	drain-source voltage	240	V
$-I_D$	DC drain current	180	mA
$R_{DS(on)}$	drain-source on-resistance	20	Ω
$-V_{GS(th)}$	gate-source threshold voltage	1.8	V

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptor in telephone sets and for application in relay, high speed and line transformer drivers.

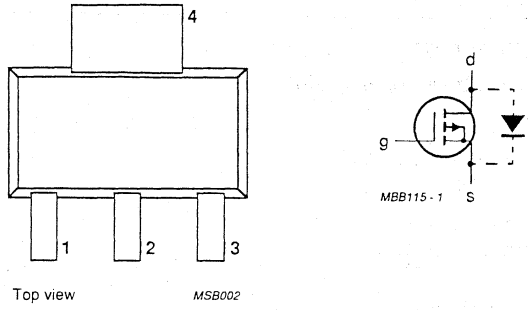


Fig.1 Simplified outline (SOT223) and symbol.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	DC drain current		–	180	mA
$-I_{DM}$	peak drain current		–	720	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

N-channel enhancement mode vertical D-MOS transistor

BSS89

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and highspeed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

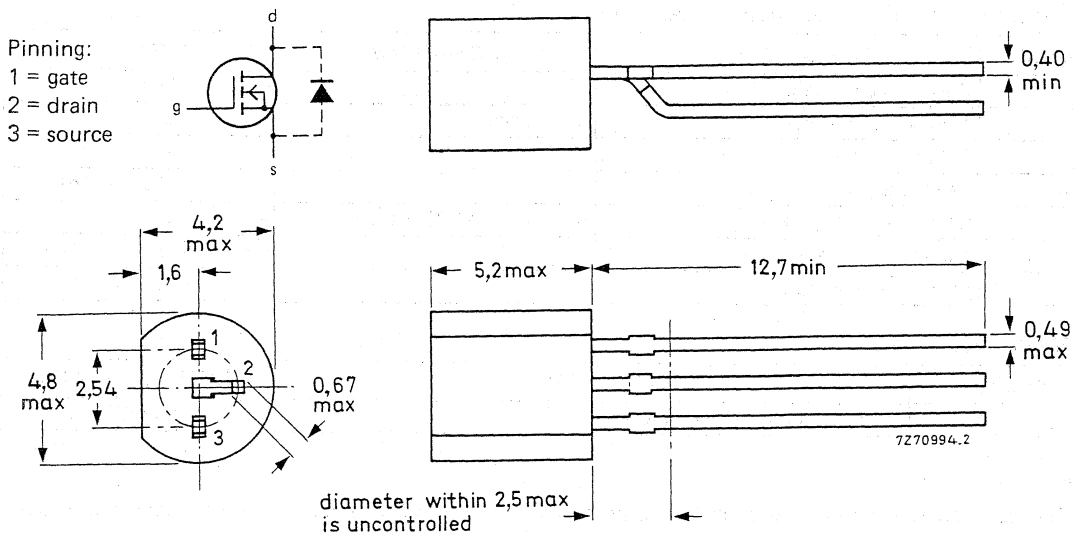
Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	140 mS 350 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = gate
2 = drain
3 = source



P-channel enhancement mode vertical D-MOS transistor

BSS92

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line-transformer drivers, and as a line current interruptor in telephony applications.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

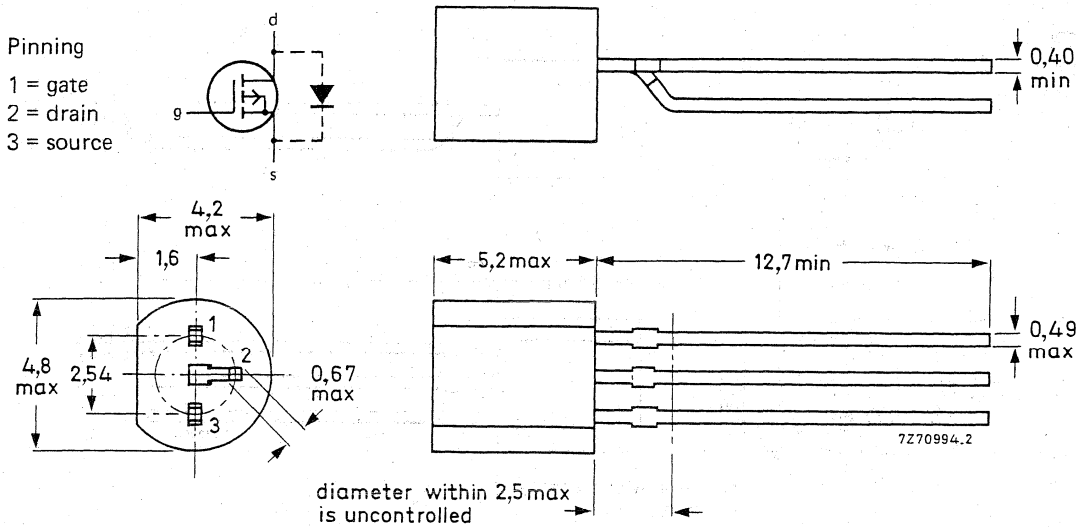
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.15 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 100 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	10 Ω 20 Ω
Transfer admittance $-I_D$ = 100 mA; $-V_{DS}$ = 25 V	$\lvert y_{fs} \rvert$	min. typ.	60 mS 200 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



N-channel vertical D-MOS transistor BST74A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	250 mS

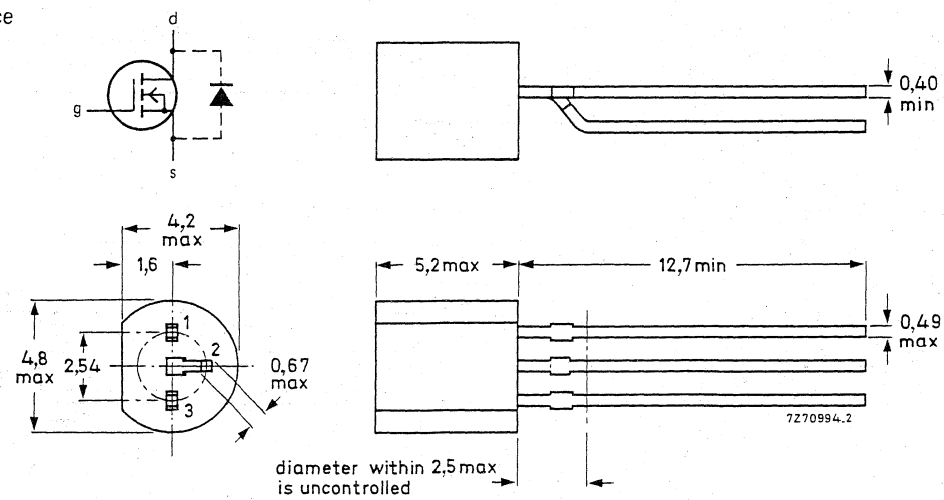
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

N-channel vertical D-MOS transistor BST76A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	250	mS

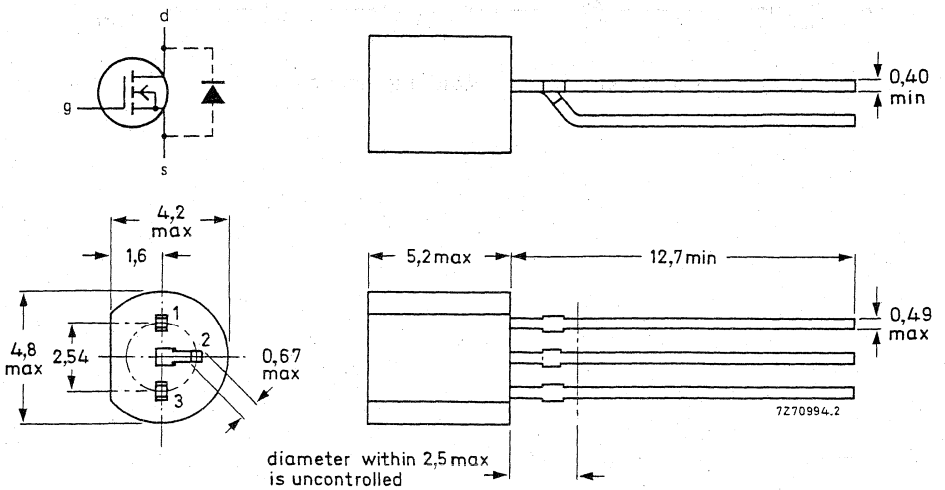
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

Regulator diodes — BZW03 series

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATA SHEET

Glass passivated diodes in hermetically sealed axial-leaded glass envelopes. They are intended for use as voltage regulator and transient suppressor diode in medium power regulation and transient suppression circuits.

The series consists of BZW03-C7V5 to BZW03-C510 in the normalized E24 range.

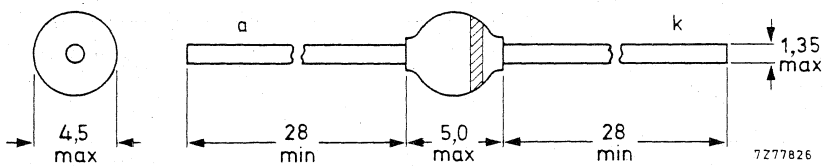
QUICK REFERENCE DATA

			voltage regulator	transient suppressor	
Working voltage range	V_Z	nom.	7,5 to 270		V
Stand-off voltage	V_R			6,2 to 430	V
Total power dissipation	P_{tot}	max.	6		W
Non-repetitive peak reverse power dissipation T_j = 25 °C; t_p = 100 μs	P_{RSM}			1000	W

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-64.



The marking band indicates the cathode.

Products approved to CECC 50 005-019.

Transient suppressor diode BZW14

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATA SHEET

A double-diffused silicon glass passivated diode in a hermetically sealed axial-leaded glass envelope intended for transient suppression in telephony equipment.

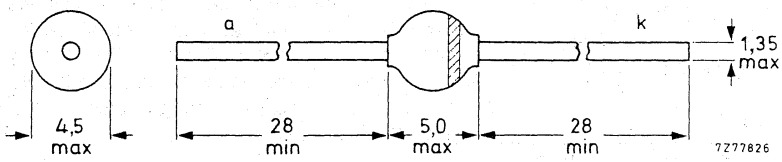
QUICK REFERENCE DATA

Stand-off voltage	V_R	max.	12 V
Non-repetitive peak reverse current	I_{RSM}	max.	50 A
Clamping voltage	$V_{(CL)R}$	<	28 V

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-64.



The marking band indicates the cathode.

RF modules for CT1 and CT1+ CT914; CT918

GENERAL DESCRIPTION

The CT914 and CT918 are radio frequency modules for the cordless telephone applications in the 900 MHz band. They are meant to be used in countries where the CT1 and CT1+ standards are approved by the local telephone authorities. The CT914 and CT918 comply with the requirements of radiation and signal handling capabilities of *"ETS1"* and *"BAPT 222 ZV 80-3"*.

The CT914 and CT918 perform full duplex communication with a 45 MHz duplex distance and a channel separation of 25 kHz. The CT914 features 40 channels in accordance with the CT1 standard, the CT918 has 80 channels in accordance with the CT1+ standard. In a normal application, types RF-units are required because frequencies are different for hand-set and base-set.

The CT914 and CT918 consist of an FM transmitter and receiver with an FM-demodulator. They are provided with a receiver signal-strength indication (RSSI). The frequency control uses a 3-wire bus interface. The transmitter amplifier can be switched on/off externally.

Table 1 Channel 1 frequencies

MODULE	TRANSMITTER (MHz)	RECEIVER (MHz)
CT1 hand-set	914.0125	959.0125
CT1 base-set	959.0125	914.0125
CT1+ hand-set	885.0125	930.0125
CT1+ base-set	930.0125	885.0125

FUNCTIONAL DESCRIPTION

The CT914 and CT918 consist of an FM transmitter together with an FM receiver in the same unit (see Fig.1). The transmitter part has a voltage-controlled oscillator (VCO) running at the transmit frequency. This VCO is frequency-locked and controlled by a phase-locked-loop (PLL) circuit. Frequency modulation (FM) of the transmit VCO is accomplished by superimposing the incoming audio signal on the PLL control voltage. The FM-modulated carrier is amplified by a three stage amplifier before entering the output bandpass filter and antenna connection.

The receiver part has a double conversion architecture. The incoming radio frequency (RF) signal is amplified and filtered before reaching the mixer. At this mixer stage it is mixed down to the first intermediate frequency (IF) by using a local phase-locked-loop VCO. The first IF signal is filtered by means of a crystal. In order to enhance selectivity and for FM demodulation the signal is mixed down again to the second IF signal. Mixer and demodulator are integrated into one IC, which also provides a receiver signal-strength indication (RSSI) and buffer demodulated audio.

Common to receiver and transmitter PLL ICs is a temperature compensated crystal oscillator (TCXO) providing a very stable reference frequency.

ORDERING INFORMATION

TYPE NUMBER	TYPE OF SET	STANDARD	MOUNTING	CATALOGUE NUMBER
CT914B	base-set	CT1	screw mounted	3139 147 20051
CT914H	hand-set	CT1	screw mounted	3139 147 20061
CT918B	base-set	CT1+	screw mounted	3139 147 20071
CT914H	hand-set	CT1+	screw mounted	3139 147 20081
CT914B/HM	base-set	CT1	solder mounted	3139 147 20011
CT914H/HM	hand-set	CT1	solder mounted	3139 147 20021
CT918B/HM	base-set	CT1+	solder mounted	3139 147 20031
CT918H/HM	hand-set	CT1+	solder mounted	3139 147 20041

BLOCK DIAGRAM

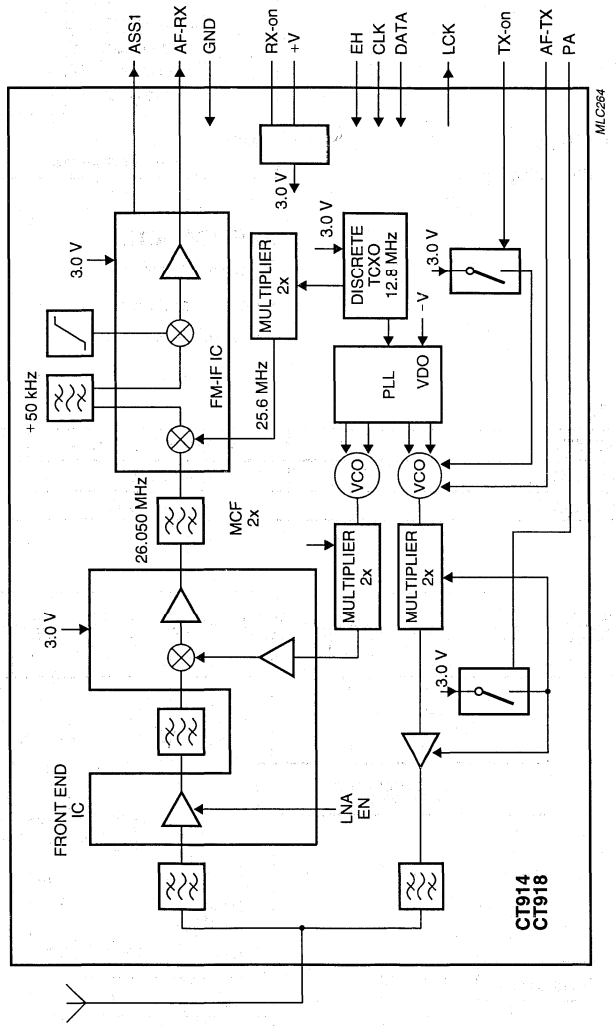


Fig.1 Electrical block diagram.

Low-power FM IF

MC3361

DESCRIPTION

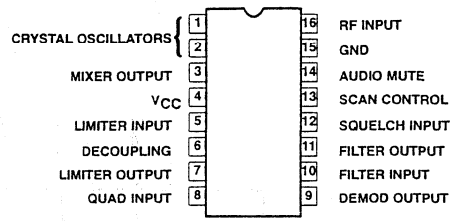
The MC3361 is a monolithic low-power FM IF signal processing system consisting of an oscillator, mixer, limiting amplifier, quadrature detector, filter amplifier, squelch, scan control and mute switch. It is intended for use in narrow band FM dual conversion communications equipment. The MC3361 is available in a 16-lead, dual-in-line plastic package and 16-lead SOL (surface-mounted miniature package).

FEATURES

- 2.0V to 8.0V operation
- Low current: 4.2mA typ at V_{CC} = 4.0V_{DC}
- Excellent sensitivity: 2.0μV for –3dB limiting typ
- Low external parts count
- Operation to 60MHz

PIN CONFIGURATION

D[1] and N Package



NOTE:
1. Available in 16-pin SOL package.

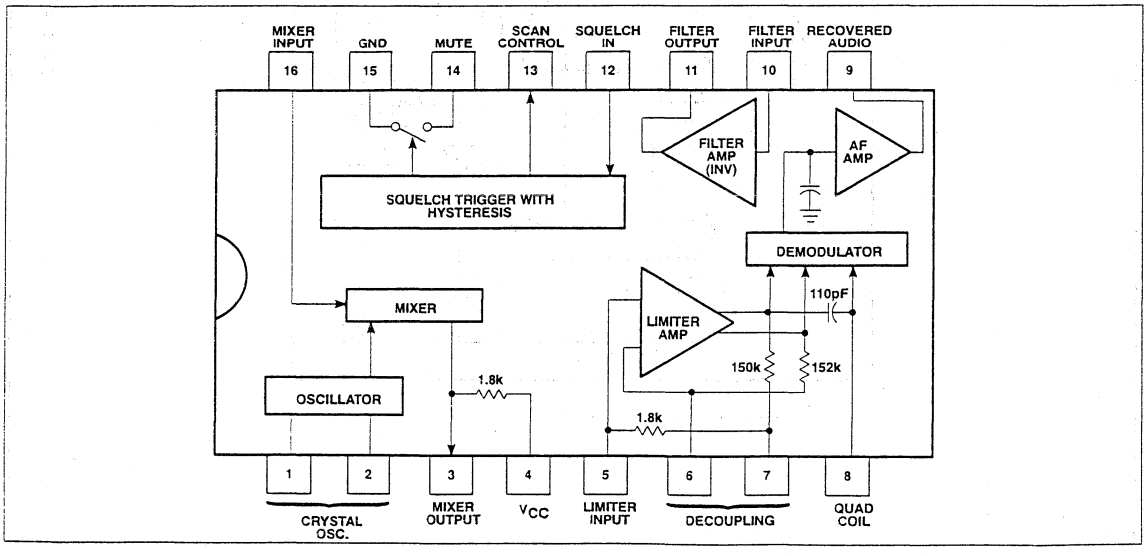
APPLICATIONS

- Cordless telephone
- Narrow band receivers
- Remote control

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	MC3361N	0406C
16-Pin Plastic Small Outline Large (SOL)	–40 to +85°C	MC3361D	0171B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

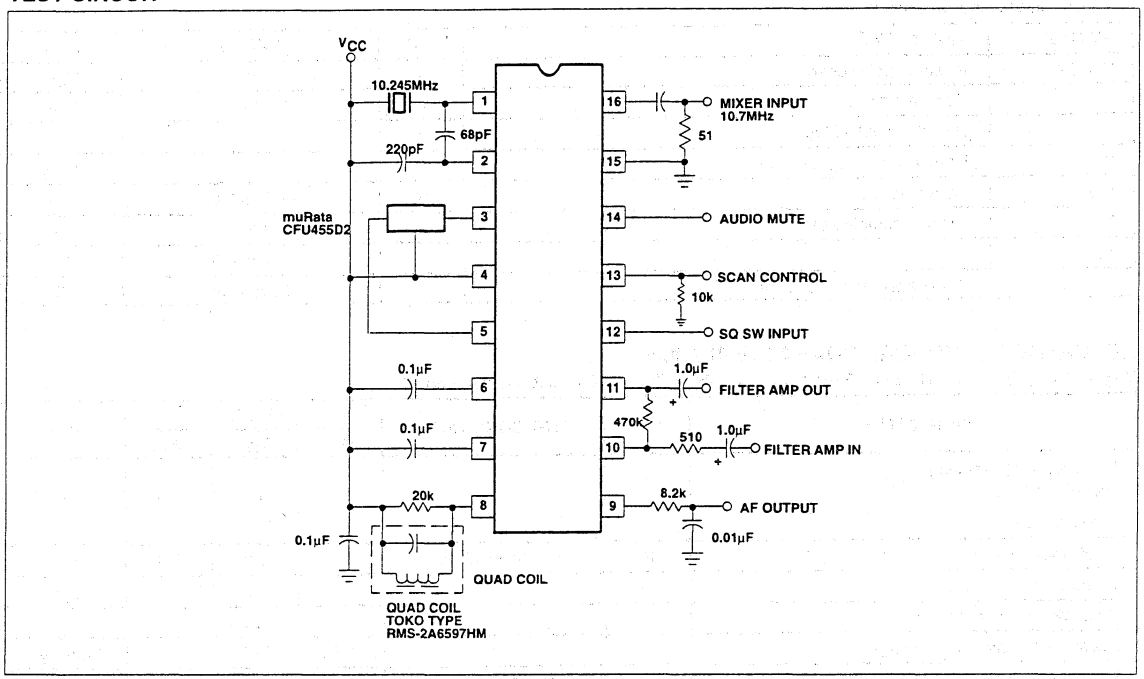
SYMBOL	PARAMETER	PIN	RATING	UNIT
V_{CC} (Max)	Power supply voltage	4	10	V_{DC}
V_{CC}	Generating supply voltage range	4	2.0 to 8.0	V_{DC}
	Detector input voltage	8	1.0	V_{P-P}
V_{16}	Input voltage (V_{CC}≥4.0V)	16	1.0	V_{RMS}
V_{14}	Mute function	14	–0.5 to 5.0	V_{PK}
T_J	Junction temperature		150	°C
T_A			–40 to +85	°C
T_{STG}	Storage temperature range		–65 to +150	°C

AC AND DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.0V_{DC}, f_O = 10.7MHz, Δf = +3.0kHz, f_{MOD} = 1.0kHz, T_A = 25°C unless otherwise noted.

PARAMETER	PIN	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Drain current (no signal) squelch off squelch on	4			4.2 5.4	7.0	mA
Input limiting voltage	16	–3.0dB limiting		2.0	6.0	μV
Detector output voltage	9			2.0		V_{DC}
Detector output impedance				450		Ω
Recovered audio output voltage	9	100	150	270		mV_{RMS}
Filter gain (10kHz)		V_{IN}=1.0mV_{RMS}	40	46		dB
Filter output voltage	11			1.7		V_{DC}
Trigger hysteresis				50		mV
Mute function low	14			10		Ω
Mute function high	14			10		MΩ
Scan function low (mute off)	13			0.5		V_{DC}
Scan function high (mute on)	13	V_{12}=GND				V_{DC}
Mixer conversion gain	3			27		dB
Mixer input resistance	16			3.6		kΩ
Mixer input capacitance	16			2.2		pF

TEST CIRCUIT



Wide-band high-frequency amplifier NE/SA/SE5205A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

DESCRIPTION

The NE/SA/SE5205A family of wideband amplifiers replace the NE/SA/SE5205 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nominally identical to the original parts.

The NE/SA/SE5205A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205A operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205A solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the -3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

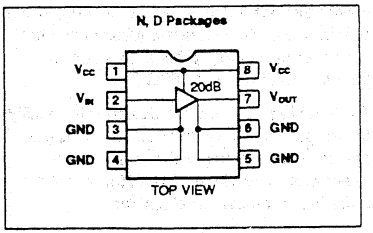
The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205As in series as required, without any degradation in amplifier stability.

FEATURES

- 600MHz bandwidth
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface mount package available
- MIL-STD processing available
- 2000V ESD protection

PIN CONFIGURATIONS



APPLICATIONS

- 75Ω cable TV decoder boxes
- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broad-band LANs
- Fiber-optics
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205AD
8-Pin Plastic DIP	0 to +70°C	NE5205AN
8-Pin Plastic SO	-40 to +85°C	SA5205AD
8-Pin Plastic DIP	-40 to +85°C	SA5205AN
8-Pin Plastic DIP	-55 to +125°C	SE5205AN

RF dual gain-stage

NE/SA5200

DESCRIPTION

The NE/SA5200 is a dual amplifier with DC to 1200MHz response. Low noise (NF = 3.6dB) makes this part ideal for RF front-ends, and a simple power-down mode saves current for battery operated equipment. Inputs and outputs are matched to 50Ω.

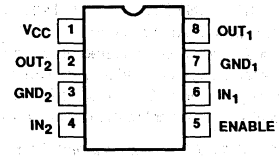
The enable pin allows the designer the ability to turn the amplifiers on or off, allowing the part to act as an amplifier as well as an attenuator. This is very useful for front-end buffering in receiver applications.

FEATURES

- Dual amplifiers
- DC - 1200MHz operation
- Low DC power consumption (4.2mA per amplifier @ V_{CC} = 5V)
- Power-Down Mode (I_{CC} = 95µA typical)
- 3.6dB noise figure at 900MHz
- Unconditionally stable
- Fully ESD protected
- Low cost
- Supply voltage 4-9V
- Gain S_{21} = 7dB at f = 1GHz
- Input and output match S_{11}, S_{22} typically <–14dB

PIN CONFIGURATION

D Package



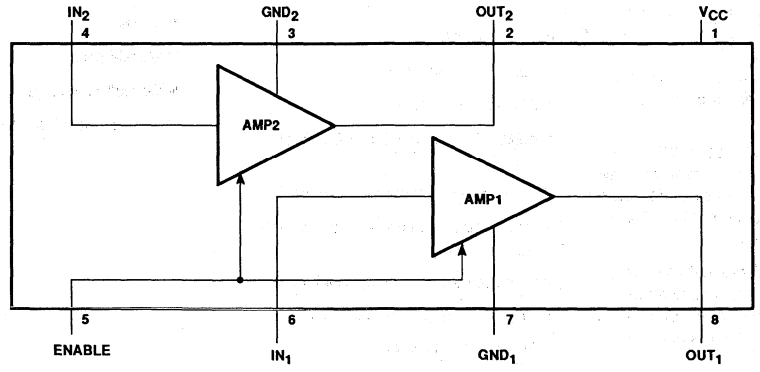
APPLICATIONS

- Cellular radios
- RF IF strips
- Portable equipment

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO (Surface–mount)	0-70°C	NE5200D
8-Pin Plastic SO (Surface–mount)	–40-+85°C	SA5200D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.5 to +9	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 8-Pin Plastic SO	780	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:

1. Transients exceeding 10.5V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin SO: θ_{JA} = 158°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.0 to 9.0	V
	Operating ambient temperature range		
	NE Grade	0 to +70	°C
T_A	SA Grade	-40 to +85	°C
	Operating junction temperature		
	NE Grade	0 to +90	°C
T_J	SA Grade	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4	5.0	9.0	V
I_{CC}	Total supply current	V_{CC} = 5V, ENABLE = High	6.4	8.4	10.4	mA
		V_{CC} = 5V, ENABLE = Low		95	255	µA
		V_{CC} = 9V, ENABLE = High		17.8	22.2	mA
		V_{CC} = 9V, ENABLE = Low		320	960	µA
V_T	TTL/CMOS logic threshold voltage[1]			1.25		V
V_{IH}	Logic 1 level	Power-up mode	2.0		V_{CC}	V
V_{IL}	Logic 0 level	Power-down mode	-0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	µA
$V_{IDC,ODC}$	Input and output DC levels		0.6	0.83	1.0	V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the NE/SA5200.

AC ELECTRICAL CHARACTERISTICS[1] V_{CC} = +5V, T_A = 25°C, either amplifier, enable = 5V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S21	Insertion gain	f = 100MHz	9.2	11	13.2	dB
		f = 900MHz	5.2	7.5		dB
S22	Output return loss	f = 900MHz		–14.3		dB
S12	Reverse isolation	f = 900MHz		–17.9		dB
S11	Input return loss	f = 900MHz		–16.5		dB
P-1	Output 1dB compression point	f = 900MHz		–4.3		dBm
NF	Noise figure in 50Ω	f = 900MHz		3.6		dB
IP_2	Input second-order intercept point	f = 900MHz		+4.3		dBm
IP_3	Input third-order intercept point	f = 900MHz		–1.8		dBm
ISOL	Amplifier-to-amplifier isolation[2]	f = 900MHz		–25		dB
P_{OUT}	Saturated output power	f = 900MHz		–1.7		dBm
S21	Insertion gain when disabled	f = 100MHz		–13		dB
		f = 900MHz		–13.5		dB

NOTE:
1. All measurements include the effects of the NE/SA5200 Evaluation Board (see Figure 2). Measurement system impedance is 50Ω.
2. Input applied to one amplifier, output taken at the other output. All ports terminated into 50Ω.

APPLICATIONS

NE/SA5200 is a user-friendly, wide-band, unconditionally stable, low power dual gain amplifier circuit. There are several advantages to using the NE/SA5200 as a high frequency gain block instead of a discrete implementation. First is the simplicity of use. The NE/SA5200 does not need any external biasing components. Due to the higher level of integration and small footprint (SO8) package it occupies less space on the printed circuit board and reduces the manufacturing cost of the system. Also the higher level of integration improves the reliability of the amplifier over a discrete implementation with several components. The power down mode in the NE/SA5200 helps reduce power consumption in applications where the amplifiers can be disabled. And last but not the least is the impedance matching at inputs and outputs. Only those who have toiled through discrete transistor implementations for 50Ω input and output impedance matching can truly appreciate the elegance and simplicity of the NE/SA5200 input and output impedance matching to 50Ω.

A simplified equivalent schematic is shown in Figure 1. Each amplifier is composed of an NPN transistor with an Ft of 13GHz in a classical series-shunt feedback configuration. The two wideband amplifiers are biased from the same bias generator. In normal operation each amplifier consumes about 4mA of quiescent current (at V_{CC} = 5V). In the disable mode the device consumes about 90μA of current, most of it is in the TTL enable buffer and the bias generator. The input impedance of the amplifiers is 50Ω. The amplifiers have typical gain of 11dB at 100MHz and 7dB of gain at 1.2GHz.

It can be seen from Figure 1 that any inductance between Pin 7, 3 and the ground plane will reduce the gain of the amplifiers at higher frequencies. Thus proper grounding of Pins 7 and 3 is essential for maximum gain and increased frequency response. Figure 2 shows the printed circuit board layout and the component placement for the NE/SA5200 evaluation board. The AC coupling capacitors should be selected such that at they are shorts at the desired frequency of operation. Since most low-cost large value surface mount capacitors cease to be simply capacitors in the UHF range and exhibit an inductive behavior, it is recommended that high frequency chip capacitors be utilized in the circuit. A good power supply bypass is also essential for the performance of the amplifier and should be as close to the device as practical.

Figure 3 shows the typical frequency response of the two channels of NE/SA5200. The low frequency gain is about 11dB at 100MHz and slowly drops off to 10dB at 500MHz. The gain is about 8dB at 900MHz and 7dB at 1.2 GHz which is typical of NE/SA5200 with a good printed circuit board layout. It can also be seen that both channels have a very well matched frequency response and matched gain to within 0.1dB at 100MHz and 0.2dB at 900MHz.

NE/SA5200 finds applications in many areas of RF communications. It is an ideal gain block for high performance, low cost, low power RF communications transceivers. A typical radio transceiver front-end is shown in Figure 4. This could be the front-end of a cellular phone, a VHF/ UHF hand-held transceiver, UHF cordless telephone or a spread spectrum system. The NE/SA5200 can be used in the receiver path of most systems as an LNA and pre-amplifier. The bandpass filter between the two amplifiers also minimize the noise into the first mixer. In the transmitter path, NE/SA5200 can be used as a buffer to the VCO and isolate the VCO from any load variations due to the power level changes in the power amplifier. This improves the stability of the VCOs. The NE/SA5200 can also be used as a pre-driver to the power amplifier modules.

The two amplifiers in NE/SA5200 can be easily cascaded to have a 13dB gain block at 900MHz. At 100MHz the gain will be 22dB and a noise figure of about 5.5dB. The NE/SA5200 can be operated at a higher voltage up to 9V for much improved 1dB output compression point and higher 3rd order intercept point.

Several stages of NE/SA5200 can also be cascaded and be used as an IF amplifier strip for DBS/TV/GPS receivers. Figure 5 shows a 60dB gain IF strip at 180MHz. The noise figure for the cascaded amplifier chain is given by equation 1.

NF (total) = NF1 + NF2/G1 + NF3/G1*G2 + NF4/G1*G2*G3 + ... (Equation. 1)

NOTE: The noise figure and gain should not be in dB in the above equation.

Since the noise figure for each stage is about 3.6dB and the gain is about 11dB, the noise figure for the 60dB gain IF strip will be about 6.4dB.

In applications where a single amplifier is required with a 7.5dB gain at 900MHz and current consumption is of paramount importance (battery powered receivers), the amplifier A1 can be used and amplifier A2 can be disabled by leaving GND2 (Pin 3) unconnected. This will reduce the total current consumption for the IC to a meager 4mA.

The ENABLE pin is useful for Time-Division-Duplex systems where the receiver can be disabled for a period of time. In this case the overall system supply curren will be decreased by 8mA.

The ENABLE pin can also be used to improve the system dynamic range. For input levels that are extremely high, the NE/SA5200 can be disabled. In this case th input signal is attenuated by 13dB. This prevents the system from being overloaded as well as improves the system's overall dynamic range. In the disabled condition th NE/SA5200 IP_3 increases to nearly +20dBm

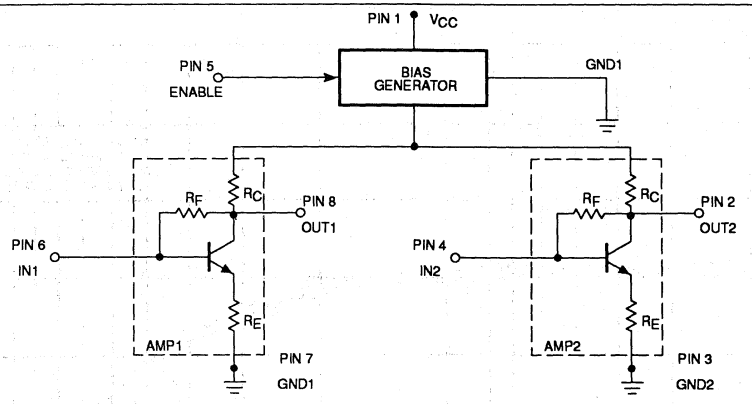
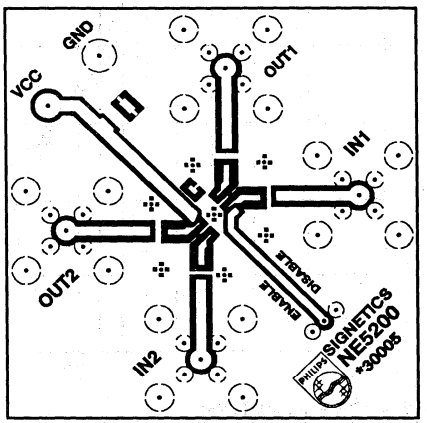
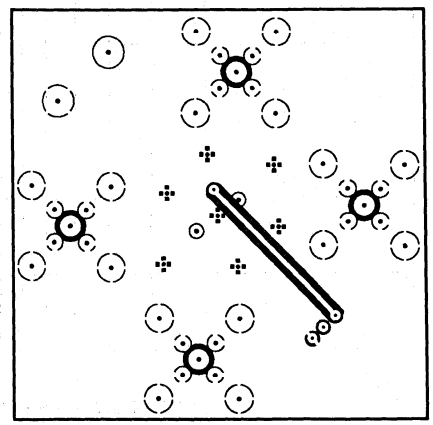


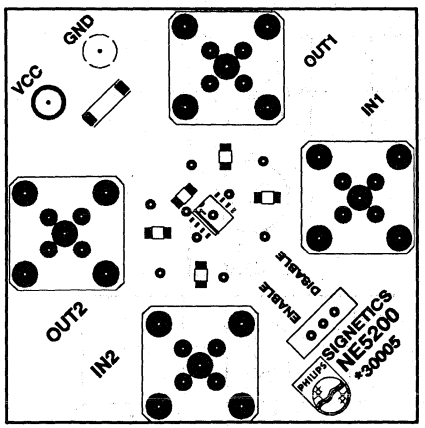
Figure 1. Simplified Equivalent Schematic of NE/SA5200



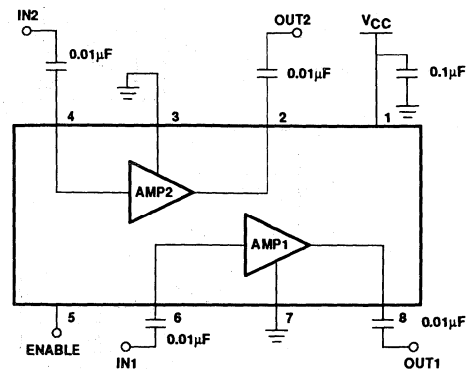
a. Top Side



b. Bottom Side



c. Top Silk Screen



d. NE/SA5200 Evaluation Board Schematic

Figure 2. Printed Circuit Board Layout of the NE/SA5200 Evaluation Board

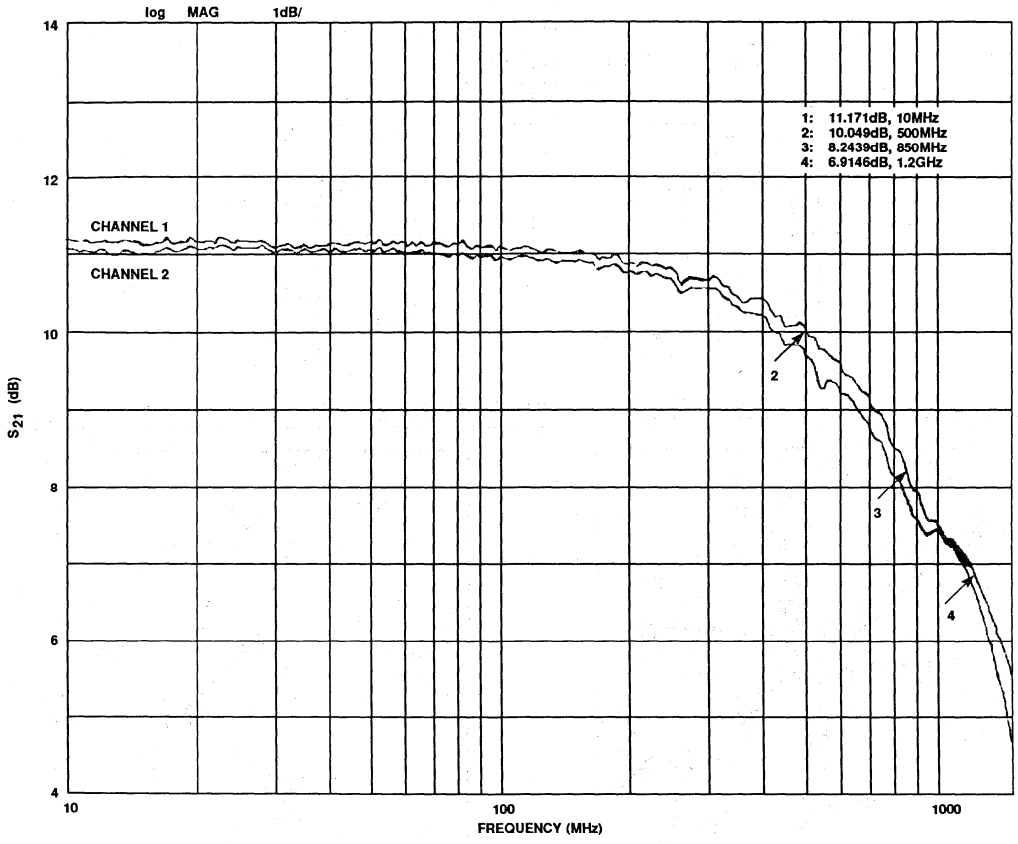


Figure 3. Typical Frequency Response of NE/SA5200 in a 50Ω System

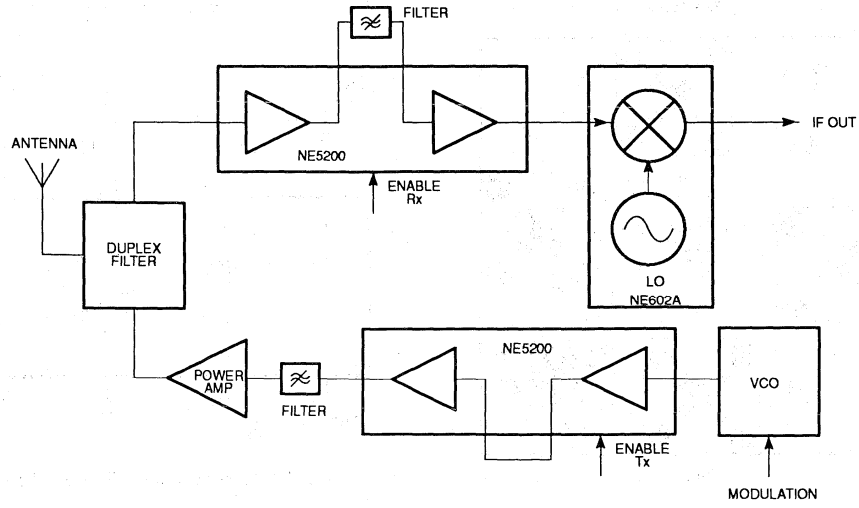


Figure 4. Typical Radio Transceiver Front-End

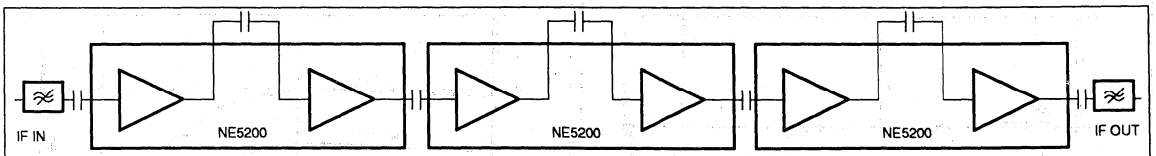


Figure 5. 60dB IF Gain Block for 100-300MHz IF for GPS/DBS Systems

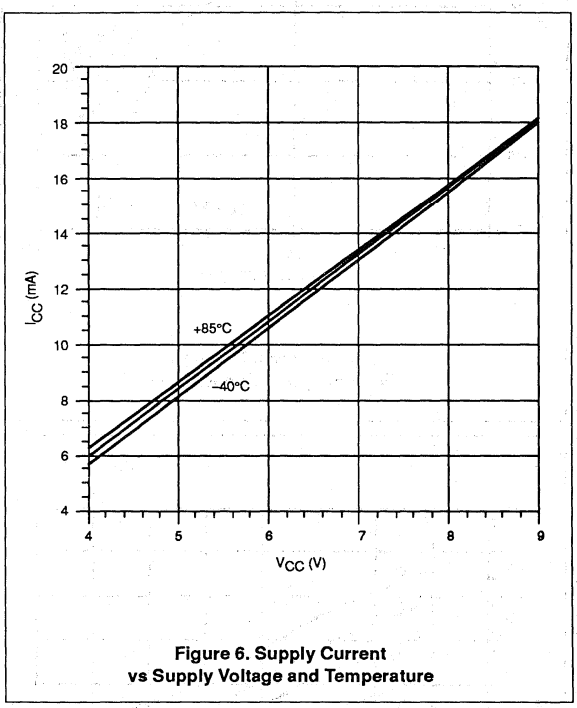


Figure 6. Supply Current vs Supply Voltage and Temperature

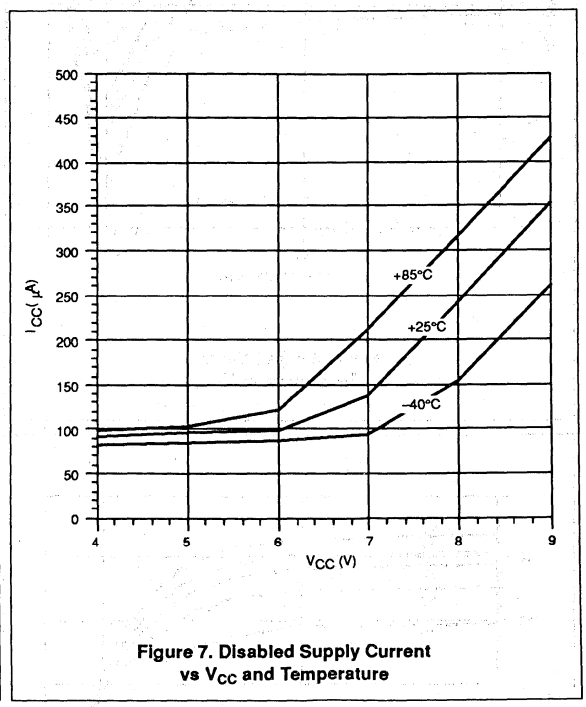


Figure 7. Disabled Supply Current vs V_{CC} and Temperature

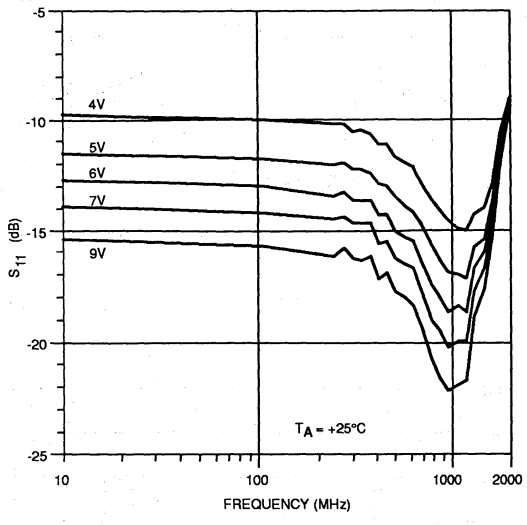


Figure 8. Input Match vs Frequency and V_{CC}

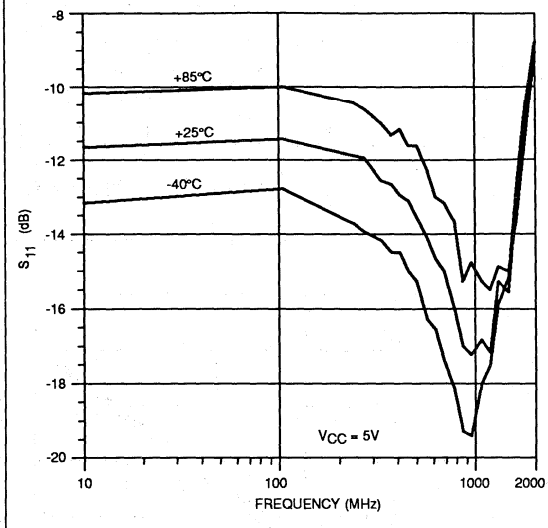


Figure 9. Input Match vs Frequency and Temperature

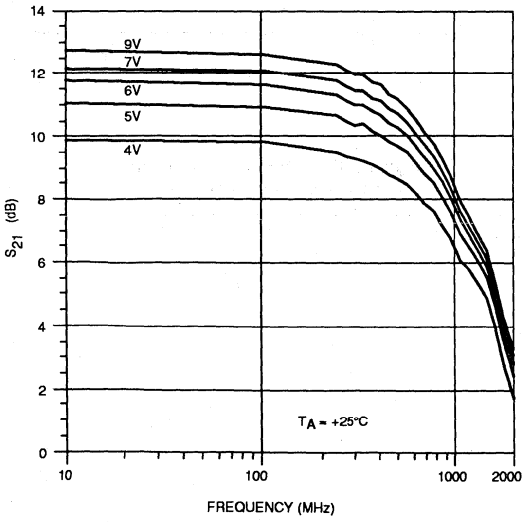


Figure 10. Insertion Gain vs Frequency and V_{CC}

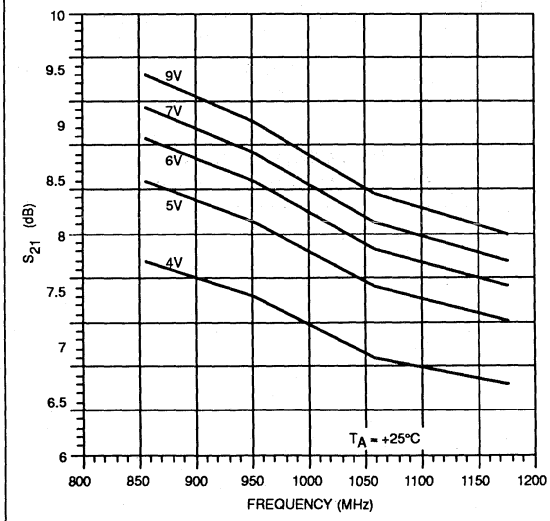


Figure 11. Insertion Gain vs Frequency and V_{CC} — Expanded Detail —

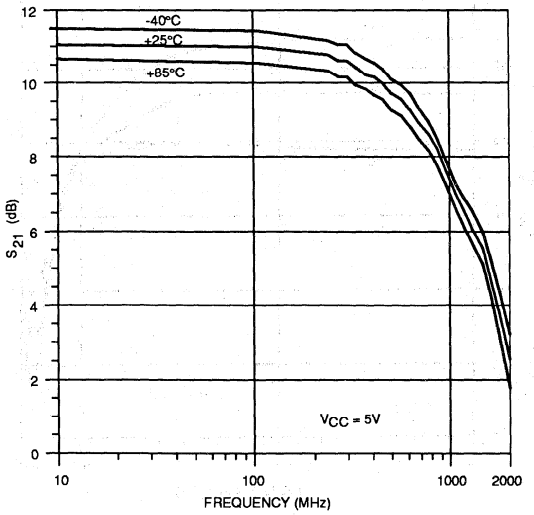


Figure 12. Insertion Gain vs Frequency and Temperature

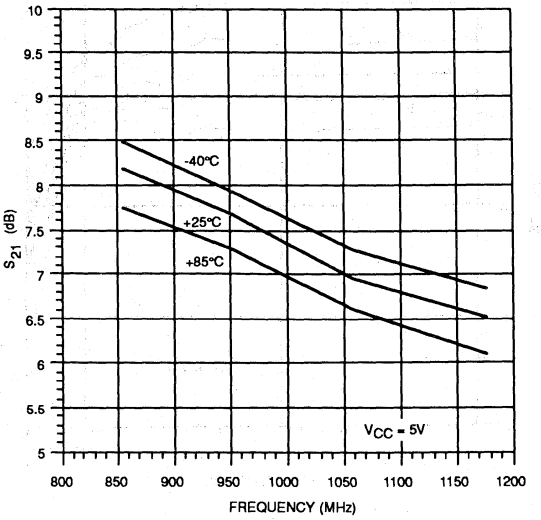


Figure 13. Insertion Gain vs Frequency and Temperature – Expanded Detail –

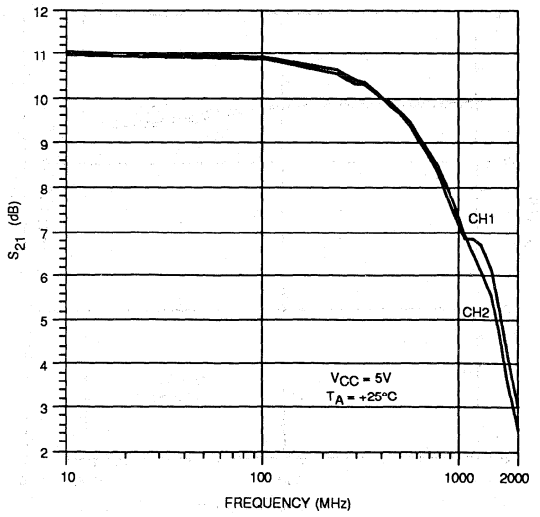


Figure 14. Insertion Gain Matching (CH1 vs CH2) vs Frequency

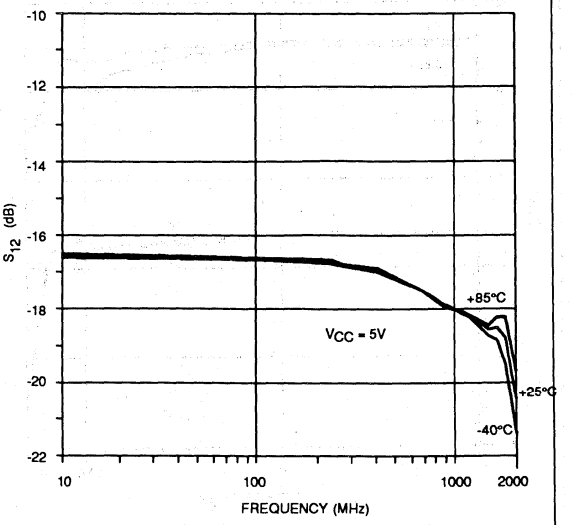


Figure 15. Reverse Insertion Gain vs Frequency and Temperature

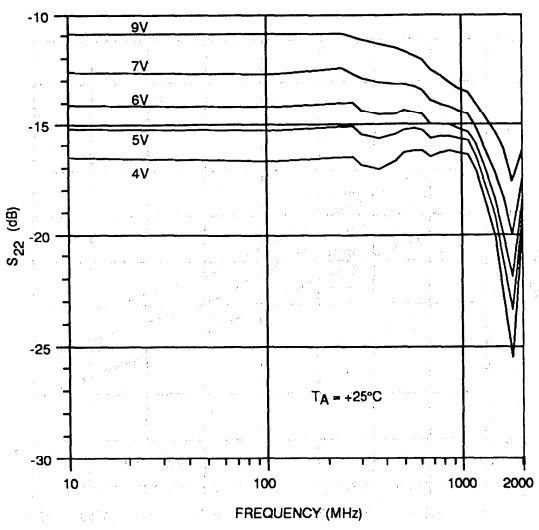


Figure 16. Output Match vs Frequency and V_{CC}

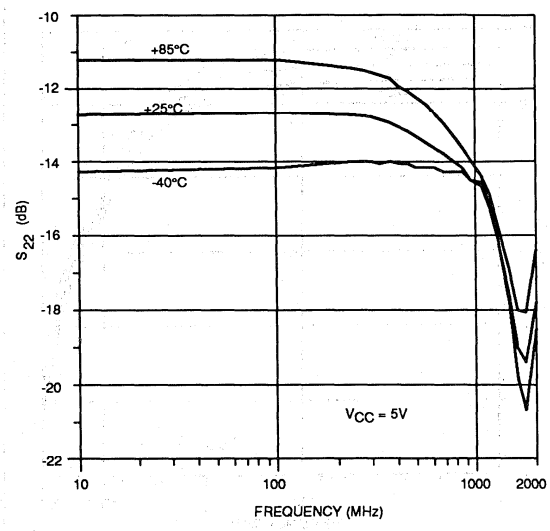


Figure 17. Output Match vs Frequency and Temperature

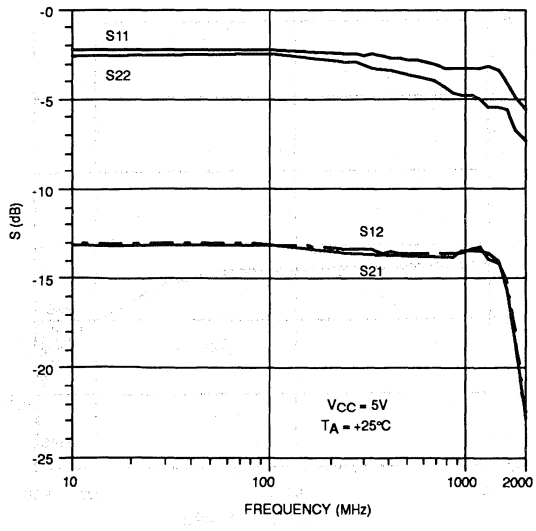


Figure 18. S-parameters vs Frequency for Disabled Amplifier

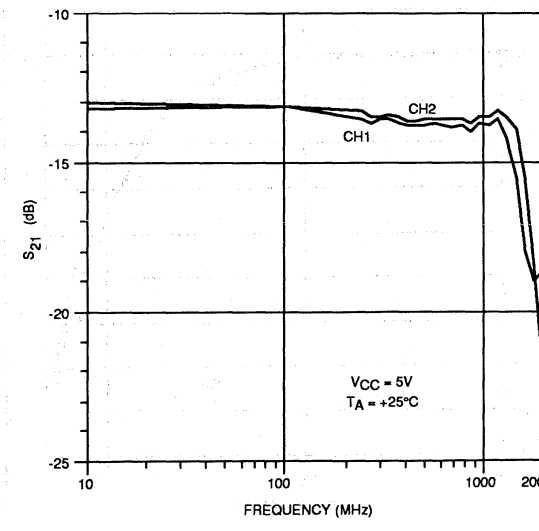


Figure 19. Insertion Gain Matching Disabled (CH1 vs CH2) vs Frequency

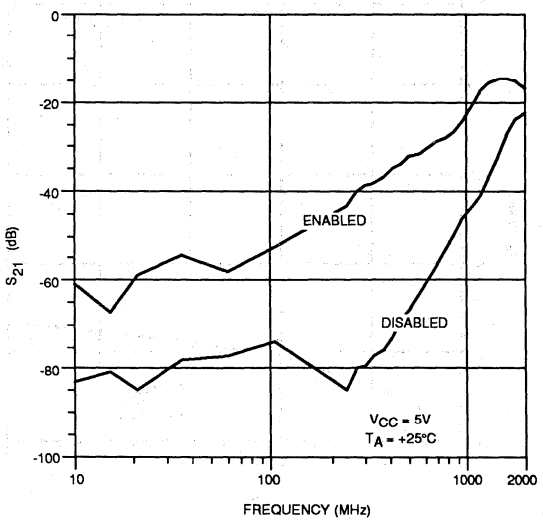


Figure 20. CH1 Input to CH2 Output Isolation vs Frequency

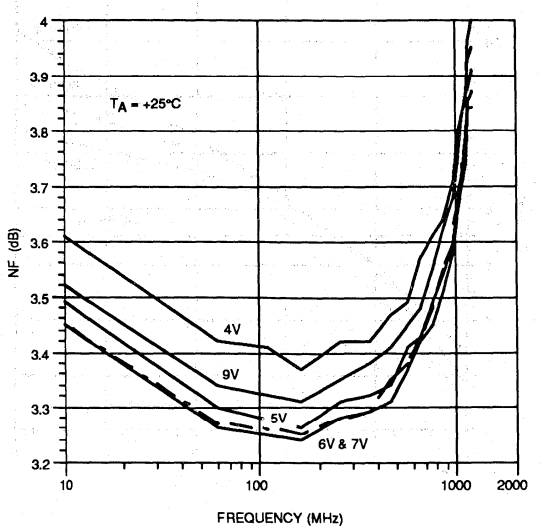


Figure 21. Noise Figure vs Frequency and V_{CC} in a 50Ω System

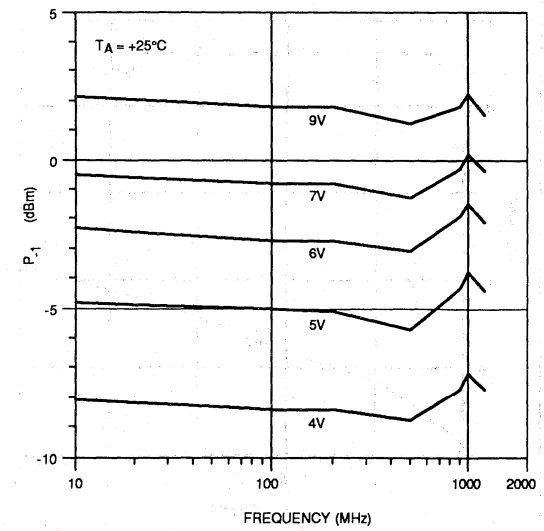


Figure 22. 1dB Output Compression Point vs Frequency and V_{CC}

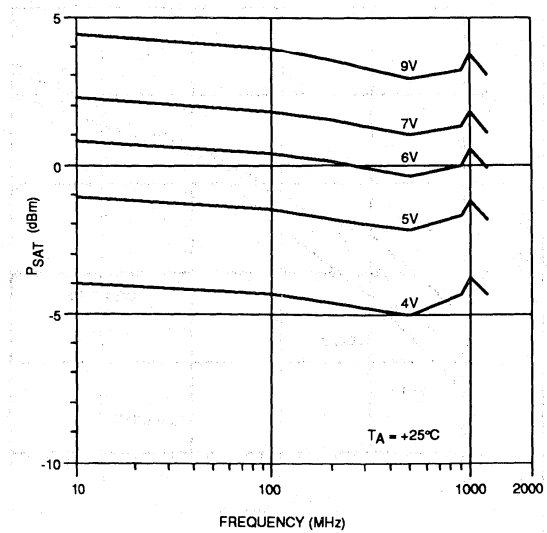


Figure 23. Saturated Output Power vs Frequency and V_{CC}

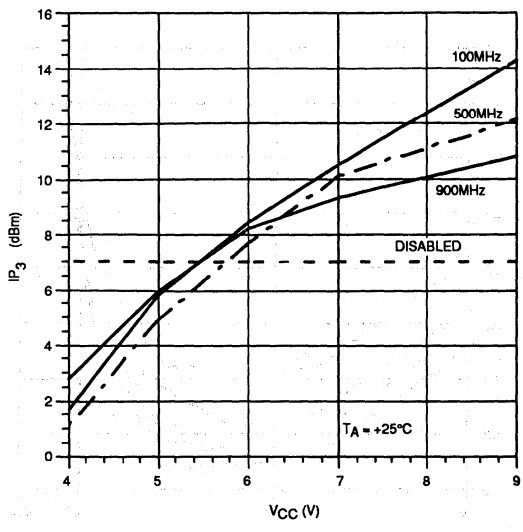


Figure 24. Third-Order Output Intercept vs Frequency and V_{CC}

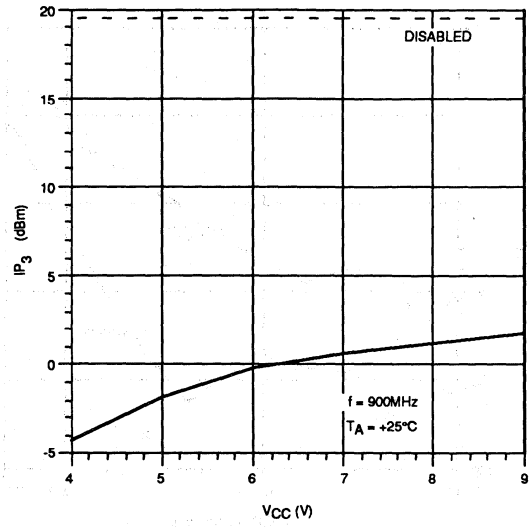


Figure 25. Third-Order Input Intercept vs Frequency and V_{CC}

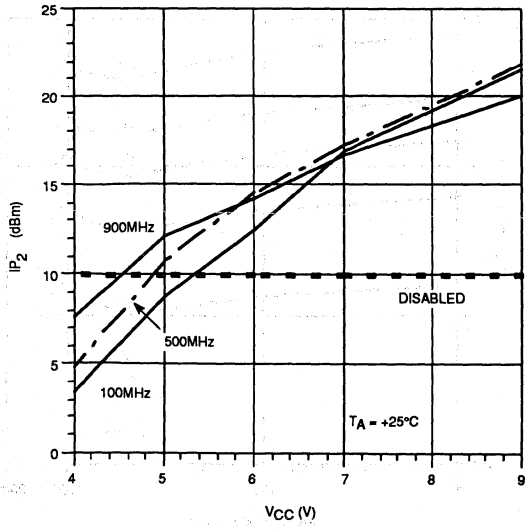


Figure 26. Second-Order Output Intercept vs Frequency and V_{CC}

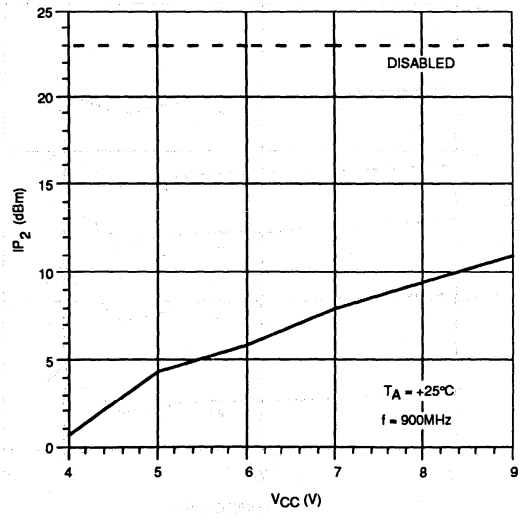


Figure 27. Second-Order Input Intercept vs Frequency and V_{CC}

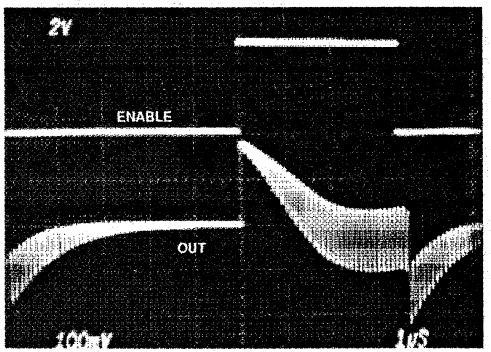


Figure 28. Switching Speed; f_{IN} = 10MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 0.01µF

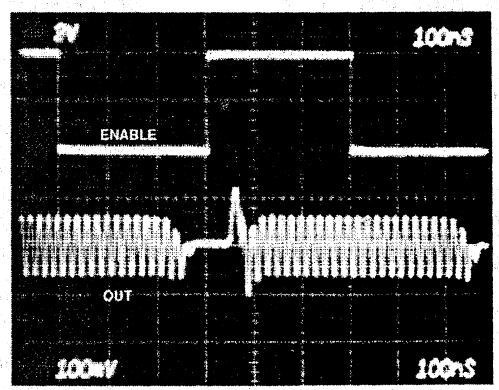


Figure 29. Switching Speed; f_{IN} = 50MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 100pF

Wide-band high-frequency amplifier — NE/SA5204A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

DESCRIPTION

The NE/SA5204A family of wideband amplifiers replaces the NE/SA5204 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nomically identical to the original parts.

The NE/SA5204A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The -3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204A operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204A is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204A solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

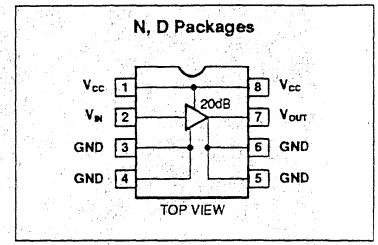
No external components are needed other than AC coupling capacitors because the NE/SA5204A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204As in series as required, without any degradation in amplifier stability.

FEATURES

- Bandwidth (min.)
  200 MHz, ±0.5dB
  350 MHz, -3dB
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface-mount package available
- Cascadable
- 2000V ESD protection

PIN CONFIGURATION



APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Networks
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C –40 to +85°C	NE5204AN SA5204AN
8-Pin Plastic SO package	0 to +70°C –40 to +85°C	NE5204AD SA5204AD

Wideband variable gain amplifier NE/SA5209

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

DESCRIPTION

The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

FEATURES

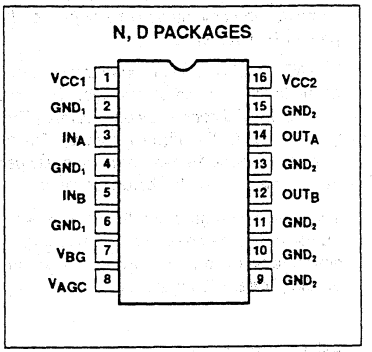
- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi–purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

PIN CONFIGURATION

N, D PACKAGES



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5209D
16-Pin Plastic DIP	0 to +70°C	NE5209N
16-Pin Plastic SO	–40 to +85°C	SA5209D
16-Pin Plastic DIP	–40 to +85°C	SA5209N

Wideband variable gain amplifier NE/SA5219

DESCRIPTION

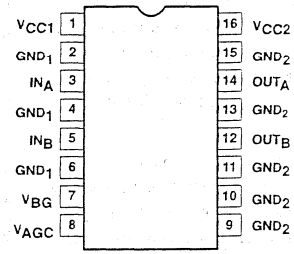
The NE5219 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5219 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5219 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

PIN CONFIGURATION

N, D PACKAGES



FEATURES

- 700MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

Description	Temperature Range	Order Code	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5219D	0005D
16-Pin Plastic Dual In-Line package (DIP)	0 to +70°C	NE5219N	0406C
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5219D	0005D
16-Pin Plastic Dual In-Line package (DIP)	-40 to +85°C	SA5219N	0406C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	36	43	50	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	16	19	22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	22	25	28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.8	1.2	1.6	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	35	60	80	Ω
V_{OS}	Output offset voltage (output referred)			±20	±150	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
PSRR	Output offset supply rejection ratio		18	45		dB
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
R_{BG}	Bandgap loading		2	10		kΩ
V_{AGC}	AGC DC control voltage range			0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	μA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth			700		MHz
GF	Gain flatness	DC - 500MHz		±0.4		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[1]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[1]	R_L = 50Ω		400		mV_{P-P}
		R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		nV/√Hz
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:
1. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5219 APPLICATIONS

The NE5219 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5219 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5219 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5219 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5219 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5219. A

maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5219 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5219 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5219 is shown in Figure 2. Three NE5219s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5219s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5219s will give a dynamic range in excess of 60dB.

The NE5219 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

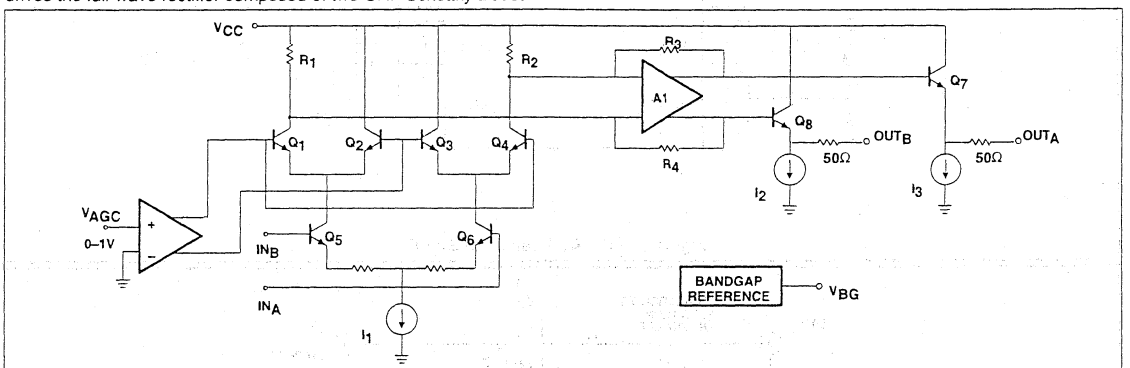


Figure 1. Equivalent Schematic of VGA

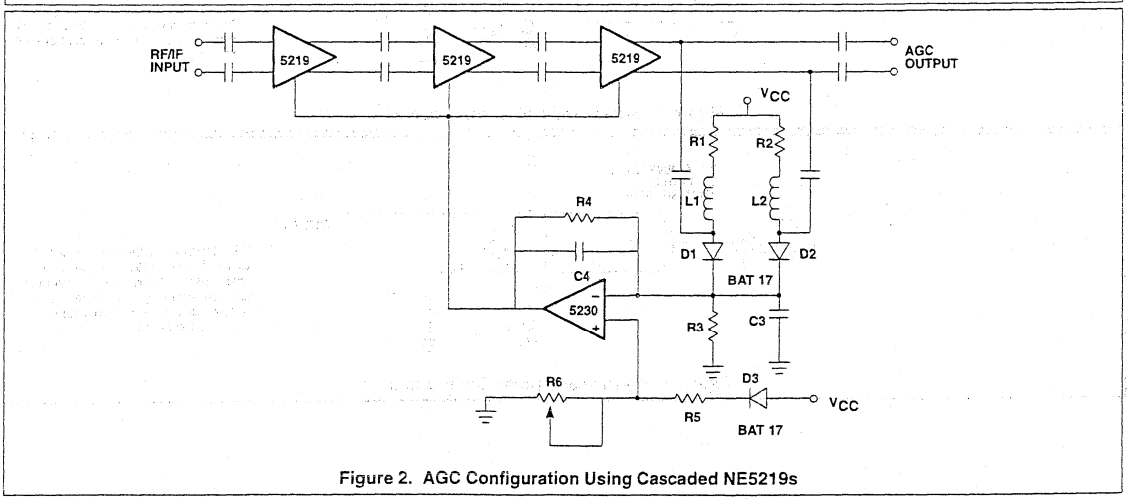


Figure 2. AGC Configuration Using Cascaded NE5219s

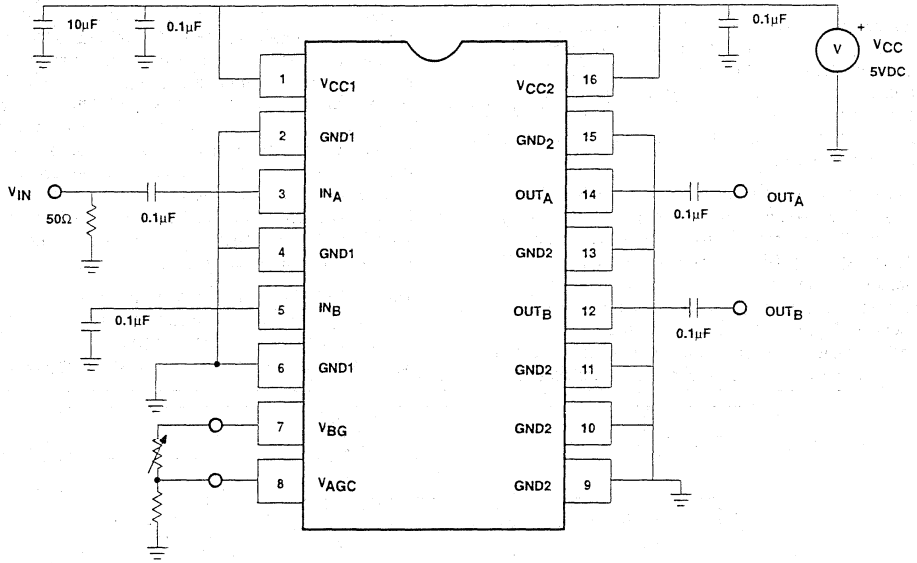
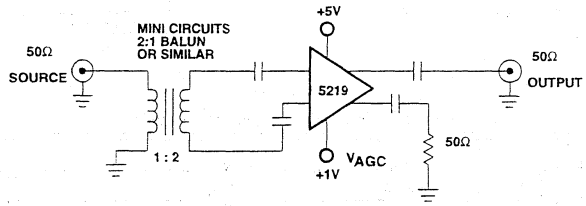
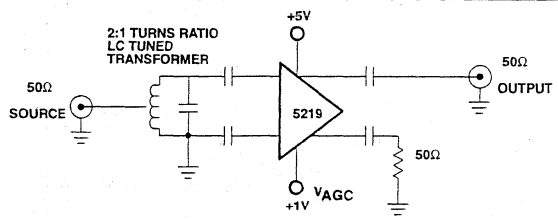


Figure 3. VGA AC Evaluation Board



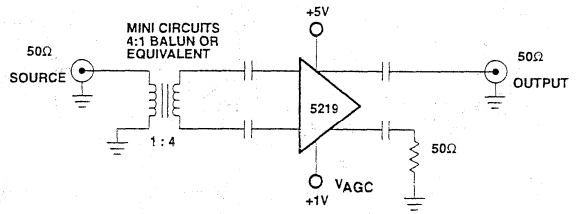
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



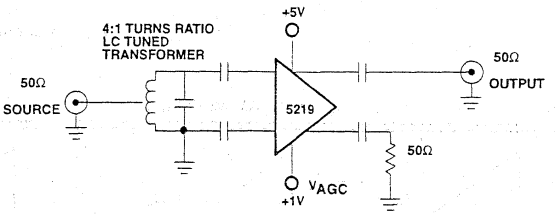
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



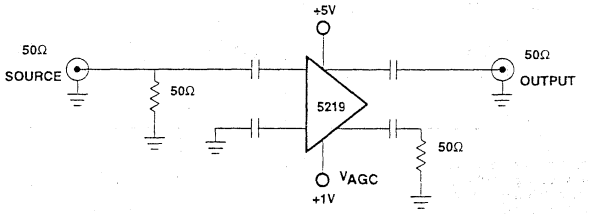
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



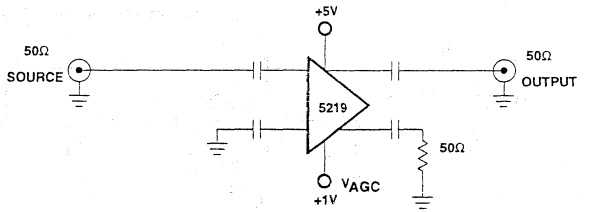
This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



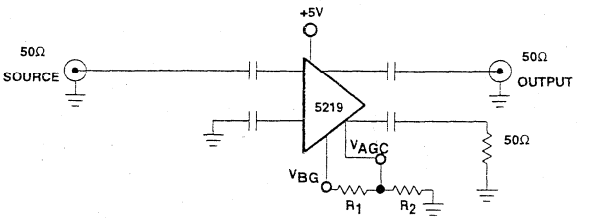
The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration



With the 50Ω source left unterminated, the noise figure is 9dB.

Figure 9. Unterminated Configuration



$$\text{Gain} = 19\text{dB} + 20\log_{10} V_{AGC}$$

$$\text{where } V_{AGC} = \left[\frac{R_2}{R_1 + R_2} V_{BG}\right]$$

and is in units of Volts, for $V_{AGC} \leq 1V$

Figure 10. User-Programmable Fixed Gain Block

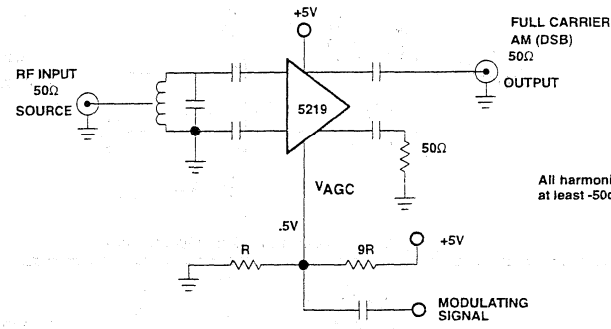
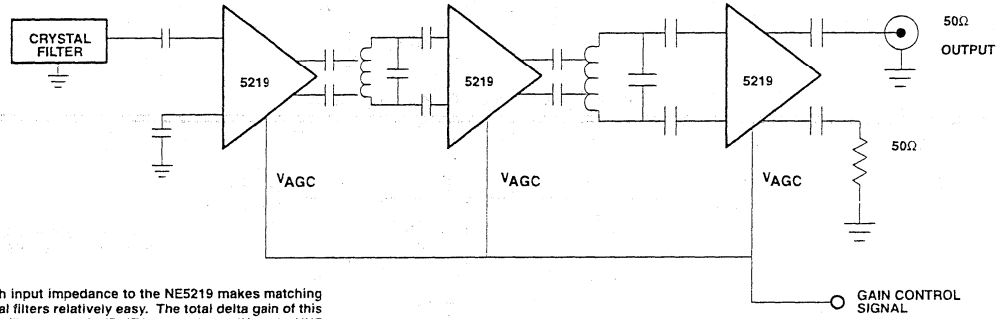


Figure 11. AM Modulator



The high input impedance to the NE5219 makes matching to crystal filters relatively easy. The total delta gain of this system will approach 80dB. IF frequencies well into the UHF region can be configured with this type of architecture.

Figure 12. Receiver AGC IF Gain

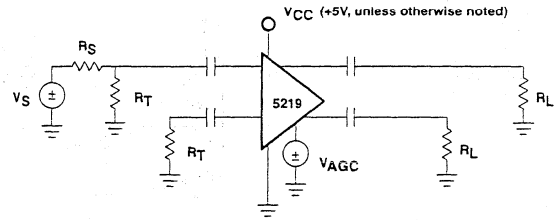


Figure 13. Test Set-up 1 (Used for all Graphs)

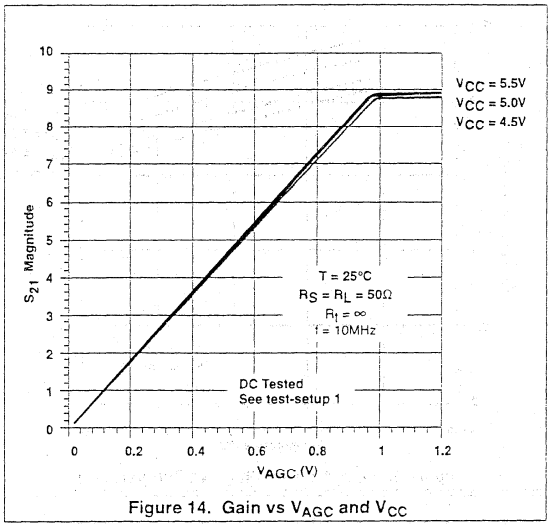


Figure 14. Gain vs V_{AGC} and V_{CC}

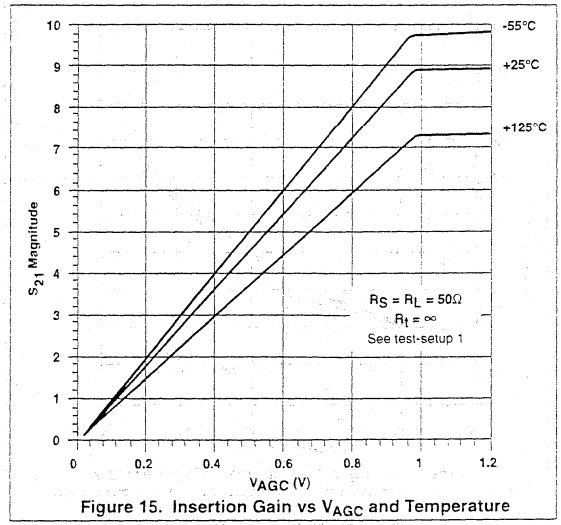


Figure 15. Insertion Gain vs V_{AGC} and Temperature

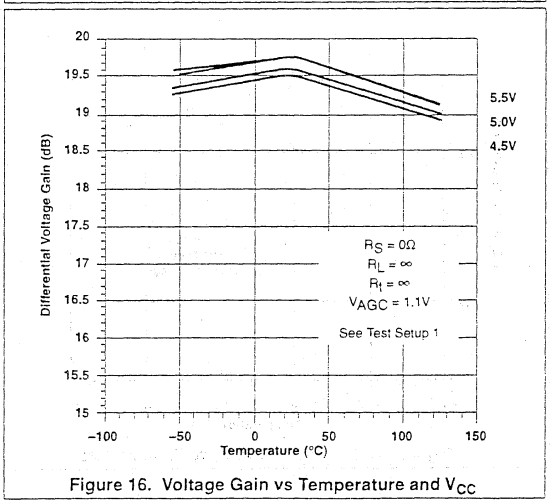


Figure 16. Voltage Gain vs Temperature and V_{CC}

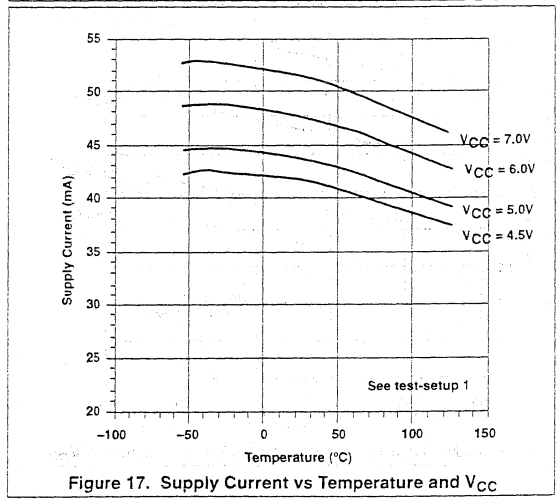


Figure 17. Supply Current vs Temperature and V_{CC}

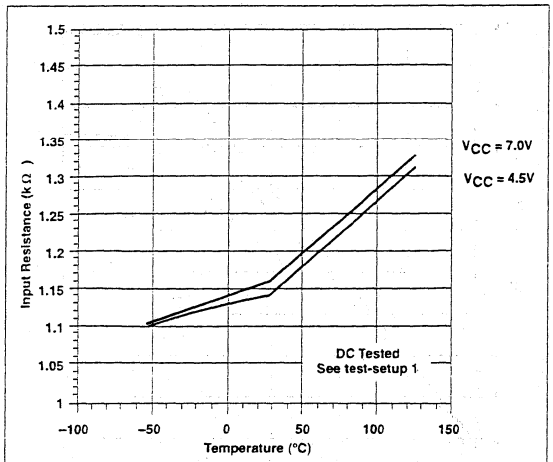


Figure 18. Input Resistance vs Temperature

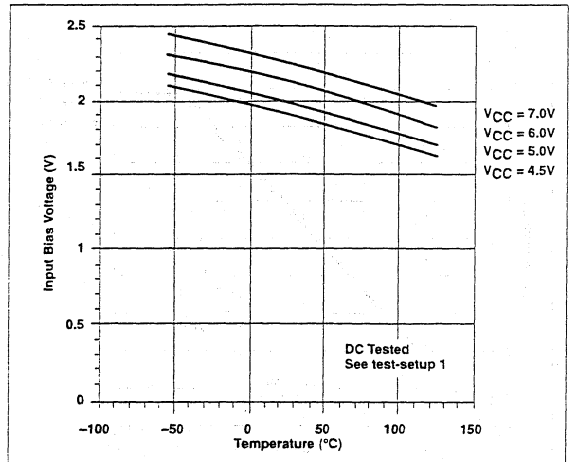


Figure 19. Input Bias Voltage vs Temperature

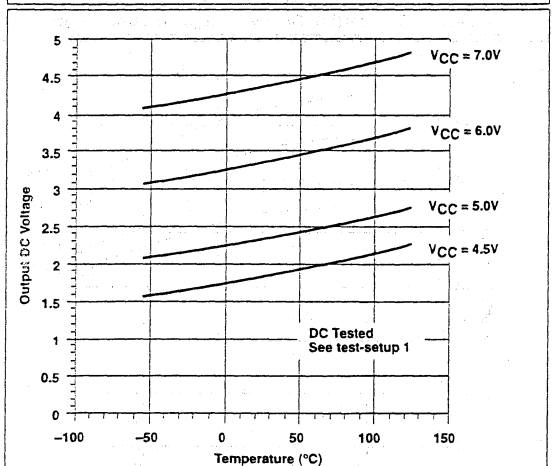


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

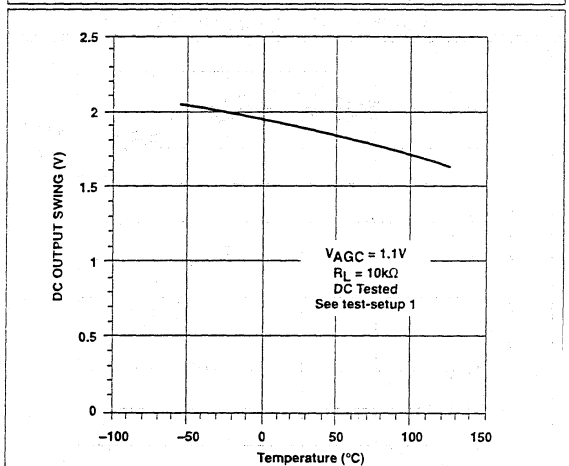


Figure 21. DC Output Swing vs Temperature

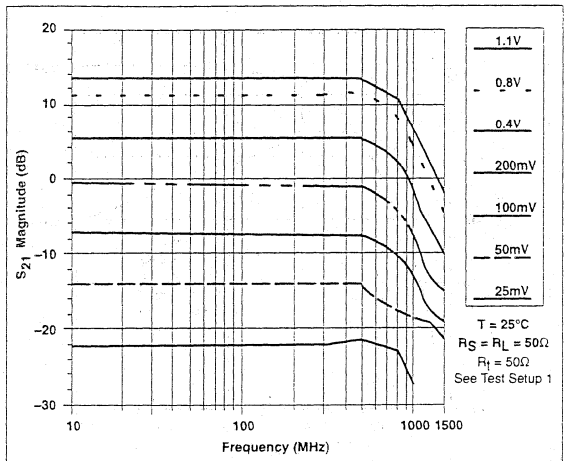


Figure 22. Insertion Gain vs Frequency and V_{AGC}

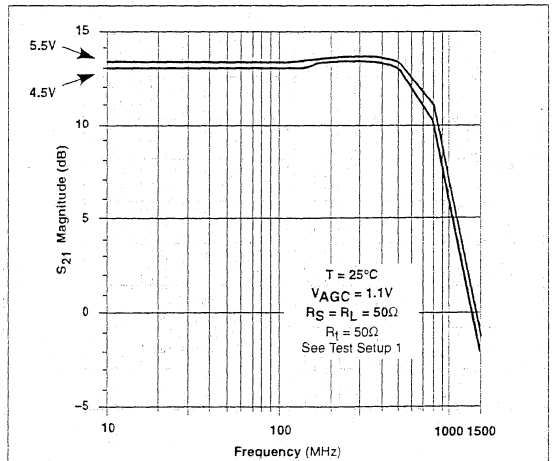


Figure 23. Insertion Gain vs Frequency and V_{CC}

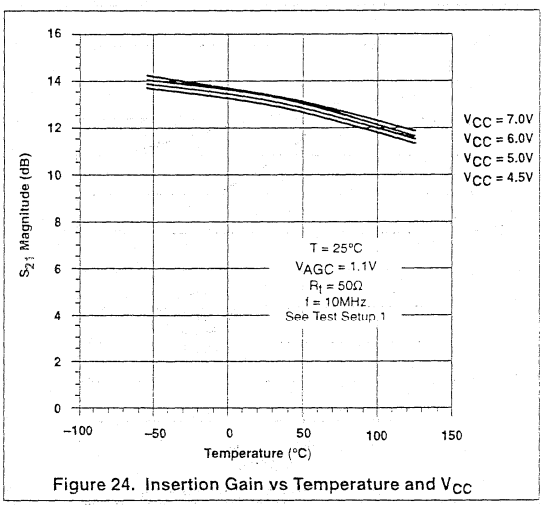


Figure 24. Insertion Gain vs Temperature and V_{CC}

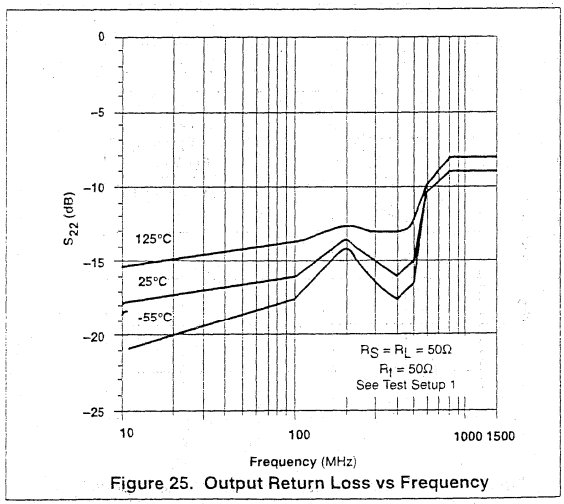


Figure 25. Output Return Loss vs Frequency

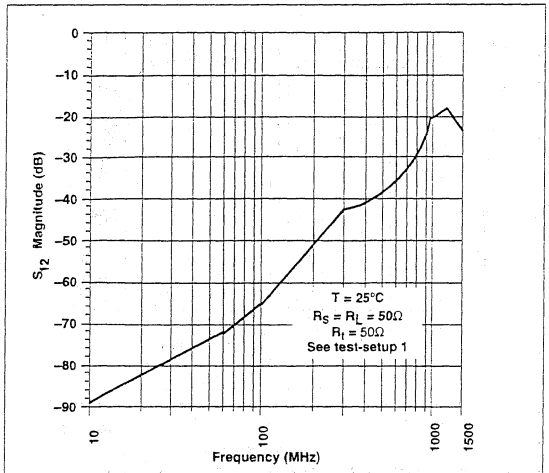


Figure 26. Reverse Isolation vs Frequency

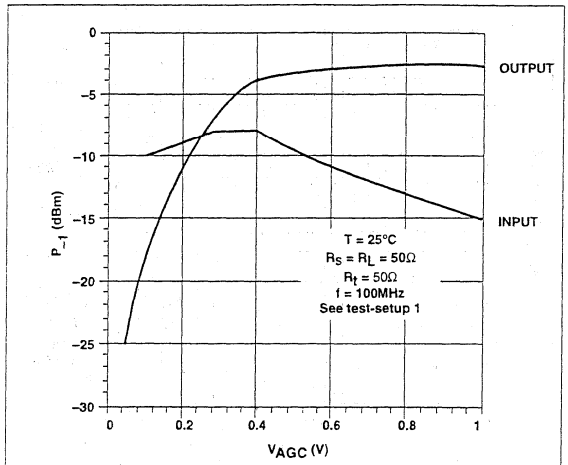


Figure 27. 1dB Gain Compression vs V_{AGC}

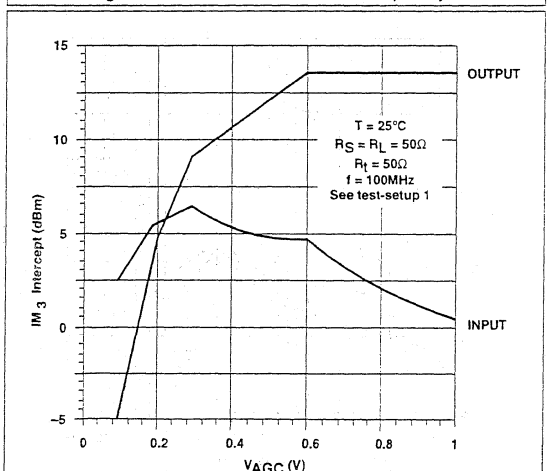


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

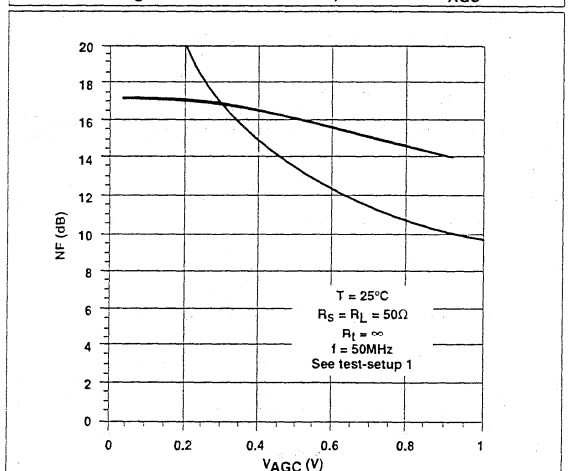


Figure 29. Noise Figure vs V_{AGC}

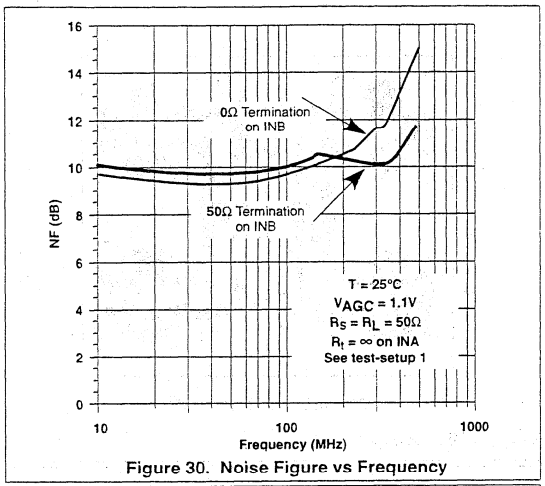


Figure 30. Noise Figure vs Frequency

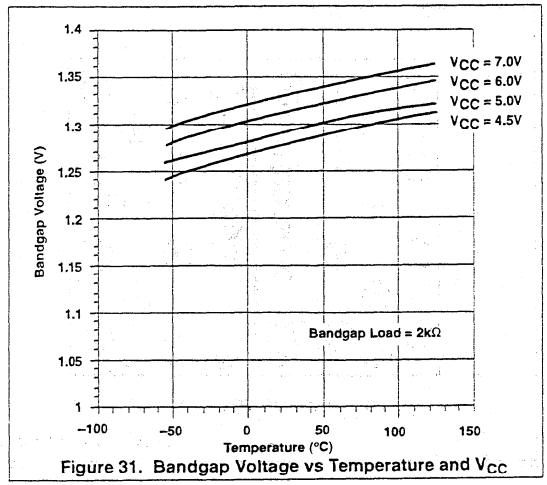


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

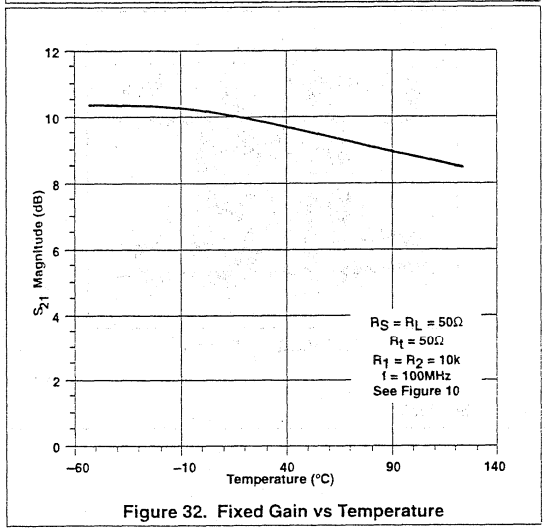
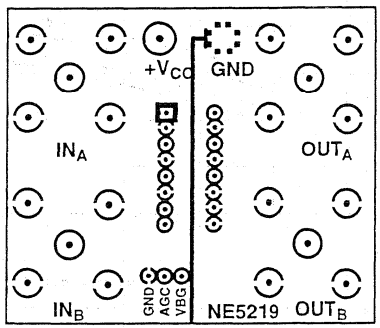
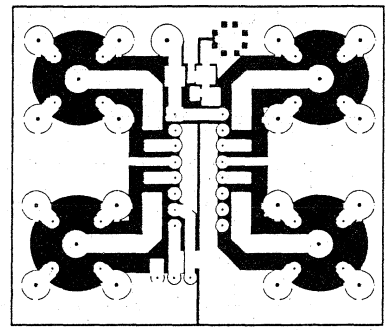


Figure 32. Fixed Gain vs Temperature

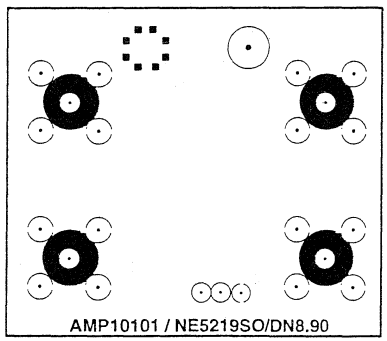


TOP VIEW - COMPONENT SIDE

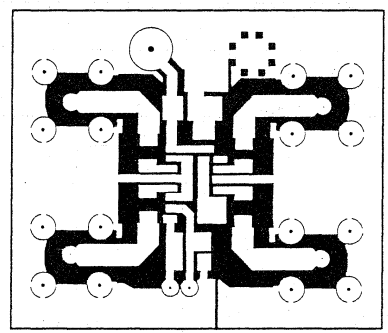


TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout (DIP Package)



BOTTOM VIEW - D Package



TOP VIEW - D Package

VGA AC Evaluation Board Layout (SO Package)

Matched quad high-performance low-voltage operational amplifier

NE/SA5234

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

DESCRIPTION

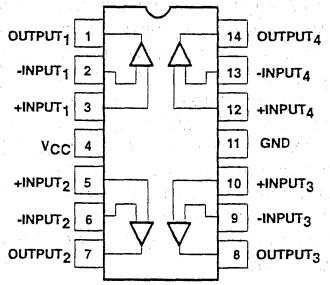
The NE/SA5234 is a matched, low voltage, high performance quad operational amplifier. Among its unique input and output characteristics is the capability for both input and output rail-to-rail operation, particularly critical in low voltage applications. The output swings to less than 50mV of both rails across the entire power supply range. The NE/SA5234 is capable of delivering 5.5V peak-to-peak across a 600Ω load and will typically draw only 700µA per amplifier. The bandwidth is 2.5MHz and the 1% settling time is 1.4µs.

FEATURES

- Wide common-mode input voltage range: 250mV beyond both rails
- Output swing within 50mV of both rails
- Functionality to 1.8V typical
- Low current consumption: 700µA per amplifier
- ±15mA output current capability
- Unity gain bandwidth: 2.5MHz
- Slew rate: 0.8V/µs
- Low noise: 25nV/√Hz
- Electrostatic discharge protection
- Short-circuit protection
- Output inversion prevention

PIN CONFIGURATION

N, and D PACKAGES



APPLICATIONS

- Automotive electronics
- Signal conditioning and sensing amplification
- Portable instrumentation
  - Test and measurement
  - Medical monitors and diagnostics
  - Remote meters
- Audio equipment
- Security systems
- Communications
  - Pagers
  - Cellular telephone
  - LAN
  - 5V Datacom bus
- Error amplifier in motor drives
- Transducer buffer amplifier

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5234D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5234N	0405B
14-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5234D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5234N	0405B

Programmable Analog Compandor NE/SA572

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

DESCRIPTION

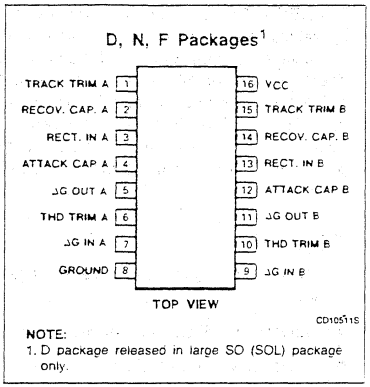
The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- Independent control of attack and recovery time
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external op amp
- Wide dynamic range — greater than 110dB
- Temperature-compensated gain control
- Low distortion gain cell
- Low noise — 6μV typical
- Wide supply voltage range — 6V – 22V
- System level adjustable with external components

PIN CONFIGURATION



NOTE:
1. D package released in large SO (SOL) package only.

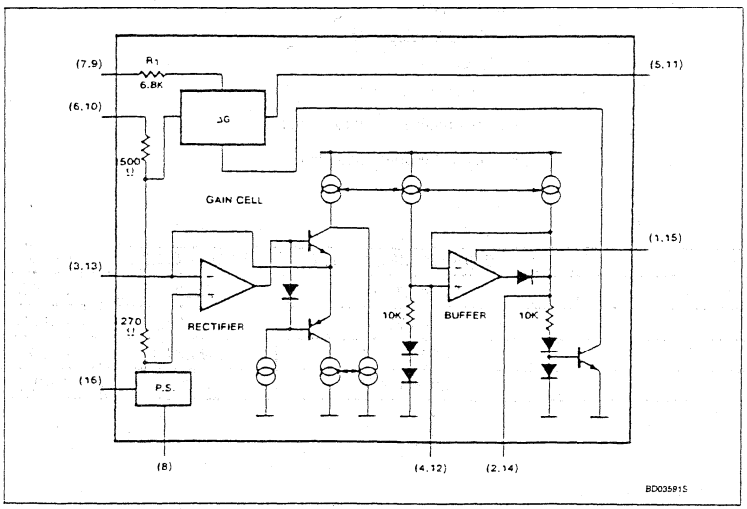
APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High-level limiter
- Low-level noise gate
- State variable filter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE572D
16-Pin Plastic DIP	0 to +70°C	NE572N
16-Pin Plastic SO	−40°C to +85°C	SA572D
16-Pin Cerdip	−40°C to +85°C	SA572F
16-Pin Plastic DIP	−40°C to +85°C	SA572N

BLOCK DIAGRAM



Low voltage Compandor NE/SA575

DESCRIPTION

The NE/SA575 is a precision dual gain control circuit designed for low voltage applications. The NE/SA575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

FEATURES

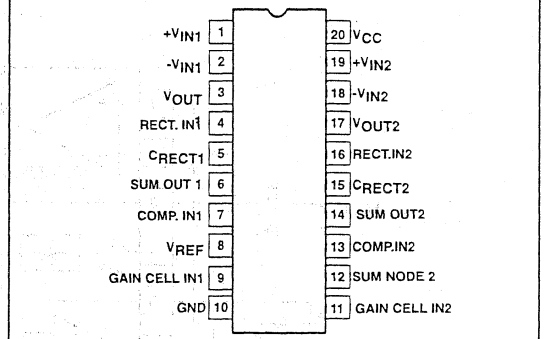
- Operating voltage range from 3V to 7V
- Reference voltage of $100mV_{RMS}$ = 0dB
- One dedicated summing op amp per channel and two extra uncommitted op amps
- 600Ω drive capability
- Single or split supply operation
- Wide input/output swing capability
- 3000V ESD protection

APPLICATIONS

- Portable communications
- Cellular radio
- Cordless telephone
- Consumer audio

PIN CONFIGURATION

N, D[1] and DK Packages



NOTE:
1. Available in large SOL package only.

- Portable broadcast mixers
- Wireless microphones
- Modems
- Electric organs
- Hearing aids

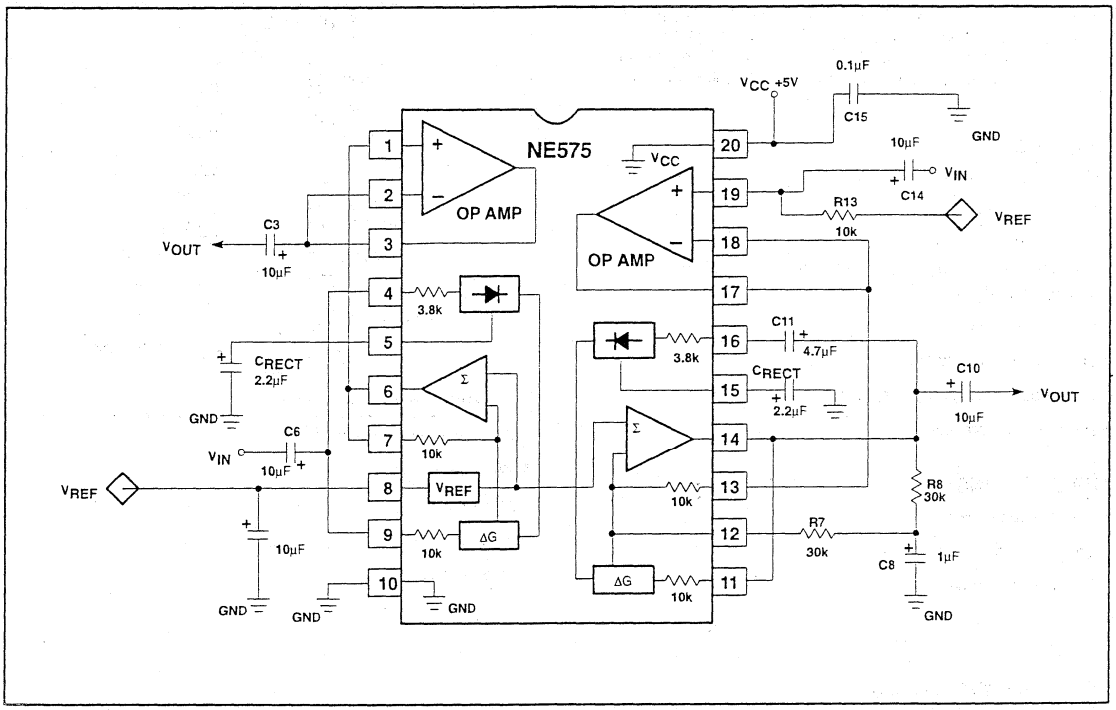
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE575N	0408
20-Pin Plastic Small Outline Large	0 to +70°C	NE575D	0172
20-Pin Plastic Shrink Small Outline Package (SSOP)	0 to +70°C	NE575DK	1563
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA575N	0408
20-Pin Plastic Small Outline Large	-40 to +85°C	SA575D	0172
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA575DK	1563

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING		UNITS
			NE575	SA575	
V_{CC}	Single supply voltage		−0.3 to 8	−0.3 to 8	V
V_{IN}	Voltage applied to any other pin		−0.3 to (V_{CC}+0.3)	−0.3 to (V_{CC}+0.3)	V
T_A	Operating ambient temperature range		-40 to +85	-40 to +85	°C
T_{STG}	Storage temperature range		-65 to +150	-65 to +150	°C
θ_{JA}	Thermal impedance	DIP	68	68	°C/W
		SOL	112	112	°C/W
		SSOP	117	117	°C/W

BLOCK DIAGRAM and TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 25°C. Minimum and Maximum values are for the full operating temperature range: 0 to 70°C for NE575, -40 to +85°C for SA575, except SSOP package is tested at +25°C only. V_{CC} = 5V, unless otherwise stated. Both channels are tested in the Expandor mode (see Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
For compandor, including summing amplifier									
V_{CC}	Supply voltage[1]		3	5	7	3	5	7	V
I_{CC}	Supply current	No signal	3	4.2	5.5	3	4.2	5.5	mA
V_{REF}	Reference voltage[2]	V_{CC} = 5V	2.4	2.5	2.6	2.4	2.5	2.6	V
R_L	Summing amp output load		10			10			kΩ
THD	Total harmonic distortion	1kHz, 0dB BW = 3.5kHz		0.12	1.0		0.12	1.5	%
E_{NO}	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	20		6	30	µV
0dB	Unity gain level	1kHz	-1.0		1.0	-1.5		1.5	dB
V_{OS}	Output voltage offset	No signal	-100		100	-150		150	mV
	Output DC shift	No signal to 0dB	-50		50	-100		100	mV
	Tracking error relative to 0dB	Gain cell input = 0dB, 1kHz Rectifier input = 6dB, 1kHz	-0.5		0.5	-1.0		1.0	dB
		Gain cell input = 0dB, 1kHz Rectifier input = -30dB, 1kHz	-0.5		0.5	-1.0		1.0	dB

DC ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Crosstalk	1kHz, 0dB, C_{REF} = 220µF		-80	-65		-80	-65	dB
For operational amplifier									
V_O	Output swing	R_L = 10kΩ	V_{CC}-0.4	V_{CC}		V_{CC}-0.4	V_{CC}		V
R_L	Output load	1kHz	600			600			Ω
CMR	Input common-mode range		0		V_{CC}	0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V to 4.5V	-0.5		0.5	-1		1	µA
V_{OS}	Input offset voltage			3			3		mV
A_{VOL}	Open-loop gain	R_L = 10kΩ		80			80		dB
SR	Slew rate	Unity gain		1			1		V/µs
GBW	Bandwidth	Unity gain		3			3		MHz
E_{NI}	Input voltage noise	BW = 20kHz		2.5			2.5		µV
PSRR	Power supply rejection ratio	1kHz, 250mV		60			60		dB

NOTES:
1. Operation down to V_{CC} = 2V is possible, but performance is reduced. See curves in Figure 5a and 5b.
2. Reference voltage, V_{REF}, is typically at 1/2V_{CC}.

FUNCTIONAL DESCRIPTION

This section describes the basic subsystems and applications of the NE/SA575 Compandor. More theory of operation on compandors can be found in AN174 and AN176. The typical applications of the NE/SA575 low voltage compandor in an Expandor (1:2), Compressor (2:1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 1, 2, 3 respectively.

The NE/SA575 has two channels for a complete companding system. The left channel, A, can be configured as a 1:2 Expandor while the right channel, B, can be configured as either a 2:1 Compressor, a 1:2 Expandor or an ALC. Each channel consists of the basic companding building blocks of rectifier cell, variable gain cell, summing amplifier and V_{REF} cell. In addition, the NE/SA575 has two additional high performance uncommitted op amps which can be utilized for application such as filtering, pre-emphasis/de-emphasis or buffering.

Figure 4 shows the complete schematic for the applications demo board. Channel A is configured as an expandor while channel B is configured so that it can be used either as a compressor or as an ALC circuit. The switch, S1, toggles the circuit between compressor and ALC mode. Jumpers J1 and J2 can be used to either include the additional op amps for signal conditioning or exclude them from the signal path. Bread boarding space is provided for R1, R2, C1, C2, R10, R11, C10 and C11 so that the response can be tailored for each individual need. The components as specified are suitable for the complete audio spectrum from 20Hz to 20kHz.

The most common configuration is as a unity gain non-inverting buffer where R1, C1, C2, R10, C10 and C11 are eliminated and R2 and R11 are shorted. Capacitors C3, C5, C8, and C12 are for DC blocking. In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors C4 and C9 are for setting the attack and release time constant.

C6 is for decoupling and stabilizing the voltage reference circuit. The value of C6 should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be. R12 provides DC reference voltage to the amplifier of channel B. R6 and R7 provide a DC feedback path for the summing amp of channel B, while C7 is a short-circuit to ground for signals. C14 and C15 are for power supply decoupling. C14 can also be eliminated if the power supply is well regulated with very low noise and ripple.

DEMONSTRATED PERFORMANCE

The applications demo board was built and tested for a frequency range of 20Hz to 20kHz with the component values as shown in Figure 4 and V_{CC} = 5V. In the expandor mode, the typical input dynamic range was from -34dB to +12dB where 0dB is equal to 100mV_{RMS}. The typical unity gain level measured at 0dB @ 1kHz input was ±0.5dB and the typical tracking error was ±0.1dB for input range of -30 to +10dB.

In the compressor mode, the typical input dynamic range was from -42dB to ±18dB with a tracking error +0.1dB and the typical unity gain level was ±0.5dB.

In the ALC mode, the typical input dynamic range was from -42dB to +8dB with typical output deviation of ±0.2dB about the nominal output of 0dB. For input greater than +9dB in ALC configuration, the summing amplifier sometimes exhibits high frequency oscillations. There are several solutions to this problem. The first is to lower the values of R6 and R7 to 20kΩ each. The second is to add a current limiting resistor in series with C12 at Pin 13. The third is to add a compensating capacitor of about 22 to 30pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18dB yielding a dynamic range of over 60dB.

EXPANDOR

The typical expandor configuration is shown in Figure 1. The variable gain cell and the rectifier cell are in the signal input path. The V_{REF} is always 1/2 V_{CC} to provide the maximum headroom without clipping. The 0dB ref is 100mV_{RMS}. The input is AC coupled through C5, and the output is AC coupled through C3. If in a system the inputs and outputs are AC coupled, then C3 and C5 can be eliminated, thus requiring only one external component, C4. The variable gain cell and rectifier cell are DC coupled so any offset

voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.
The expandor gain expression and the attack and release time constant is given by Equation 1 and Equation 2, respectively.

Equation 1.

$$\text{Expandor gain} = \frac{4V_{IN}(avg)}{3.8k \times 100\mu A}$$

where $V_{IN}(avg) = 0.95V_{IN(RMS)}$

Equation 2.

$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$

COMPRESSOR

The typical compressor configuration is shown in Figure 2. In this mode, the rectifier cell and variable gain cell are in the feedback path. R6 and R7 provide the DC feedback to the summing amplifier. The input is AC coupled through C12 and output is AC coupled through C8. In a system with inputs and outputs AC coupled, C8 and C12 could be eliminated and only R6, R7, C7, and C13 would be required. If the external components R6, R7 and C7 are eliminated, then the output of the summing amplifier will motor-boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.
The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4, respectively.

Equation 3.

$$\text{Compressor gain} = \left[\frac{3.8k \times 100\mu A}{4V_{IN}(avg)}\right]^{1/2}$$

where $V_{IN}(avg) = 0.95V_{IN(RMS)}$

Equation 4.

$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$

AUTOMATIC LEVEL CONTROL

The typical Automatic Level Control circuit configuration is shown in Figure 3. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through C12 and C13 and the output is AC coupled through C8. Once again, as in the previous cases, if the system input and output signals are already AC coupled, then C12, C13 and C8 could be eliminated. Concerning the compressor, removing R6, R7 and C7 will cause motor-boating in absence of signals. C_{COMP} is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60dB with the output within ±0.5dB typical. The necessary design expressions are given by Equation 5 and Equation 6, respectively.

Equation 5.

$$\text{ALC gain} = \frac{3.8k \times 100\mu A}{4V_{IN}(avg)}$$

Equation 6.

$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C9$

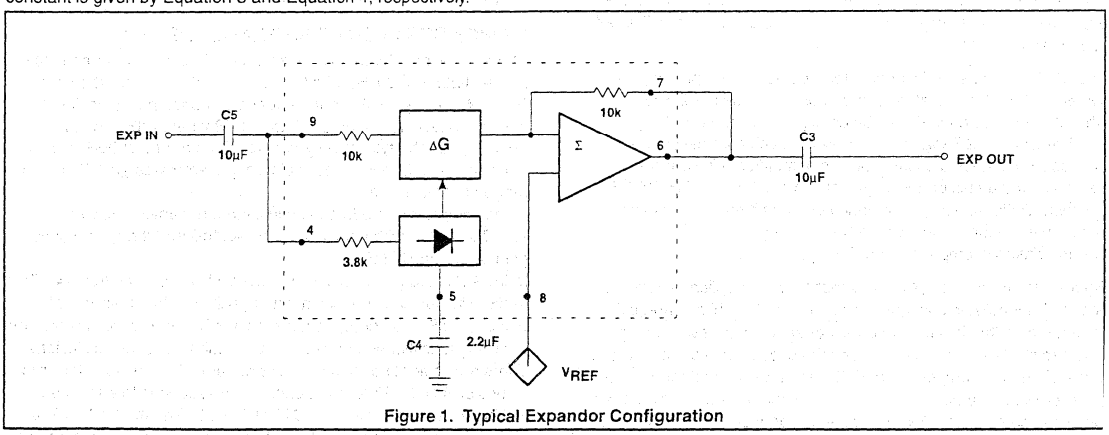


Figure 1. Typical Expandor Configuration

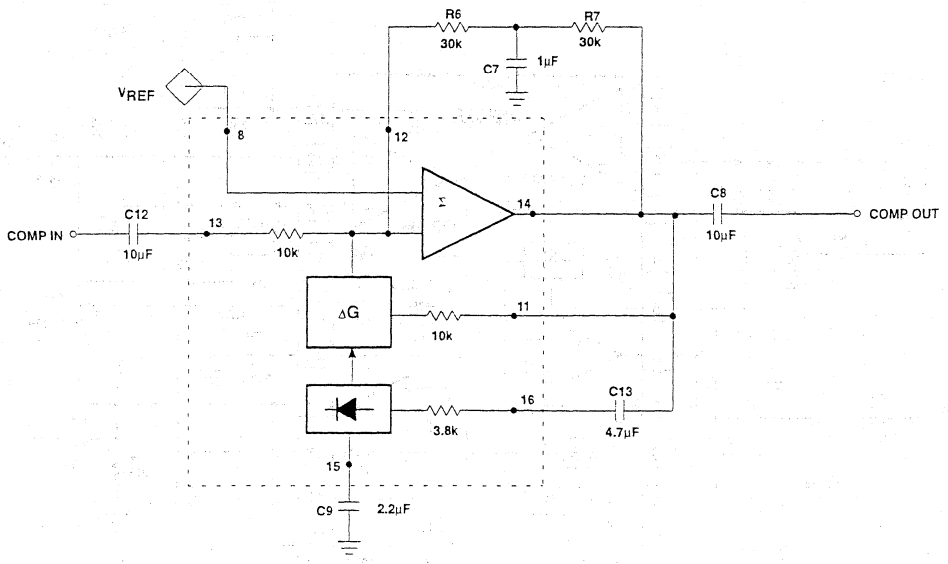


Figure 2. Typical Compressor Configuration

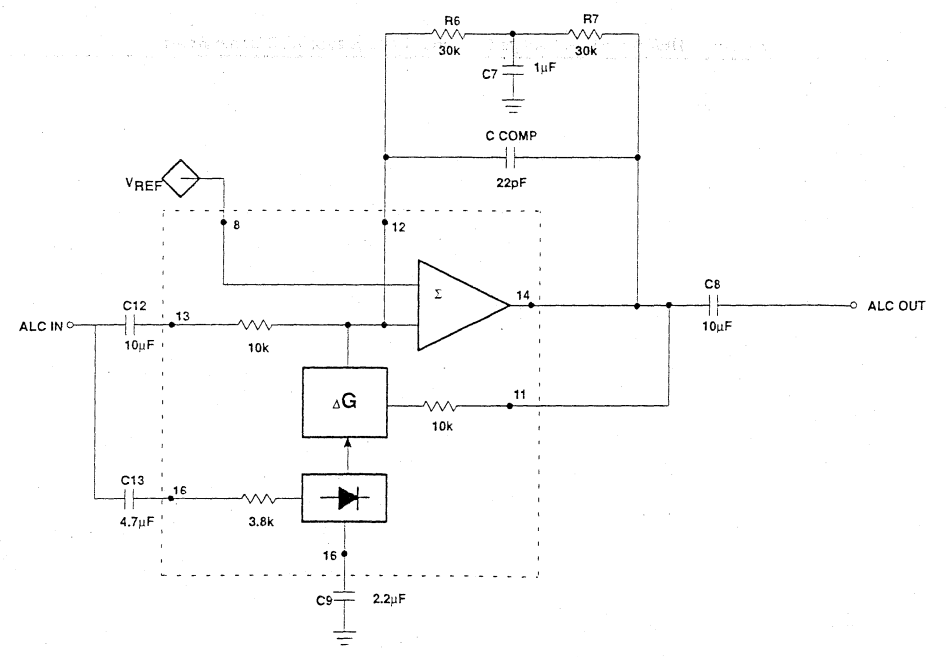


Figure 3. Typical ALC Configuration

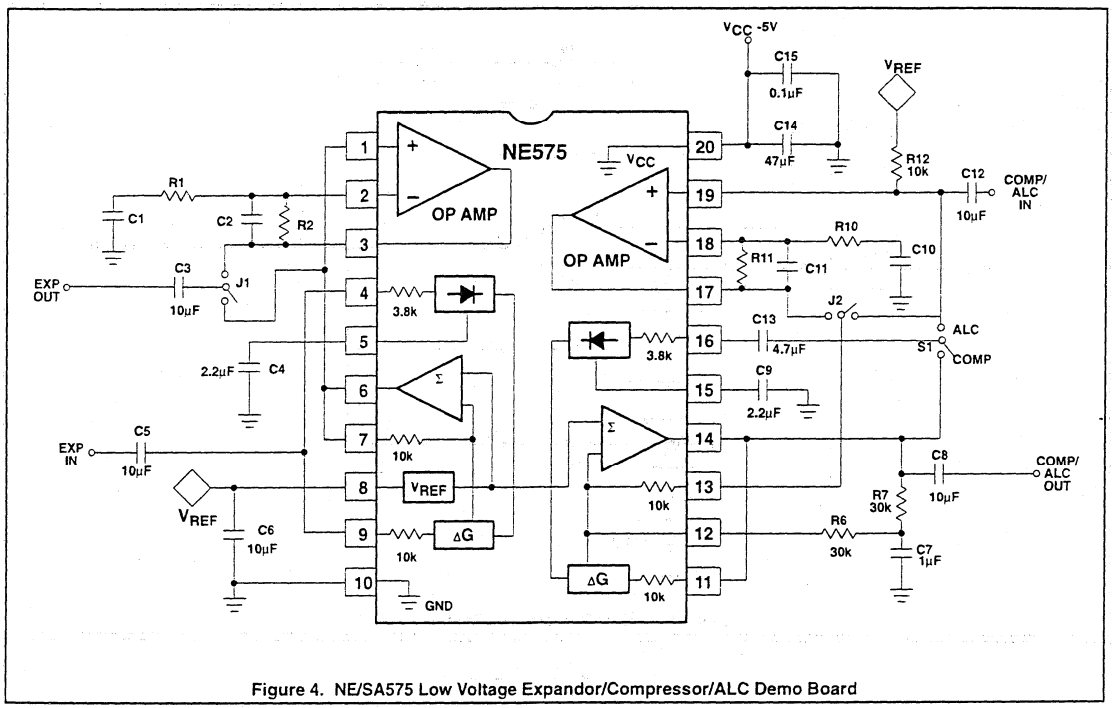
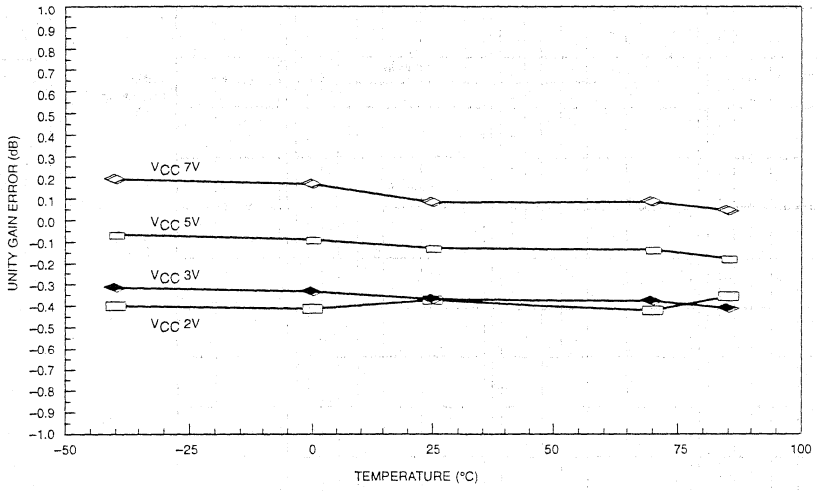
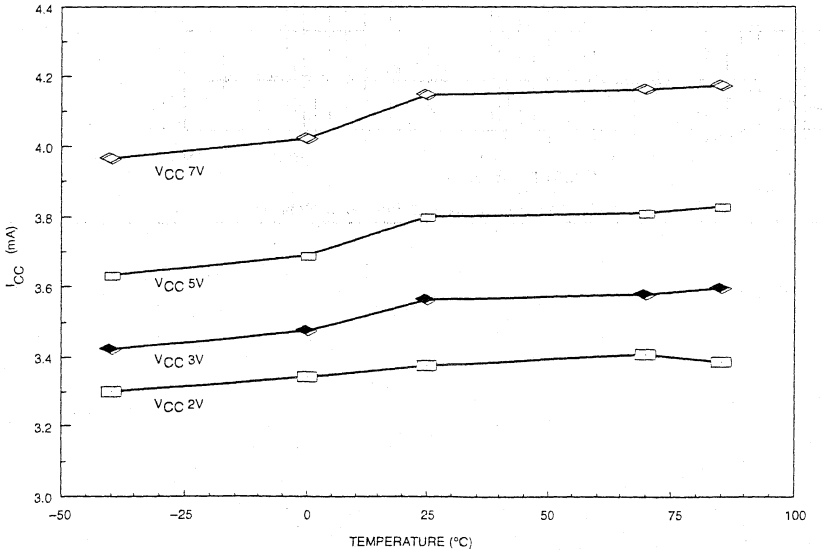


Figure 4. NE/SA575 Low Voltage Expandor/Compressor/ALC Demo Board



a. Unity Gain Error vs Temperature and V_{CC}



b. I_{CC} vs Temperature and V_{CC}

Figure 5. Temperature and V_{CC} Curves

TYPICAL PERFORMANCE CHARACTERISTICS

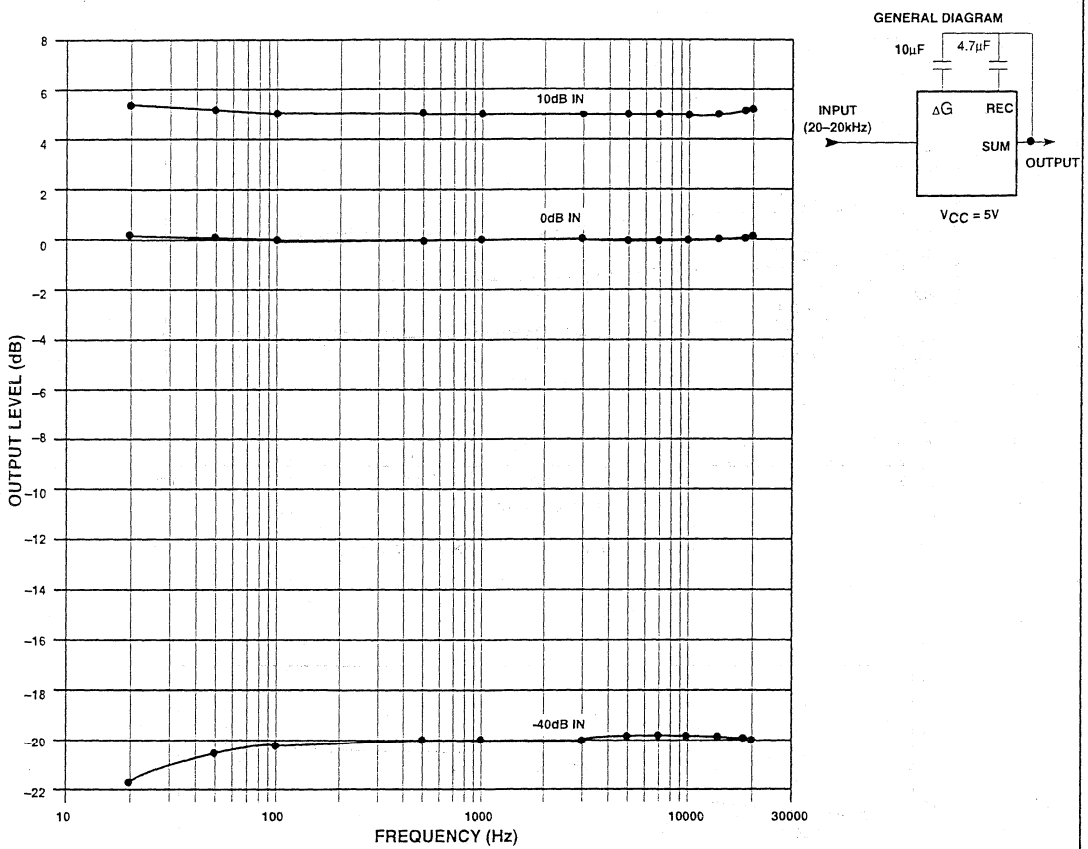


Figure 6. Compressor Output Frequency Response

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

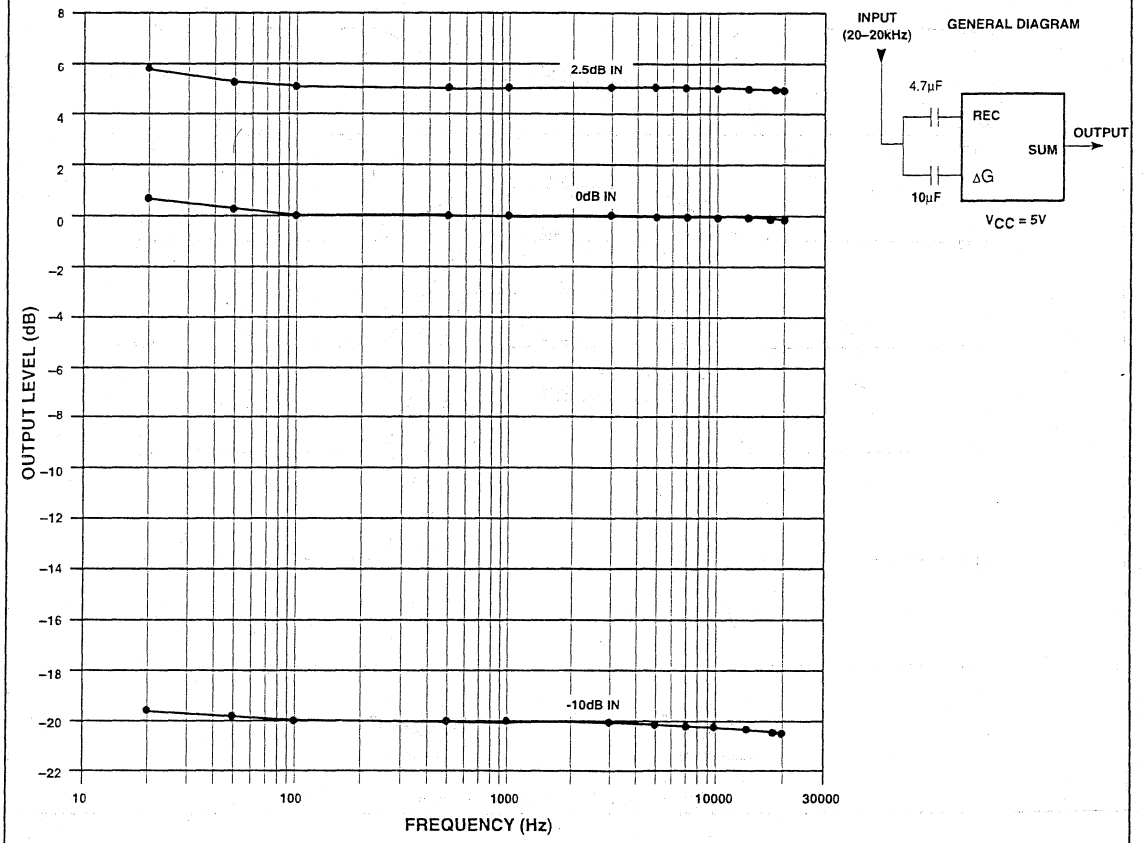


Figure 7. Expandor Output Frequency Response

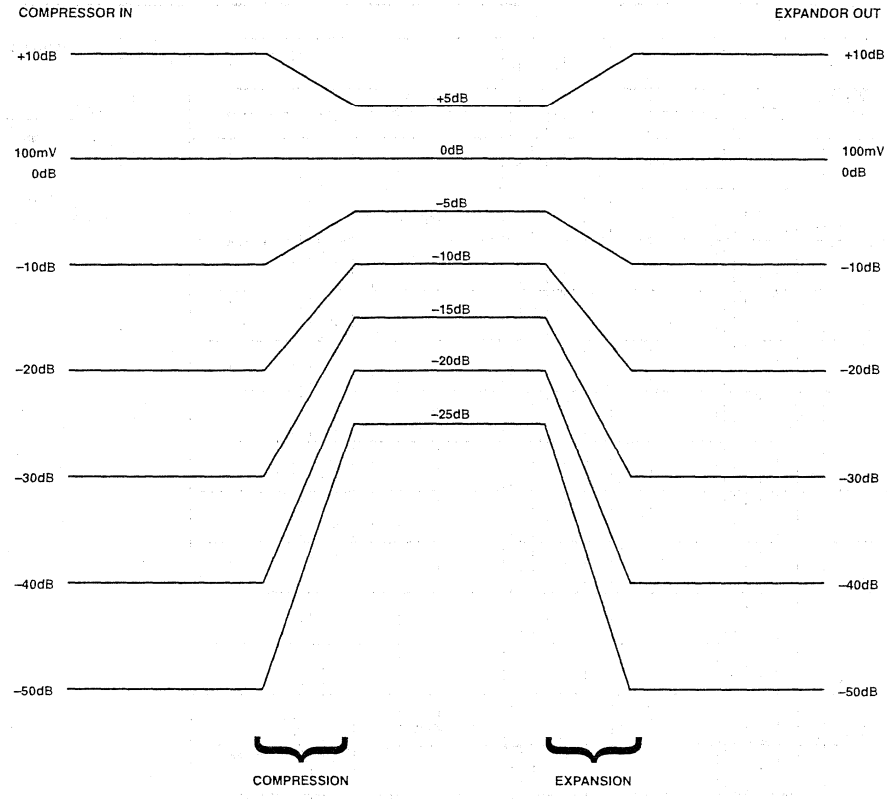


Figure 8. The Companding Function

Audio processor - companding and amplifier section

NE/SA5750

DESCRIPTION

The NE/SA5750 is a high performance low power audio signal processing system. The NE/SA5750 subsystems include a low noise microphone preamplifier with adustable gain, a noise cancellation switching amplifier with adjustable threshold, a voice operated transmitter (VOX) switch, VOX control, an audio compressor with buffered input, audio expandor, a unity gain power amplifier to drive a speaker, a summing power amplifier for sidetone attenuation and headphone (earpiece) drive, and an internal bandgap voltage regulator with power down capability. When used with Signetics' NE/SA5751, the complete audio processing function of an AMPS or TACS cellular telephone is easily implemented. The NE/SA5750 can also be used without the NE/SA5751 in a wide variety of radio communications applications.

FEATURES

- High performance
- 5V supply
- Adjustable VOX and noise cancellation threshold
- Adjustable gain preamplifier
- Audio companding
- ESD protected
- Open collector VOX output
- Logic inputs CMOS compatible
- Power down mode
- Built-in drivers for speaker and earpiece
- Few external components
- SOL and DIP packages

BENEFITS

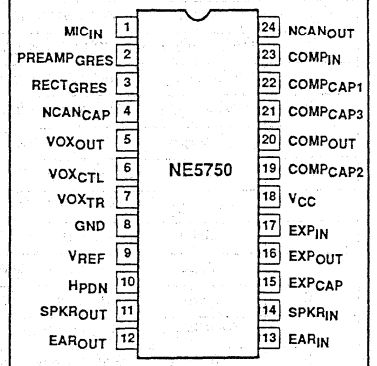
- Very compact applications
- Long battery life in portable equipment
- Complete cellular audio function with the SA5751

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION

D[1] and N PACKAGE



NOTE:
1. Available only in SOL (large SO) package.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	0 to +70°C	NE5750N
24-Pin Plastic SOL	0 to +70°C	NE5750D
24-Pin Plastic DIP	–40 to +85°C	SA5750N
24-Pin Plastic SOL	–40 to +85°C	SA5750D

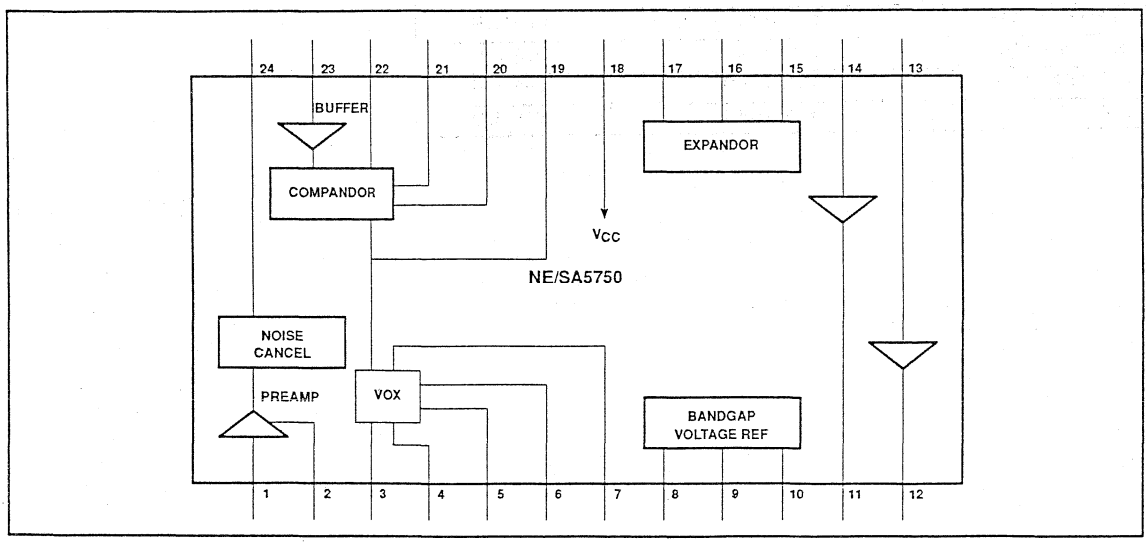
Audio processor - companding and amplifier section

NE/SA5750

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	MIC_{IN}	Microphone input
2	$PREAMP_{GRES}$	Preamplifier gain resistor
3	$RECT_{GRES}$	Reactifier gain resistor
4	$NCAN_{CAP}$	Noise cancellation timing capacitor
5	VOX_{OUT}	Voice operated transmission output
6	VOX_{CTL}	Voice operated transmission control
7	VOX_{TR}	Voice operated transmission threshold resistor
8	GND	Ground
9	V_{REF}	Reference voltage
10	H_{PDN}	Hardware power down
11	$SPKR_{OUT}$	Speaker output
12	EAR_{OUT}	Earpiece output
13	EAR_{IN}	Earpiece input, side tone input
14	$SPKR_{IN}$	Speaker input
15	EXP_{CAp}	Expandor timing capacitor
16	EXP_{OUT}	Expandor output
17	EXP_{IN}	Expandor input
18	V_{CC}	Positive supply
19	$COMP_{CAP2}$	Compressor timing capacitor 2
20	$COMP_{OUT}$	Compressor output
21	$COMP_{CAP3}$	Compressor timing capacitor 3
22	$COMP_{CAP1}$	Compressor timing capacitor 1
23	$COMP_{IN}$	Compressor input
24	$NCAN_{OUT}$	Noise cancellation output

BLOCK DIAGRAM



Audio processor - companding and amplifier section

NE/SA5750

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage Voltage applied to any pin	6 –0.3 to (V_{CC} + 0.3)	V V
T_{STG}	Storage temperature	–65 to +150	°C
T_A	Ambient operating temperature NE5750 SA5750	 0 to 70 –40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5.0V, 0dB = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
V_{CC}	Supply voltage		4.75	5.0	5.25	V
I_{CC}	Supply current	No signal Power down mode		8.4 1.8	12.0 3.0	mA mA
Z_L	Load impedance pins $NCAN_{OUT}$, EXP_{OUT}		50			kΩ
	$COMP_{OUT}$[1]		10			kΩ
Z_{IN}	Input impedance $COMP_{IN}$, MIC_{IN}, $SPKR_{IN}$		40	50	60	kΩ
	EXP_{IN}[2]		2.0	2.5		kΩ
	Noise cancellation current	Pin 7, grounded	40	50	60	µA
V_{OS}	DC offset $NCAN_{OUT}$[3]		–50		50	mV

NOTES:
1. Compressor is tested in production with 50kΩ load.
2. Not tested in production.
3. Offset values are identical for both gain states of noise reduction circuit.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5.0V, 0dB level = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
	Preamplifier gain range Preamplifier voltage gain 0dB Preamplifier voltage gain 40dB	 Pin 2 open Pin 2 AC ground	0 –1.0 39.0	 0 40	40 1.0 41.0	dB dB dB
	Preamplifier noise density	Pin 2 AC grounded RS = 0 – 50kΩ unweighted 20Hz–20kHz		7		$nV/\sqrt{Hz}$
		weighted CCIR DIN45405 20–20kHz		8		$nV/\sqrt{Hz}$
	Switch amplifier gain		9	10	11	dB
	Sidetone attenuation range				30	dB
Compandor 1kHz, all tests[1]						
$COMP_{OUT}$	Compressor error at –21dB output level	Input level = –42dB		0.38		dB
$COMP_{OUT}$	Compressor error at –10dB output level	Input level = –20dB	–1.0		1.0	dB
$COMP_{OUT}$	Compressor error at 0dB output level	Input level = 0dB	–1.5	0.12	1.5	dB
$COMP_{OUT}$	Compressor error at +5dB output level	Input level = +10dB	–1.0		1.0	dB
$COMP_{OUT}$	Compressor error at +12.3dB output level	Input level = +24.6dB	–1.0		1.0	dB
EXP_{OUT}	Expandor error at –42dB output level	Input level = –21dB		–0.41		dB
EXP_{OUT}	Expandor error at –21dB output level	Input level = –10.5dB	–1.0		1.0	dB

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5.0V$, 0dB level = $77.5mV_{RMS}$. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
EXP_{OUT}	Expandor error at –10dB output level	Input level = –5dB	–1.0		1.0	dB
EXP_{OUT}	Expandor error at 0dB output level	Input level = 0dB	–1.5	–0.18	1.5	dB
EXP_{OUT}	Expandor error at +10dB output level	Input level = +5dB	–1.0		1.0	dB
EXP_{OUT}	Expandor error at +24.6dB output level[2]	Input level = +12.3dB	–1.5		1.5	dB
EXP_{OUT}	Expandor V_{OS}	No signal	–50.0		50.0	mV
EXP_{OUT}	Expandor output DC shift	No signal to 0dB	–100		100	mV
	Timing capacitors compandor			2.2		µF
THD	Total harmonic distortion					
	Compressor	1kHz, 0dB		0.09	1	%
	Expandor	1kHz, 0dB		0.09	1	%
	$NCAN_{OUT}$	1kHz. Pin 2 open output level = 0dB		0.18	1	%
		1kHz, Pin 2 open output level = +25dB		0.13	1	%
	Speaker amplifier Drive capability				40	mA_{P-P}
	Output swing (<1% THD)	50Ω load	2	3.2		V_{P-P}
		100Ω load	3	4.1		V_{P-P}
		No load	4	4.9		V_{P-P}
	Ear amplifier Drive capability				10	mA_{P-P}
	Output swing (<1% THD)	300Ω load	3	4.3		V_{P-P}
		2000Ω load	4	4.9		V_{P-P}
		No load	4	4.9		V_{P-P}
VOX_{OUT}	Sink current				0.5	mA
	Low level High level	Open collector $I_L = 0.5mA$	 4	0.07 5	0.4	V V
VOX_{CTL}	Input current Low		–50	–21	0	µA
	High		–10		+10	µA
	Input level Low High		0 3.5		1.5 5	V V
H_{PDN}	Input current Low		–10		+10	µA
	High		–10		+10	µA
	Input level Low High		0 3.5		1.5 5	V V
	Reference filter capacitor			10		µF

NOTE:
1. Measurements are relative to 0dB output.
2. Measurement is absolute and indicative of the output dynamic range capability.

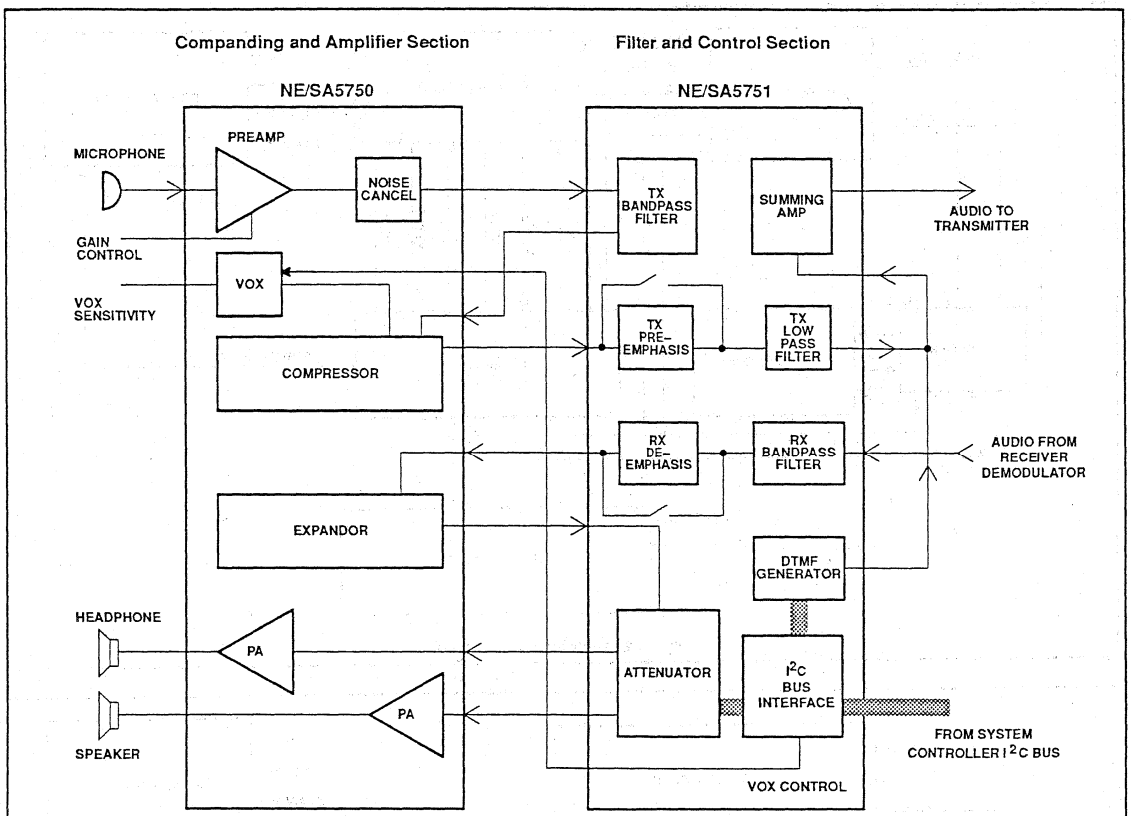


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

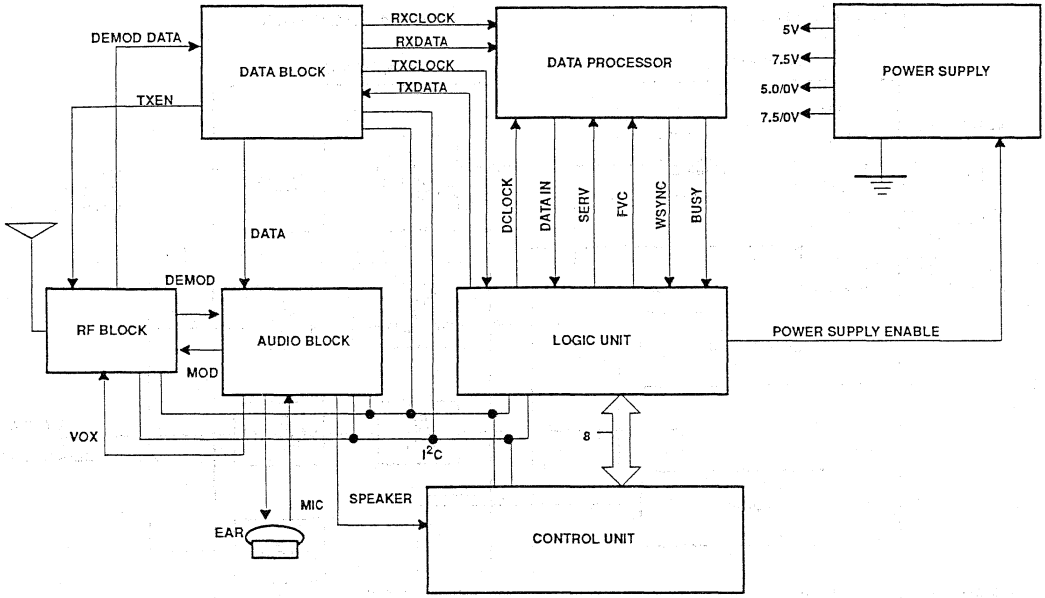


Figure 2. Cellular Radio System

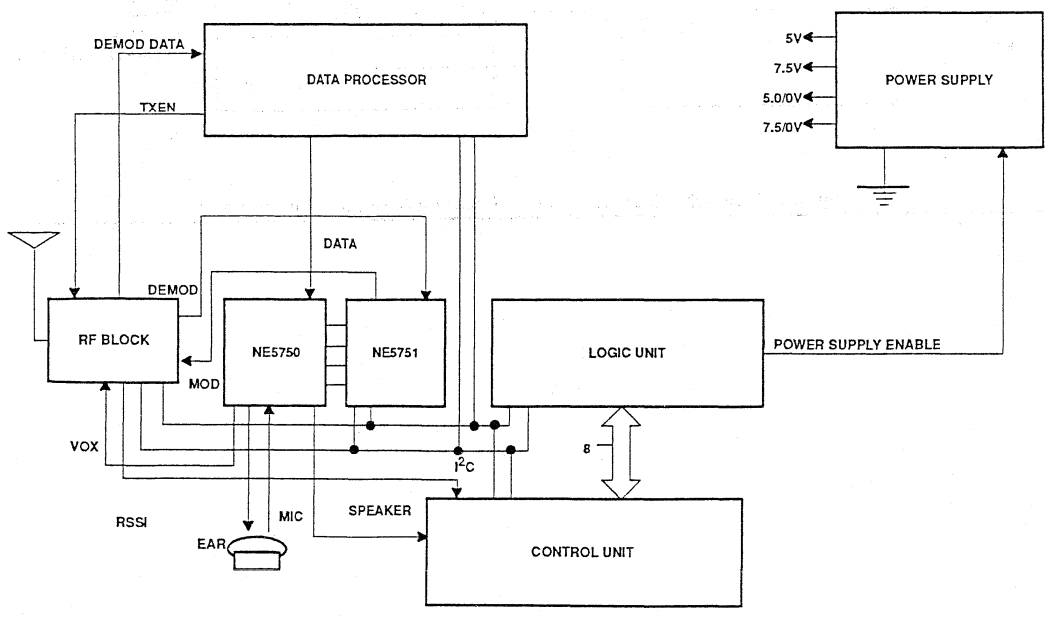


Figure 3. APROC Application Diagram

Audio processor - companding and amplifier section

NE/SA5750

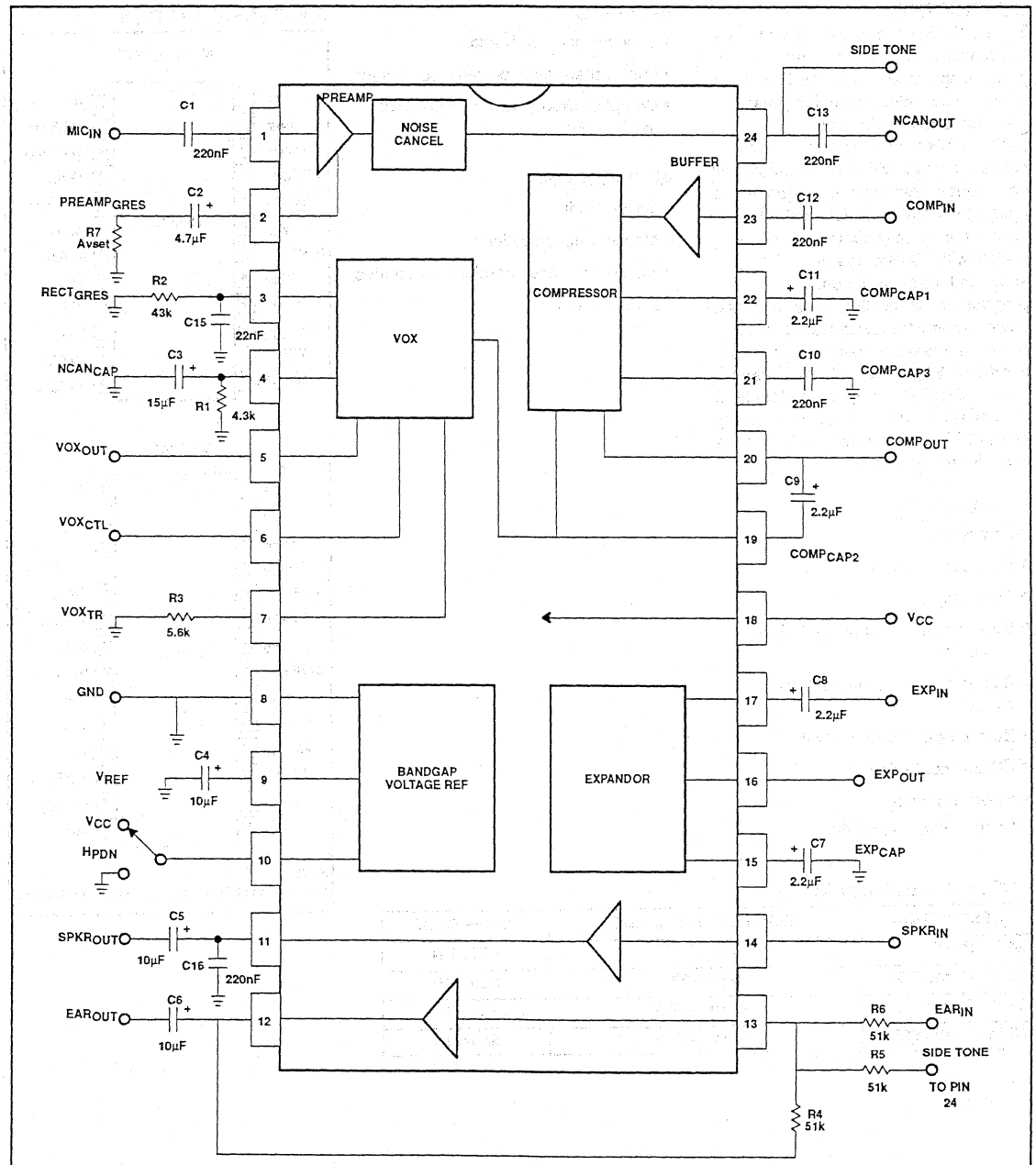


Figure 4. NE/SA5750 Test and Application Circuit

Audio processor - filter and control section

NE/SA5751

DESCRIPTION

The NE/SA5751 is a high performance low power CMOS audio signal processing system. The NE/SA5751 subsystems include complementary transmit/receive voice band (300–3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, a digitally controlled volume control with 30dB range (in 2dB steps), audio path mute switches, a programmable DTMF generator, power-down circuitry for low current standby, power-on reset capability, and an I^2C interface. When the SA5751 is used with an SA5750 (companding function), the complete audio processing system of an AMPS or TACS cellular telephone is easily implemented.

FEATURES

- Low power
- High performance
- 5V supply
- Built-in programmable DTMF generator
- Built-in digitally controlled volume control
- Built-in peak-deviation limit
- I^2C Bus controlled
- Power-on reset
- Power-down capability

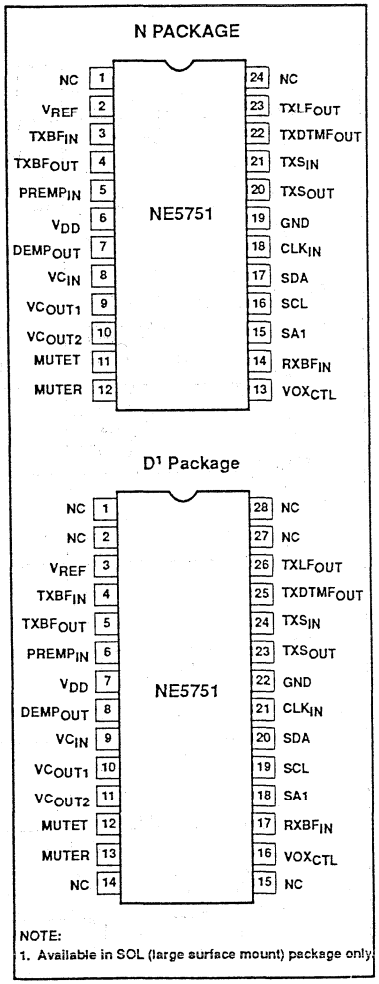
BENEFITS

- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5750

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION



NOTE:
1. Available in SOL (large surface mount) package only.

ORDERING INFORMATION

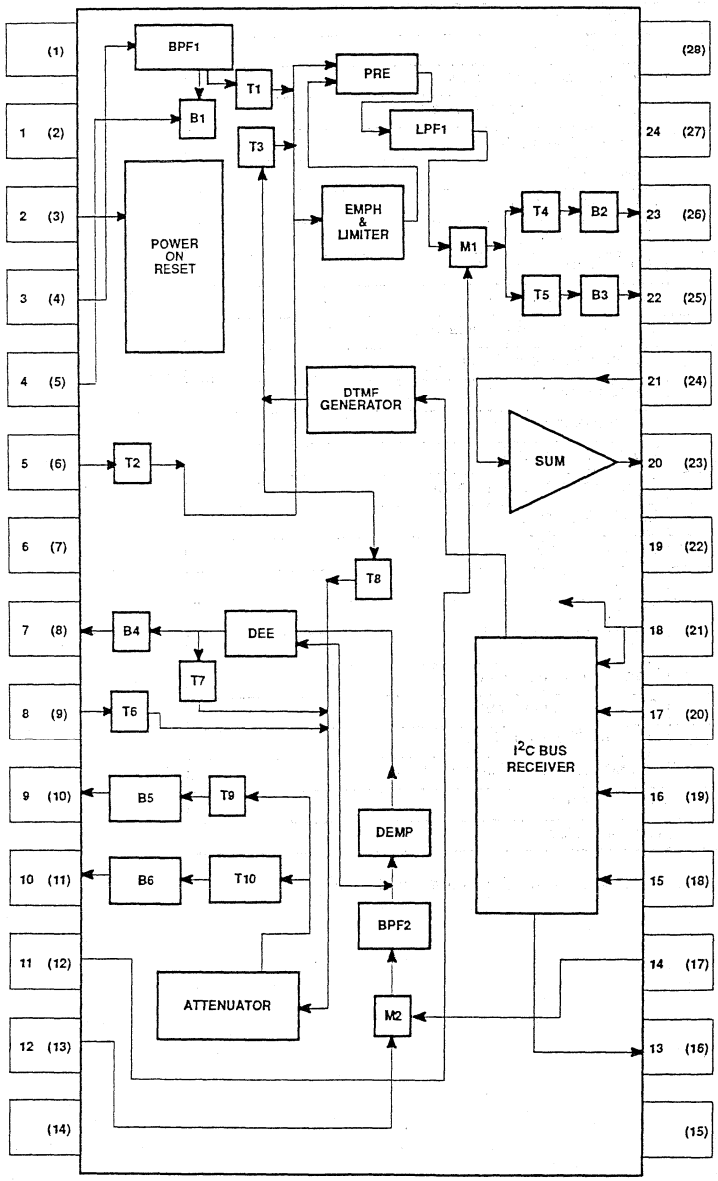
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	0 to +70°C	NE5751N
28-Pin Plastic SOL	0 to +70°C	NE5751D
24-Pin Plastic DIP	–40 to +85°C	SA5751N
28-Pin Plastic SOL	–40 to +85°C	SA5751D

PIN DESCRIPTIONS

PIN NO.		SYMBOL	DESCRIPTION
	(1)	NC	Not connected
1	(2)	NC	Not connected
2	(3)	V_{REF}	Reference voltage
3	(4)	$TXBF_{IN}$	Transmit bandpass filter input
4	(5)	$TXBF_{OUT}$	Transmit bandpass filter output
5	(6)	$PREMP_{IN}$	Pre–emphasis input
6	(7)	V_{DD}	Positive supply
7	(8)	$DEMP_{OUT}$	De–emphasis output
8	(9)	VC_{IN}	Volume control input
9	(10)	VC_{OUT1}	Volume control output 1
10	(11)	VC_{OUT2}	Volume control output 2
11	(12)	MUTET	TX analog voice path mute input
12	(13)	MUTER	RX analog voice path mute input
	(14)	NC	Not connected
	(15)	NC	Not connected
13	(16)	VOX_{CTL}	Vox control output
14	(17)	$RXBF_{IN}$	Receive bandpass filter input
15	(18)	SA1	Serial bus address
16	(19)	SCL	Serial clock line
17	(20)	SDA	Serial data line
18	(21)	CLK_{IN}	Clock input
19	(22)	GND	Ground
20	(23)	TXS_{OUT}	Transmit summer output
21	(24)	TXS_{IN}	Transmit summer input
22	(25)	$TXDTMF_{OUT}$	Transmit DTMF output
23	(26)	$TXLF_{OUT}$	Transmit low–pass filter output
24	(27)	NC	Not connected
	(28)	NC	Not connected

NOTE:
1. Callouts are for N package; those in parentheses are for the D (SOL) package.

BLOCK DIAGRAM



NOTES:
1. T1 to T10 represent the signal path switches.
2. M1 and M2 represent the mute switches.
3. PRE and DEE represent the bypass switches for pre–emphasis and de–emphasis, respectively.
4. B1 to B6 represent the output buffers.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Power supply voltage[1]	6	V
T_{STG}	Storage temperature	–65 to +150	°C
T_A	Ambient operating temperature NE5751	0 to 70	°C
	SA5751	–40 to +85	°C

NOTE:
1. Voltage applied to any pin –0.3 to V_{DD} +0.3V

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V, unless otherwise specified. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Power supply voltage range		4.75	5.0	5.25	V
I_{DD}	Supply current	Operating Standby		2.7 0.9	5.0 2.0	mA mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V. See test circuit, Figure 4. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV_{RMS} = –20dBm, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		500		kΩ
	RX BPF gain with de–emphasis	f = 1kHz	–0.5	0	0.5	dB
	RX BPF gain with de–emphasis	f = 100Hz		–31	–29	dBm0
	RX BPF gain with de–emphasis	f = 300Hz	9.0	9.6	11.0	dBm0
	RX BPF gain with de–emphasis	f = 3kHz	–11.0	–10.0	–9.0	dBm0
	RX BPF gain with de–emphasis	f = 5.9kHz		–68	–50	dBm0
	RX BPF noise with de–emphasis	300Hz–3kHz		170		μV_{RMS}
	RX dynamic range	with deemphasis		80		dB
	$DEMP_{OUT}$ output impedance	f = 1kHz		40		Ω
	$DEMP_{OUT}$ output swing (1%)	2.3kΩ to V_{REF}; f = 1kHz	V_{DD} –3	3.5		V_{P-P}
	VC_{OUT1} ouput swing (1%)	50kΩ toV_{REF}; f = 1kHz	V_{DD} –1	4.5		V_{P-P}
	VC_{OUT2} output swing (1%)	50kΩ to V_{REF}; f = 1kHz	V_{DD} –1	4.5		V_{P-P}
	VC_{OUT1} noise	VC_{IN} grounded C – message		25		μV_{RMS}
	VC_{OUT2} noise	VC_{IN} grounded C – message		25		μV_{RMS}
	Mute threshold off		0		0.8	V
	Mute threshold on		2.0		5.0	V
	CLK1, 2 high		4.0		5.0	V
	CLK1, 2 low		0		1.0	V
	TX BPF anti alias rejection			40		dB
	TX BPF input impedance	f = 3kHz		500		KΩ

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
	TX BPF noise	300 – 3000kHz		90		μV_{RMS}
	TX LPF gain	f = 5.9kHz		–39	–36	dB
	TX LPF gain with pre–emphasis	f = 1kHz, 20dBV		12.06		dB
	TX LPF gain with pre–emphasis	f = 100Hz		–19		dBm0
	TX LPF gain with pre–emphasis	f = 300Hz		–10.45		dBm0
	TX LPF gain with pre–emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre–emphasis	f = 5900Hz		–39		dBm0
	TX LPF gain with pre–emphasis	f = 9kHz		–51		dBm0
	TX overall gain	1kHz	11.3	11.8	12.5	dB
	TX overall gain	100Hz		–47	–45	dBm0
	TX overall gain	300Hz	–11	–10.4	–9	dBm0
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		–52	–45	dBm0
	TX BPF output impedance	f = 1kHz		360		Ω
	TX BPF output swing (1%THD)	50kΩ to V_{REF} f = 1kHz		4.5		V_{P-P}
	TX BPF dynamic range			90		dB
	$PREMP_{IN}$ input impedance	f = 3kHz		500		kΩ
	Summing op amp					
	Slew rate	C_L = 15pF		0.75		V/µs
	Output impedance	Unity gain; f = 3kHz		40		Ω
	Output swing (1% THD)	1kHz, 5kΩ load (25°C)		4.3		V_{P-P}
	Volume control accuracy	–30dB to 0dB	–1	0	+1	dB
	Analog switches					
	Insertion loss			60		dB
	On time transition	MUTET, MUTER 0.8V –>2.0V		3		µs
	Off time transition	MUTET, MUTER 2.0V –>0.8V		0.25		µs

I²C CHARACTERISTICS

The I²C bus is for 2–way, 2–line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull–up resistor. When the bus is free, both lines are high. Data transfer may be initiated only when the bus is not busy.

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired–AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

Due to the variety of different devices which can be connected to the I²C bus, the levels of the logical "0" and "1" are not fixed and depend on the appropriate level of V_{DD}. For the typical supply voltage of 5V which is chosen here, logical "1" and logical "0" are, however, fixed respectively on maximum input LOW voltage, 1.5V and minimum input HIGH voltage, 3.0V.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock's cycle. If it does not remain HIGH, it may be ir terrupted as a control signal.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH whe the bus is not busy. A HIGH to LOW transitic of the data line while the clock line is HIGH defined as a start condition S. A LOW to HIG transition of the data line while the clock HIGH is defined as a stop condition.

SYSTEM CONFIGURATIONS

A device generating a message is "transmitter"; a device receiving a message the "receiver". The device that controls tl message is the "master"; and devices whic are controlled by the master are the "slaves'

ACKNOWLEDGE

The number of data bytes transferred between the start and the stop condition from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set up and hold times must be taken into account.

I²C BUS DATA CONFIGURATIONS

The NE5751 is always a slave receiver in the I²C bus configuration (R/W bit–0). The slave address consists of seven bits in the serial mode where the least significant bit is selectable by hardware on input A0 and the other more significant bits are internally fixed.

POWER ON RESET

In order to avoid undefined states of the NE5751 when the power is switched on, a power on reset is supplied. The reset is active when Pin V_{REF} is held below 0.8V. The reset is off when Pin V_{REF} is above 2.0V. Pin V_{REF} is normally at 2.5V generated by a resistive divider from V_{DD}. Nominal impedance is 20kΩ. In a typical application a capacitor is connected to Pin V_{REF} to improve power supply rejection. The time delay of the network resets the internal registers when power is first applied. The signal paths are off in the reset condition. The NE5751 must be programmed via the I²C bus for normal operation. The Power Down mode is defined only when all register values are zero.

CONTROL REGISTERS

Register Map

The address register is as follows:

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	SA1	0

SA1 is controlled by serial bus address pin.

Signal Path Register

MSB							LSB
T10	T9	T8	T6	VOX_{EN}	T4	T3T5	T2

T2 is the transmission gate between Pin $PREEMP_{IN}$ and the emphasis input.

T3T5 connects the output of the DTMF generator to the emphasis input and connects the output of the XMT LPF to Pin $TXDTMF_{OUT}$.

T4 connects the output of the XMT LPF to Pin $TXLF_{OUT}$.

VOX_{EN} enables the VOX function of NE5750.

T6 connects Pin VC_{IN} to the volume control.

T8 connects the output of the DTMF generator to the volume control.

T9 enables VC_{OUT1}.

T10 enables VC_{OUT2}.

Volume Control and Test Register

MSB							LSB
PDW	T1T7	DEE	PRE	V1	V2	V3	V4

V4 is volume control bit 4. This is the MSB. A zero is 16dB attenuation.

V3 is volume control bit 3. A zero is 8dB attenuation.

V2 is volume control bit 2. A zero is 4dB attenuation.

V1 is volume control bit 1. A zero is 2dB attenuation.

PRE is the bypass for the pre–emphasis.

DEE is the bypass for the de–emphasis.

T1T7 is the bypass for the compressor and expandor.

PDW is the control for power down mode.

This mode is defined only when all register values are reset to zero.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

High Frequency = 1200kHz/6/HD
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

Low Frequency = 1200kHz/12/LD
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading the two DTMF registers before 96ms have elapsed.

Single tones can be obtained by loading 0, 1 or 2 into one of the registers to silence it.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during operation.

Audio processor - filter and control section

NE/SA5751

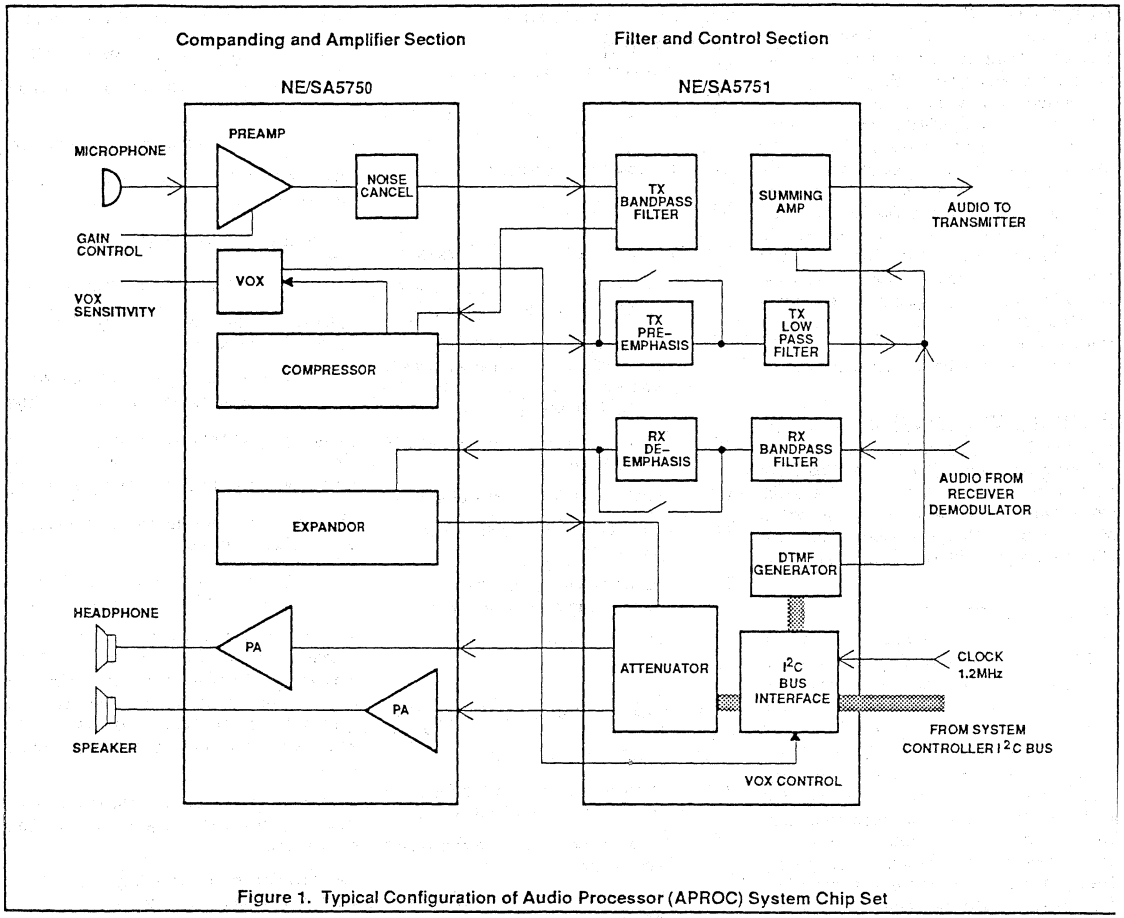


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

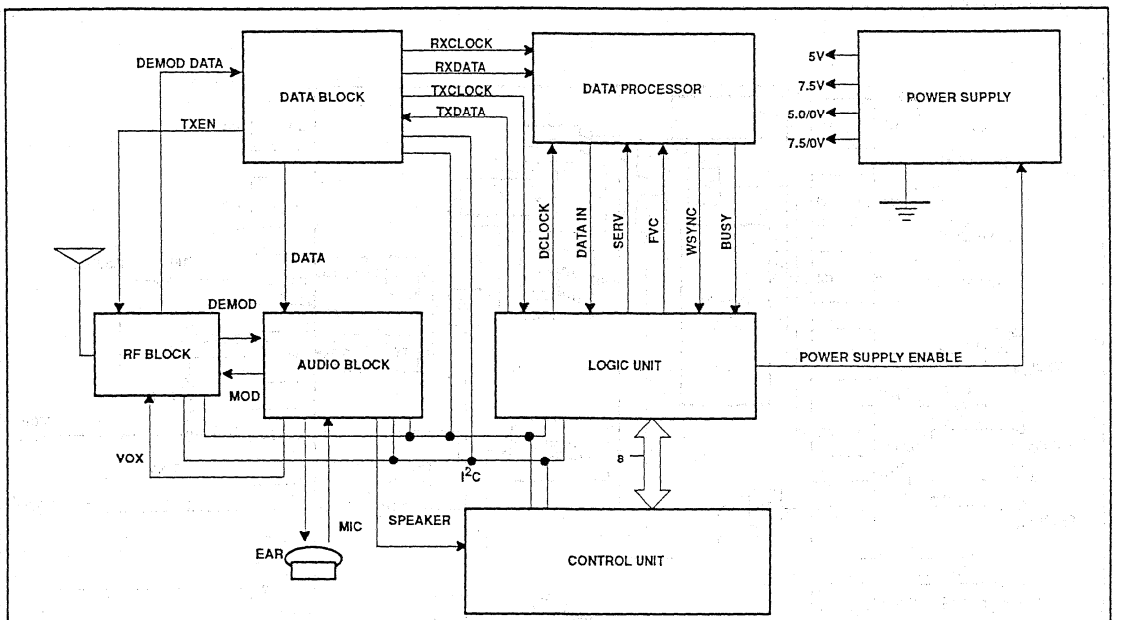


Figure 2. Cellular Radio System

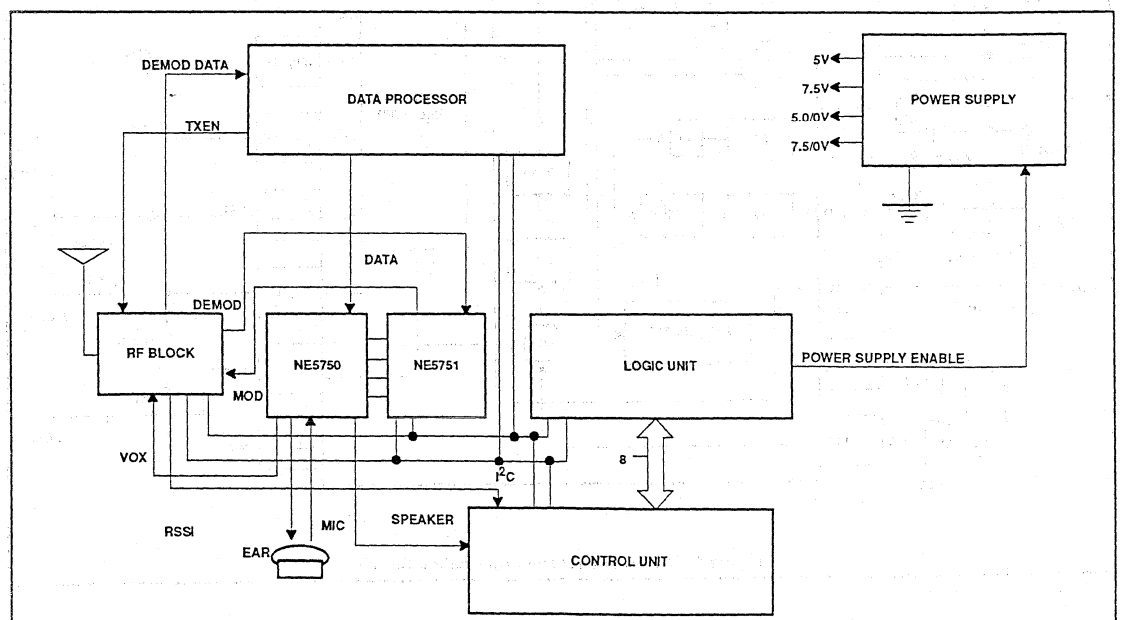


Figure 3. APROC Application Diagram

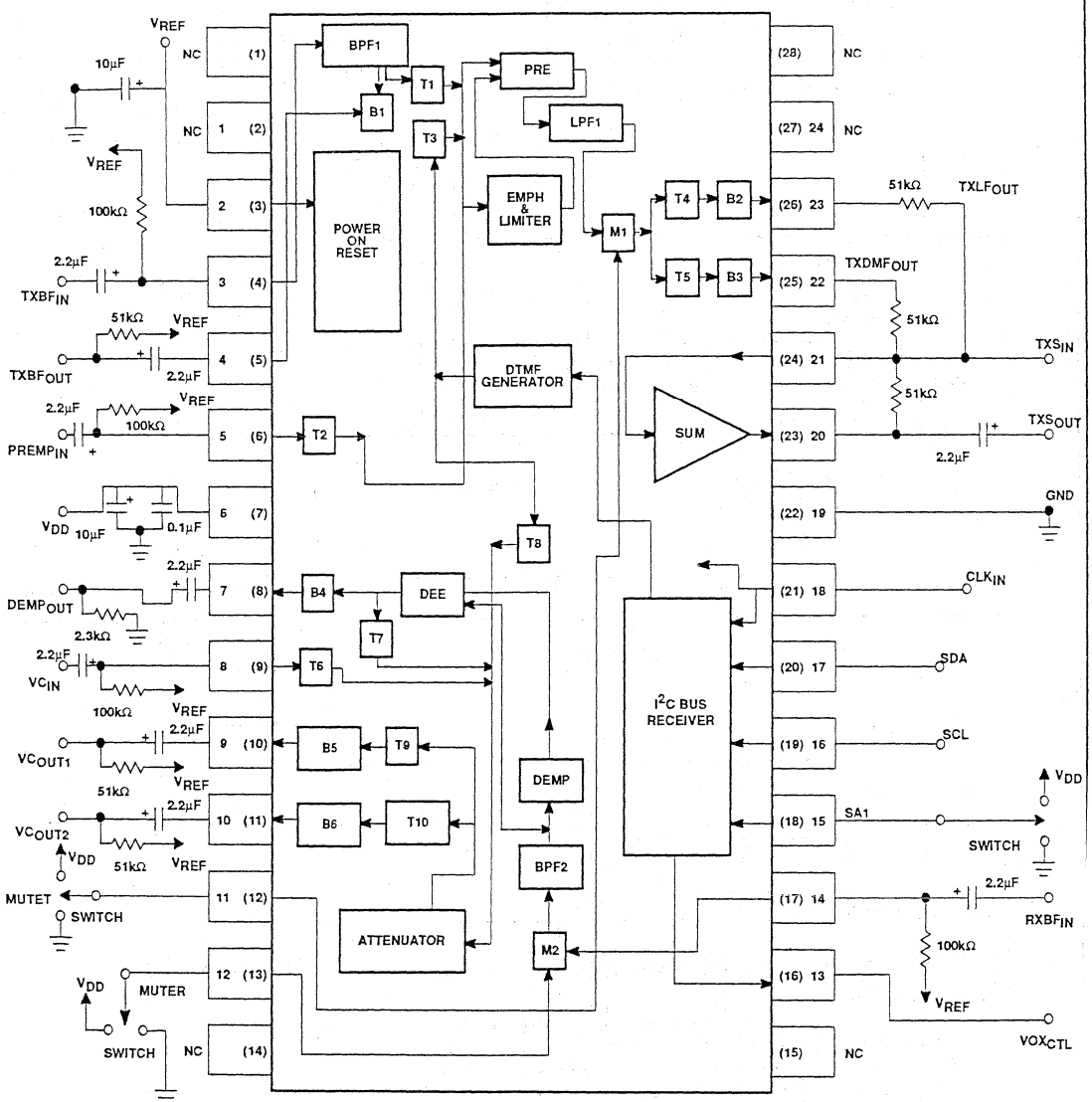
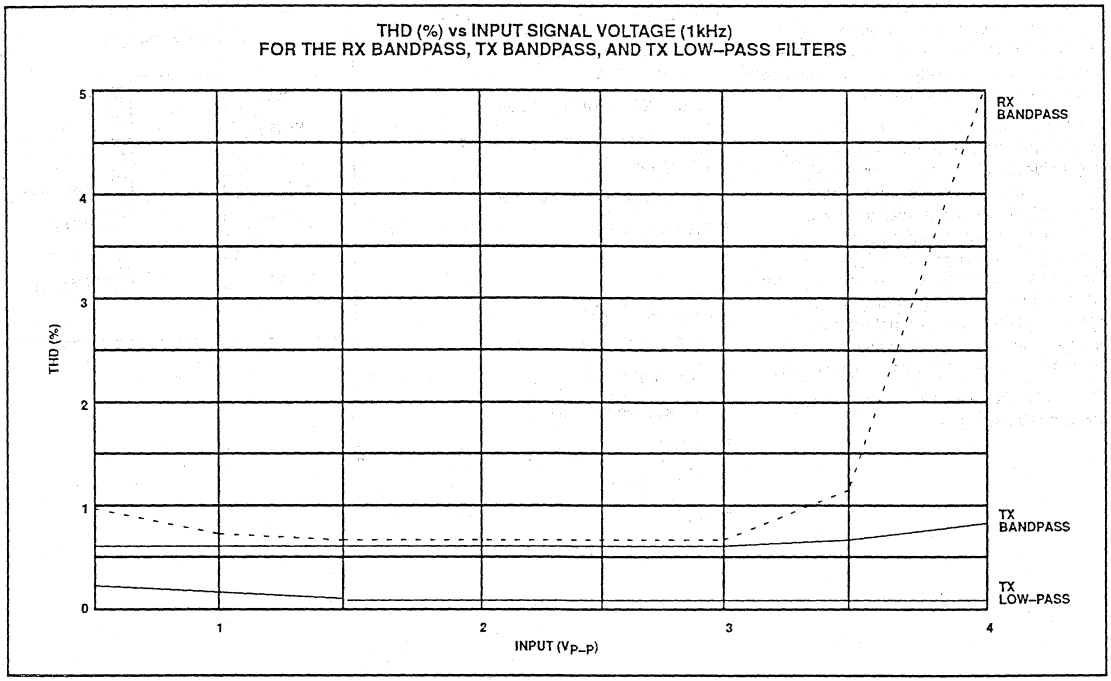


Figure 4. NE/SA5751 Test and Application Circuit

PERFORMANCE CHARACTERISTIC



Low power compandor

NE/SA576

DESCRIPTION

The NE/SA576 is a unity gain level programmable compandor designed for low power applications. The NE576 is internally configured as an expandor and a compressor to minimize external component count.

The NE576 can operate at 1.8V. During normal operations, the NE576 can operate from at least a 2V battery. If the battery voltage drops to 1.8V, this part will still continue to function, however, turning on the part at a V_{CC} of 1.8V requires two external resistors to bring V_{REF} to half V_{CC}. One resistor connects between V_{CC} and V_{REF}; the other connects from V_{REF} to ground. A typical value for these external resistors is approximately 20k. A lower value can be used, but the power consumption will go up.

The NE576 is available in a 14-pin plastic DIP and SO packages.

FEATURES

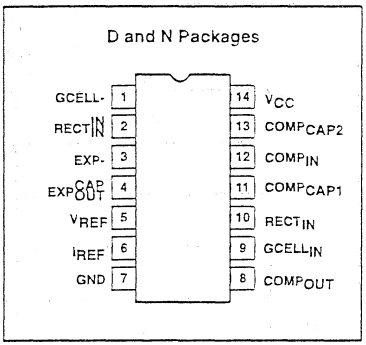
- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- Over 80dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- ESD hardened

APPLICATIONS

- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control

PIN CONFIGURATION

D and N Packages



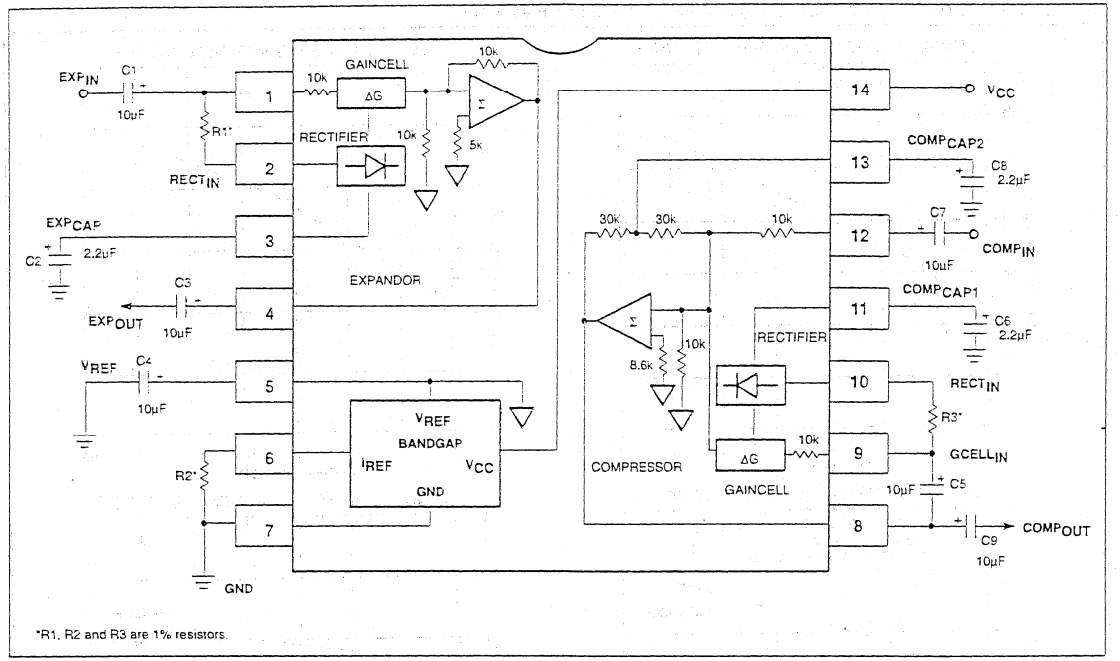
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE576N	0405B
14-Pin Plastic Small Outline (SO)	0 to +70°C	NE576D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA576N	0405B
14-Pin Plastic Small Outline (SO)	–40 to +85°C	SA576D	0175D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING		UNITS
			NE576	SA576	
V_{CC}	Supply voltage		8	8	V
T_A	Operating ambient temperature range		0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range		–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance	DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



*R1, R2 and R3 are 1% resistors.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

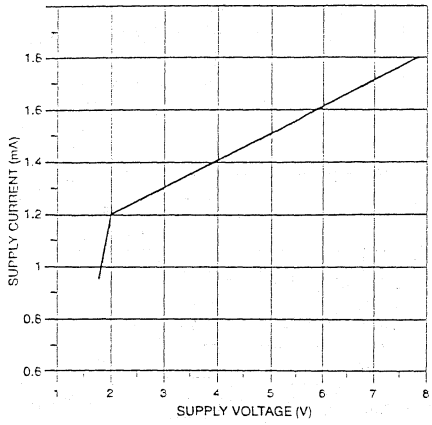
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA576 MIN	LIMITS NE/SA576 TYP	LIMITS NE/SA576 MAX	UNITS
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	3	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V		1.8		V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	30	µV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80		dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		V

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see description on front page of NE576 data sheet.
2. Reference voltage, V_{REF} is typically at 1/2 V_{CC}.

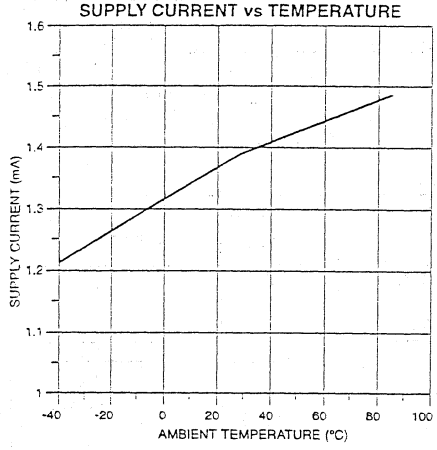
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

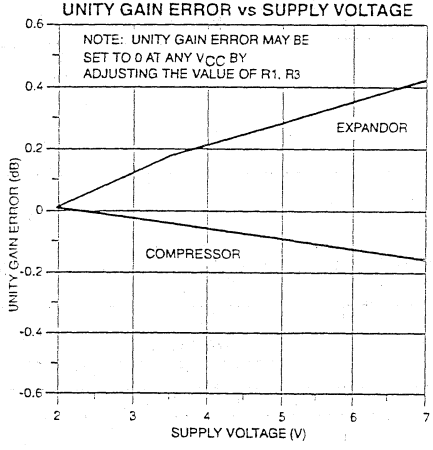
SUPPLY CURRENT vs SUPPLY VOLTAGE



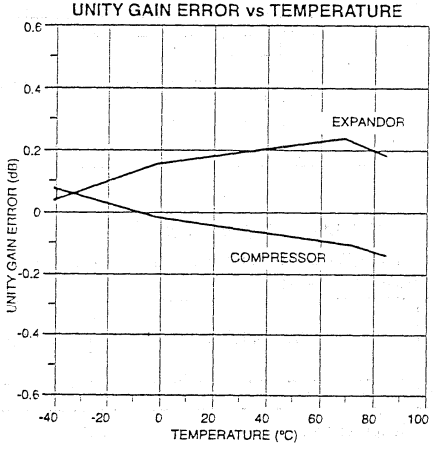
SUPPLY CURRENT vs TEMPERATURE



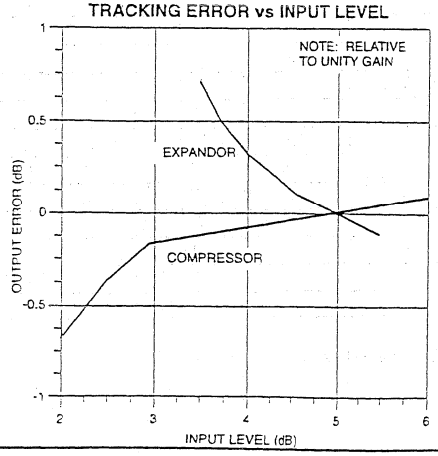
UNITY GAIN ERROR vs SUPPLY VOLTAGE



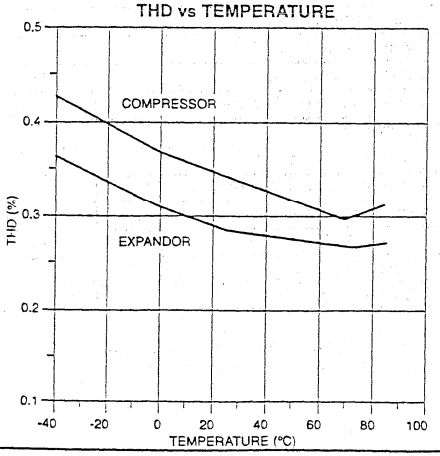
UNITY GAIN ERROR vs TEMPERATURE



TRACKING ERROR vs INPUT LEVEL



THD vs TEMPERATURE



Unity gain level programmable low power compandor

NE/SA577

DESCRIPTION

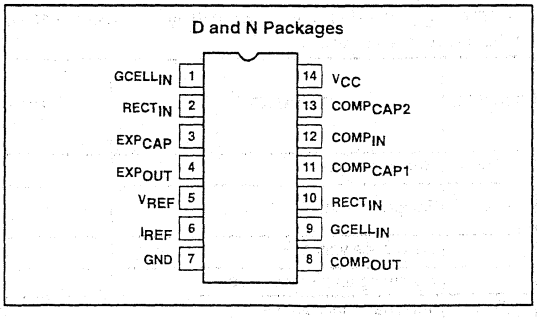
The NE/SA577 is a unity gain level programmable compandor designed for low power applications. The NE577 is internally configured as an expandor and a compressor to minimize external component count.

The NE577 is available in a 14-pin plastic DIP and SO packages.

FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable ($10mV_{RMS}$ to $1.0V_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- SA577 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION



APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE577N	0405B
14-Pin Plastic Small Outline (SO)	0 to +70°C	NE577D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA577N	0405B
14-Pin Plastic Small Outline (SO)	–40 to +85°C	SA577D	0175D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE577	SA577	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

Unity gain level programmable low power compandor

NE/SA577

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

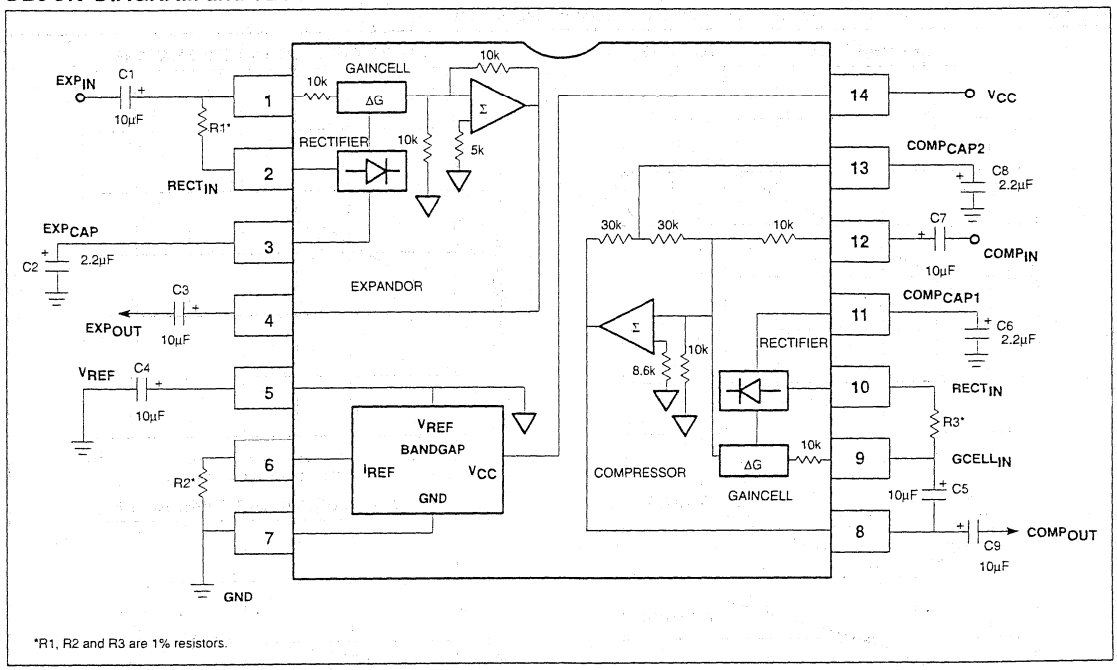
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA577			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	2	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	25	μV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10μF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see application note AN1762.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

Unity gain level programmable low power compandor

NE/SA577

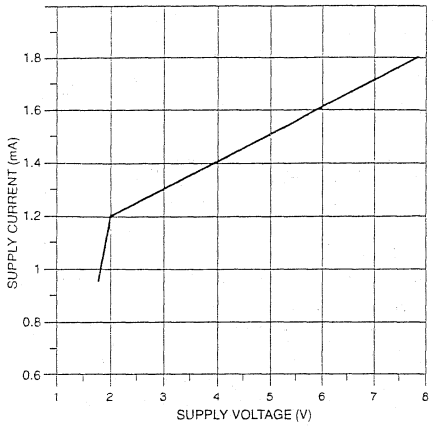
BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



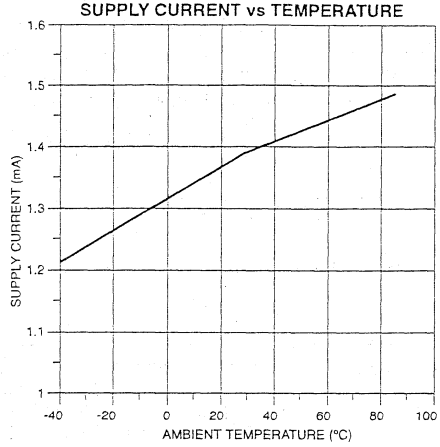
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

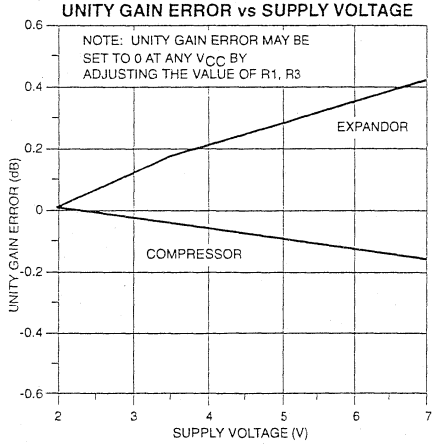
SUPPLY CURRENT vs SUPPLY VOLTAGE



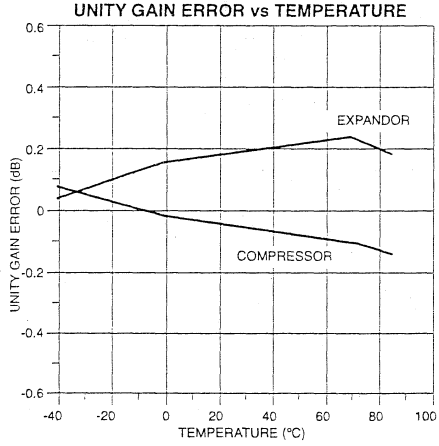
SUPPLY CURRENT vs TEMPERATURE



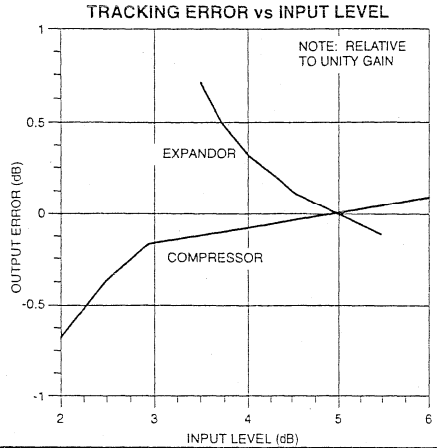
UNITY GAIN ERROR vs SUPPLY VOLTAGE



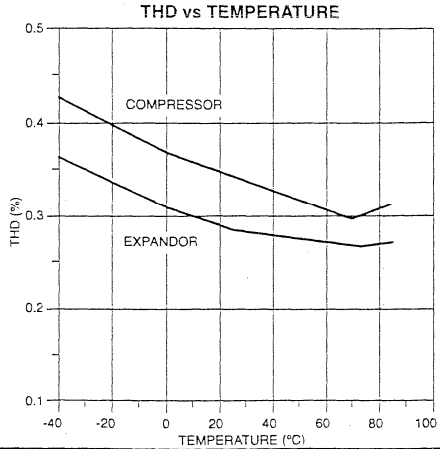
UNITY GAIN ERROR vs TEMPERATURE



TRACKING ERROR vs INPUT LEVEL



THD vs TEMPERATURE



Unity gain level programmable low power compandor

NE/SA578

DESCRIPTION

The NE/SA578 is a unity gain level programmable compandor designed for low power applications. The NE578 is internally configured as an expandor and a compressor to minimize external component count.

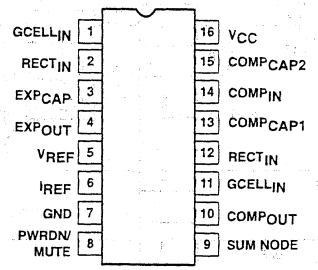
The summing amplifiers of the NE578 have 600Ω drive capability and the inverting input of the compressor amplifier is accessible through Pin 9 for summing multiple external signals. Power Down/Mute function is active low and requires an open collector output logic configuration at Pin 8. If Power Down/Mute is not needed, Pin 8 should be left open. When the part is muted, supply current drops to 170mA at 3.6V. The NE578 is available in a 16-pin plastic DIP and SO packages.

FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable ($10mV_{RMS}$ to $1.0V_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability
- Low external component count
- SA578 meets cellular radio specifications
- ESD hardened
- Power Down mode (I_{CC} = 170μA @ 3.6V)
- Mute function
- Multiple external summing capability
- 600Ω drive capability

PIN CONFIGURATION

D and N Packages



APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE578N	0406C
16-Pin Plastic Small Outline (SO)	0 to +70°C	NE578D	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA578N	0406C
16-Pin Plastic Small Outline (SO)	–40 to +85°C	SA578D	0005D

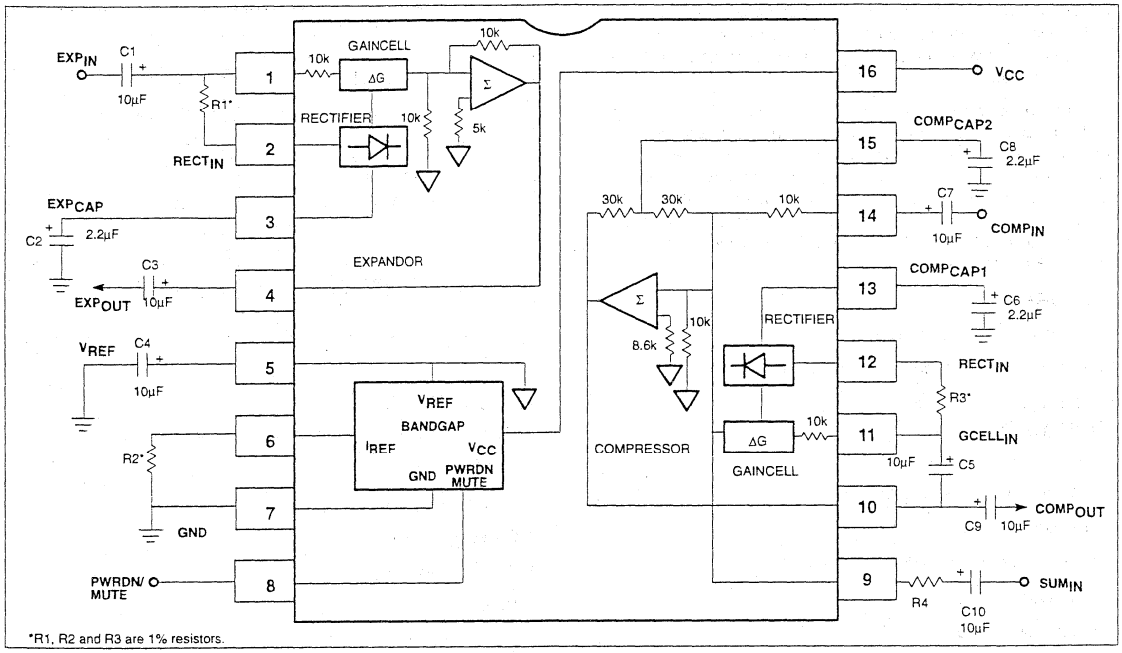
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE578	SA578	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

Unity gain level programmable low power compandor

NE/SA578

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



*R1, R2 and R3 are 1% resistors.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

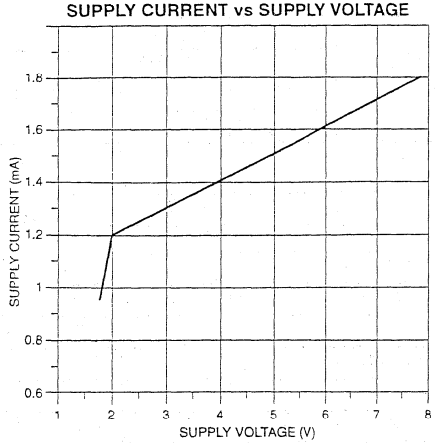
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA578			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current operating power down	No signal, R_2 = 100kΩ		1.4 170	2	mA µA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp minimum output load			600		Ω
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.0	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	20	µV
0dB	Unity gain level	0dB at 1kHz	–1.0	0.18	1.0	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		
	Power Down/Mute low level		0		0.4	V
	Power Down/Mute input current	Pin 8 grounded		–65		µA

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see application note AN1762.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

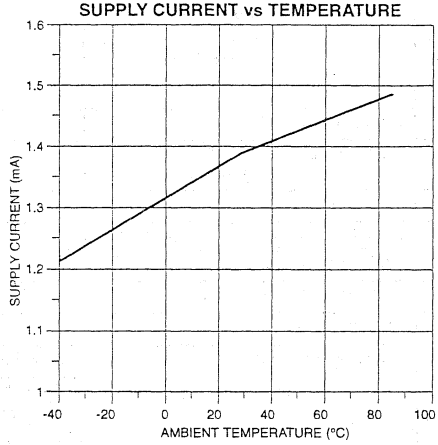
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

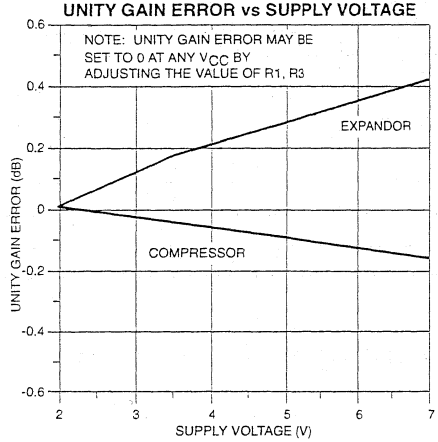
SUPPLY CURRENT vs SUPPLY VOLTAGE



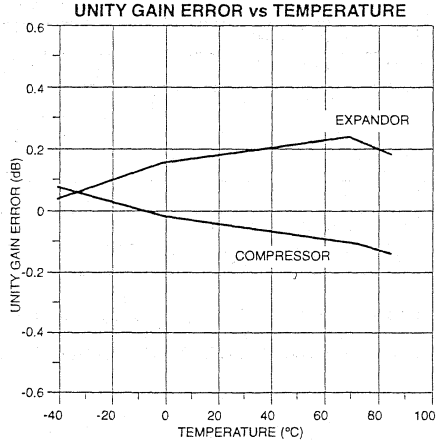
SUPPLY CURRENT vs TEMPERATURE



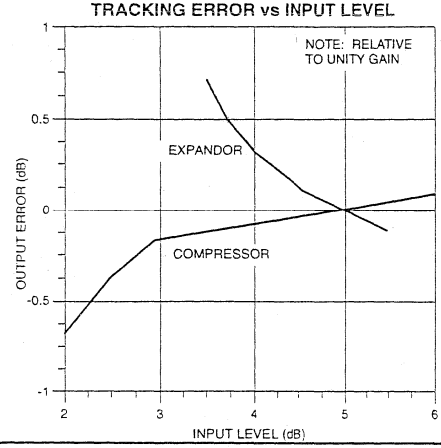
UNITY GAIN ERROR vs SUPPLY VOLTAGE



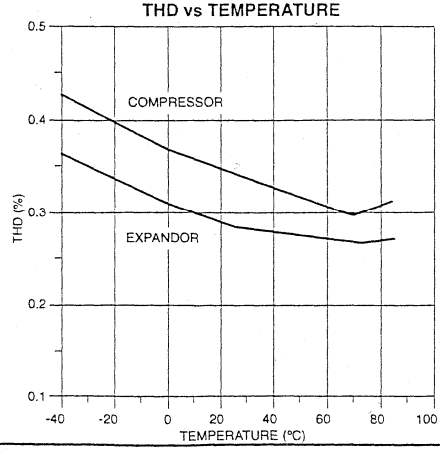
UNITY GAIN ERROR vs TEMPERATURE



TRACKING ERROR vs INPUT LEVEL



THD vs TEMPERATURE

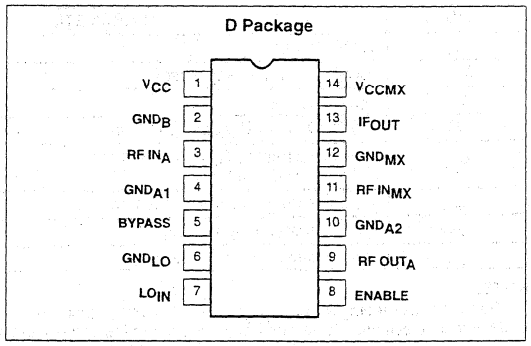


1 GHz LNA and mixer NE/SA600

DESCRIPTION

The NE/SA600 is a combined low noise amplifier (LNA) and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 2dB noise figure at 900MHz with 16dB gain and an IM_3 intercept of -10dBm at the input. Input and output impedances are 50Ω and the gain is stabilized by on-chip compensation to vary less than ±0.5dB over the -40 to +85°C temperature range. The wide-dynamic-range mixer has a 14dB noise figure and IM_3 intercept of +6dBm at the input at 900MHz. Mixer input impedance is 50Ω with an open-collector output. The chip incorporates an option so the LNA can be disabled and replaced by a through connection. The amplifier IM_3 intercept increases to +26dBm in this mode; thus, large signals can be handled. The nominal current drawn from a single 5V supply is 13mA and 4.2mA in the LNA thru mode.

PIN CONFIGURATION



FEATURES

- Low current consumption: 13mA nominal, 4.2mA in the LNA thru mode
- Excellent noise figure: 2dB for the amplifier and 14dB for the mixer at 900MHz
- Excellent gain stability versus temperature
- Switchable overload capability
- Amplifier matched to 50Ω
- Mixer input matched to 50Ω
- Oscillator input matched to 50Ω

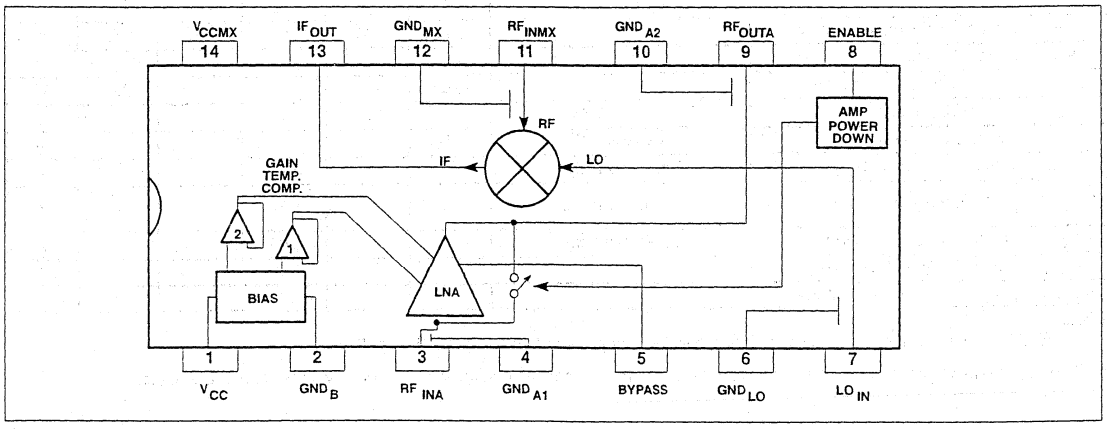
APPLICATIONS

- 900MHz front end for GSM/AMPS/TACS/ hand-held units
- RF data links
- UHF frequency conversion
- Portable radio
- Spread spectrum receivers
- 900MHz cordless phones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to +70°C	NE600D	0175D
14-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA600D	0175D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}, V_{CCMX}	Supply voltage[1]	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC}+0.3)	V
ΔV	V_{CC} to V_{CCMX}	-0.3 to +0.3	V
ΔG	Any GND pin to any other GND pin	-0.3 to +0.3	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 14-Pin Plastic SO	 980	 mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 9V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   14-Pin SO: θ_{JA} = 125°C/W
3. CAUTION: The NE/SA600 is built on a BiCMOS process and is sensitive to electrostatic discharge.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}, V_{CCMX}	Supply voltage	4.5 to 5.5	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS[1,2]

V_{CC} = V_{CCMX} = +5V, T_A = 25°C; Test Figure 1, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
I_{CC}	Supply current (Pin 1, 13, 14)	Enable input high	10	11	13.0	15	16	mA
		Enable input low	3.2	3.6	4.2	4.8	5.2	
V_T	Enable logic threshold voltage		1.12	1.17	1.27	1.37	1.42	V
V_{IH}	Logic 1 level: LNA gain mode		2.0				V_{CC}	V
V_{IL}	Logic 0 level: LNA thru mode		–0.3				0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1		0		1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1		0		1	µA
V_{LNA-IN}	LNA input bias voltage	Enable input high			0.78			V
$V_{LNA-OUT}$	LNA output bias voltage	Enable input high			1.27			V
V_{BY}	LNA bypass bias voltage	Enable input high			1.05			V
V_{MX-IN}	Mixer RF input bias voltage				1.43			V
V_{LO-IN}	Mixer LO input bias voltage				3.35			V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the NE/SA600.
2. Standard deviations are estimated from design simulations to represent manufacturing variations over the life of the product.

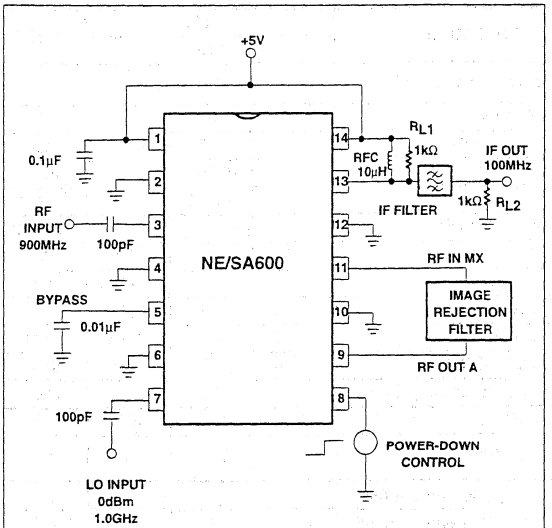
AC ELECTRICAL CHARACTERISTICS[1,2]

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNITS
				−3σ	TYP	+3σ	
LNA (V_{CC} = V_{CCMX} = +5V, T_A = 25°C; Enable = Hi, Test Figure 1, unless otherwise stated.)							
S_{21}	Amplifier gain	900MHz		14.9	16	17.1	dB
S_{21}	Amplifier gain in thru mode	Enable = LO, 900MHz		−9.0	-7.5	−6.0	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled	900MHz			-0.008		dB/°C
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity in thru mode	Enable = LO, 900MHz			-0.014		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz			-0.014		dB/MHz
S_{12}	Amplifier reverse isolation	900MHz		−47	-42	−37	dB
S_{11}	Amplifier input match[3]	900MHz		−11	-10	−9	dB
S_{22}	Amplifier output match	900MHz		−16.8	-15	−13.2	dB
P_{-1dB}	Amplifier input 1dB gain compression	900MHz		−21.2	-20	−18.8	dBm
IP_3	Amp input 3rd-order intercept	Test Fig. 2, 900MHz		−11.6	-10	−8.6	dBm
	Amp input 3rd-order intercept (thru mode)	Test Fig. 2, 900MHz, Enable = LO			+26		dBm
NF	Amplifier noise figure	900MHz		1.9	2.2	2.5	dB
	Amp noise figure w/shunt 15nH inductor at input	900MHz		1.7	2.0	2.3	dB
t_{ON}	Amplifier turn-on time	Enable Lo Hi	Coupling = 100pF		30		µs
			Coupling = 0.01µF		3		ms
t_{OFF}	Amplifier turn-off time	Enable Hi Lo	Coupling = 100pF		10		µs
			Coupling = 0.01µF		1		ms
Mixer (V_{CC} = V_{CCMX} = +5V, T_A = 25°C, Enable = Hi, f_{LO} = 1GHz @ 0dBm, f_{RF} = 900MHz, f_{IF} = 100MHz, Test Fig. 1, unless otherwise stated)							
VG_C	Mixer voltage conversion gain	R_{L1} = R_{L2} = 1kΩ		9.5	10.4	11.3	dB
PG_C	Mixer power conversion gain	R_{L1} = R_{L2} = 1kΩ		−3.05	−2.6	−2.15	dB
S_{11RF}	Mixer input match	900MHz		−23	-20	−17	dB
NF_M	Mixer SSB noise figure	Test Fig. 3, 900MHz, f_{IF} = 80MHz		12.2	14	15.8	dB
P_{-1dB}	Mixer input 1dB gain compression	900MHz		−5.3	-4	−2.7	dBm
IP_{3INT}	Mixer input third order intercept	900MHz		+5	+6	+7	dBm
IP_{2INT}	Mixer input second order intercept	900MHz		+18	+20	+22	dBm
G_{RFM-IF}	Mixer RF feedthrough	900MHz, C_{IF} = 3pF			−7		dB
G_{LO-IF}	Mixer LO feedthrough	900MHz, C_{IF} = 3pF			-10		dB
G_{LO-RFM}	Local oscillator to mixer input feedthrough	900MHz			-33		dB
S_{11LO}	LO input match	900MHz		−24	−20	−16	dB
G_{LO-RF}	Local oscillator to RF input feedthrough	900MHz			-46		dB
$G_{RFO-RFM}$	Filter feedthrough	900MHz			-39		dB
LNA + Mixer (V_{CC}=V_{CCMX}=+5V, T_A=25°C, Enable=Hi, f_{LO}=1GHz @ 0dBm, f_{RF} = 900MHz, f_{IF} = 100MHz, Test Fig. 1, unless otherwise stated)							
PG_C	Overall power conversion gain				13.4		dB
NF	Overall noise figure				3.5		dB
IP_3	Overall input 3rd-order intercept				−13		dBm

NOTE:

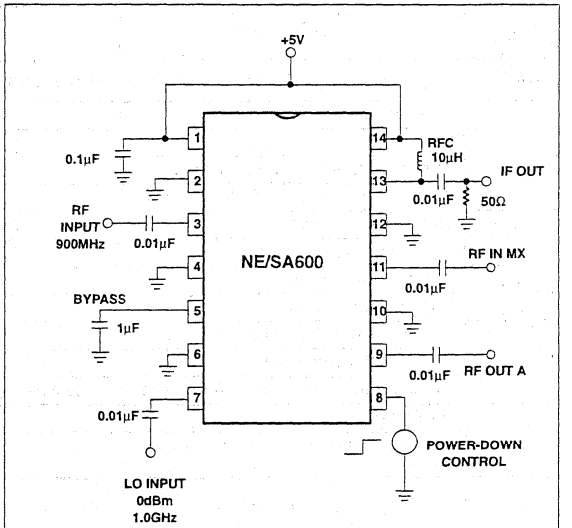
1. All measurements include the effects of the NE/SA600 Evaluation Board (see Figure) unless otherwise noted. Measurement system impedance is 50Ω.
2. Standard deviations are estimated from design simulations to represent manufacturing variations over the life of the product.
3. With a shunt 15nH inductor at the input of the LNA, the value of S_{11} is typically −15dB.

TYPICAL APPLICATION

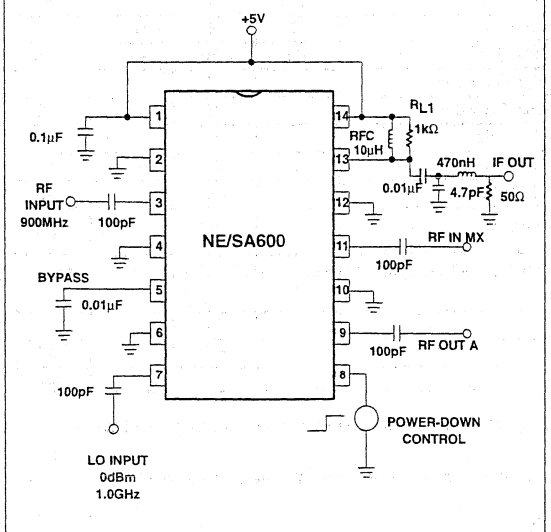


NOTES:
RATIO OF BYPASS TO SIGNAL COUPLING CAPS FOR LNA SHOULD BE 100:1 OR GREATER.
IF FILTER SHOULD BE AC COUPLED.

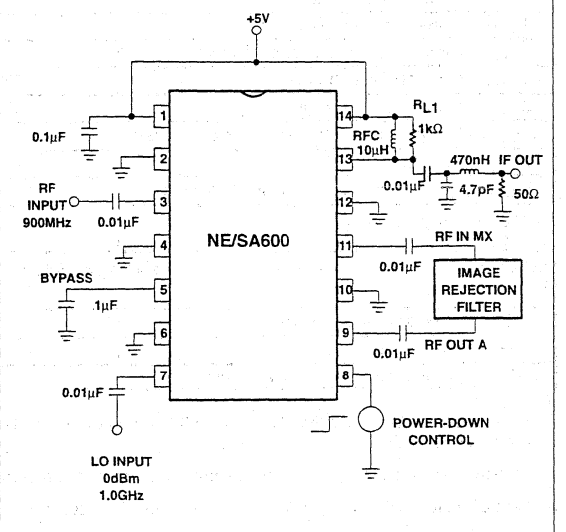
TEST FIGURE 1



TEST FIGURE 2



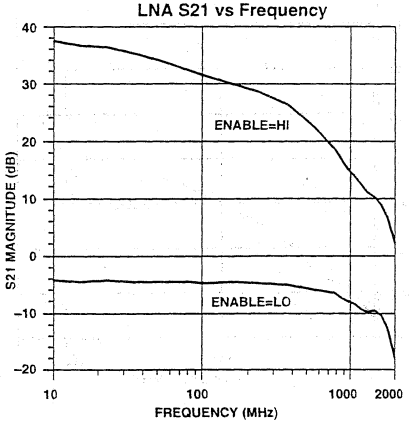
TEST FIGURE 3



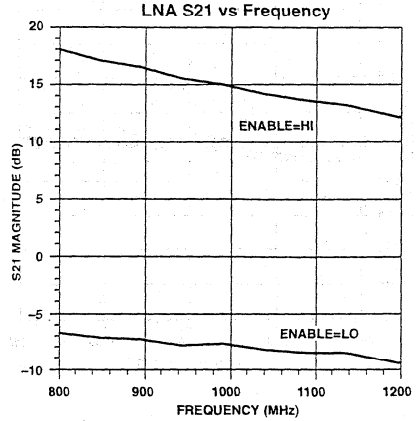
NOTE: All performance curves include the effects of the NE/SA600 evaluation board.

LNA S21 CHARACTERISTICS $4.5V \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Figure 1, unless otherwise specified.

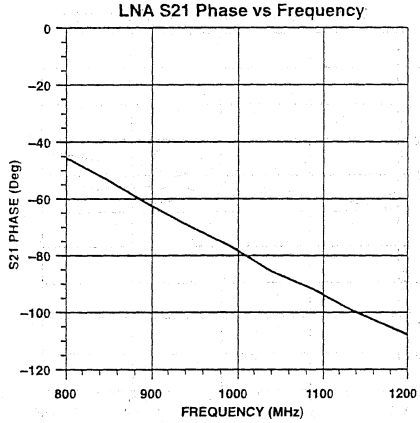
LNA S21 vs Frequency



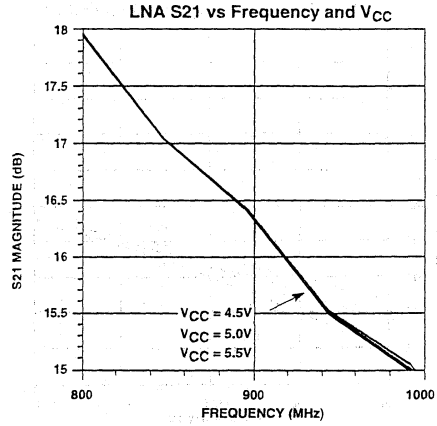
LNA S21 vs Frequency



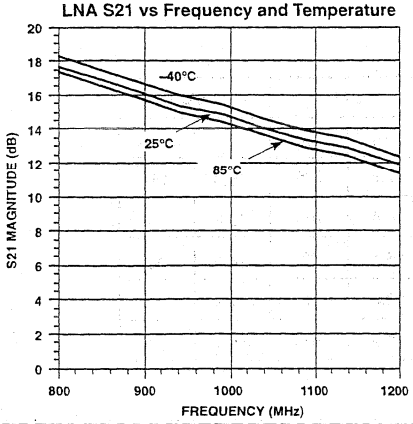
LNA S21 Phase vs Frequency



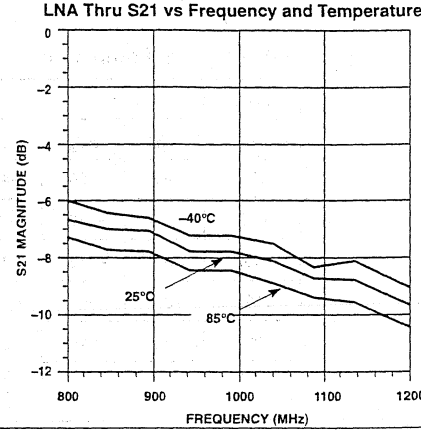
LNA S21 vs Frequency and V_{CC}



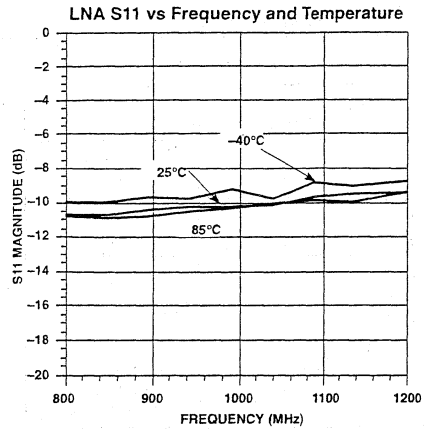
LNA S21 vs Frequency and Temperature

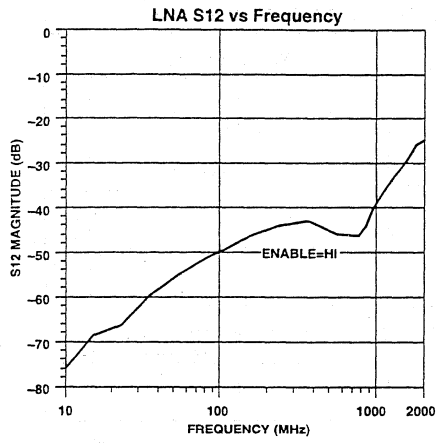


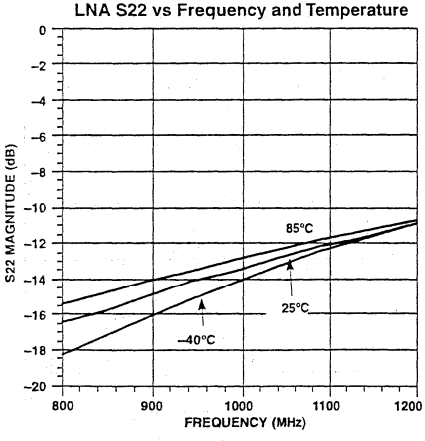
LNA Thru S21 vs Frequency and Temperature



LNA S11/S12/S22 CHARACTERISTICS $4.5V \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Figure 1, unless otherwise specified.







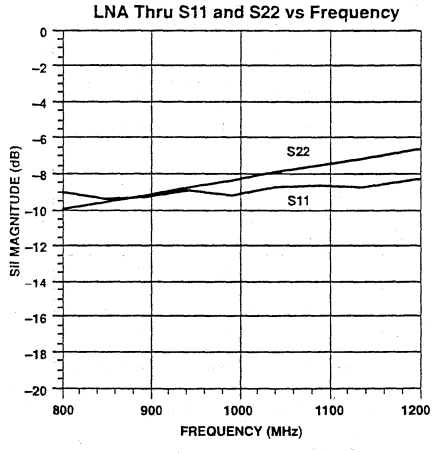


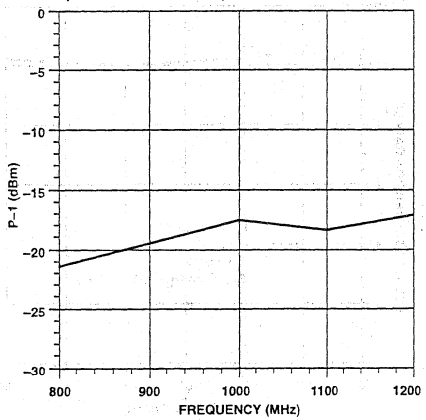
Table 1. S-Parameters

Freq	S11		S12		S21		S22	
MHz	dB	deg.	dB	deg.	dB	deg.	dB	deg.
800	–9.5	–160	–46	8	17.9	125	–18.0	151
900	–9.5	–172	–43	19	16.4	105	–15.8	122
1000	–9.4	–173	–40	17	15.1	88	–14.0	98
1100	–9.1	–200	–37	12	13.8	70	–12.4	77
1200	–8.9	–216	–35	1	12.9	55	–11.1	58

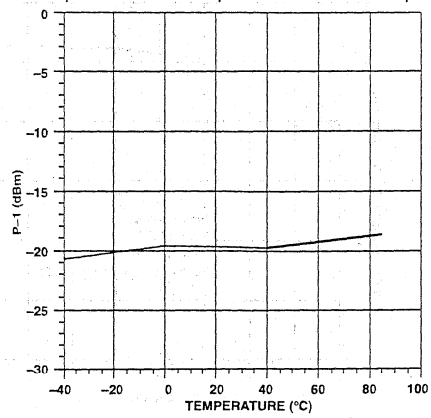
LNA OVERLOAD/NOISE/DISTORTION CHARACTERISTICS

4.5V ≤ V_{CC} = V_{CCMX} ≤ 5.5V, Test Fig. 1, unless otherwise specified.

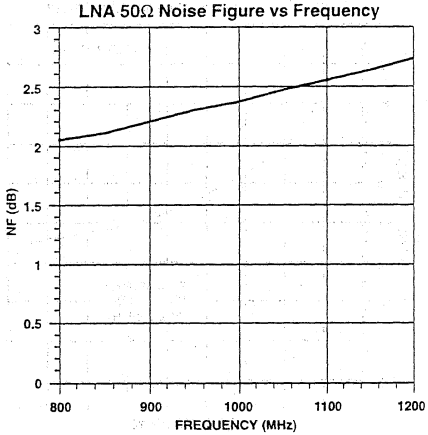
LNA Input 1dB Gain Compression Point vs Frequency



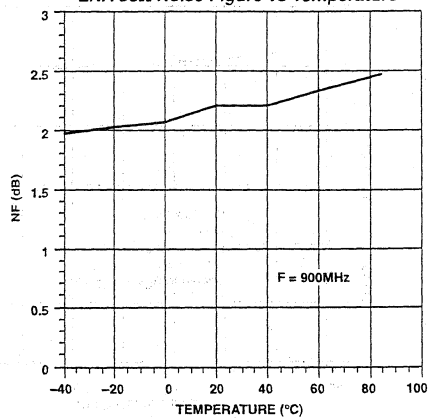
LNA Input 1dB Gain Compression Point vs Temperature



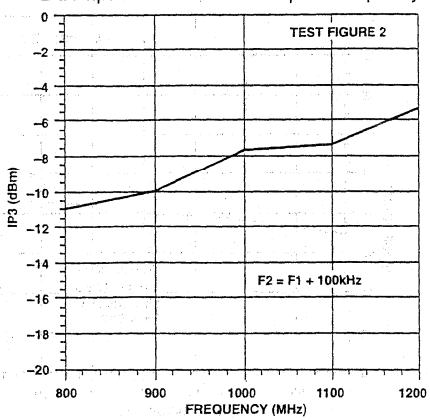
LNA 50Ω Noise Figure vs Frequency



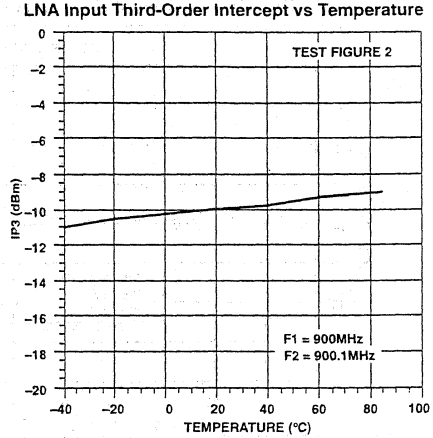
LNA 50Ω Noise Figure vs Temperature



LNA Input Third-Order Intercept vs Frequency

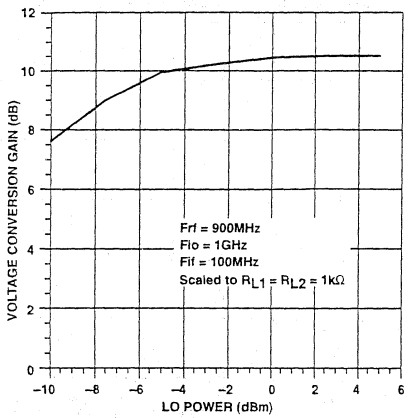


LNA Input Third-Order Intercept vs Temperature

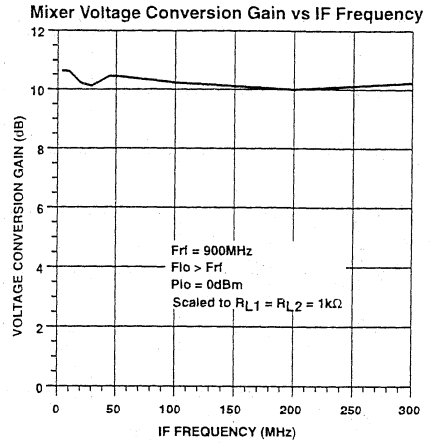


MIXER GAIN/NOISE CHARACTERISTICS $4.5V \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Figure 1, unless otherwise specified.

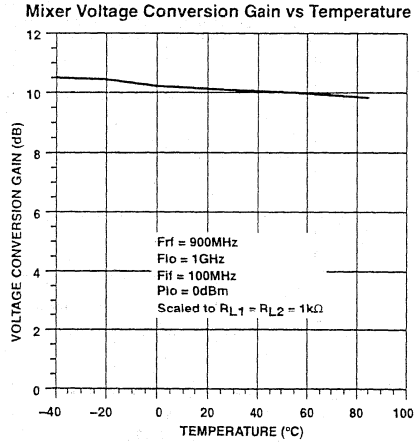
Mixer Voltage Conversion Gain vs LO Power



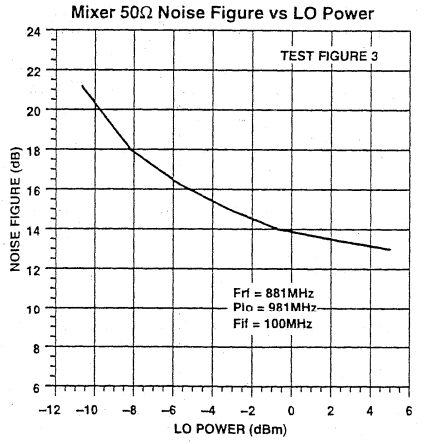
Mixer Voltage Conversion Gain vs IF Frequency



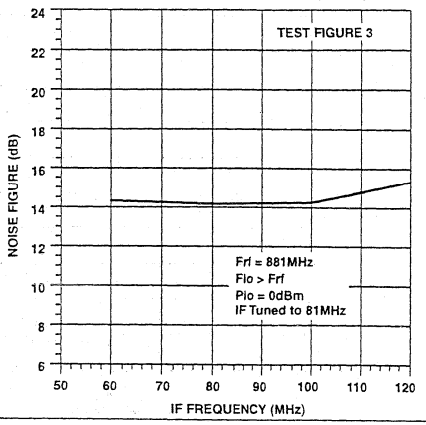
Mixer Voltage Conversion Gain vs Temperature



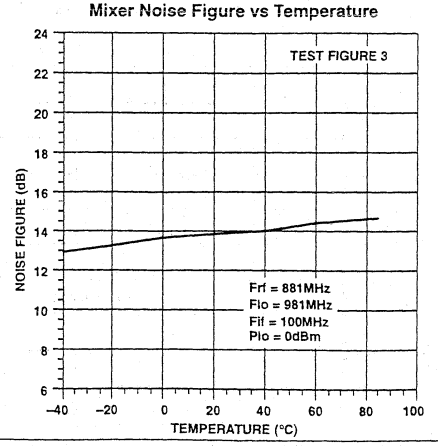
Mixer 50Ω Noise Figure vs LO Power



Mixer Noise Figure vs IF Frequency

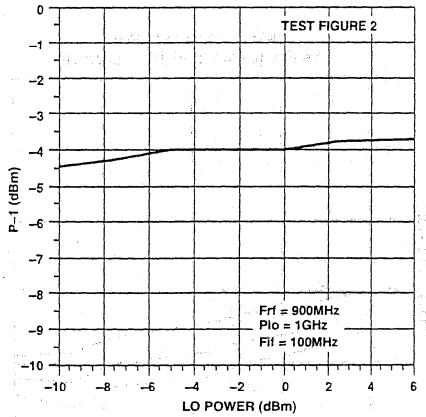


Mixer Noise Figure vs Temperature

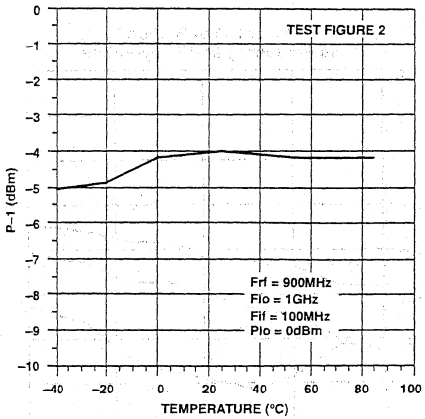


MIXER OVERLOAD/DISTORTION CHARACTERISTICS $4.5 \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Fig. 1, unless otherwise specified

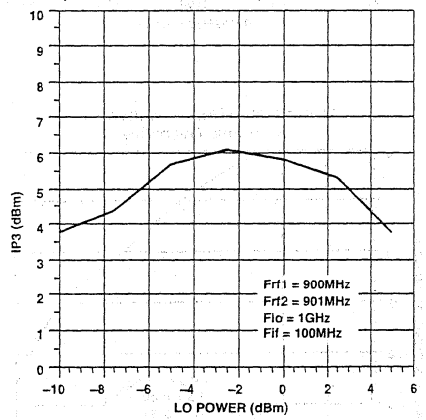
Mixer Input 1dB Gain Compression Point vs LO Power



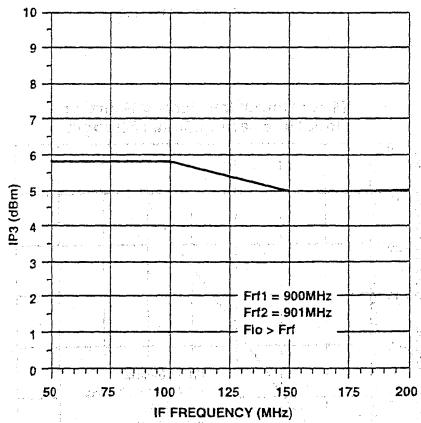
Mixer Input 1dB Gain Compression Point vs Temperature



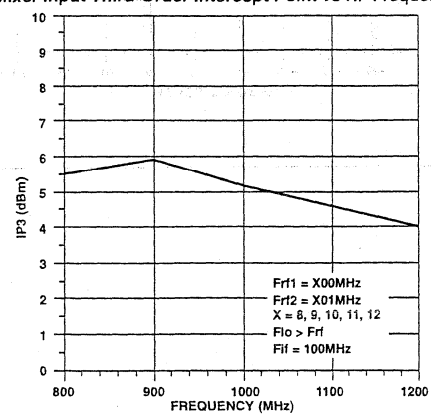
Mixer Input Third-Order Intercept Point vs LO Power



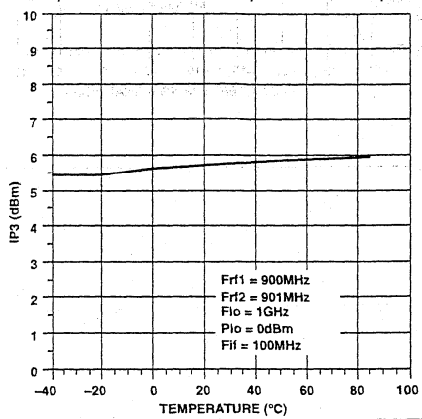
Mixer Input Third-Order Intercept Point vs IF Frequency



Mixer Input Third-Order Intercept Point vs RF Frequency



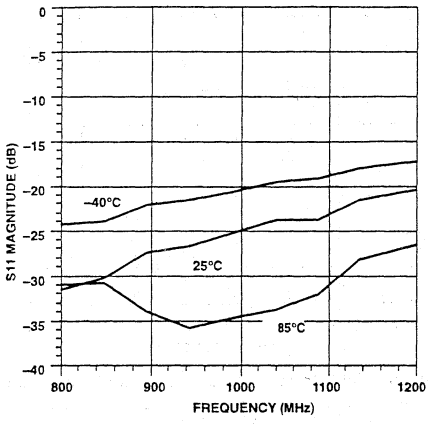
Mixer Input Third-Order Intercept Point vs Temperature



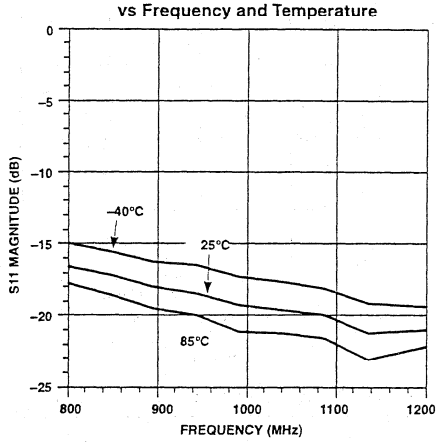
MIXER S11/ISOLATION/INTERFERENCE CHARACTERISTICS

4.5 ≤ V_{CC} = V_{CCMX} ≤ 5.5V, Test Fig. 1, unless otherwise specified

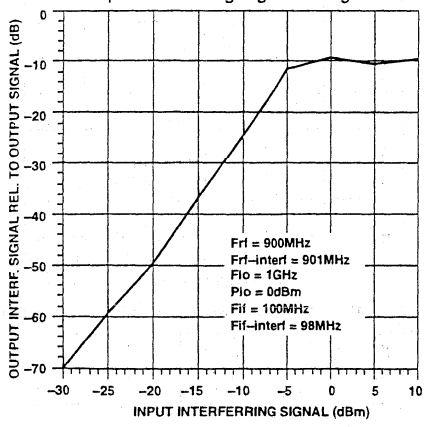
Mixer S11 at RF Port
vs Frequency and Temperature



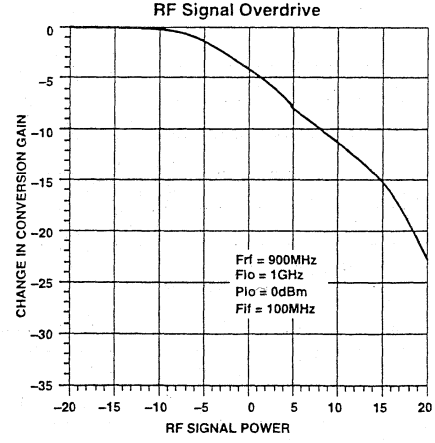
Mixer S11 at LO Port
vs Frequency and Temperature



Mixer Output Interferring Signal vs
Input Interferring Signal Strength

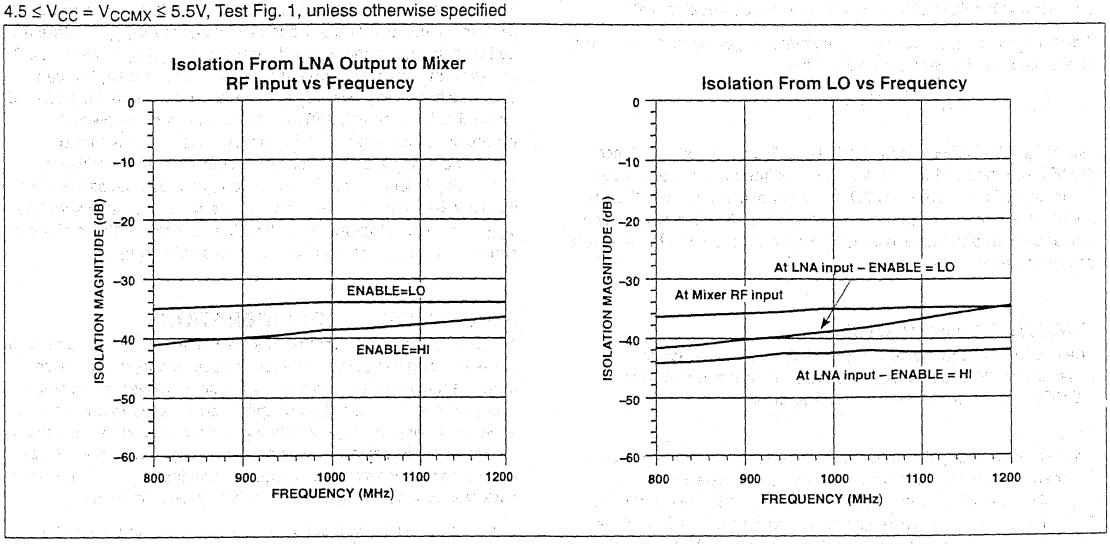


Conversion Gain Variation vs
RF Signal Overdrive



OVERALL PERFORMANCE: ISOLATION CHARACTERISTICS

4.5 ≤ V_{CC} = V_{CCMX} ≤ 5.5V, Test Fig. 1, unless otherwise specified



SPECIFICATIONS

The goal of the Specifications section of the datasheet is to provide information on the NE/SA600 in such a way that the designer can estimate statistical variations, and can reproduce the measurements. To this end the high frequency measurements are specified with a particular PC board layout. Variations in board layout will cause parameter variations (sensitive parameters are discussed in the sections on the LNA and mixer below). For many RF parameters the ±3 sigma limits are specified. Statistically only 0.26% of the units will be outside these limits.

The LNA + mixer conversion gain is measured with an incident 900MHz signal and a 83MHZ SAW filter at the IF output. This measurement along with a gain measurement of the LNA ensure the correct operation of the chip and also allows a calculation of mixer conversion gain.

PIN DESCRIPTIONS AND OPERATIONAL LIMITS

RF_{INA}
Input of LNA, AC coupling required, DC = 0.78V, frequency range from DC to 2GHz, gain at low frequencies is 40dB — so be careful of overload, impedance below 50Ω, shunt 15-18nH inductor helps input match and noise figure.

RF_{OUTA}
Output of LNA, AC coupling required, DC = 1.27V, frequency range from DC to 2GHz, impedance above 50Ω.

BYPASS
Bypass capacitor should be 100 times larger than the largest signal coupling capacitor for the LNA, DC = 1.05V.

RF_{INMX}
Mixer RF port, AC coupling required, DC = 1.43V, frequency range from 100MHz to 2.5GHz, impedance close to 50Ω resistive.

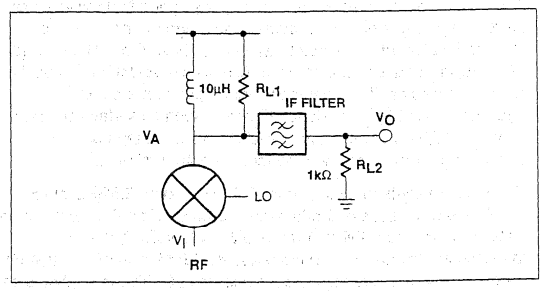
LO_{IN}
Mixer LO port, AC coupling required, DC=3.35V, frequency range from 100MHz to 2.5GHz, impedance close to 50Ω resistive.

IF_{OUT}
Mixer IF port, open-collector output with 1.6mA DC, frequency range DC to 1GHz, impedance approximately 1pF capacitive.

Enable
TTL/CMOS compatible input. Bias current approximately zero.

CONVERSION GAIN DEFINITIONS

Referring to the figure above, we define the ratio of V_A (at the IF frequency) to V_I (at the RF frequency) to be the Available Voltage Conversion Gain, or more simply Voltage Conversion Gain,



$$VG_C = 20\log\left(\frac{V_A}{V_I}\right)$$

where V_A and V_I are expressed in similar voltage units (such as peak-to-peak). The voltage output V_A is decreased by the IF Filter

loss (and any other matching required). Typically, VG_C is 10.4dB for the NE/SA600 mixer with the net IF impedance equal to 500Ω.

It is more common to express the conversion gain in terms of power, so we have the Power Conversion Gain,

$$PG_C = 10\log\left(\frac{P_A}{P_I}\right) - 3dB$$

where $P_A = V_A^2 / R_{IF}$ and $P_I = V_I^2 / R_{RF}$. R_{IF} is the net resistance at the IF frequency at the IF port, and R_{RF} is the input impedance at the mixer RF port. With a 500Ω IF impedance and a 50Ω RF input impedance, the conversion gain works out to –2.6dB typically. The power delivered to the load is down 3dB with respect to the available power because of loss in R_{L1}.

THEORY OF OPERATION

The NE/SA600 is fabricated on the Philips Semiconductors advanced QUBiC technology that features 1µm channel length MOSFETs and 13GHz FT bipolar transistors.

LNA

The Low Noise Amplifier (LNA) is a two stage design incorporating feedback to stablize the amplifier. An external bypass capacitor of (typically) 0.01µF is used. The inputs and outputs are matched to 50Ω. The amplifier has two gain states: when the ENABLE pin is taken high, the amplifier draws 9mA of current and has 16dB of gain at 900MHz. When the ENABLE pin is low, the amplifier current goes to zero, and the amplifier is replaced by a thru. Typical loss for the thru is 7dB. This dual-gain state approach can be used in bang-bang control systems to achieve a low gain, high overload front-end as well as the more usual high gain, low overload front-end.

The amplifier has gain to frequencies past 2GHz, but a practical upper end is 1.6-1.7GHz. Both the input match and the noise figure (NF) can be improved with a shunt 15-18nH inductor at the input. Typically, the gain increases 0.4dB, the match improves to 13-16dB, and the noise figure drops to 1.95-2dB. Variations of any of the RF parameters with V_{CC} is negliglible, and variation with temperature is minimal.

Mixer

The mixer is a single-balanced topology designed to draw very low current, typically 4mA, and provide a very high input third-order intermodulation intercept point , typically IP3=+6dBm. The RF and LO ports impedances are nearly 50Ω resistive, and the IF output is an open collector. The open-collector output allows direct interfacing with high impedance IF filters, such as surface acoustic wave (SAW) filters without the need for external step-up transformers (which are needed for 50Ω output mixers).

The basic mixer is functional from DC to well over 2.5GHz, but RF and LO return losses degrade below 100MHz. The IF output can be used from DC to 500MHz or more, although typically the intermediate frequency is in the range 45-120MHz in many 900MHz receivers. To achieve the lowest noise, the LO drive level should be increased as high as possible, consistent with power dissipation limitations.

POWER SUPPLY ISSUES

V_{CC} bypassing is important, but not extremely critical because of the internal supply regulation of the NE/SA600. The Pin 1 V_{CC} supplies the LNA and powers overhead circuitry. Typical current draw is 9.8mA while enable is high (1mA powered down). The Pin 14 V_{CCMX} powers the mixer and typically has 3.2mA of current (assuming an inductor biasing the IFout back to V_{CCMX}). Care must be taken to avoid bringing any IC pin above V_{CC} by more than 0.3V, or below any ground by more than 0.3V. For example, this can occur if the enable pin is fed from a microcontroller that is powered up quicker than the NE/SA600. In this condition the internal electrostatic discharge (ESD) protection network may turn-on, possibly causing a part misfunction. Generally this condition is reversible, so long as the source creating the overstress is current limited to less than 100mA. To avoid the problem, make sure both V_{CC} pins are tied together near the IC, and install a 1kΩ resistor in series with the enable pin if it is likely to go above V_{CC}.

BOARD LAYOUT CONSIDERATIONS

The LNA is sensitive to mutual inductance from the input to ground. Therefore long narrow input traces will degrade the input match. Ideally, a top side ground-plane should be employed to maximize LNA gain and minimize stray coupling (such as LO to antenna). To avoid amplifier peaking, the output and input grounds should not be run together. Attach both grounds to a solid ground plane. A solid ground plane beneath the package will maximize gain. Top side to back side ground through holes are highly recommended.

The mixer is relatively insensitive to grounding. Care should be taken to minimize the capacitance on the RF port (Pin 11) for best noise figure. Also, the capacitance on the IFout pin must be kept small to avoid conversion gain rolloff when using high IF frequencies. The purpose of the inductor from IFout to V_{CC} is to set the midpoint of the IF swing to be V_{CC}. Without this inductor the part is sensitive to output overload under low V_{CC} (V_{CC} = 4.5V) and hot temperature conditions. The V_{CCMX} pin must be kept at the same potential as the V_{CC} pin.

APPLICATIONS INFORMATION

The NE/SA600 is a high performance, wide-band, low power, low noise amplifier (LNA) and mixer circuit integrated in a BiCMOS technology. It is ideally suited for RF receiver front-ends for both analog and digital communications systems.

There are several advantages to using the NE/SA600 as a high frequency front-end block instead of a discrete implementation. First is the simplicity of use. The NE/SA600 does not need any external biasing components. Due to the higher level of integration and small footprint (SO14) package it occupies less space on the printed circuit board and reduces the manufacturing cost of the system. Also the higher level of integration improves the reliability of the LNA and mixer over a discrete implementation with several components.

The LNA thru mode in NE/SA600 helps reduce power consumption in applications where the amplifiers can be disabled due to higher received signal strength (RSSI). Other advantages of this feature are described later in this section.

The mixer is an active mixer with excellent conversion gain at low LO input levels, so LO levels as low as -5dBm to -10dBm can be used depending on the applications requirement for mixer gain, mixer noise figure and mixer third order intercept point. This reduces the LO drive requirements from the VCO buffer, thus reducing its current consumption. Also, due to lower LO levels, the shielding requirements can be minimized or eliminated, resulting in substantial cost savings and weight and space reduction.

And last but not least, is the impedance matching at LNA inputs and outputs and mixer RF and LO input ports. Only those who have toiled through discrete transistor implementations for 50Ω input and output impedance matching can truly appreciate the elegance and simplicity of the NE/SA600 input and output impedance matching to 50Ω. Also, the mixer output impedance is high, so matching to a crystal or SAW IF filter becomes extremely easy without the need for additional IF impedance transformers (tapped-C networks with inductors or baluns).

The NE/SA600 applications and demo board features standard low cost 62mil FR-4 board. A top-side ground plane is used and 50Ω coplanar transmission lines are used. LO and RF_{INA} traces are perpendicular. Provisions for the image reject filter between RF_{OUTA} and RF_{INMX} are provided. A simple LC match for 80MHz IF is used so that 50Ω measurements can be made on the demo board.

The NE/SA600 applications evaluation board schematic is shown in Figure 1. The V_{CC} (Pin 1) and V_{CCMX} (Pin 14) are tied together and the power supply is bypassed with capacitors C5 and C6. These capacitors should be placed as close to the device as practically possible.

C1 is the DC blocking capacitor to the input of the LNA. L1 provides additional input matching to the LNA for an improved return loss (S11). This inductor can be a surface-mount component or can be easily drawn on the printed circuit board (small spiral or serpentine). This additional match improves the gain of the LNA by 0.4dB and lowers the noise figure to 2dB or less. If the typical gain of the LNA of 16dB is acceptable with 2.2dB of noise figure, then L1 can be eliminated. If the LNA input is fed from a duplexer or selectivity filter after the antenna, C1 can also be eliminated since the filter will also provide DC blocking. The LNA bypass capacitor C3 should be at least 100 times C1 or C9 for low frequency stability. Switch S1 toggles the LNA gain/through function. R1 is used only to limit the maximum current into the enable pin and only necessary if enable may power up before the V_{CC}.

C4 is a DC blocking capacitor for the LO input pin and may not be needed in actual applications if the VCO output is isolated and will not upset the internal DC biasing of the mixer. The image reject filter goes between the output of the LNA and the RF input to the mixer. Since the LO input, RF output and mixer input are all 50Ω matched impedances internally, there is no need for any external components. C8 and C9 are DC blocking capacitors to the connectors and will not be needed in an actual application.

R2 and L2 are the load to the mixer output which is typical of the IF crystal or SAW filters. C2 and L3 provide a match from the high impedance mixer output to a 50Ω test set-up (spectrum analyzer, etc.) and C7 is a DC blocking capacitor for the mixer output.

The printed circuit board layout for the schematic of Figure 1 is shown in Figure 3. It is a very simple printed circuit board layout with all the components on a single side. The layout also accomodates a two pole image reject filter between the LNA outupt and mixer input. All the input and output traces to the LNA and mixer should be 50Ω tracks with the exception of mixer output, which can be very narrow due to the higher impedances of the filter.

The NE/SA600 internal supply is very well regulated. This is seen from Figure 4 which shows the I_{CC} vs. V_{CC} for the NE/SA600. Table 1 shows the S11, S21, S22 and S21 for the LNA from 800-1200MHz. Typical measurements at 900MHz for the critical parameters such as gain, noise figure, IP_3, 1dB compression point, etc. as measured on an applications evaluation board are as follows

LNA gain = 16.5dB
LNA through = −7dB
Mixer gain =−3dB (into a 50Ω load)
LNA noise figure = 2dB
Mixer noise figure = 14dB
LNA IP_3 = −10dBm (in gain mode)
LNA IP_3 = +26dBm (in through mode)
LNA 1dB compression point = −20dBm
Mixer 1dB compression point = −4dBm

The shunt inductor L1 for input match is optional. Figure 5 shows the effect of the inductor value from 8.2nH to 15nH on gain, noise figure and input match.

The total power gain for the LNA and mixer (excluding the image reject filter) in a system where the output of the mixer is loaded with 50Ω is about 14dB. In an actual system the output impedance of the mixer is usually much higher than 50Ω (more like 1kΩ or higher) and so it is more important to consider the voltage gain from the input at the LNA to the mixer output. The voltage gain in this case will be about 29.85V/V. The total noise figure for the LNA and mixer combination is be about 3.27dB. The input third order intercept point for the LNA and mixer is about -11dBm. In the LNA through mode, the intercept point for the combination is higher than +19dBm. This LNA through feature provides an additional boost to the total dynamic range of the system.

The NE/SA600 finds applications in many areas of RF communications. It is an ideal down converter block for high performance, low cost, low power RF communications transceivers. The front-end of a typical AMPS/TACS/NMT/TDMA/CDMA cellular phone is shown in Figure 2. This could also be the front-end of a VHF/UHF handheld transceiver, UHF cordless telephone or a spread spectrum system.

The antenna is connected to the duplexer input. The receiver output of the duplexer is connected to the RF input of the LNA. If the additional improvement in noise figure and gain are not needed to meet the system specifications then L1 and C1 can be eliminated. In TDMA systems, the NE/SA600 can be totally powered down by Q1 and the two resistors. In this mode the current consumption will be zero mA. Care should be taken in the software of the system to insure that the enable pin on NE/SA600 tied to the LNA gain control port is held low while the device is in total power down mode. L2 and C2 can be tuned to the IF frequency and to match to the IF filter impedance.

A complete analysis of the front-end shows that the total voltage gain from the antenna input to the mixer output is about 9.5V/V. This value includes a 3.2dB loss for the duplexer and a 1.8dB loss for the bandpass filter. The noise figure as referred to the antenna is 7dB and the input third order intercept point is about -7.5dBm. In LNA through mode the input third order intercept point increases to about +24dBm.

During normal operation of a handheld RF receiver the received signal strength (RSSI) is nominally greater than -100dBm. The signal only drops below this level due to severe multipath fading, shadow effect or when the receiver is at extreme fringes of cell coverage. The LNA through mode can be used here as a two step gain control such that when RSSI is below a certain threshold level (e.g. -90dBm), the LNA has a -7dB loss and the total current consumption of the NE/SA600 is only 4.3mA. The sensitivity of the system will not suffer because the received RF signal is much higher than the noise floor of the system. When the RSSI falls below a certain threshold (e.g. -95dBm) the LNA is enabled to give the full

16.5dB of gain with 2dB of noise figure. In this mode the current consumption is increased to 13mA. But for hand-held equipment, the average current consumption will be closer to 5-6mA. The other advantage of the LNA through mode besides power savings is the input overload characteristics. Due to the much higher input third order intercept point of the LNA (+26dBm), the receiver is immune to strong adjacent channel interference. Implementing this feature with an FM/IF device such as the NE625/7 with fast RSSI response and a window comparator toggling the LNA mode of NE/SA600, a fast two-step AGC with response time less than 10μs can be achieved.

This is a very useful feature to equalize multipath fading effects in a mobile radio system.

In conclusion, the NE/SA600 offers higher level of integration, higher reliability, higher level of performance, ease of use, simpler system design at a cost lower than the discrete multi-transistor implementations. In addition, the NE/SA600 provides unique features to enhance receiver performance which are almost unattainable with discrete implementations.

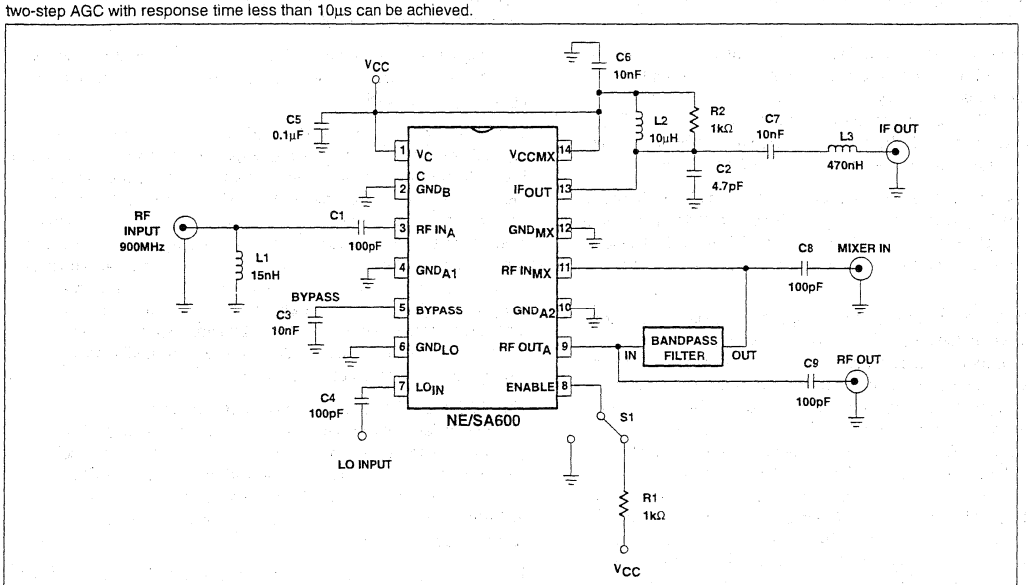


Figure 1.

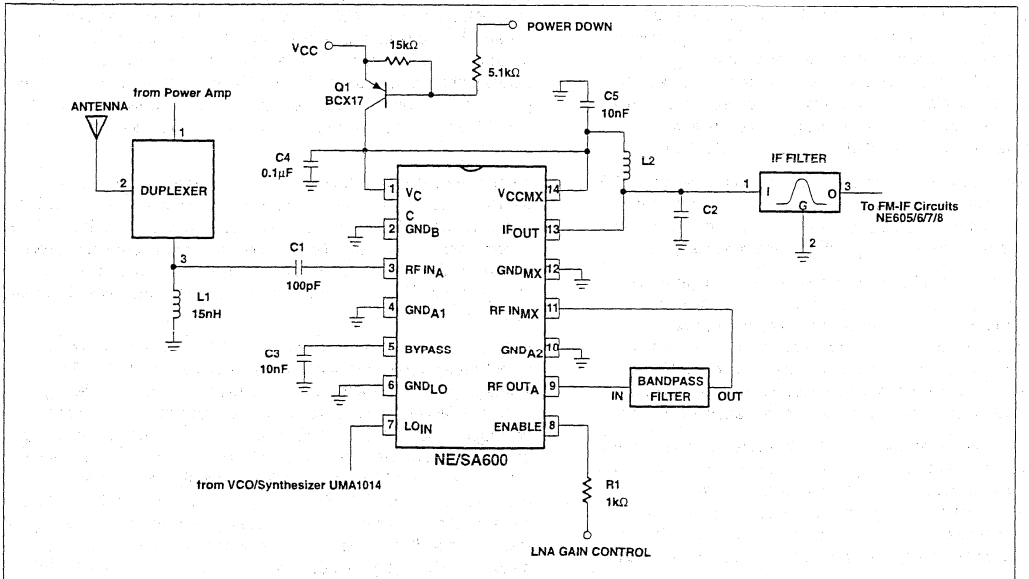
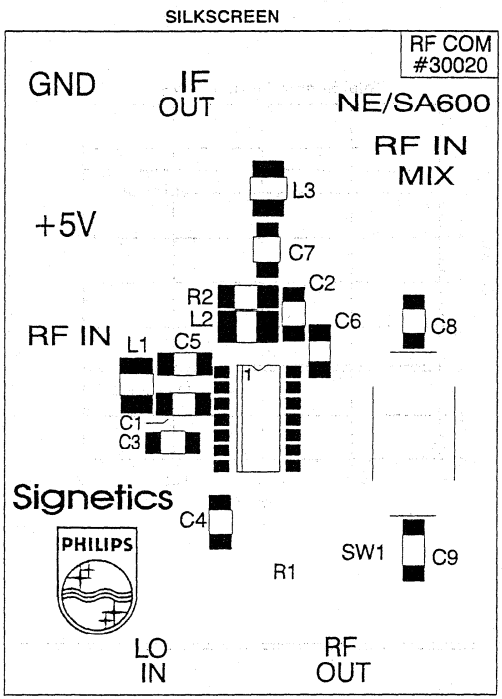
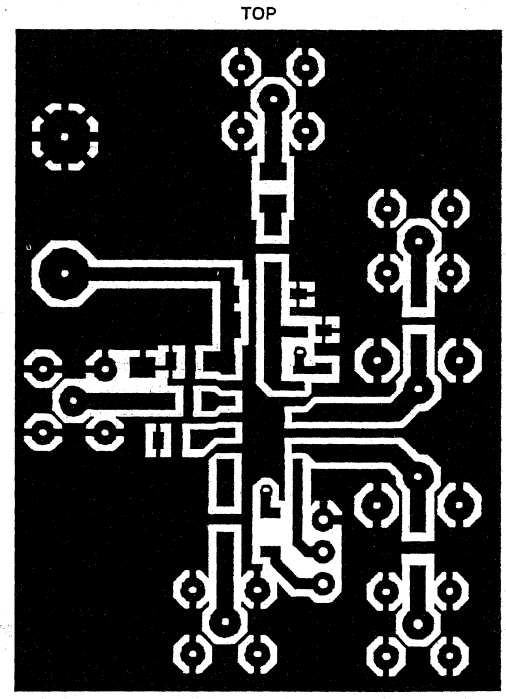


Figure 2.





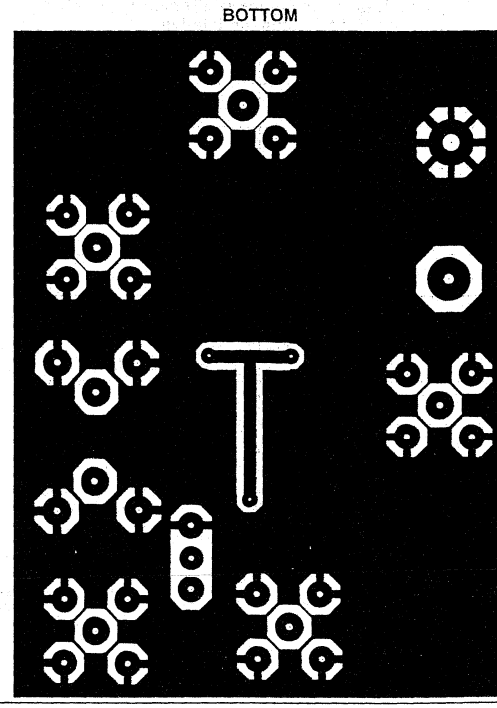
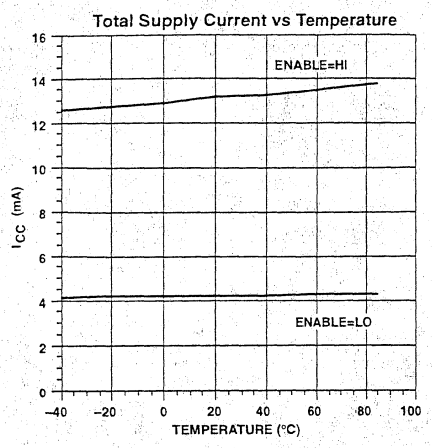


Figure 3. PC Board Layout



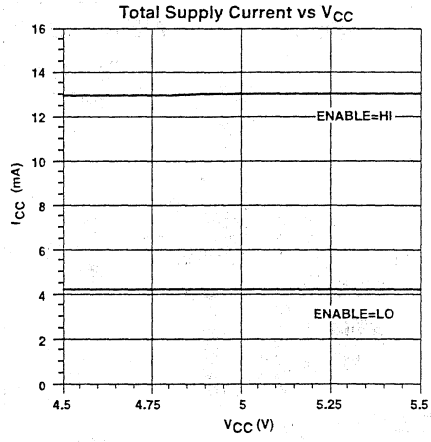
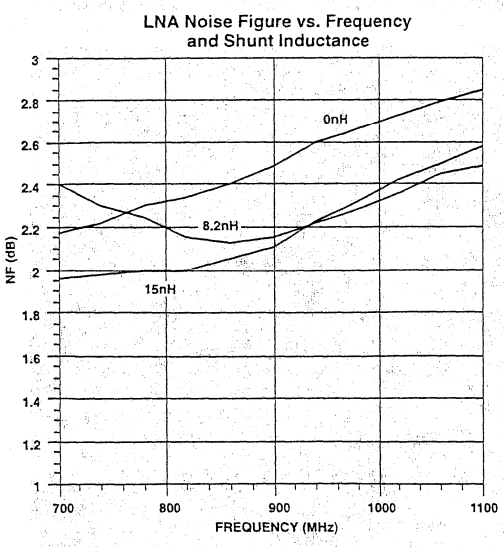


Figure 4.



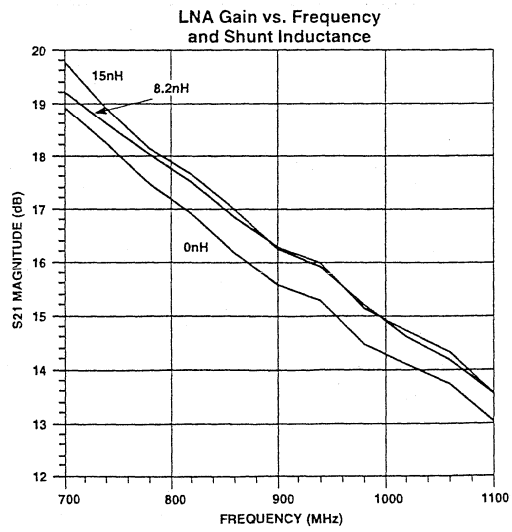


Figure 5.

Double-balanced mixer and oscillator NE/SA602A

DESCRIPTION

The NE/SA602A is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602A make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external LO. For higher frequencies the LO input may be externally driven. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the NE/SA602A a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

FEATURES

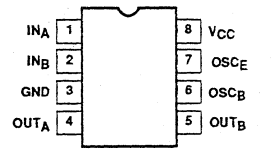
- Low current consumption: 2.4mA typical
- Excellent noise figure: <4.7dB typical at 45MHz
- High operating frequency
- Excellent gain, intercept and sensitivity
- Low external parts count; suitable for crystal/ceramic filters
- SA602A meets cellular radio specifications

APPLICATIONS

- Cellular radio mixer/oscillator
- Portable radio
- VHF transceivers
- RF data links
- HF/VHF frequency conversion
- Instrumentation frequency conversion
- Broadband LANs

PIN CONFIGURATION

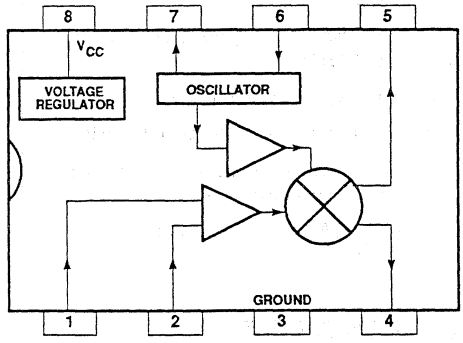
F, D and N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE602AN
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE602AD
8-Pin Cerdip	0 to +70°C	NE602AFE
8-Pin Plastic DIP	–40 to +85°C	SA602AN
8-Pin Plastic SO (Surface-mount)	–40 to +85°C	SA602AD
8-Pin Cerdip	–40 to +85°C	SA602AFE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Maximum operating voltage		9	V
T_{STG}	Storage temperature range		–65 to +150	°C
T_A	Operating ambient temperature range	NE602A	0 to +70	°C
		SA602A	–40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W

AC/DC ELECTRICAL CHARACTERISTICS V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA602A			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figure at 45MHz			5.0	5.5	dB
	Third–order intercept point	RF_{IN} = –45dBm: f_1 = 45.0MHz, f_2 = 45.06MHz		–13	–15	dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The NE/SA602A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA602A is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio second IF and demodulator, the SA602A is capable of receiving –119dBm signals with a 12dB S/N ratio. Third–order intercept is typically –13dBm (that is approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small–signal or signal–to–noise issues are not critical, the input to the NE602A should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE/SA602A is designed to be flexible. The input, RF mixer output and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required LO is beyond oscillation limits, or the system calls for an external LO, the external signal can be injected at Pin 6 through a DC blocking capacitor. External LO should be at least 200mV_{P-P}.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varactor tuned tank oscillator suitable for synthesizer–controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual–gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non–critical applications. The resistive divider in the emitter–follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor.

This improves the AC operating characteristic of the transistor and should help the oscillator to start. A 22kΩ resistor will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

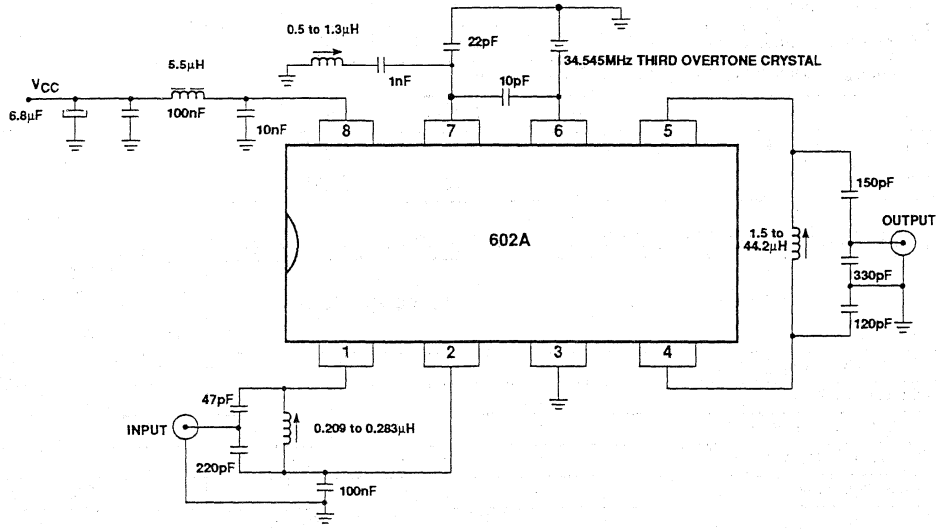


Figure 1. Test Configuration

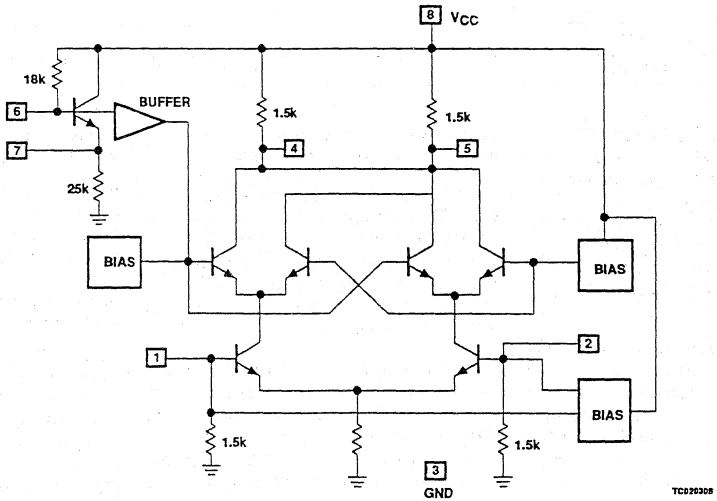
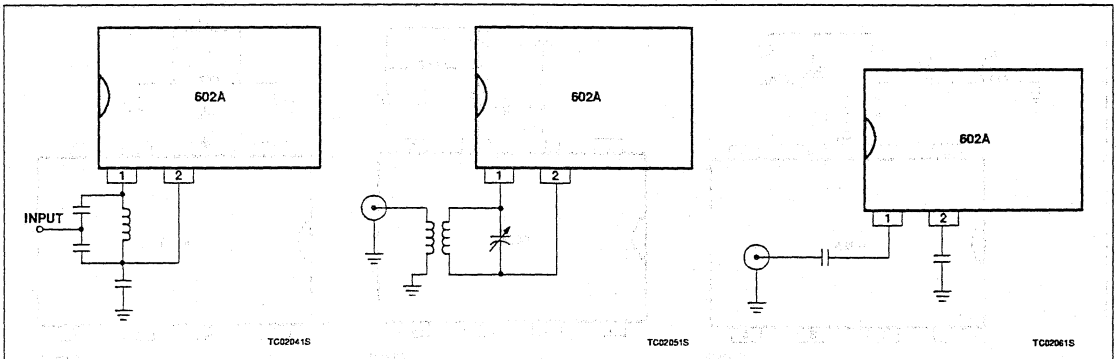


Figure 2. Equivalent Circuit

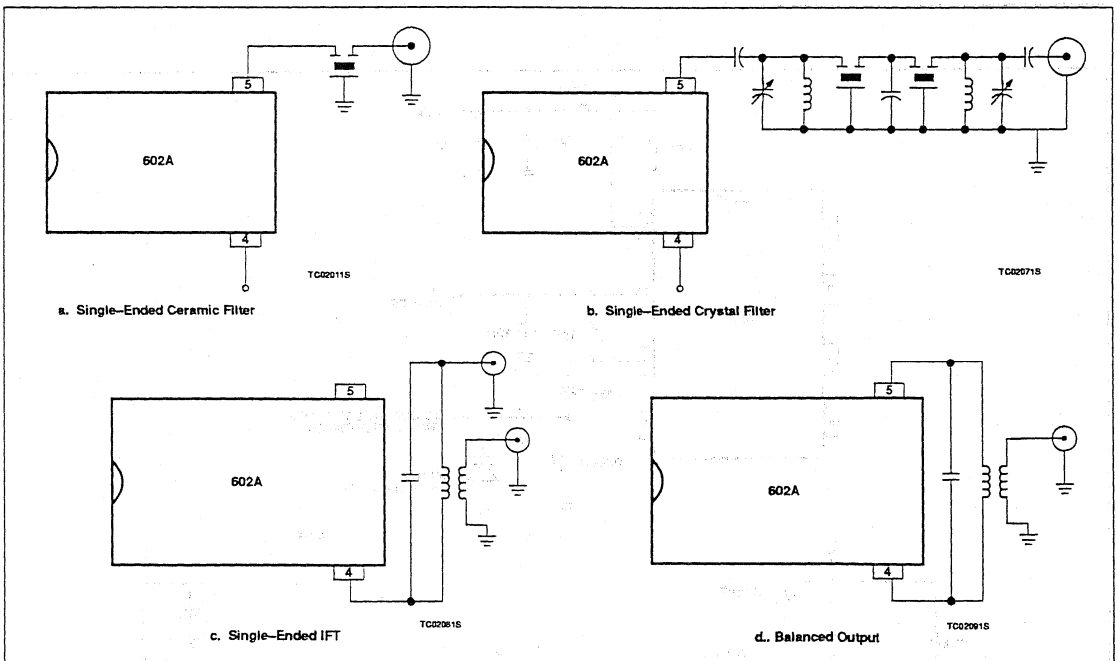


a. Single-Ended Tuned Input

b. Balanced Input (For Attenuation of Second-Order Products)

c. Single-Ended Untuned Input

Figure 3. Input Configuration



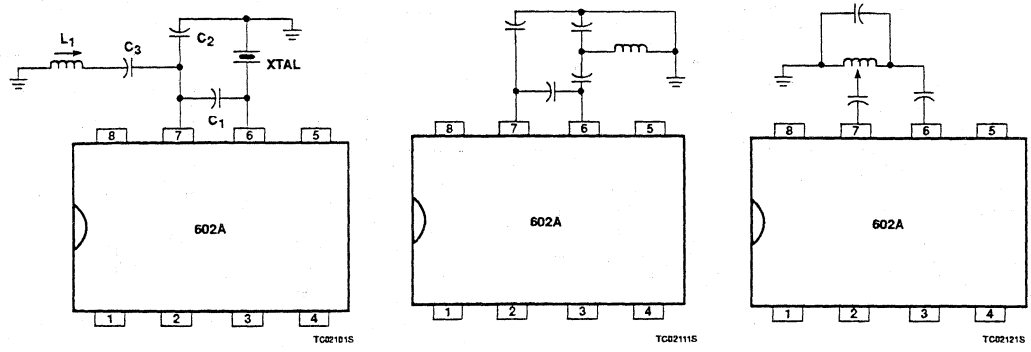
a. Single-Ended Ceramic Filter

b. Single-Ended Crystal Filter

c. Single-Ended IFT

d. Balanced Output

Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)

b. Colpitts L/C Tank Oscillator

c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

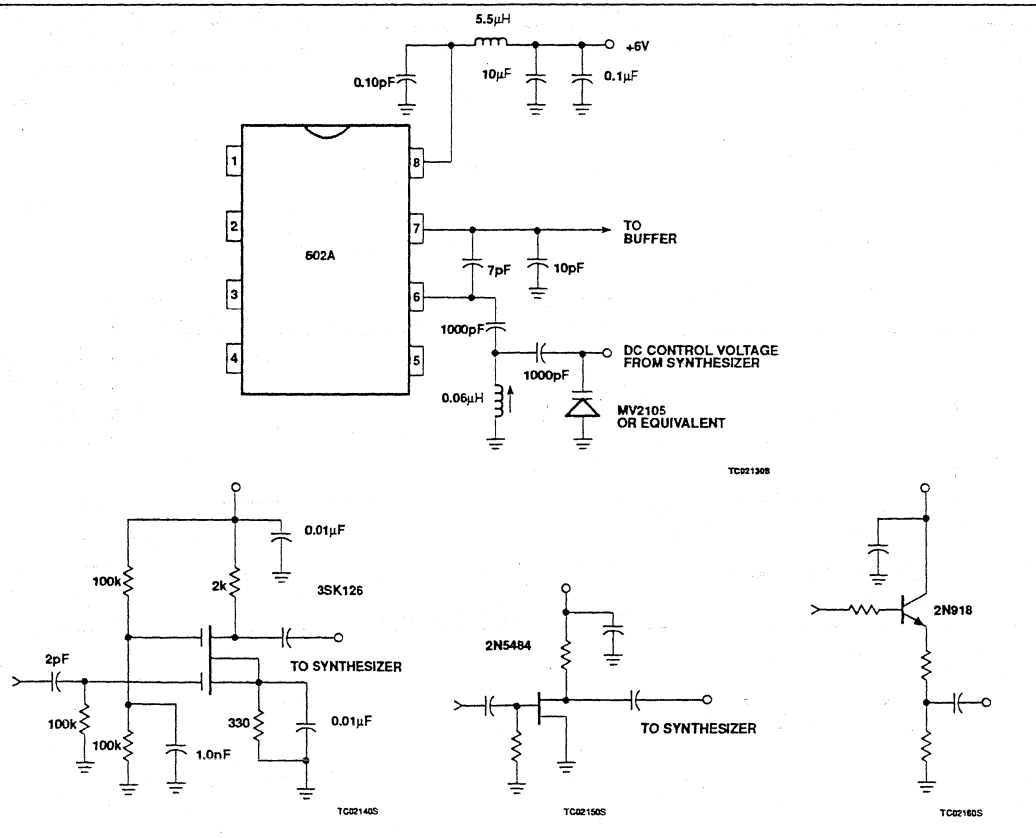


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

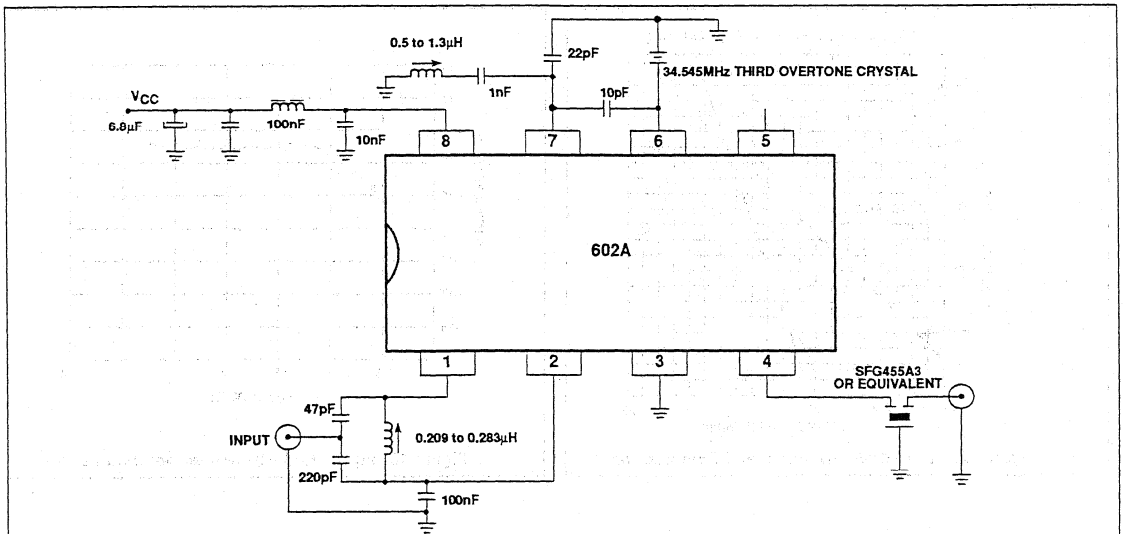


Figure 7. Typical Application for Cellular Radio

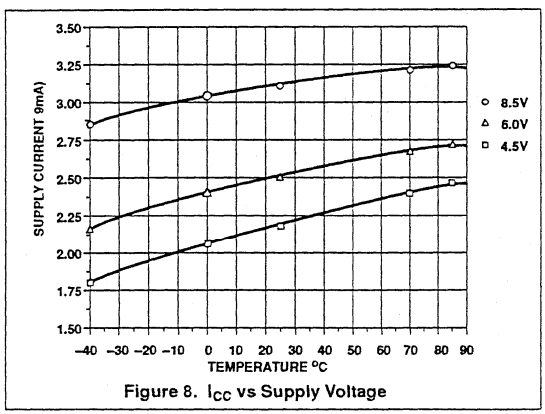


Figure 8. I_{CC} vs Supply Voltage

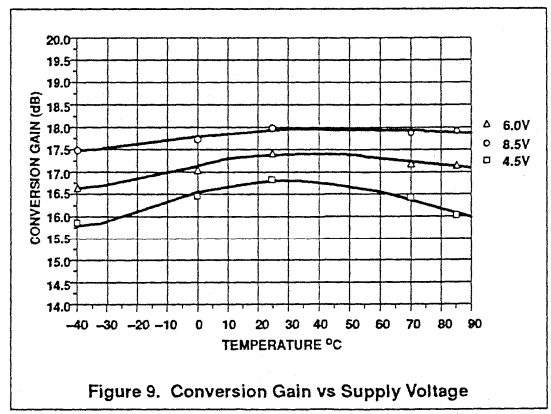


Figure 9. Conversion Gain vs Supply Voltage

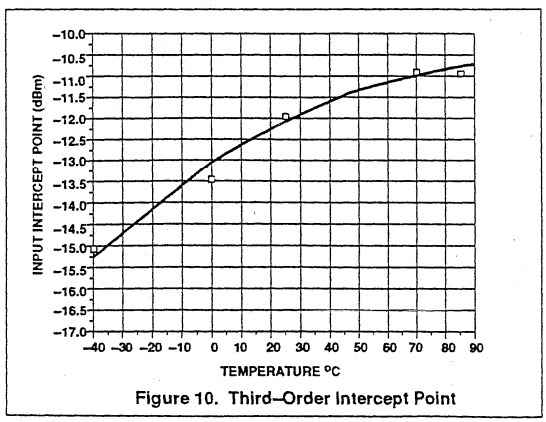


Figure 10. Third–Order Intercept Point

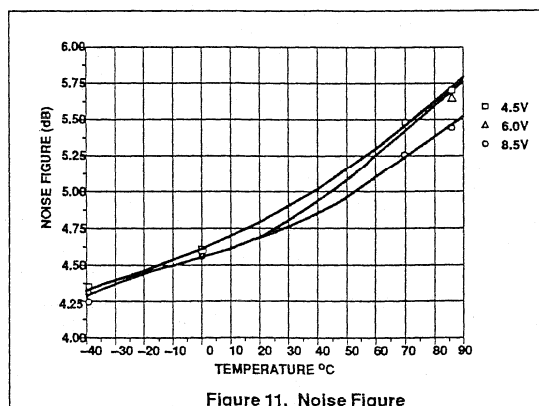


Figure 11. Noise Figure

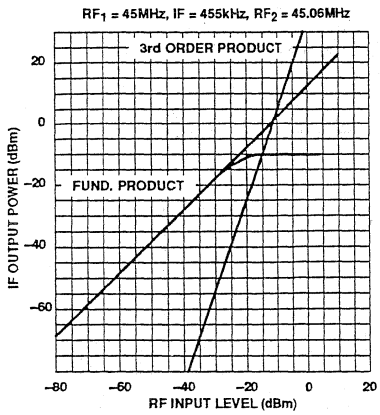


Figure 12. Third–Order Intercept and Compression

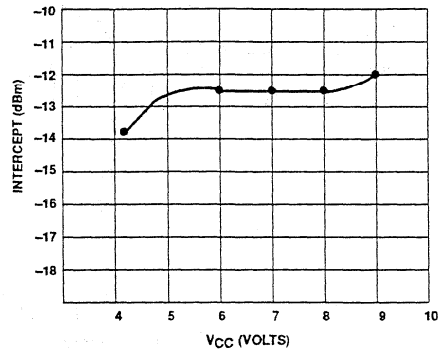


Figure 13. Input Third–Order Intermod Point vs V_{CC}

High performance low power FM IF system

NE/SA604A

DESCRIPTION

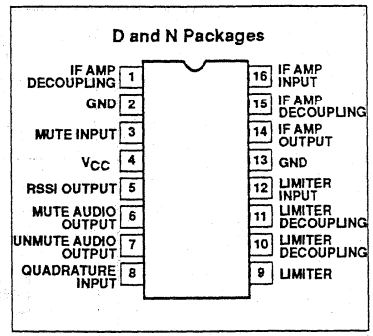
The NE/SA604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA604A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA604A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

PIN CONFIGURATION

D and N Packages



FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA604A meets cellular radio specifications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic DIP	0 to +70°C	NE604AN	0406C
16-Pin Plastic SO (Surface-mount)	0 to +70°C	NE604AD	0005D
16-Pin Plastic DIP	-40 to +85°C	SA604AN	0406C
16-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA604AD	0005D

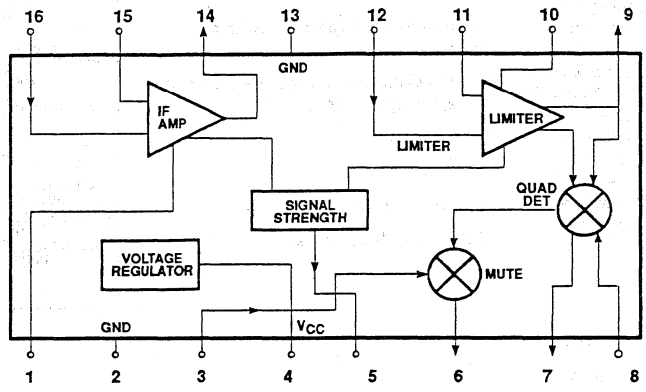
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range	NE604A SA604A	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance	D package N package	90 75	°C/W °C/W

High performance low power FM IF system

NE/SA604A

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92			-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530			530		mV_{RMS}
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = -118dBm	0	160	550	0	160	650	mV
		RF level = -68dBm	2.0	2.65	3.0	1.9	2.65	3.1	V
		RF level = -18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI range	R_4 = 100k (Pin 5)		90			90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

NOTE:

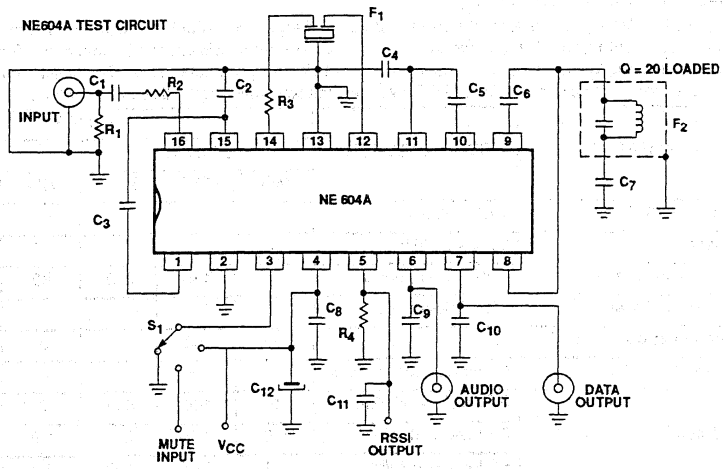
1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE604 (50)	NE604A (1.5k)/NE605 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

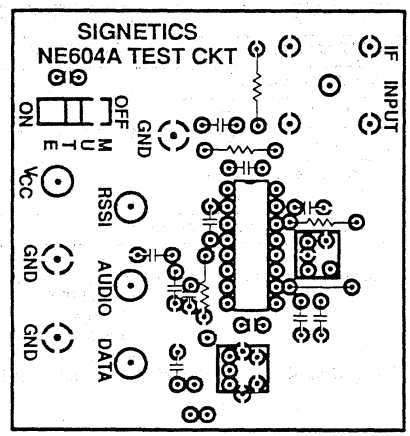
The NE605 and NE604A are both derived from the same basic die. The NE605 performance plots are directly applicable to the NE604A.

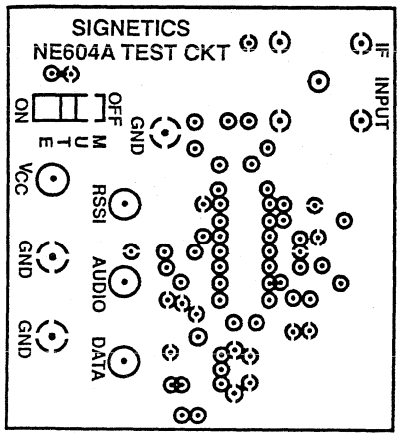
High performance low power FM IF system

NE/SA604A



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





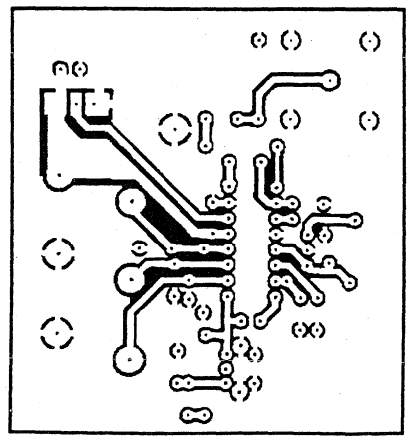


Figure 1. NE/SA604A Test Circuit

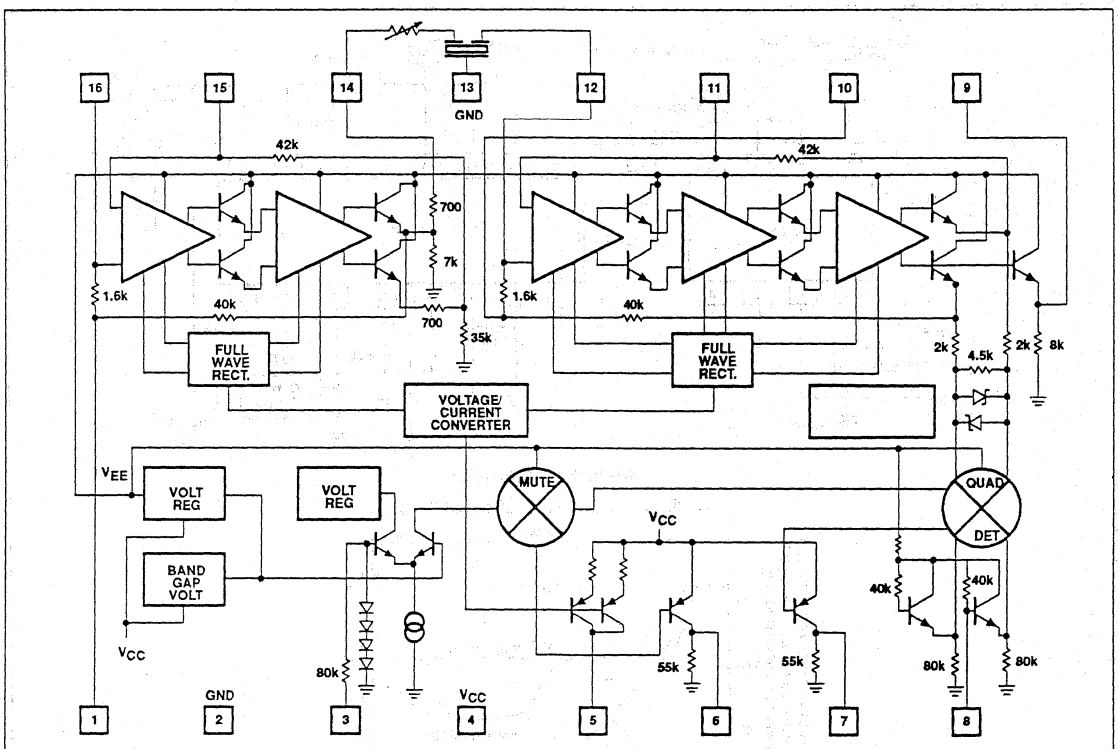


Figure 2. Equivalent Circuit

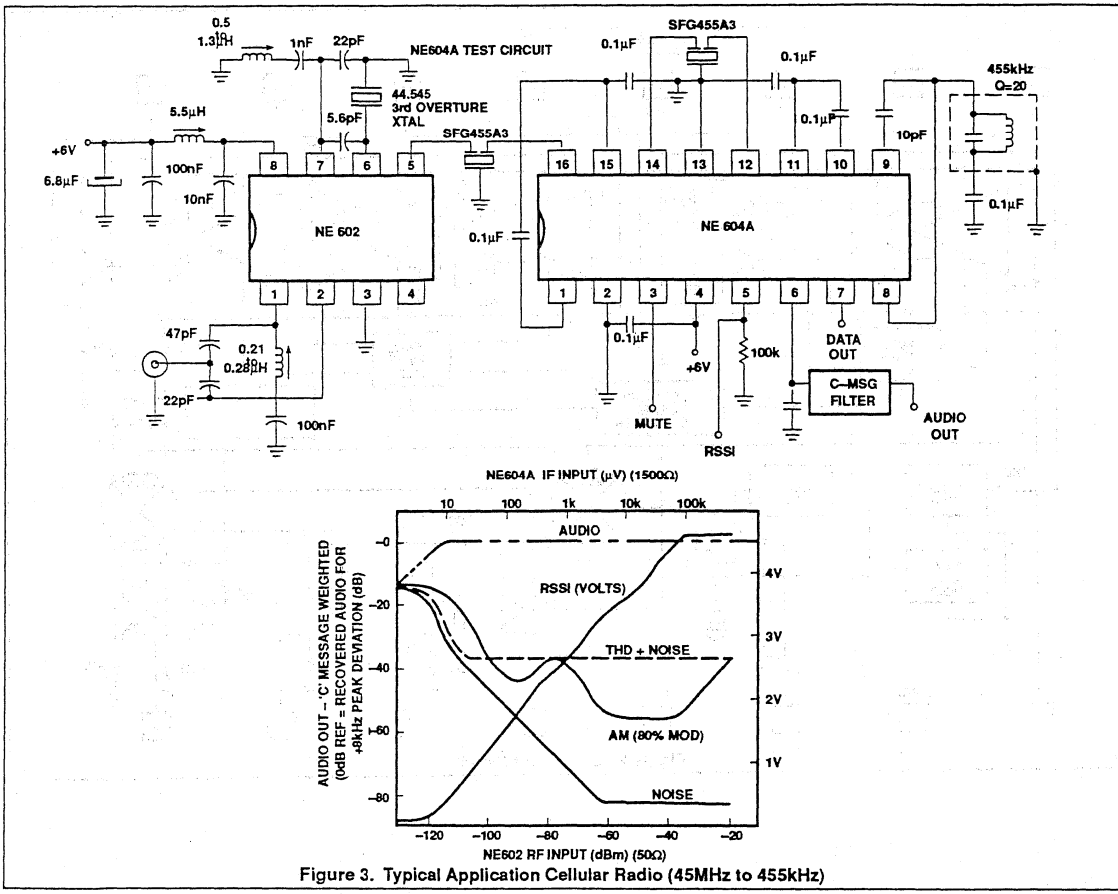


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA604A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

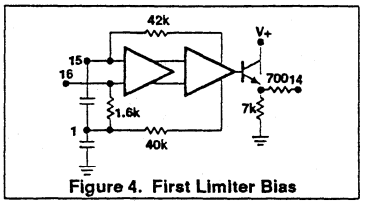


Figure 4. First Limiter Bias

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields)

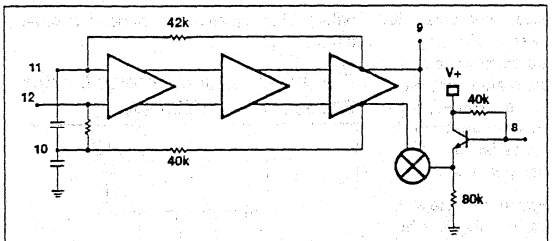


Figure 5. Second Limiter and Quadrature Detector

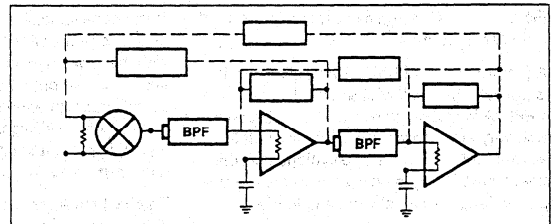
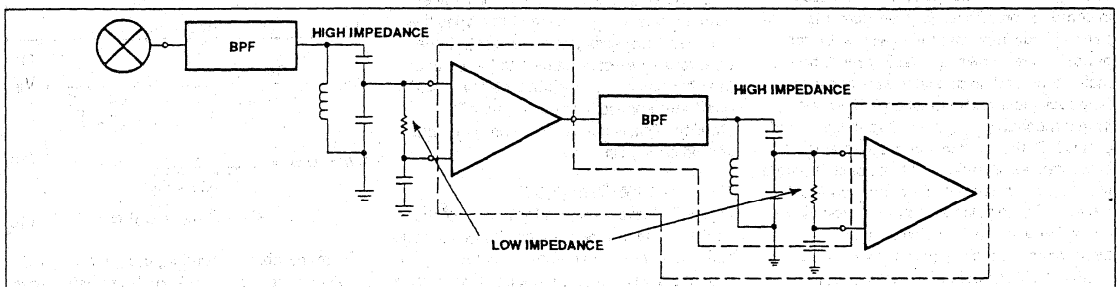
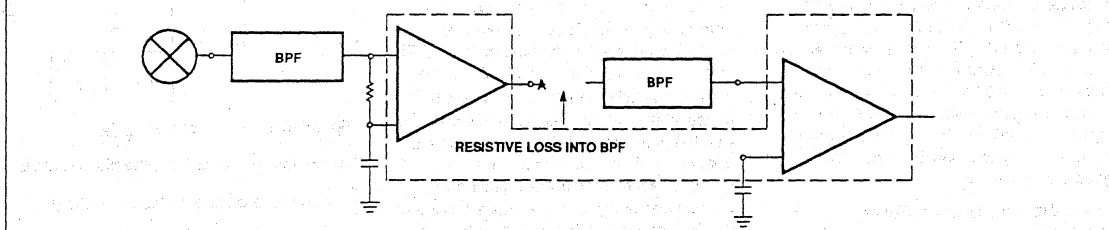


Figure 6. Feedback Paths



7a. Terminating High Impedance Filters with Transformation to Low Impedance



7b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

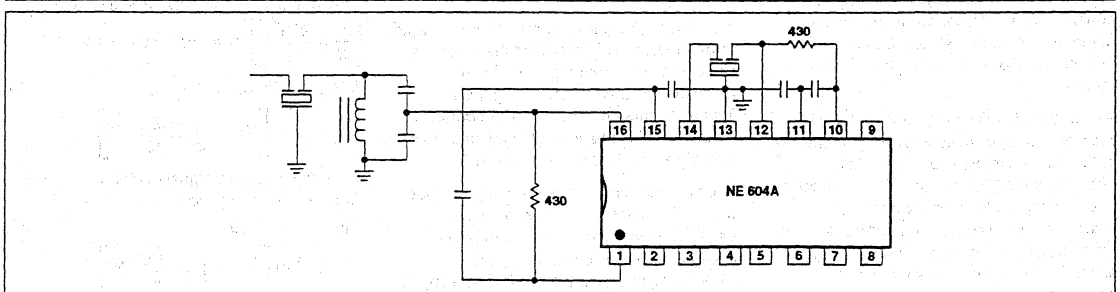


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in

Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE604A IF amplifiers, which is not specified, is low phase shift. The NE604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

Stability Considerations

The high gain and bandwidth of the NE604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE604A

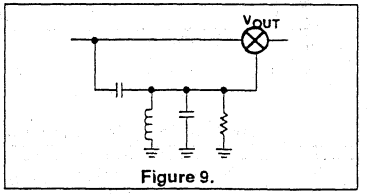


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \cdot \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \cdot V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = \tan^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

$$\text{If } V_{IN} = A \sin \omega t \Rightarrow V_O = A \quad (3)$$

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \quad (4)$$

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega_1}{\omega} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5kHz}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174pF$ and $L = 0.7mH$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10pF$ and $C_P = 164pF$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1pF$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers.

Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

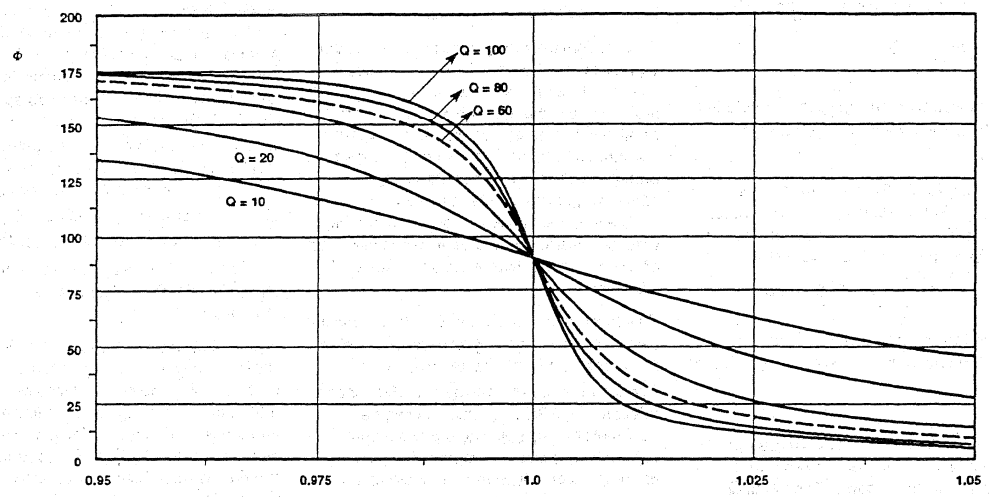


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

High performance low power mixer FM IF system

NE/SA605

DESCRIPTION

The NE/SA605 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA605 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA605 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA605. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

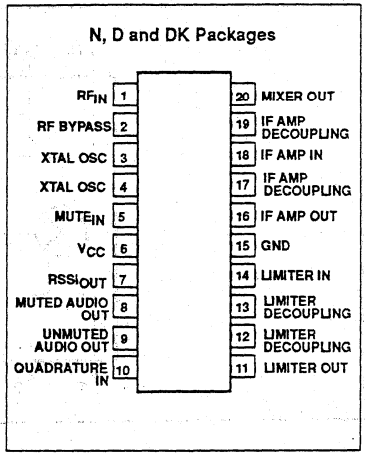
For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA605 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

N, D and DK Packages



APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

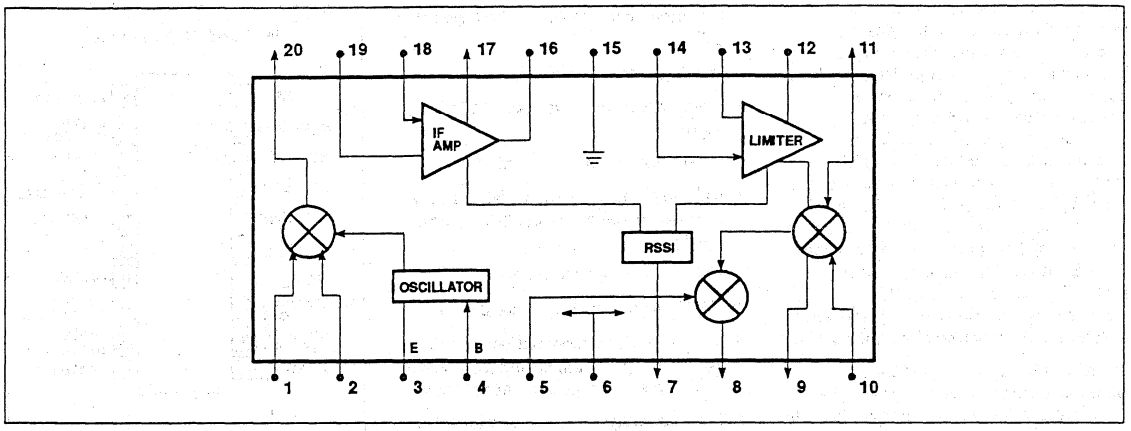
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	0 to +70°C	NE605N	0408B
20-Pin Plastic DIP	–40 to +85°C	SA605N	0408B
20-Pin Plastic SOL	0 to +70°C	NE605D	0172D
20-Pin Plastic SOL	–40 to +85°C	SA605D	0172D
20-Pin Plastic SSOP	0 to +70°C	NE605DK	1563
20-Pin Plastic SSOP	–40 to +85°C	SA605DK	1563

High performance low power mixer FM IF system

NE/SA605

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range NE605		0 to +70	°C
	SA605		-40 to +85	°C
θ_{JA}	Thermal impedance	D package N package SSOP package	90 75 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.7	6.5	4.55	5.7	6.55	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480			480		mV
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		1.40	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ
RF/IF section (int LO)									
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450			450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA605 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

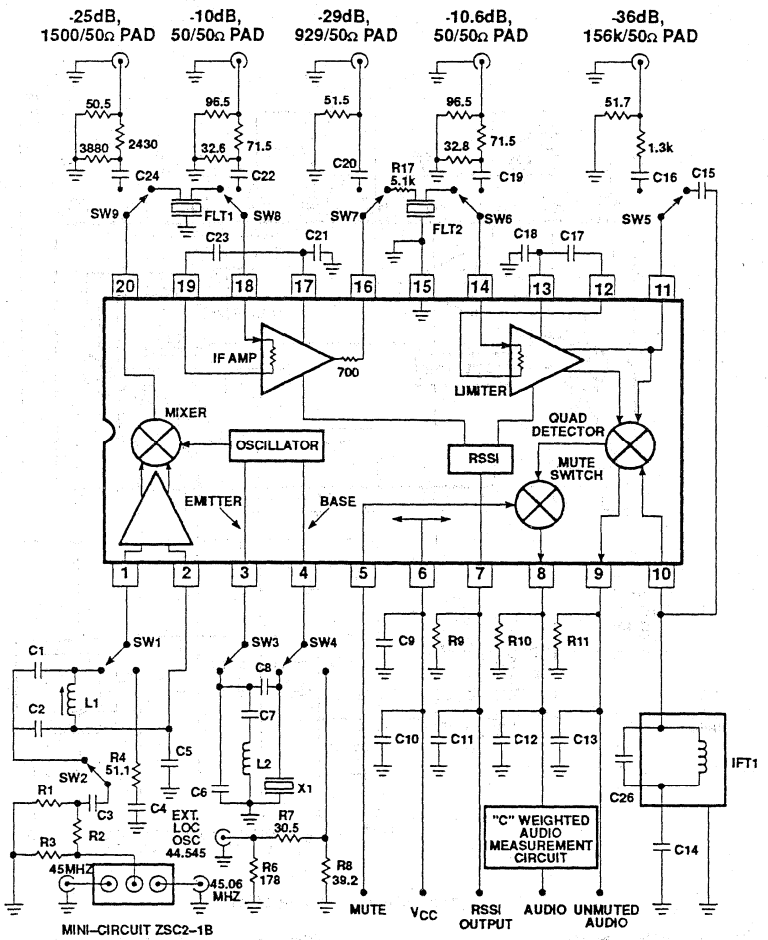
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

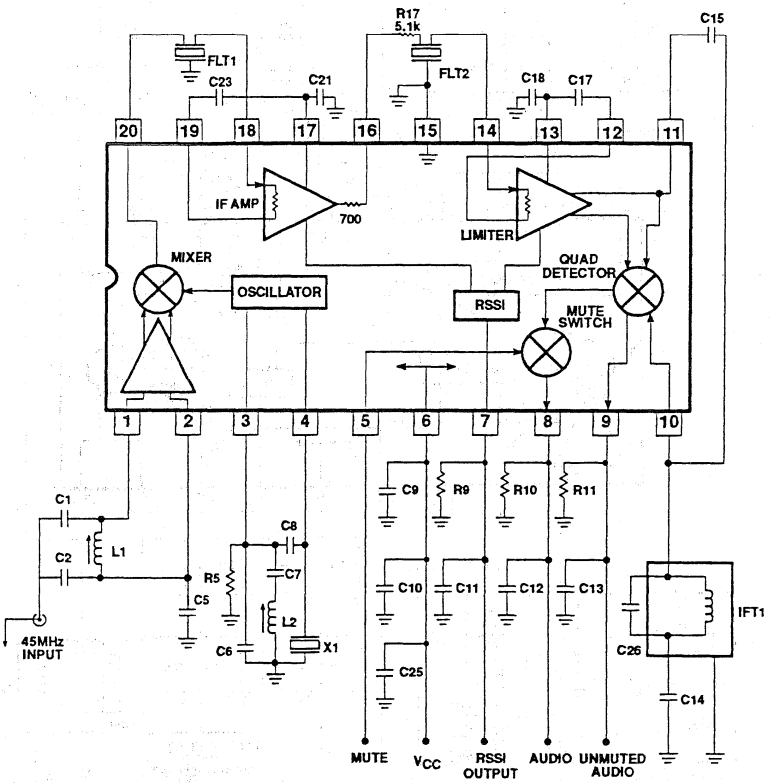


Automatic Test Circuit Component List

C1	47pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	180pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	C26	390pF ±10% Monolithic Ceramic
C7	1nF Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C9	100nF ±10% Monolithic Ceramic	IFT 1	455kHz 270μH TOKO #303LN-1129
C10	6.8μF Tantalum (minimum) *	L1	300nH TOKO #5CB-1055Z
C11	100nF ±10% Monolithic Ceramic	L2	0.8μH TOKO 292CNS-T1038Z
C12	15nF ±10% Ceramic	X1	44.545MHz Crystal ICM4712701
C13	150pF ±2% N1500 Ceramic	R9	100k ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C15	10pF NPO Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

* NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA605 45MHz Test Circuit (Relays as shown)



Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270μH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8μH TOKO 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

* NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA605 45MHz Application Circuit

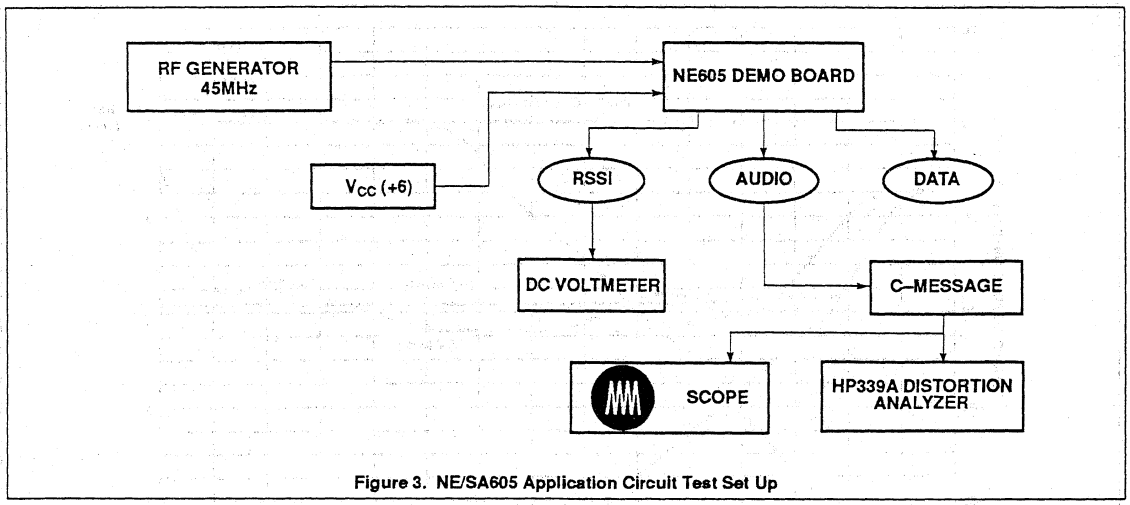


Figure 3. NE/SA605 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

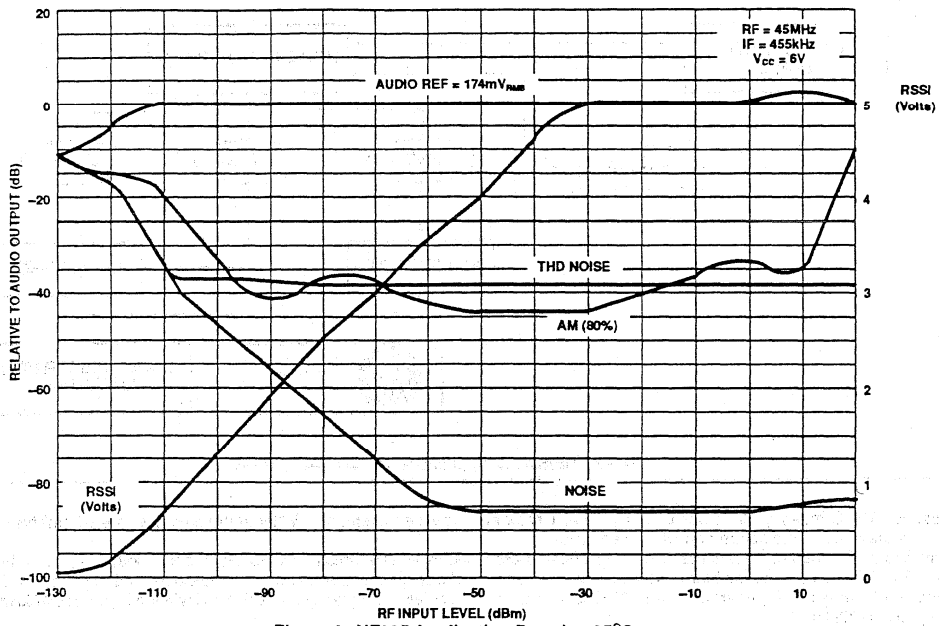


Figure 4. NE605 Application Board at 25°C

Double-balanced mixer and oscillator NE/SA612A

DESCRIPTION

The NE/SA612A is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 45MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 45MHz is typically below 6dB and makes the device well suited for high performance cordless phone/cellular radio. The low power consumption makes the NE/SA612A excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE/SA612A is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

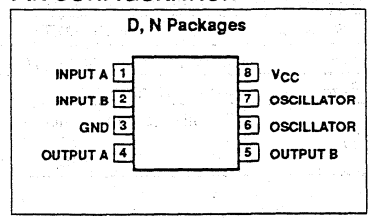
FEATURES

- Low current consumption
- Low cost
- Operation to 500MHz
- Low radiated energy
- Low external parts count; suitable for crystal/ceramic filter
- Excellent sensitivity, gain, and noise figure

APPLICATIONS

- Cordless telephone
- Portable radio
- VHF transceivers
- RF data links
- Sonabuoys
- Communications receivers
- Broadband LANs
- HF and VHF frequency conversion
- Cellular radio mixer/oscillator

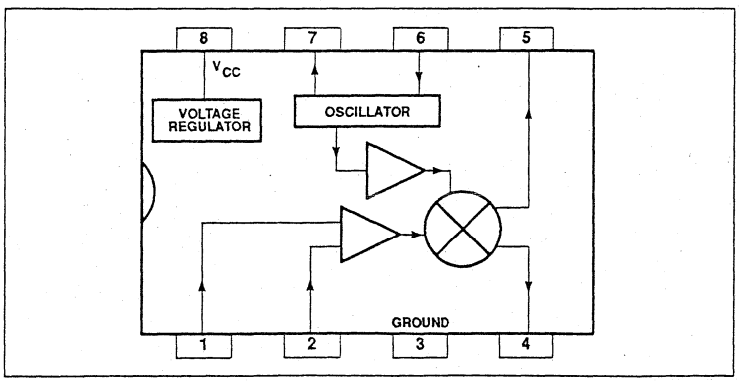
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE612AN
8-Pin Plastic SO (Surface-Mount)	0 to +70°C	NE612AD
8-Pin Plastic DIP	-40 to +85°C	SA612AN
8-Pin Plastic SO (Surface-Mount)	-40 to +85°C	SA612AD

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Operating ambient temperature range NE SA	 0 to +70 -40 to +85	°C

AC/DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC} = 6V, Figure 1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	3.0	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0		dB
	Third-order intercept point at 45MHz	RF_{IN}=-45dBm		-13		dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The NE/SA612A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA612A is designed for optimum low power performance. When used with the NE614A as a 45MHz cordless phone/cellular radio 2nd IF and demodulator, the NE/SA612A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE/SA612A should be appropriately scaled.

TEST CONFIGURATION

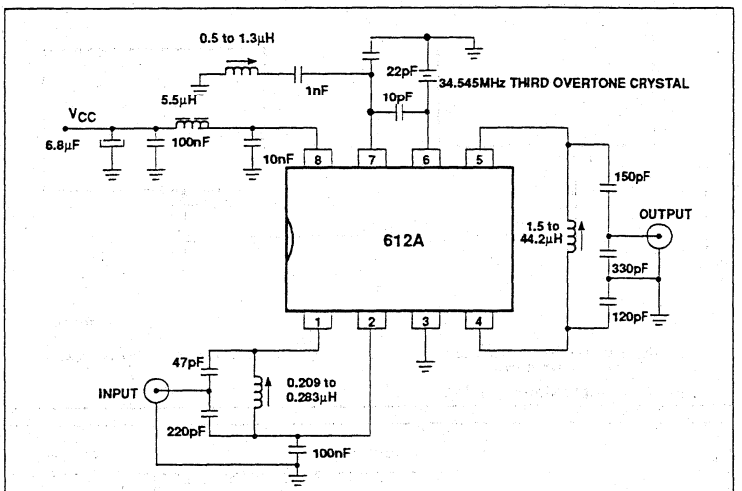


Figure 1. Test Configuration

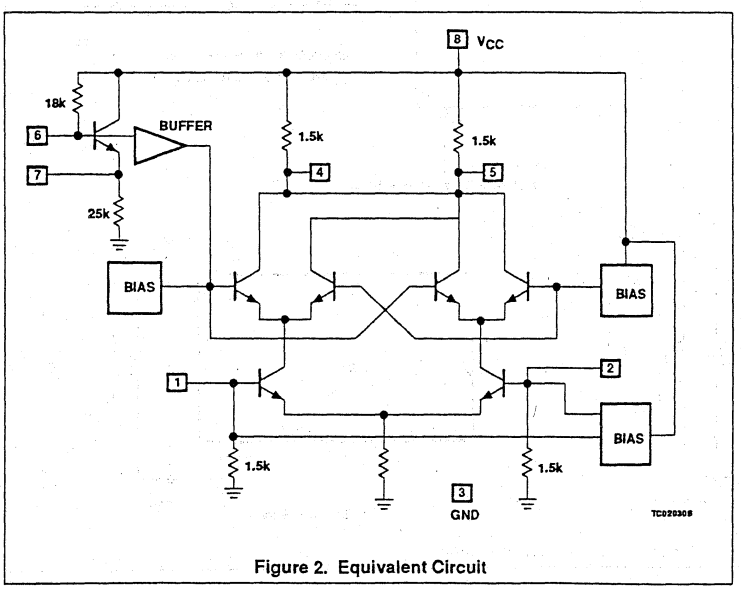


Figure 2. Equivalent Circuit

Besides excellent low power performance well into VHF, the NE/SA612A is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

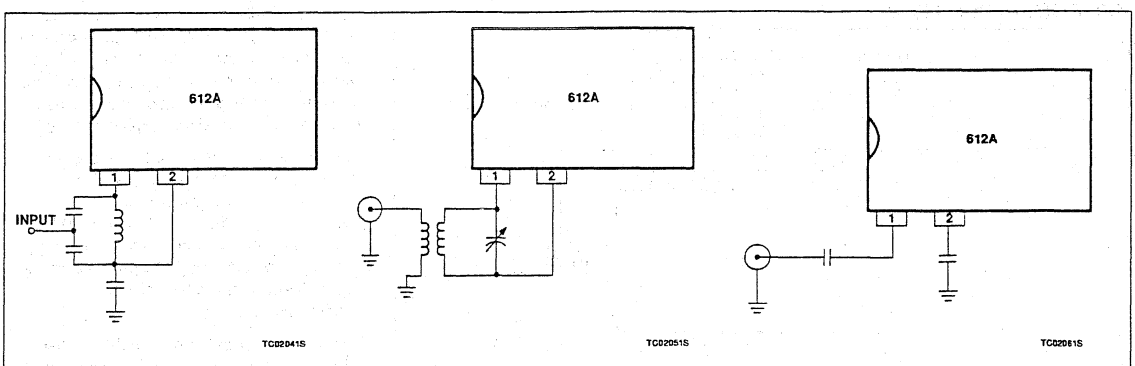
The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the

permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be 200mV$_{P-P}$ minimum to 300mV$_{P-P}$ maximum.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cordless phones/cellular radio. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

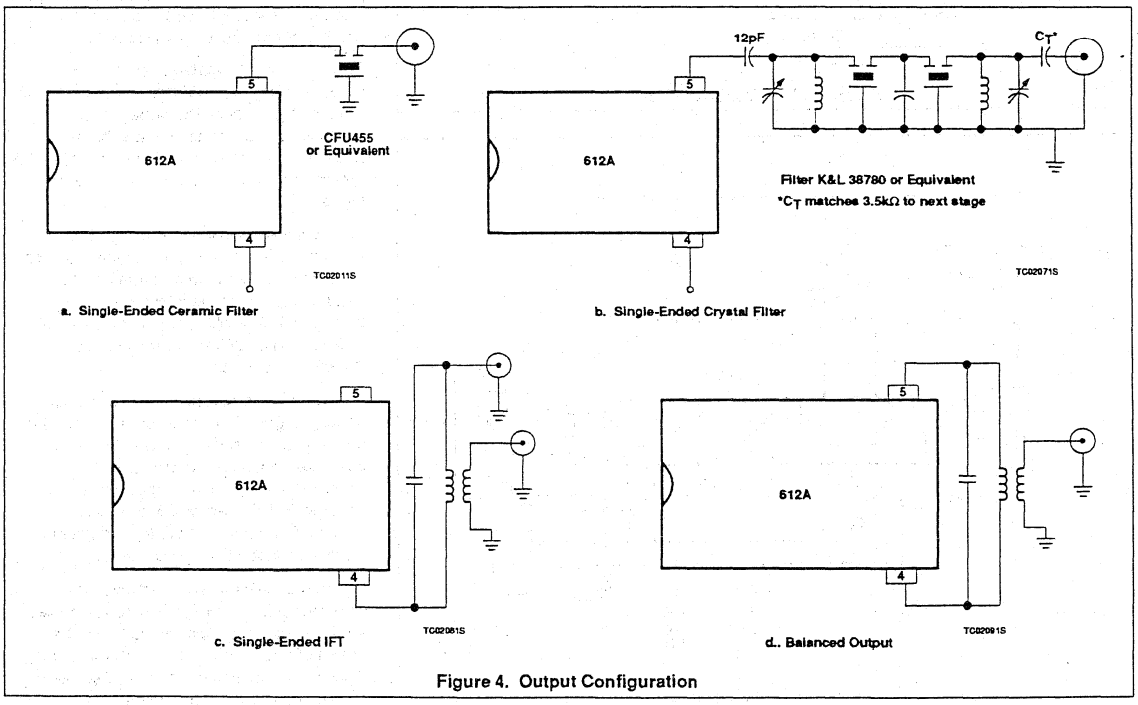


a. Single-Ended Tuned Input

b. Balanced Input (For Attenuation of Second-Order Products)

c. Single-Ended Untuned Input

Figure 3. Input Configuration



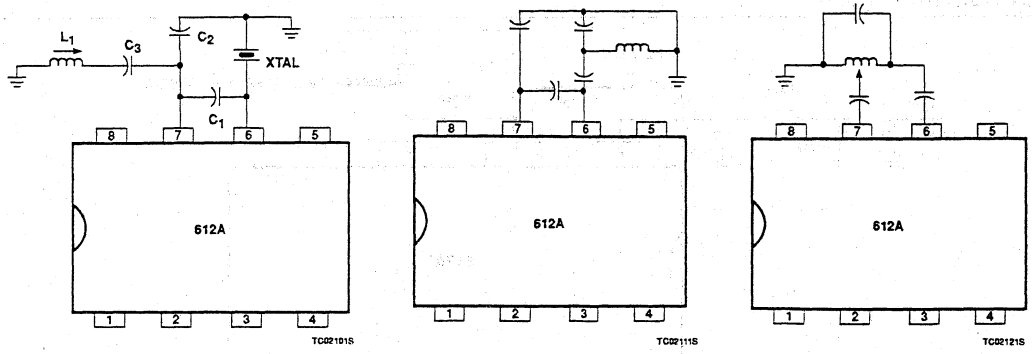
a. Single-Ended Ceramic Filter

b. Single-Ended Crystal Filter

c. Single-Ended IFT

d. Balanced Output

Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)

b. Colpitts L/C Tank Oscillator

c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

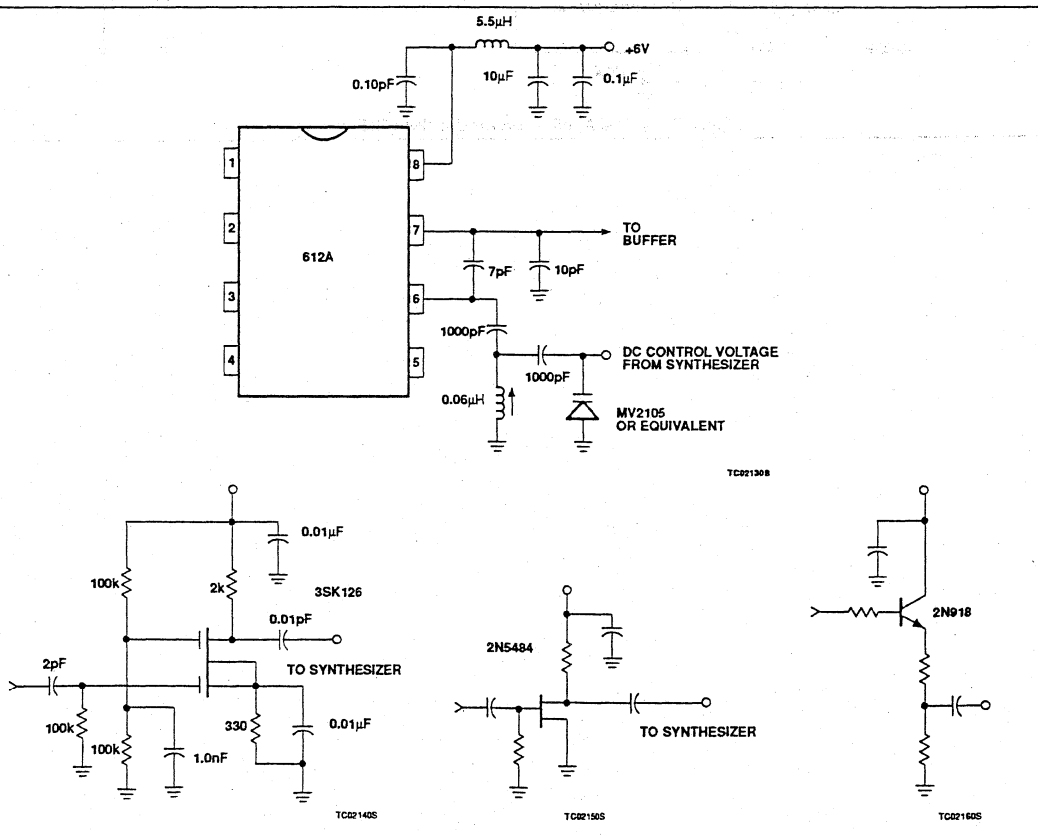


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

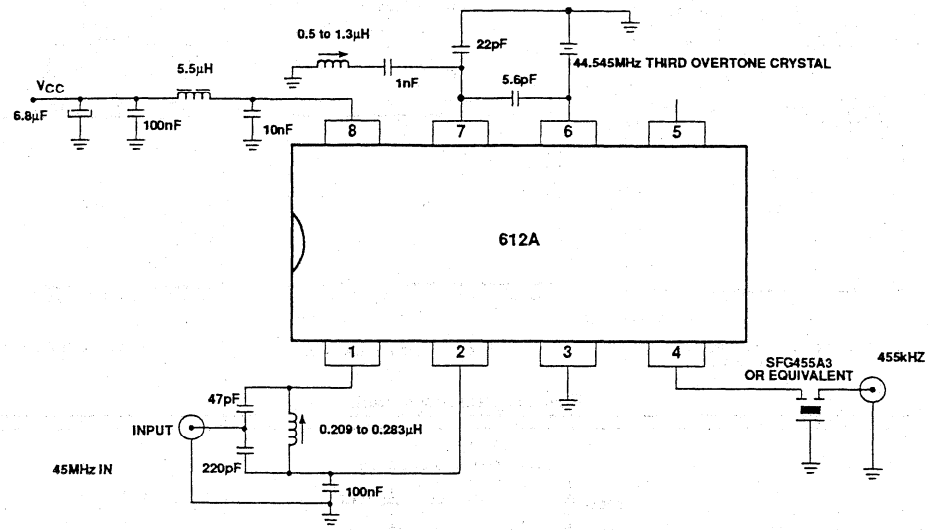


Figure 7. Typical Application for Cordless/Cellular Radio

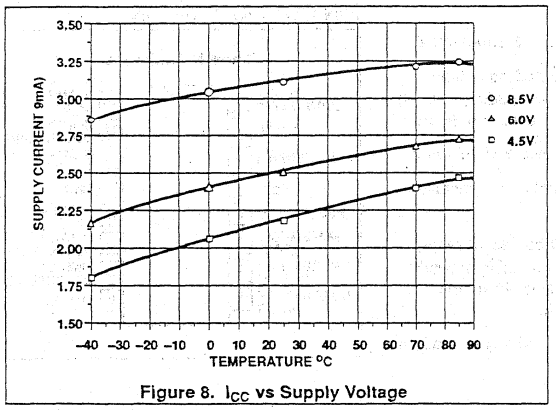


Figure 8. I_{CC} vs Supply Voltage

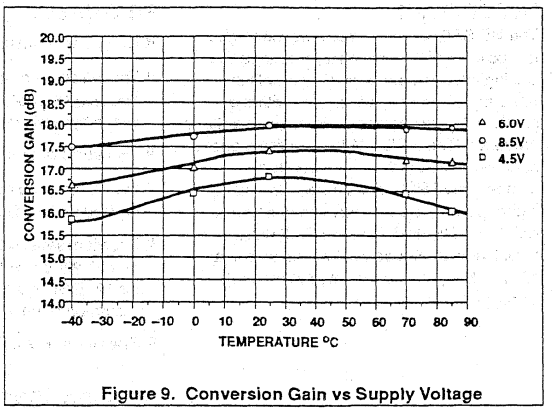


Figure 9. Conversion Gain vs Supply Voltage

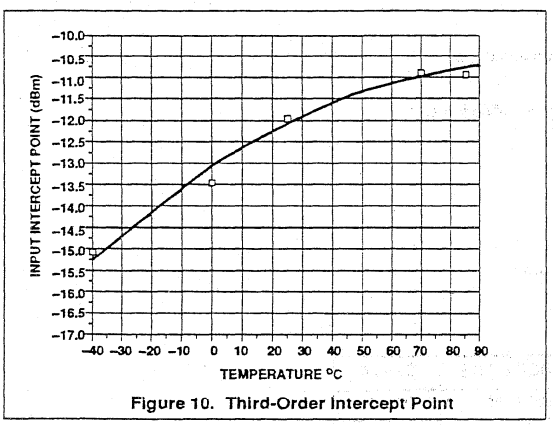


Figure 10. Third-Order Intercept Point

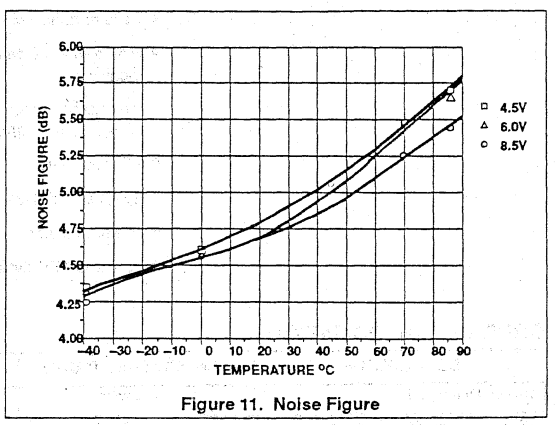


Figure 11. Noise Figure

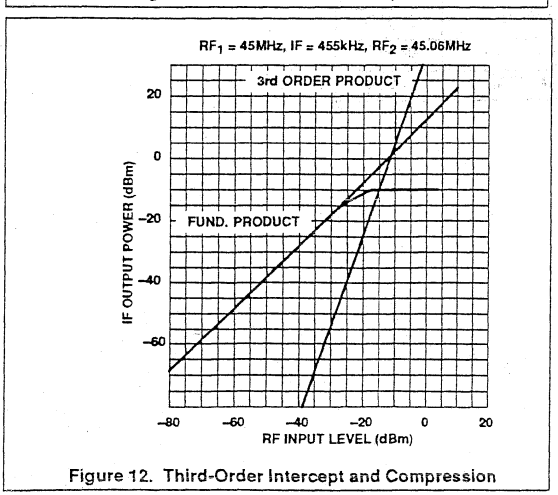


Figure 12. Third-Order Intercept and Compression

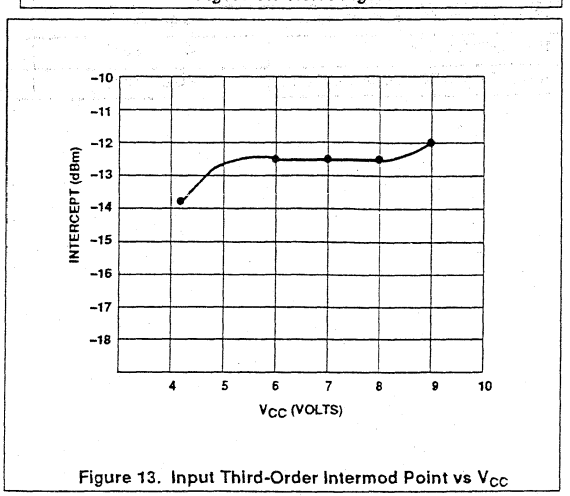


Figure 13. Input Third-Order Intermod Point vs V_{CC}

Low power FM IF system NE/SA614A

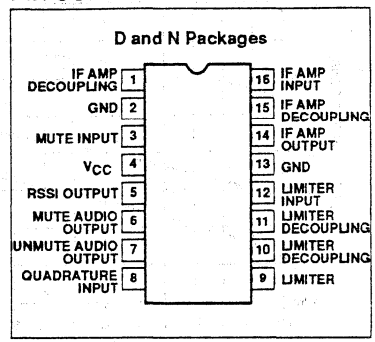
DESCRIPTION

The NE/SA614A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA614A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA614A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5µV across input pins (0.22µV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA614A meets cellular radio specifications

PIN CONFIGURATION



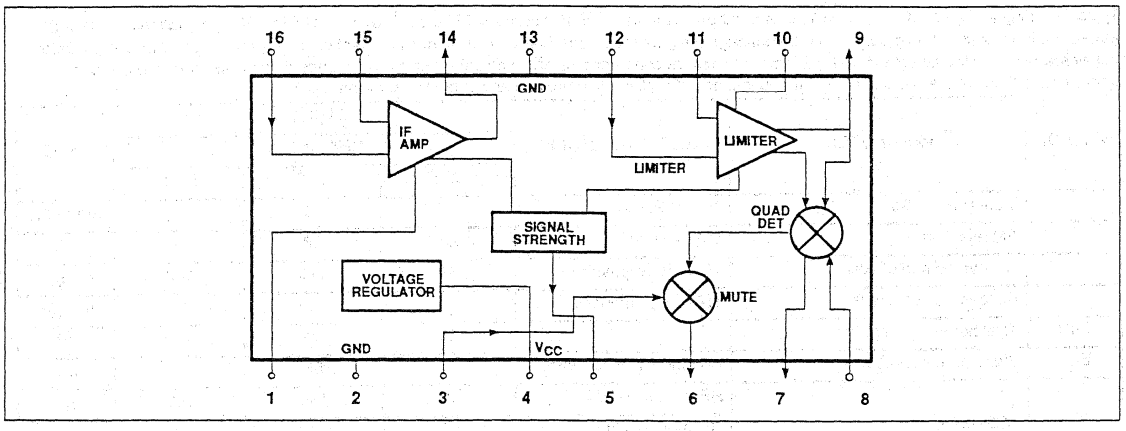
APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic DIP	0 to +70°C	NE614AN	0406C
16-Pin Plastic SO (Surface-mount)	0 to +70°C	NE614AD	0005D
16-Pin Plastic DIP	-40 to +85°C	SA614AN	0406C
16-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA614AD	0005D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE614A SA614A	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE614A			SA614A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

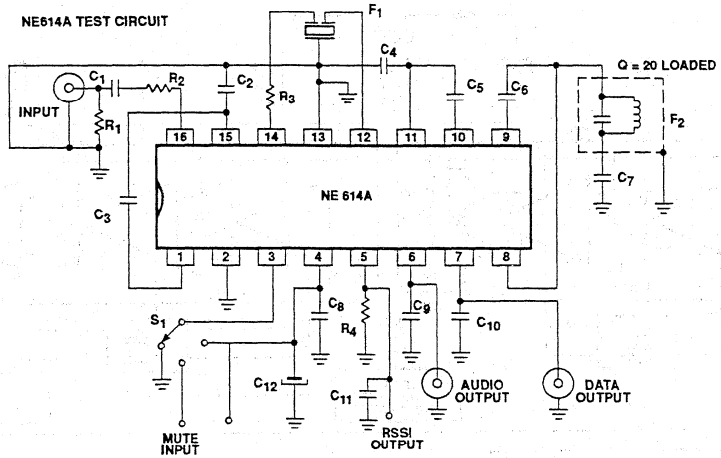
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA614A			
			MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92		dBm/50Ω
	AM rejection	80% AM 1kHz	25	33		dB
	Recovered audio level	15nF de-emphasis	60	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530		mV_{RMS}
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	RSSI output[1]	RF level = -118dBm	0	160	800	mV
		RF level = -68dBm	1.7	2.50	3.3	V
		RF level = -18dBm	3.6	4.80	5.8	V
	RSSI range	R_4 = 100k (Pin 5)		80		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±2.0		dB
	IF input impedance		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ

NOTE:

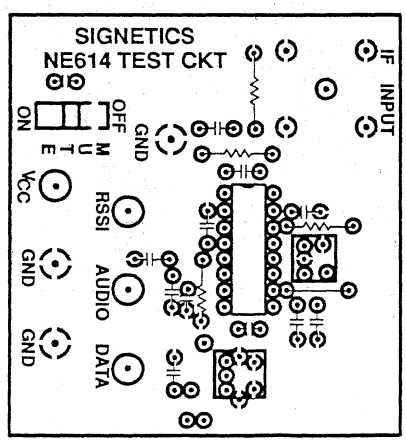
1. NE614A data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

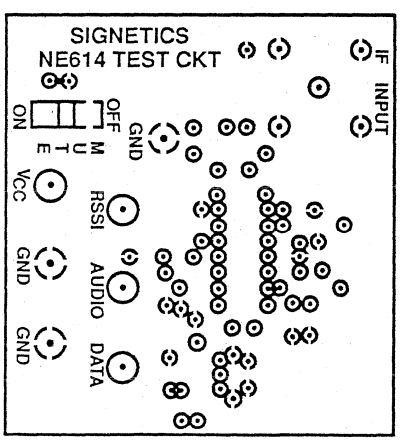
NE614A (50)	NE614A (1.5k)/NE615 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

The NE615 and NE614A are both derived from the same basic die. The NE615 performance plots are directly applicable to the NE614A.



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF ±10% 50V
C3	100nF ±10% 50V
C4	100nF ±10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





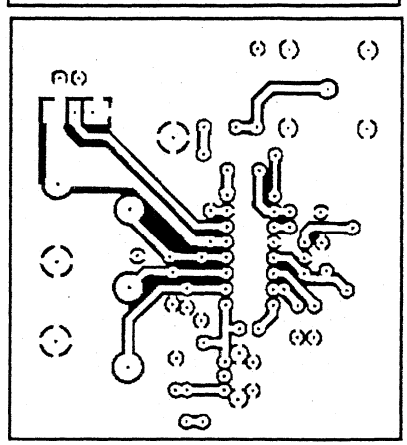


Figure 1. NE/SA614A Test Circuit

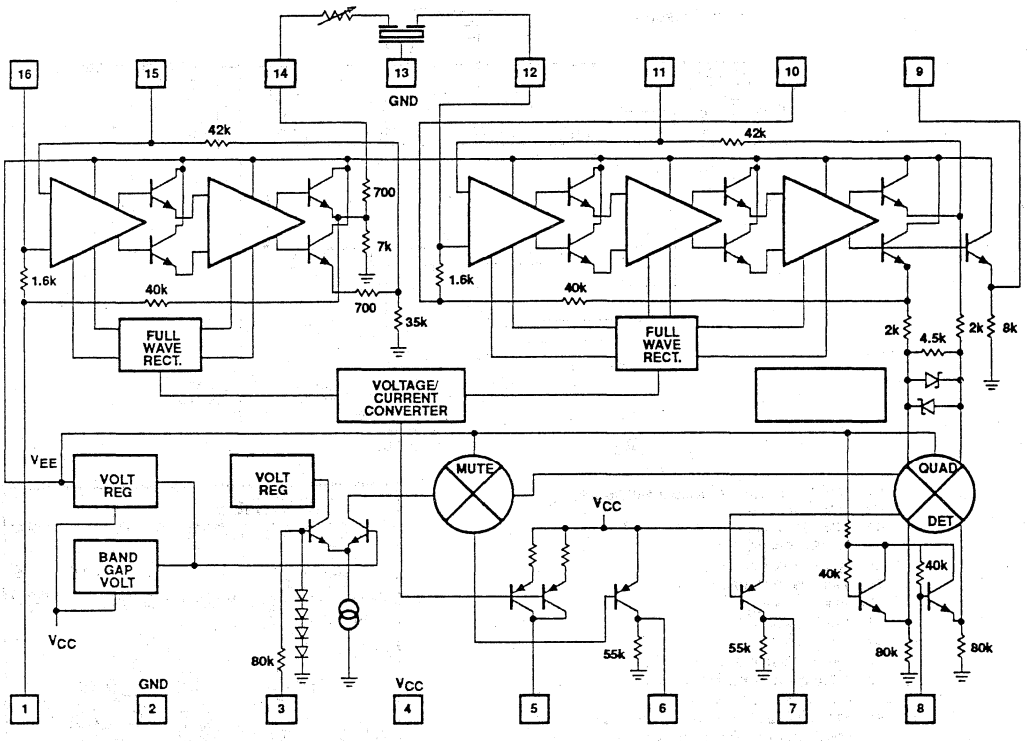


Figure 2. Equivalent Circuit

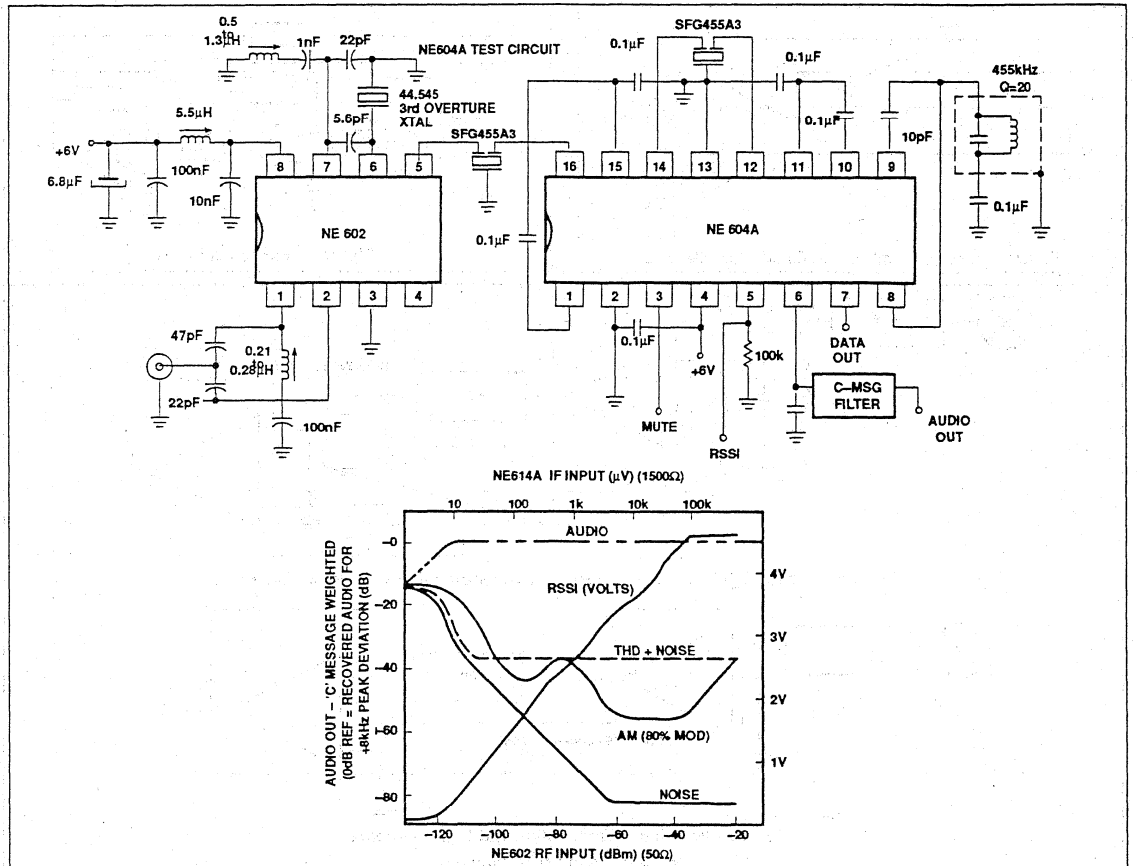


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA614A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA614A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA614A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

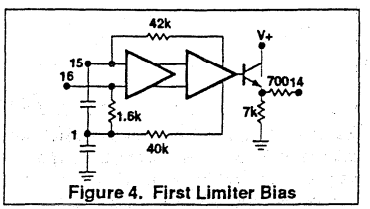


Figure 4. First Limiter Bias

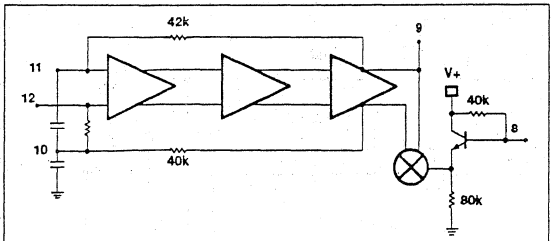


Figure 5. Second Limiter and Quadrature Detector

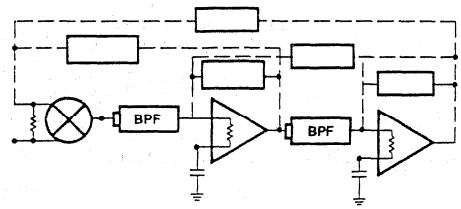
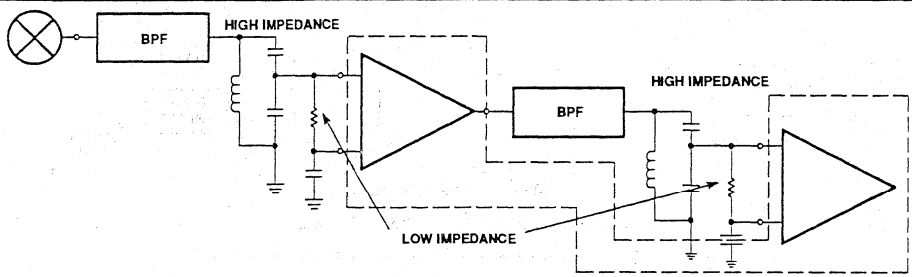
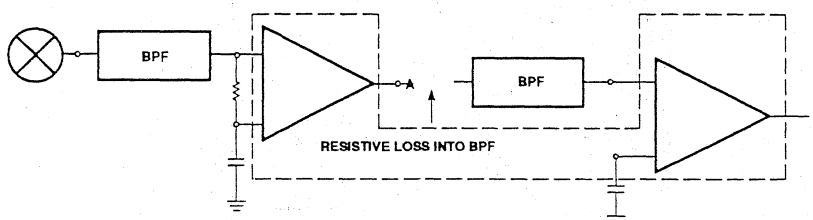


Figure 6. Feedback Paths



7a. Terminating High Impedance Filters with Transformation to Low Impedance



7b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

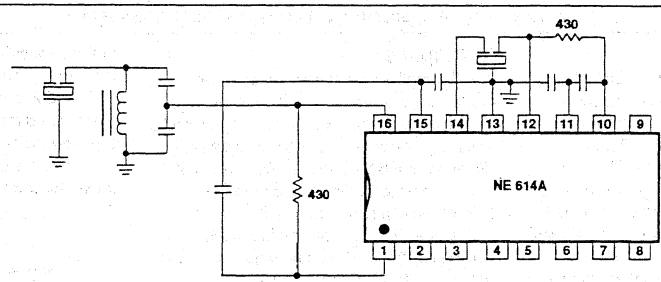


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain.

Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE614A IF amplifiers, which is not specified, is low phase shift. The NE614A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

Stability Considerations

The high gain and bandwidth of the NE614A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE614A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE614A

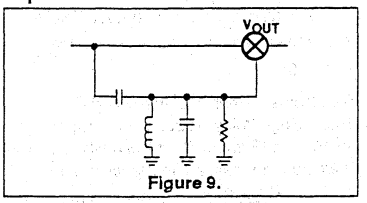


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \cdot \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \cdot V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \sin \omega t \Rightarrow V_O = A$ (3)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$V_{IN} \bullet V_O = A^2 \sin \omega t$ (4)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] \quad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega_1}{\omega} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5kHz}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 614A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174pF$ and $L = 0.7mH$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10pF$ and $C_P = 164pF$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1pF$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE614A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE614A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

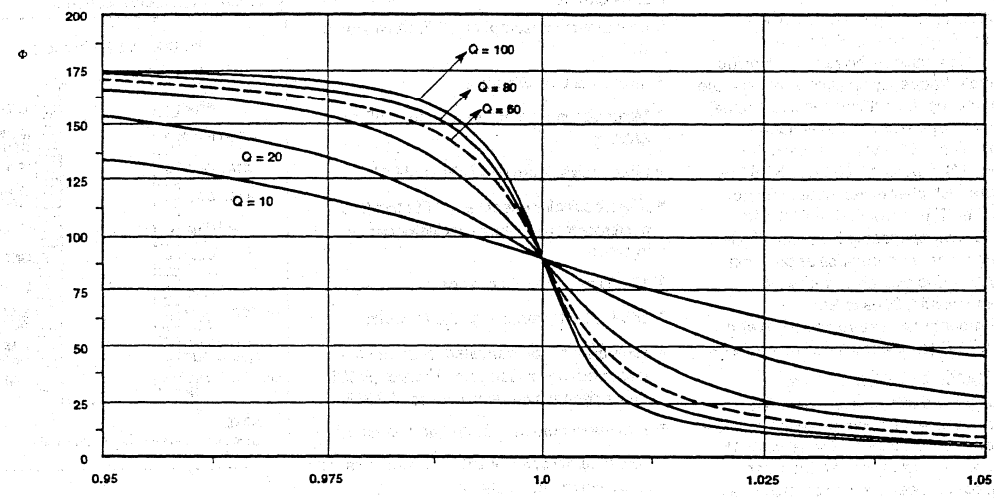


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_I} = 1 + \frac{\Delta\omega}{\omega_I}$

High performance low power mixer FM IF system

NE/SA615

DESCRIPTION

The NE/SA615 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA615 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA615 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA615. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

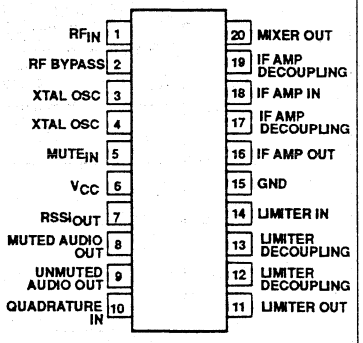
For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs – muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA615 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

N, D and DK Packages



NOTE:
See back page for package dimensions

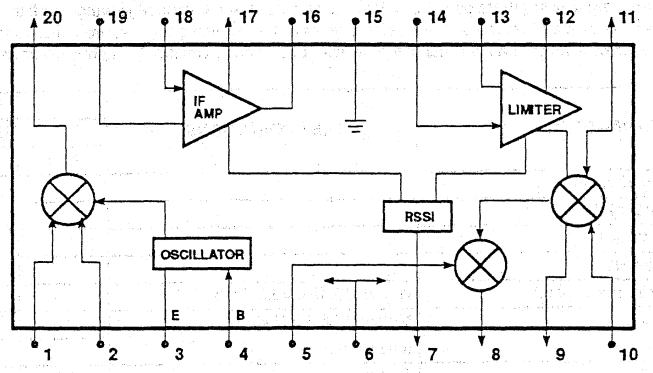
APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	0 to +70°C	NE615N	0408B
20-Pin Plastic DIP	–40 to +85°C	SA615N	0408B
20-Pin Plastic SOL	0 to +70°C	NE615D	0175D
20-Pin Plastic SOL	–40 to +85°C	SA615D	0175D
20-Pin Plastic SSOP	0 to +70°C	NE615DK	1563
20-Pin Plastic SSOP	–40 to +85°C	SA615DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		–65 to +150	°C
T_A	Operating ambient temperature range NE615		0 to +70	°C
		SA615	–40 to +85	°C
θ_{JA}	Thermal impedance	D package N package SSOP package	90 75 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA615			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain			5.7	7.4	mA
	Mute switch input threshold (ON)		1.7			V
	(OFF)				1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step–up; IF frequency = 455kHz; R17 = 5.1k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA615 MIN	LIMITS NE/SA615 TYP	LIMITS NE/SA615 MAX	UNITS
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.00; f2 = 45.06MHz		-12		dBm
	Conversion power gain	Matched 14.5dBV step-up	8.0	13		dB
		50Ω source		-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.50		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz	25	33	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	60	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		530		mV
	SINAD sensitivity	RF level -118dB		12		dB
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	800	mV
		IF level = -68dBm	1.7	2.5	3.3	V
		IF level = -18dBm	3.6	4.8	5.8	V
	RSSI range	R_9 = 100kΩ Pin 16		80		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±2		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ
RF/IF section (Int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA615 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of –10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to

100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

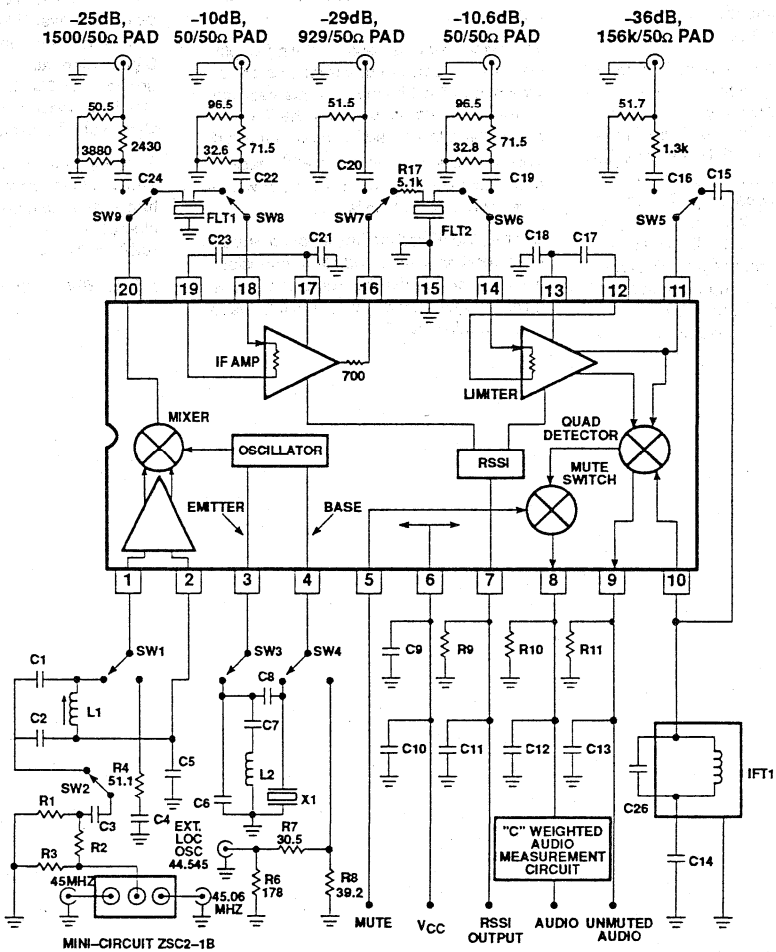
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

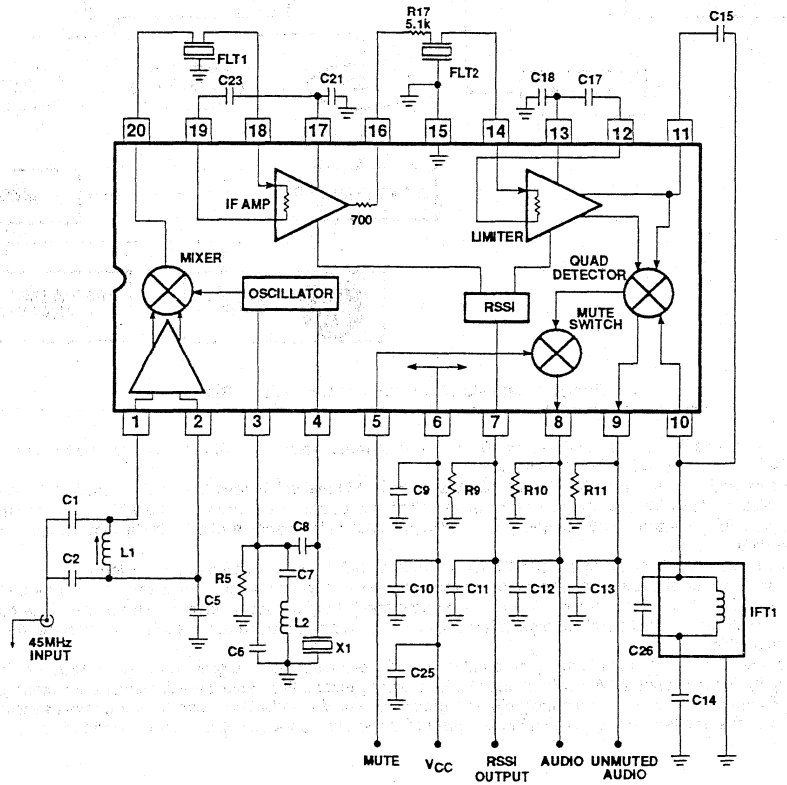


Automatic Test Circuit Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270µH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8µH TOKO 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA615 45MHz Test Circuit (Relays as shown)



NE/SA615N
Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270μH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8μH TOKO 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA615 45MHz Application Circuit

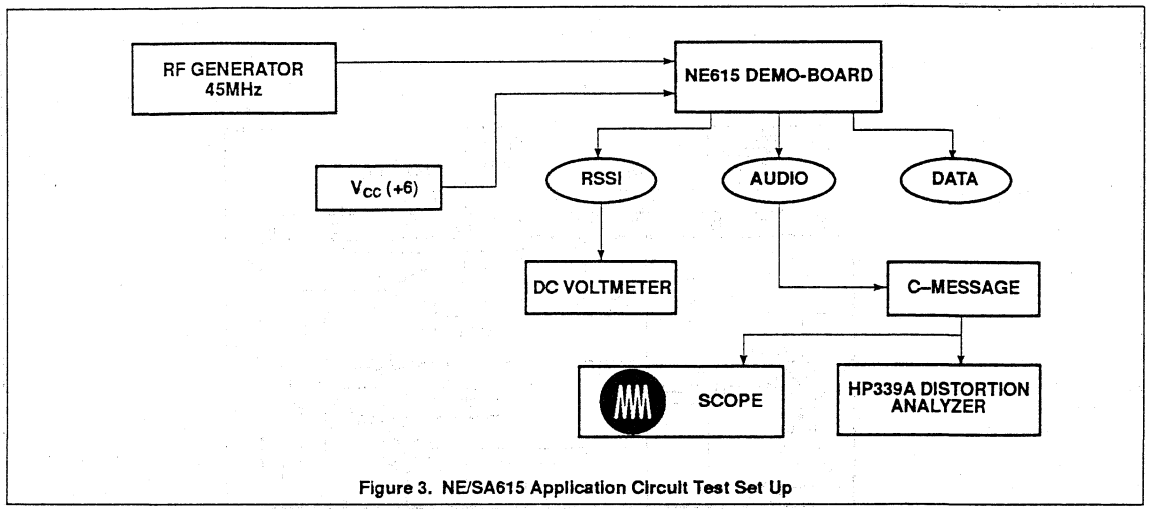


Figure 3. NE/SA615 Application Circuit Test Set Up

NOTES:
1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or –120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10–15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2–3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

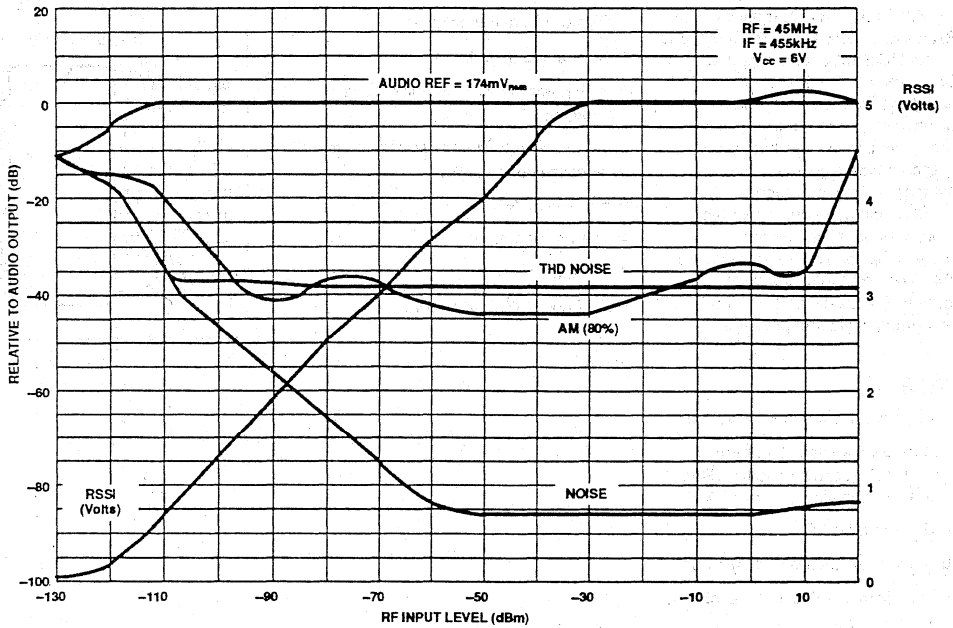


Figure 4. NE615 Application Board at 25°C

High performance low power FM IF system with high-speed RSSI

NE/SA624

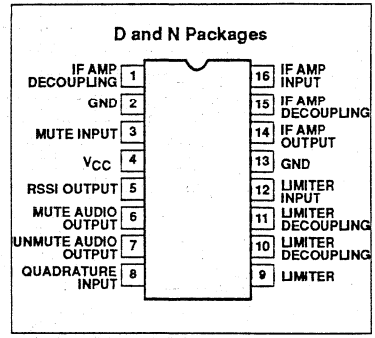
DESCRIPTION

The NE/SA624 is pin-to-pin compatible with the NE/SA604A, but has faster RSSI rise and fall time. The NE/SA624 is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA624 features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA624 is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

APPLICATIONS

- Digital cellular base station
- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

PIN CONFIGURATION



FEATURES

- Low power consumption: 3.4mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Fast RSSI rise and fall time
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA624 meets cellular radio specifications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic DIP	0 to +70°C	NE624N	0406C
16-Pin Plastic SO (Surface-mount)	0 to +70°C	NE624D	0005D
16-Pin Plastic DIP	-40 to +85°C	SA624N	0406C
16-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA624D	0005D

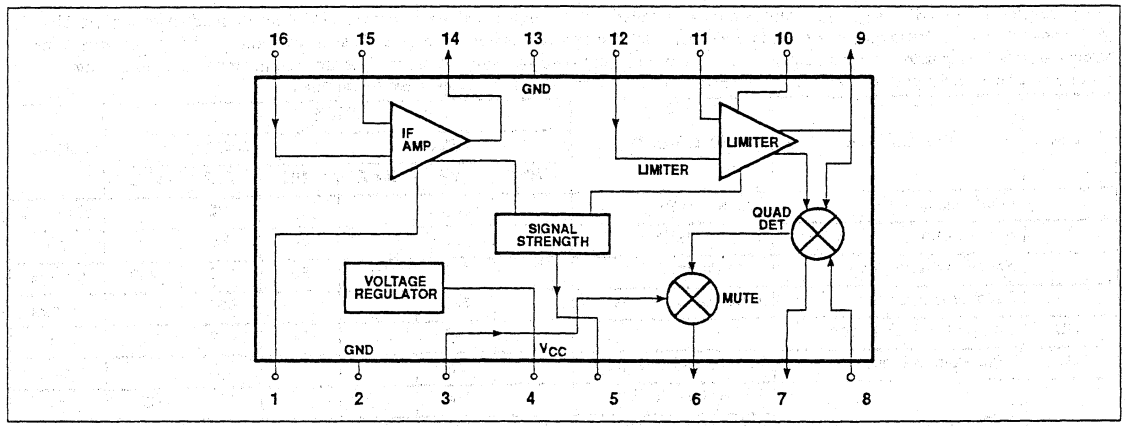
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE624 SA624	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

High performance low power FM IF system with high-speed RSSI

NE/SA624

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE624			SA624			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.4	4.2	2.5	3.4	4.2	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

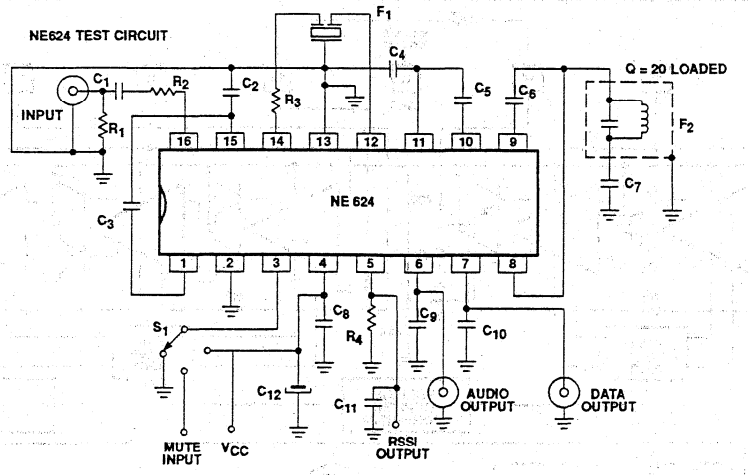
Typical reading at $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE624			SA624			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92			-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530			530		mV_{RMS}
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = -118dBm	0	160	550	0	160	650	mV
		RF level = -68dBm	2.0	2.65	3.0	1.9	2.65	3.1	V
		RF level = -18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI output rise time (10kHz pulse, no IF filter)	IF freq. = 455kHz							
		IF level = -44dBm		1.1			1.1		µs
		IF level = -16dBm		1.2			1.2		µs
		IF freq. = 10.7MHz							
		IF level = -44dBm		1.2			1.2		µs
		IF level = -16dBm		1.1			1.1		µs
	RSSI output fall time (10kHz pulse, no IF filter)	IF freq. = 455kHz							
		IF level = -44dBm		1.3			1.3		µs
		IF level = -16dBm		4.7			4.7		µs
		IF freq. = 10.7MHz							
		IF level = -44dBm		1.6			1.6		µs
		IF level = -16dBm		4.2			4.2		µs
	RSSI range	R_4 = 100k (Pin 5)		90			90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Limiter output impedance			300			300		Ω
	Limiter output level no load			280			280		mV_{RMS}
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

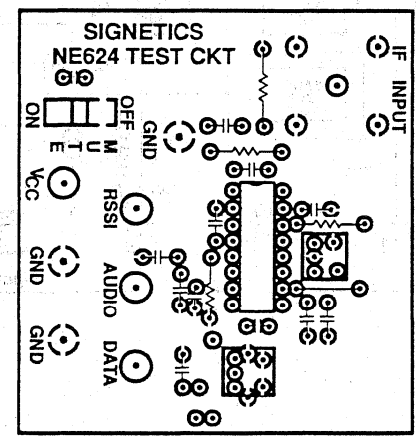
NOTE:

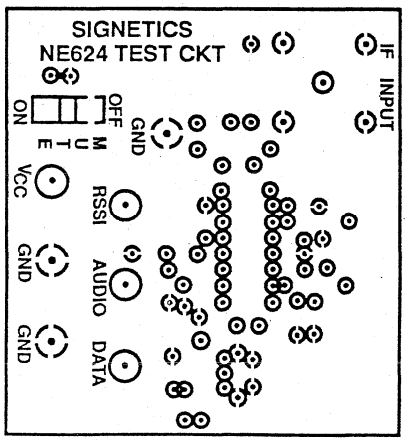
1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE604 (50)	NE624 (1.5k)/NE605 (1.5k)
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF ±10% 50V
C3	100nF ±10% 50V
C4	100nF ±10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





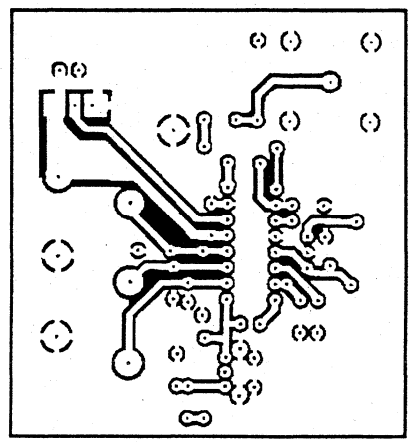


Figure 1. NE/SA624 Test Circuit

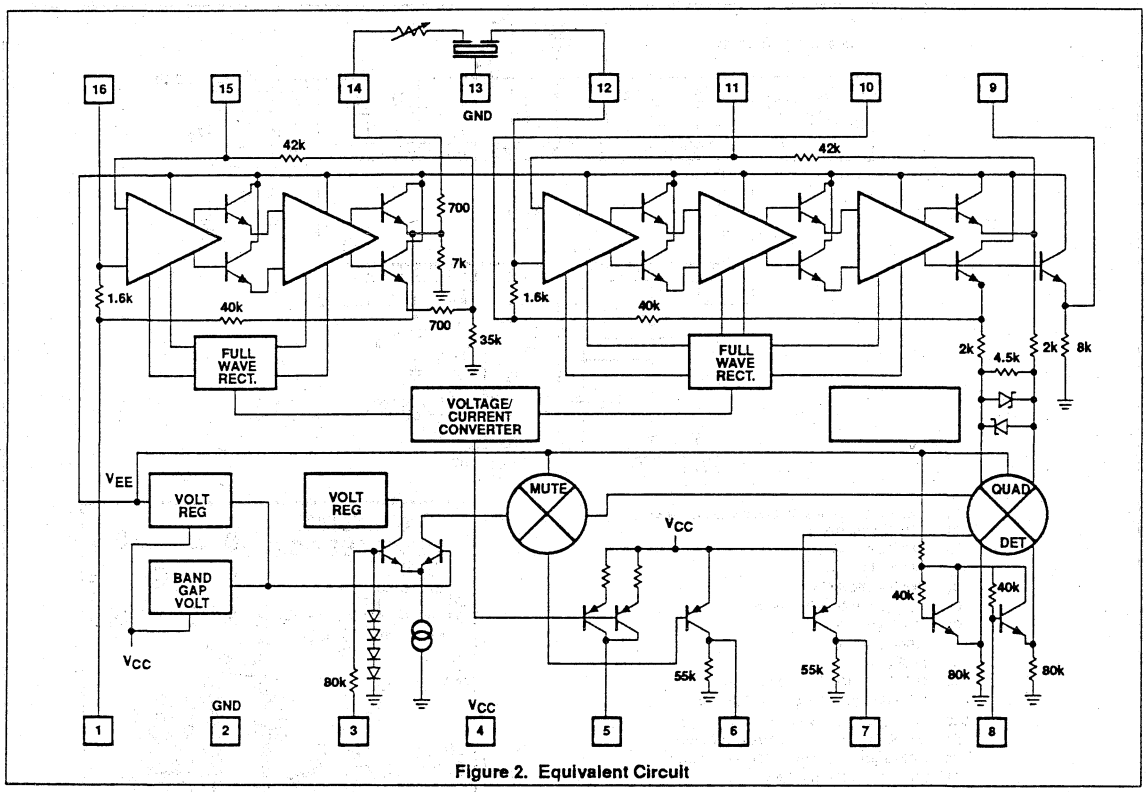


Figure 2. Equivalent Circuit

High performance low power FM IF system with high-speed RSSI

NE/SA624

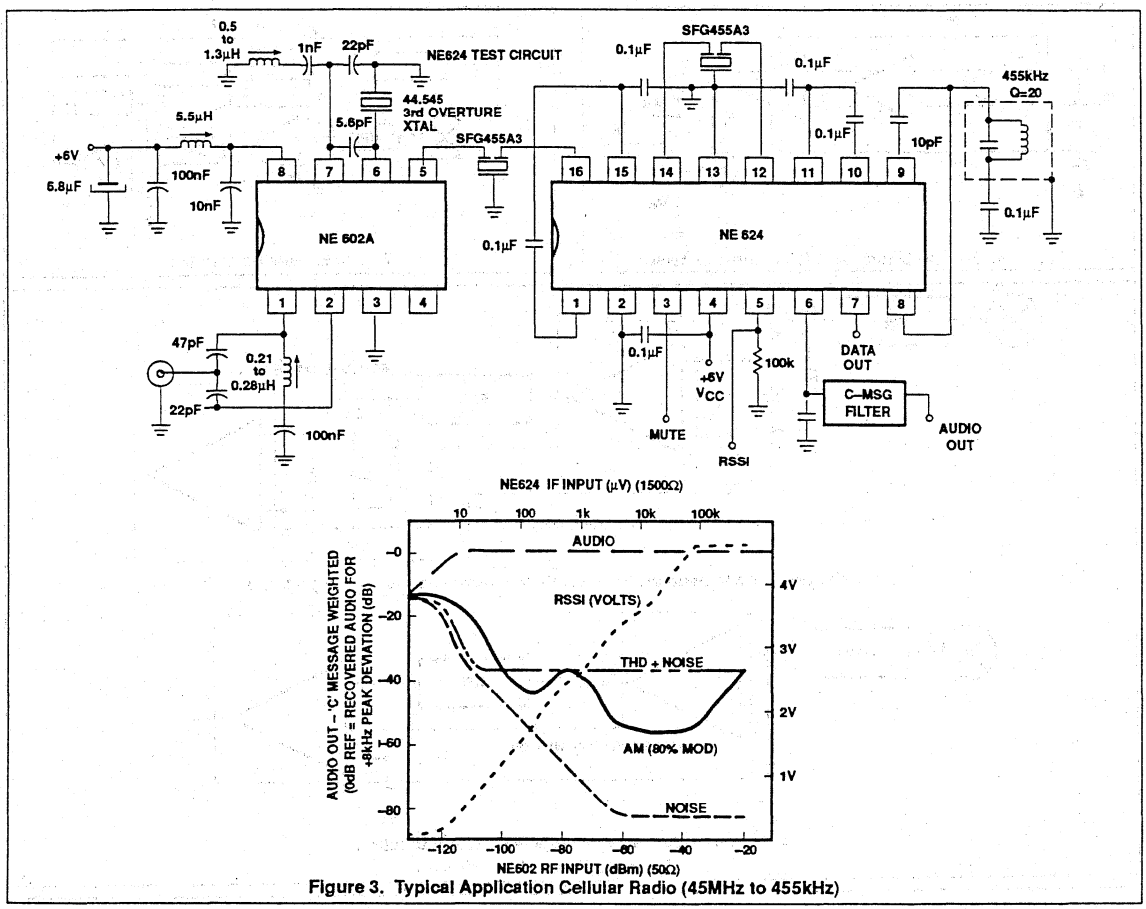


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA624 is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA624 cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA624 is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

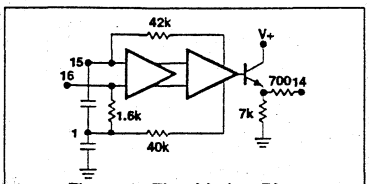


Figure 4. First Limiter Bias

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields)

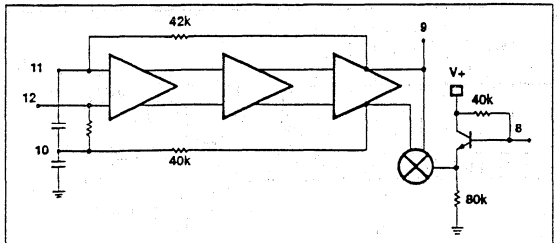


Figure 5. Second Limiter and Quadrature Detector

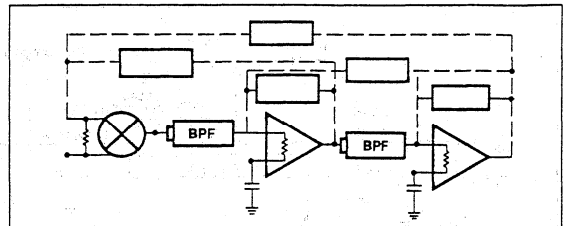
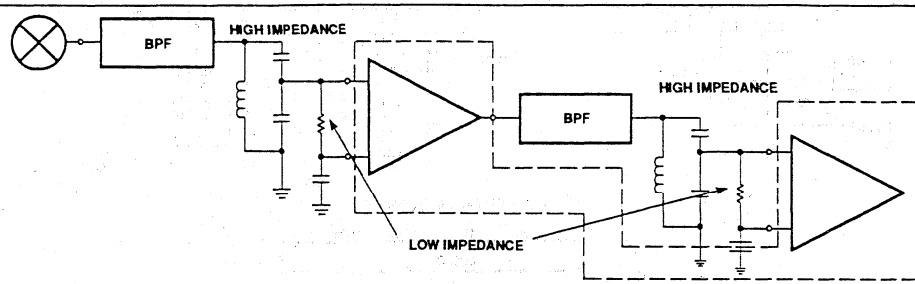
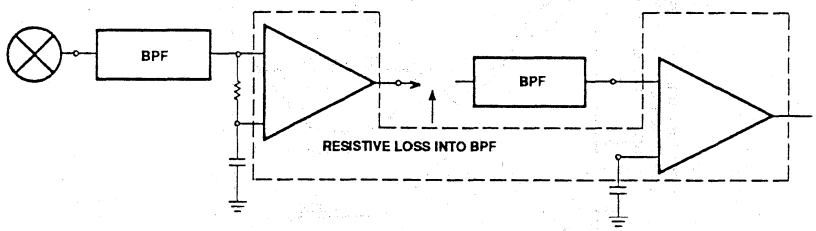


Figure 6. Feedback Paths



a. Terminating High Impedance Filters with Transformation to Low Impedance



b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

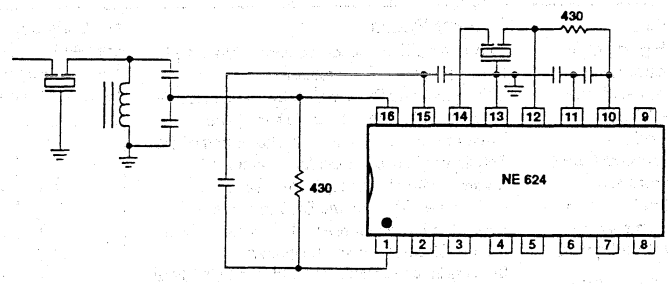


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in

Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE624 IF amplifiers, which is not specified, is low phase shift. The NE624 is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

Stability Considerations

The high gain and bandwidth of the NE624 in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE624 quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE624

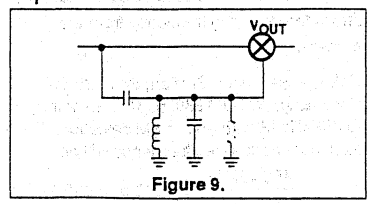


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1 \omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

$$\text{If } V_{IN} = A \sin \omega t \Rightarrow V_O = A \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (3)$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (4)$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega_1}{\omega} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5kHz}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) ⇒ Choose a Q = 20

The internal R of the 624 is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174pF$ and L = 0.7mH.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a C_S = 10pF and C_P = 164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of C_S = 1pF is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE624 demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE624 are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

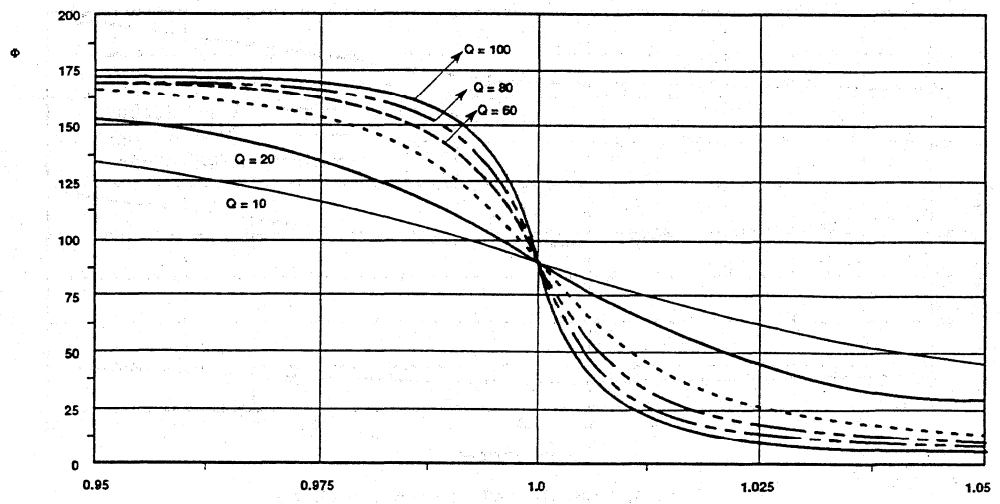


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

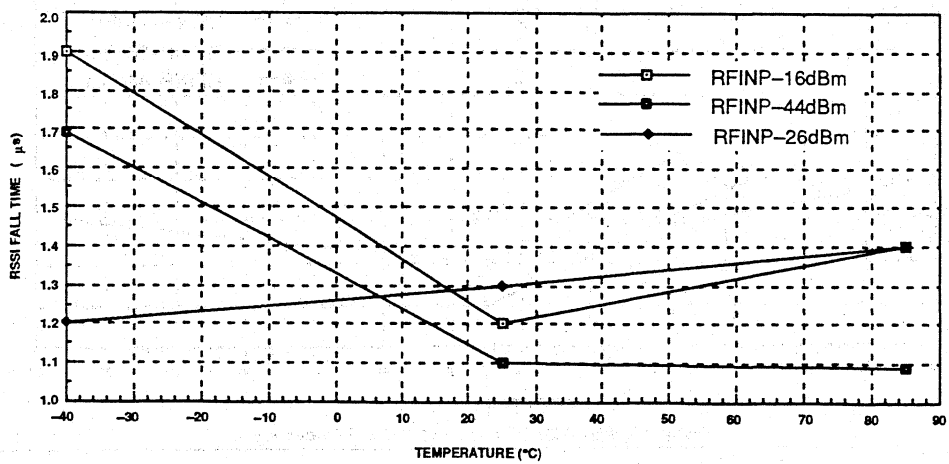


Figure 11. NE/SA624 Rise Time 455kHz IF Frequency

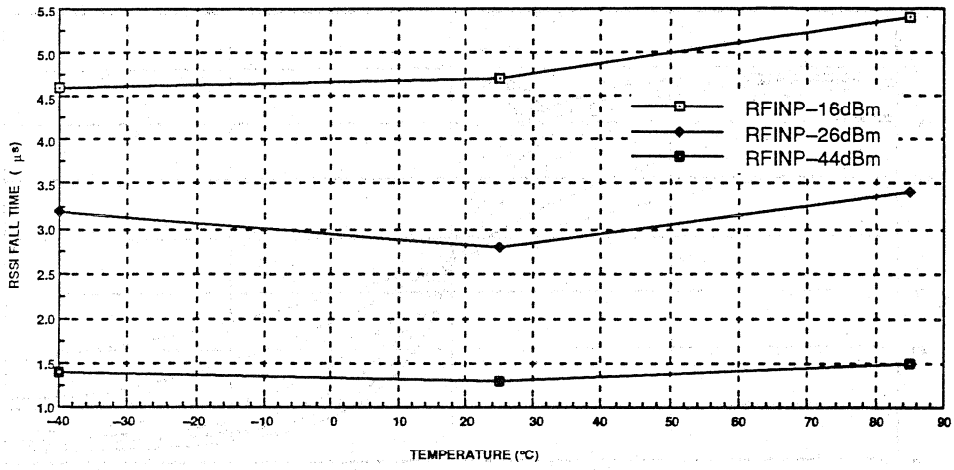


Figure 12. NE/SA624 Fall Time 455kHz IF Frequency

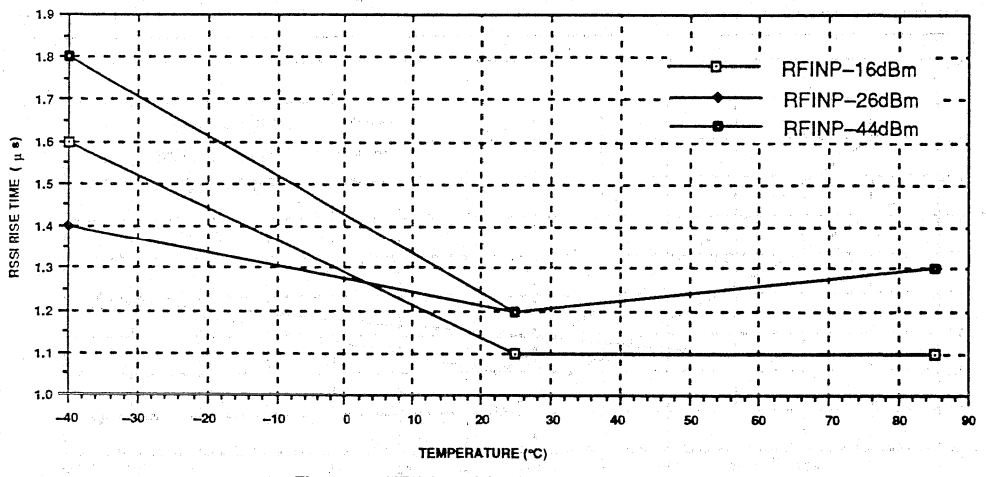


Figure 13. NE/SA624 Rise Time 10.7MHz IF Frequency

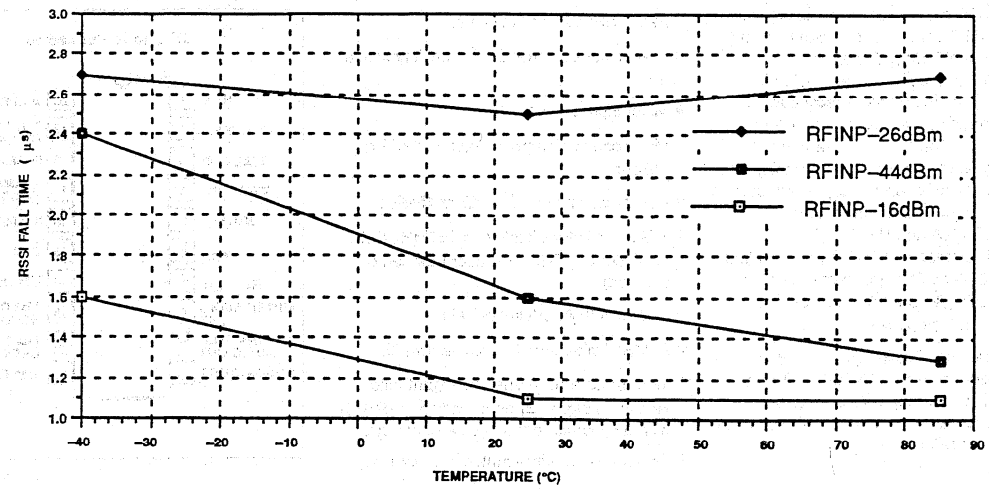


Figure 14. NE/SA624 Fall Time 10.7MHz IF Frequency

High performance low power mixer FM IF system with high-speed RSSI

NE/SA625

DESCRIPTION

The NE/SA625 is pin-to-pin compatible with the NE/SA605, but has faster RSSI rise and fall times. The NE/SA625 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI) with fast rise and fall time, and voltage regulator. The NE/SA625 combines the functions of Signetics' NE602A and NE624. The NE/SA625 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

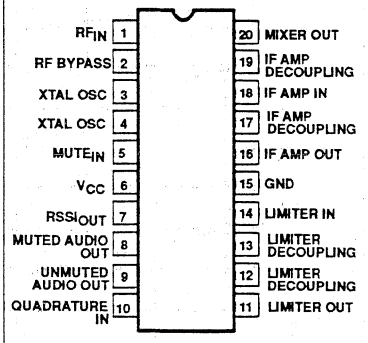
For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product and artwork for reference.

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 5.8mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA625 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

D, DK and N Packages



APPLICATIONS

- Digital cellular base stations
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification
- Digital cordless telephones

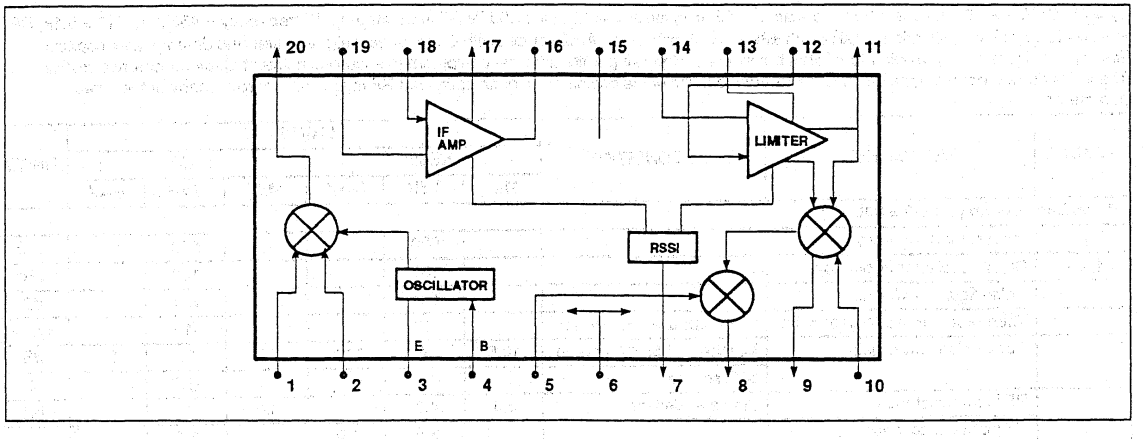
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	0 to +70°C	NE625N	0408B
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE625D	0172D
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE625DK	1563
20-Pin Plastic DIP	-40 to +85°C	SA625N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA625D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA625DK	1563

High performance low power mixer FM IF system with high-speed RSSI

NE/SA625

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range NE625		0 to +70	°C
		SA625	-40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W
		DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.8	6.7	4.55	5.8	6.75	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480			480		mV
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	IF RSSI output rise time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.2			1.2		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.1			1.1		µs
	IF RSSI output fall time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		2.1			2.1		µs
		RF level = -28dBm		7.6			7.6		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		2.0			2.0		µs
		RF level = -28dBm		7.3			7.3		µs
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		1.40	1.6		kΩ
	Limiter output impedance			300			300		Ω
	Limiter output level with no load			280			280		mV_{RMS}

AC ELECTRICAL CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
IF section (continued)									
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ
RF/IF section (Int LO)									
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450			450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA625 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA625 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA625 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

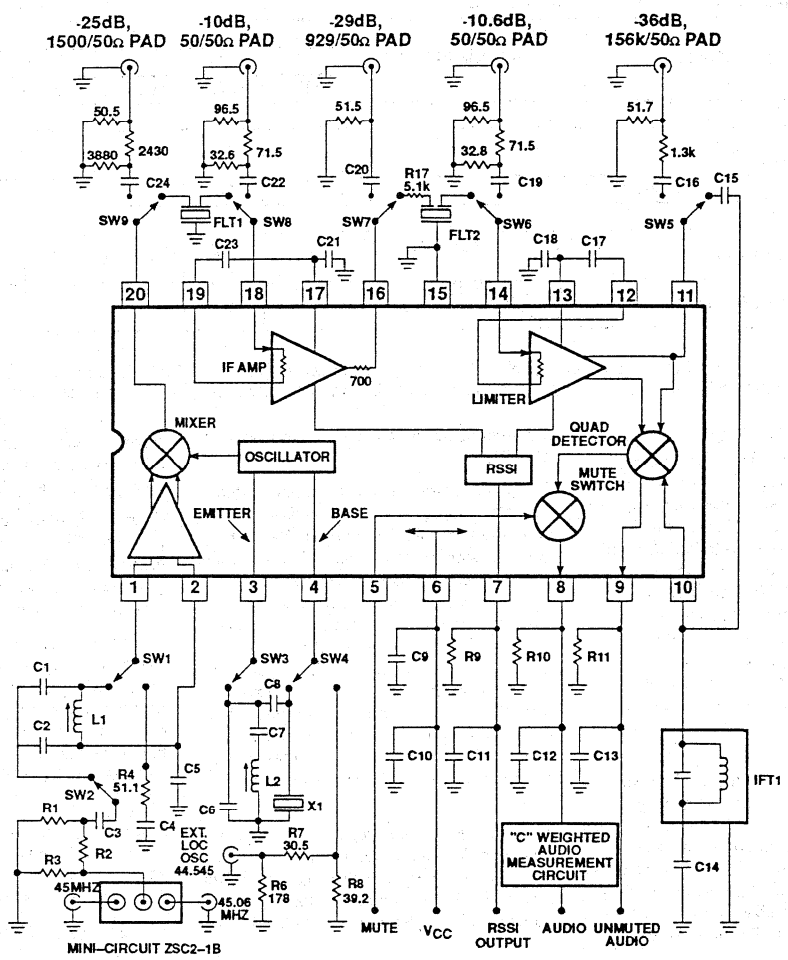
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

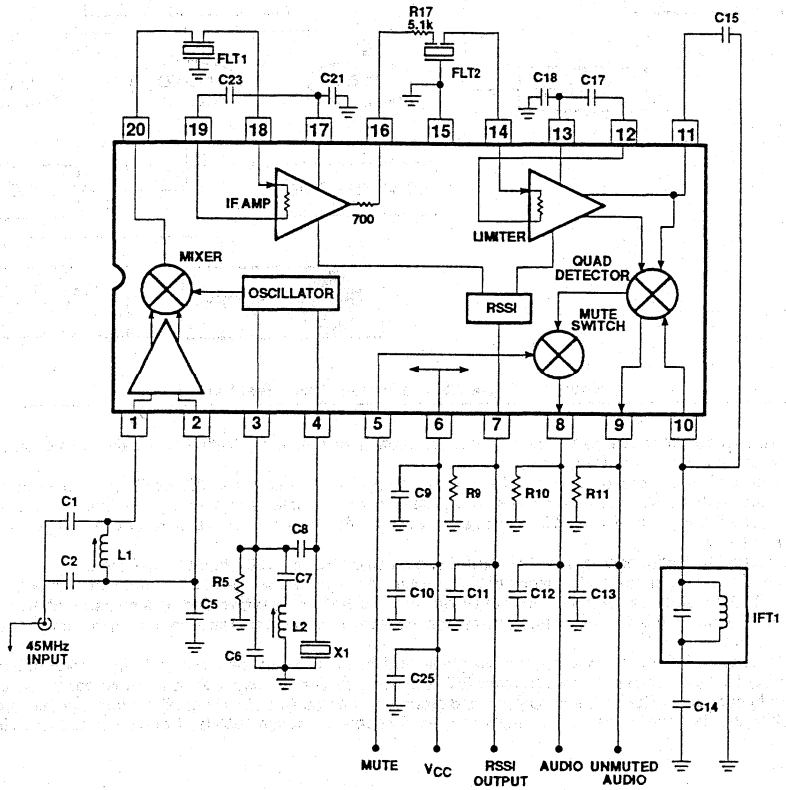


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA625 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8µH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA625 45MHz Application Circuit

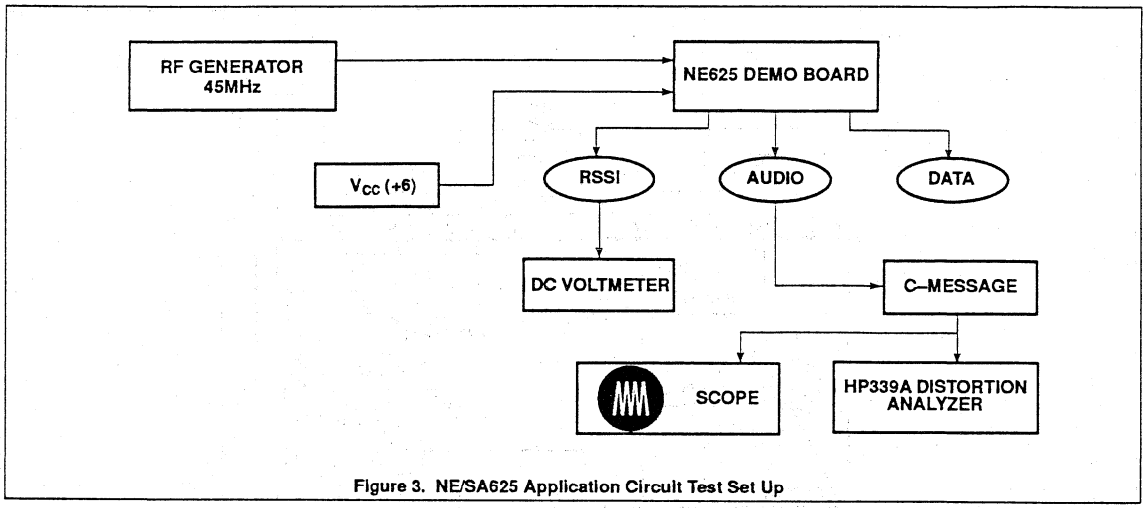


Figure 3. NE/SA625 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

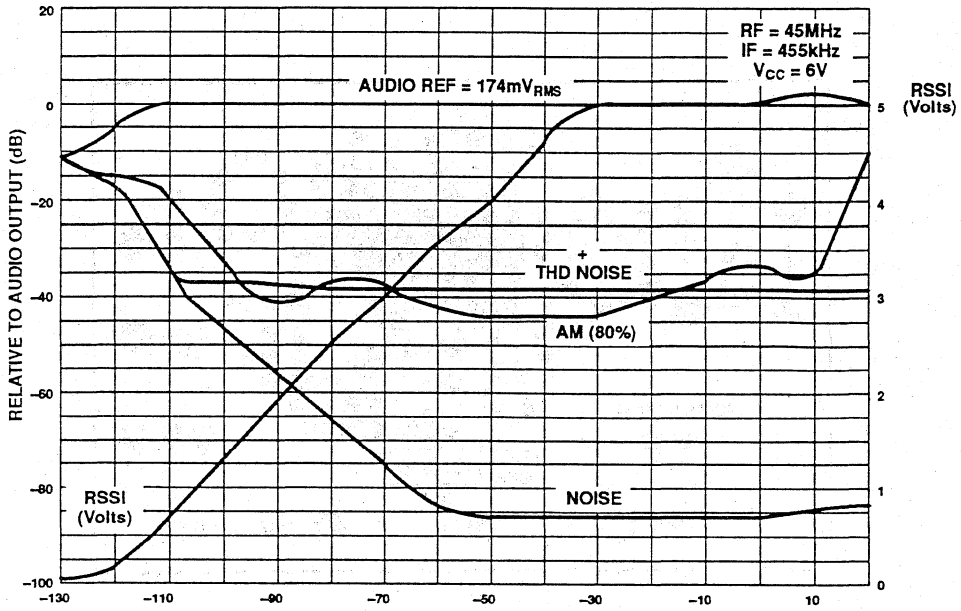


Figure 4. NE625 Application Board at 25°C

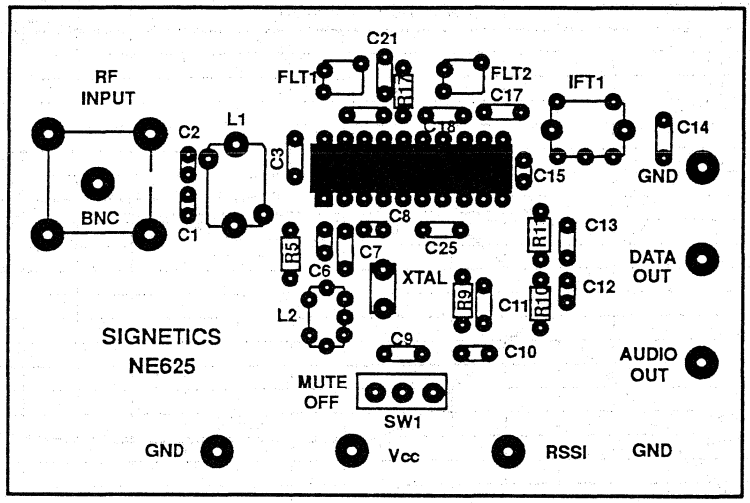
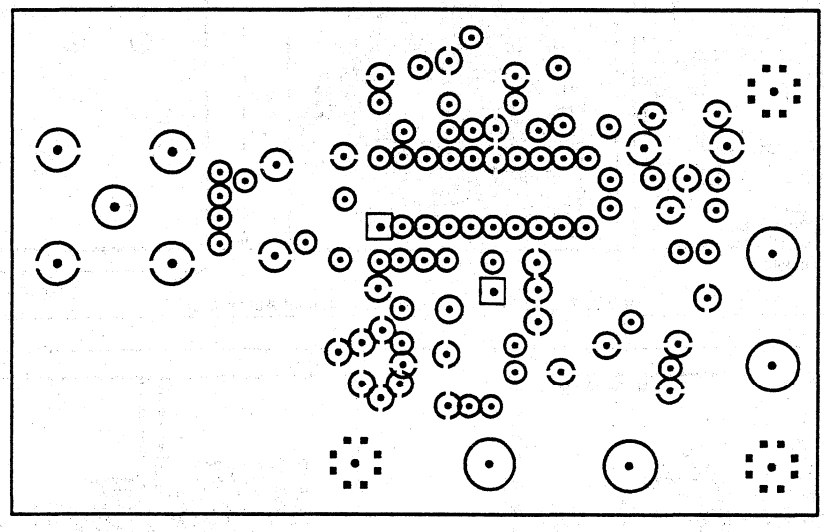
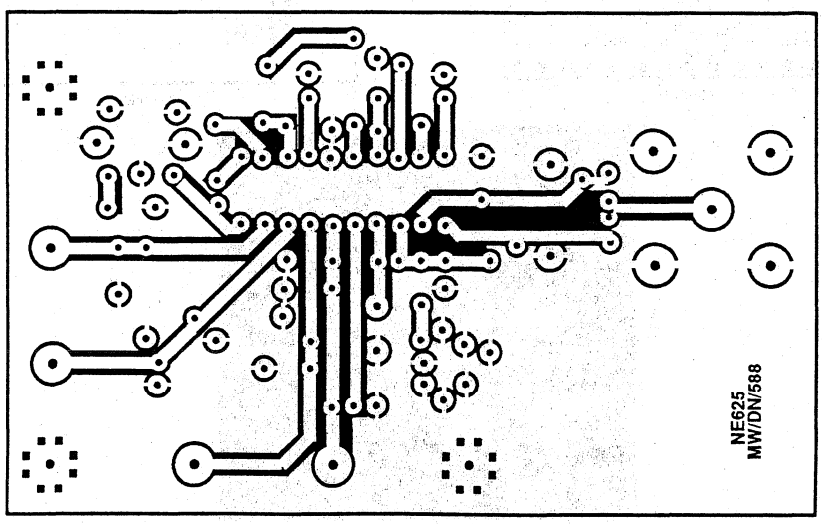


Figure 5. Component Placement for NE625 Application Circuit



TOP VIEW



BOTTOM VIEW

Figure 6. Layout for NE/SA625 Application Board

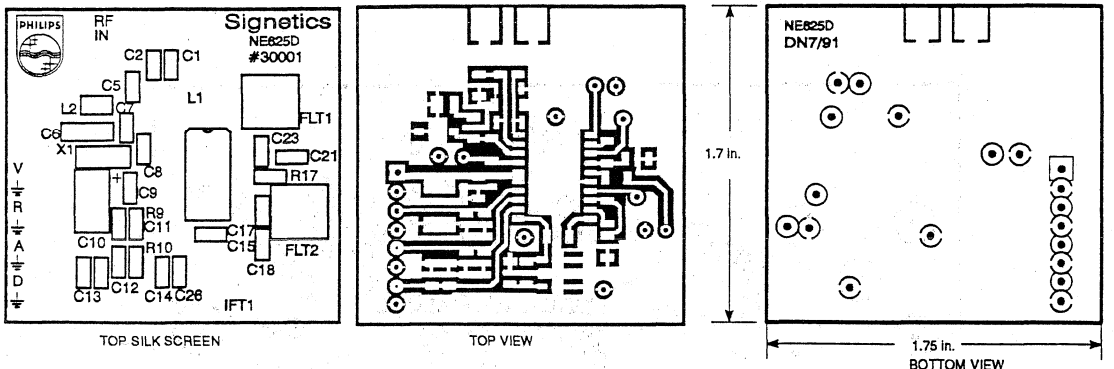


Figure 7. NE625 SO Demo-board Layout (Not Actual Size)

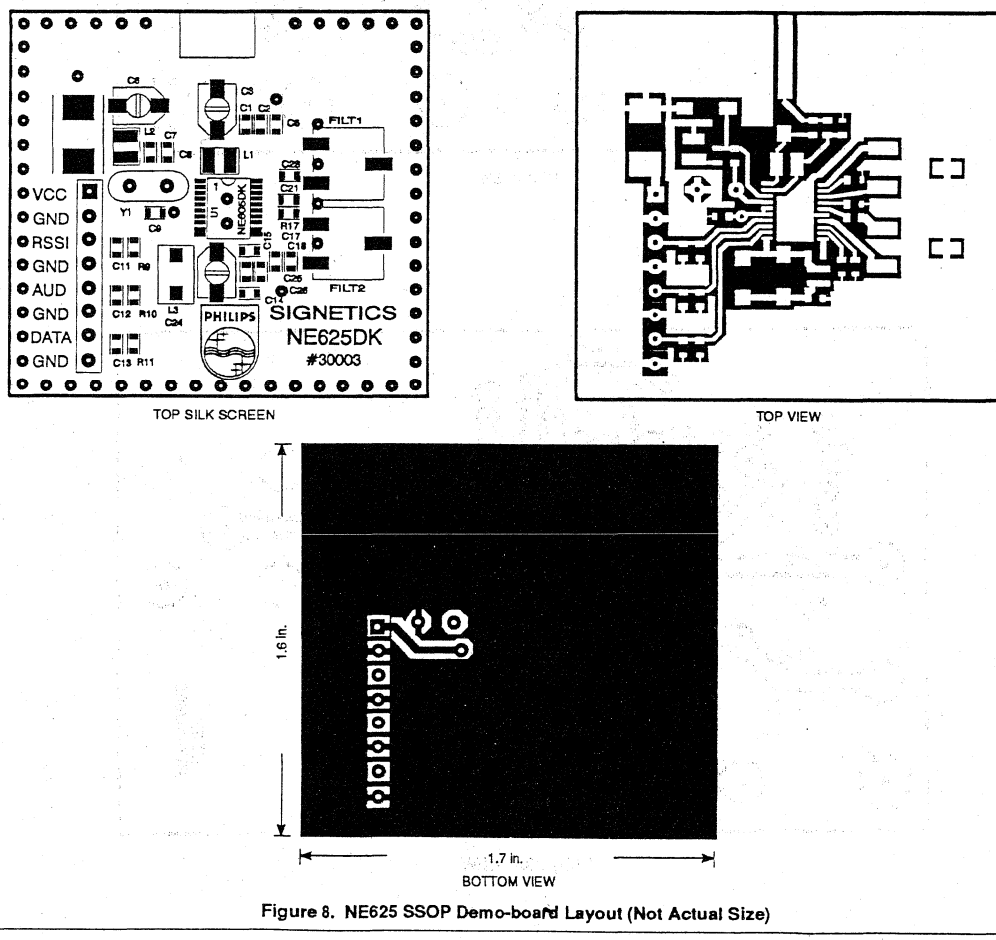


Figure 8. NE625 SSOP Demo-board Layout (Not Actual Size)

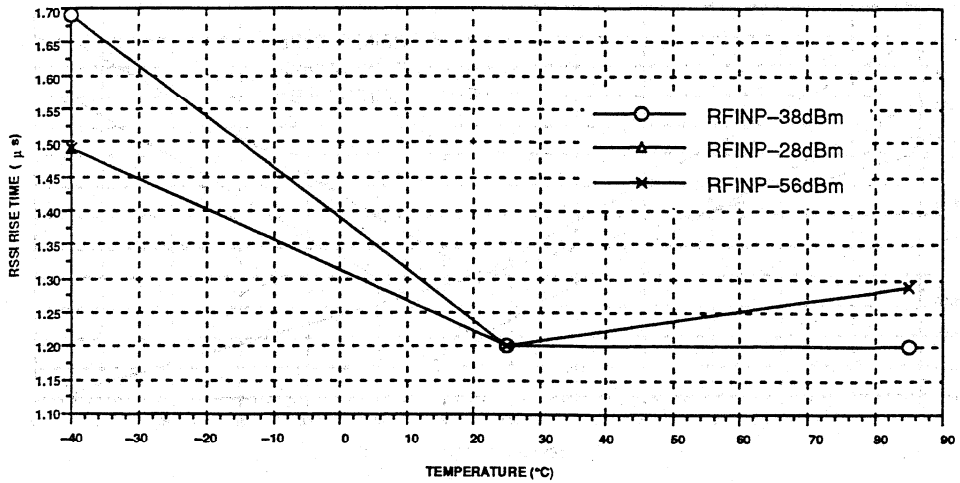


Figure 9. NE/SA625 Rise Time 455kHz IF Frequency

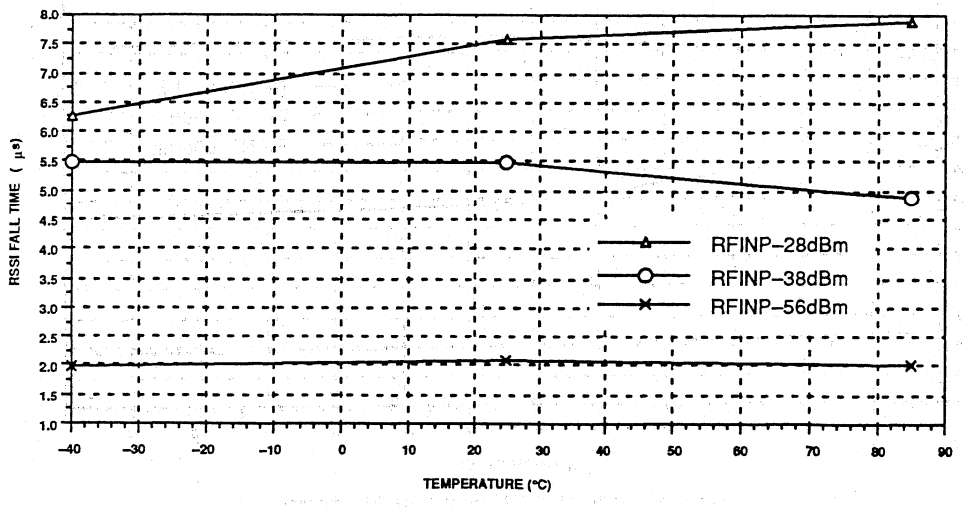


Figure 10. NE/SA625 Fall Time 455kHz IF Frequency

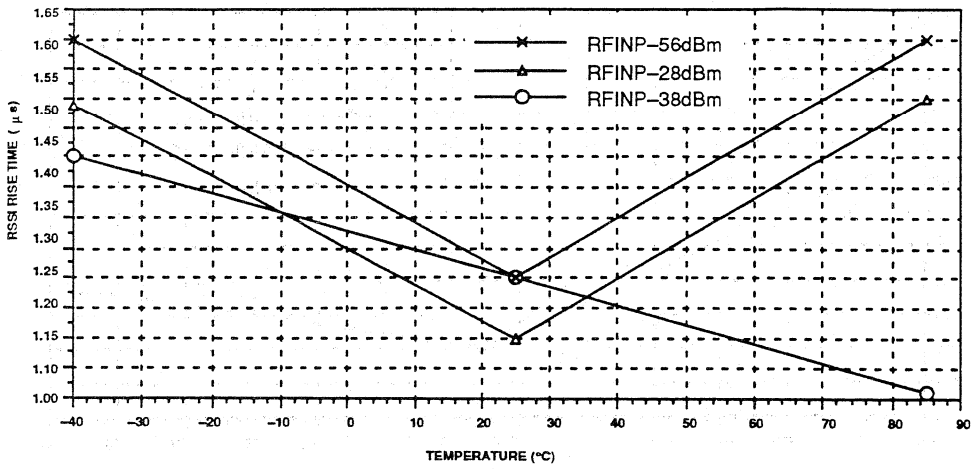


Figure 11. NE/SA625 Rise Time 10.7MHz IF Frequency

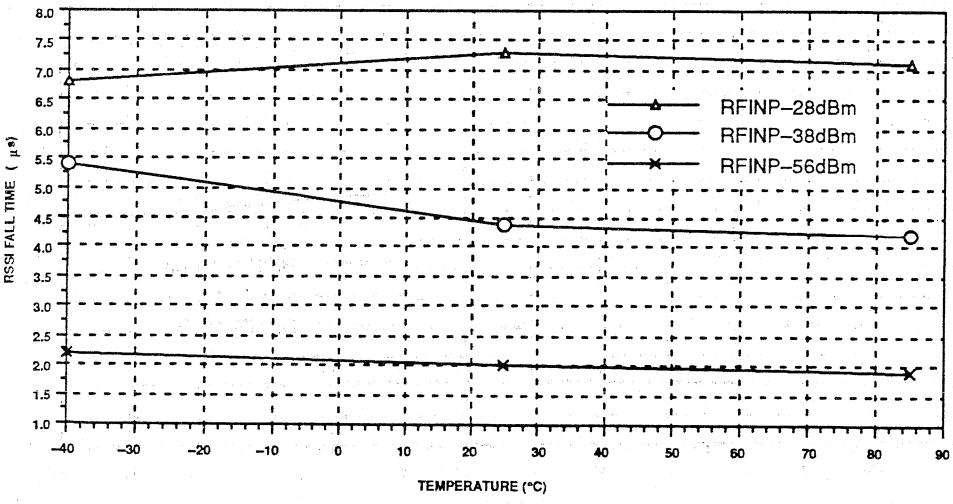


Figure 12. NE/SA625 Fall Time 10.7MHz IF Frequency

High performance low power mixer FM IF system with high-speed RSSI

NE/SA627

DESCRIPTION

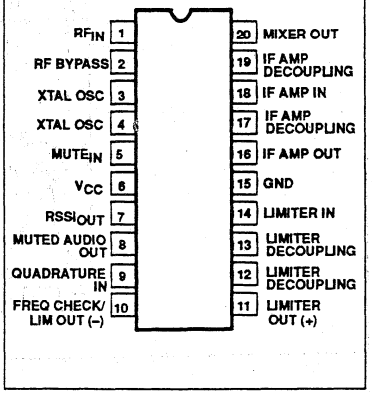
The NE/SA627 has faster RSSI rise and fall times. The NE/SA627 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI) with fast rise and fall time, voltage regulator and frequency check/limiter out (–). The NE/SA627 also has an extra limiter output. This signal is buffered from the output of the limiter and provides a negative (–) limiter output. This can be used to provide a frequency check function. The NE/SA627 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 5.8mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Audio output - mutable
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA627 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

D, DK and N Packages



APPLICATIONS

- Digital cellular base stations
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification
- Digital cordless telephones

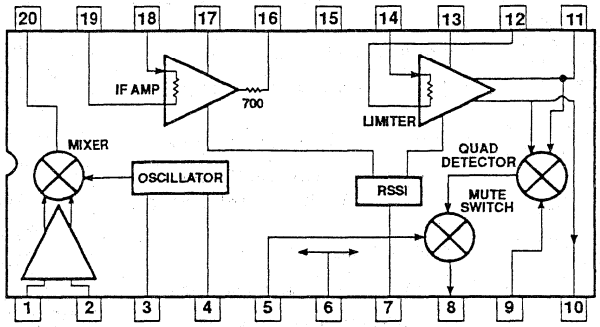
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	0 to +70°C	NE627N	0408B
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE627D	0172D
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE627DK	1563
20-Pin Plastic DIP	-40 to +85°C	SA627N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA627D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA627DK	1563

High performance low power mixer FM IF system with high-speed RSSI

NE/SA627

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range NE627		0 to +70	°C
		SA627	-40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W
		DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.8	6.7	4.55	5.8	6.75	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	IF RSSI output rise time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.2			1.2		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.1			1.1		µs
	IF RSSI output fall time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		2.1			2.1		µs
		RF level = -28dBm		7.6			7.6		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		2.0			2.0		µs
		RF level = -28dBm		7.3			7.3		µs
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		1.40	1.6		kΩ
	Limiter output impedance	Pin 10 or 11		300			300		Ω
	Limiter output level	Pin 10 or 11 with no load 3kΩ load (min)		280 250			280 250		mV_{RMS}

AC ELECTRICAL CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
IF section (continued)									
	Muted audio output resistance			58			58		kΩ
RF/IF section (int LO)									
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA627 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA627 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA627 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

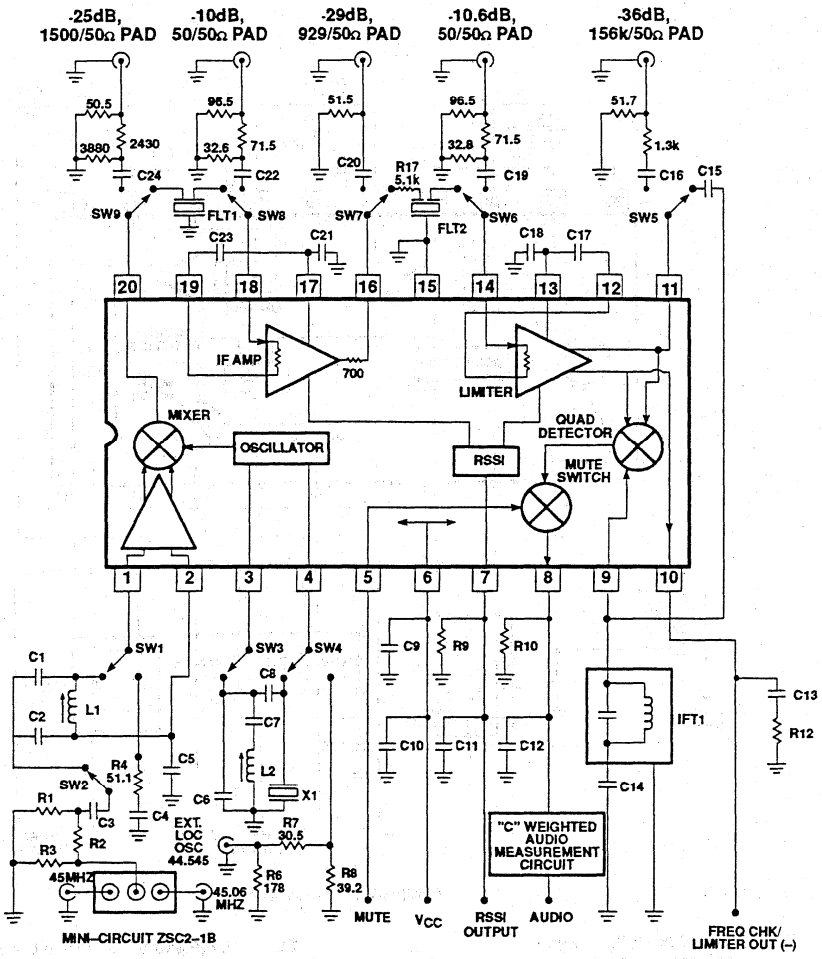
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}

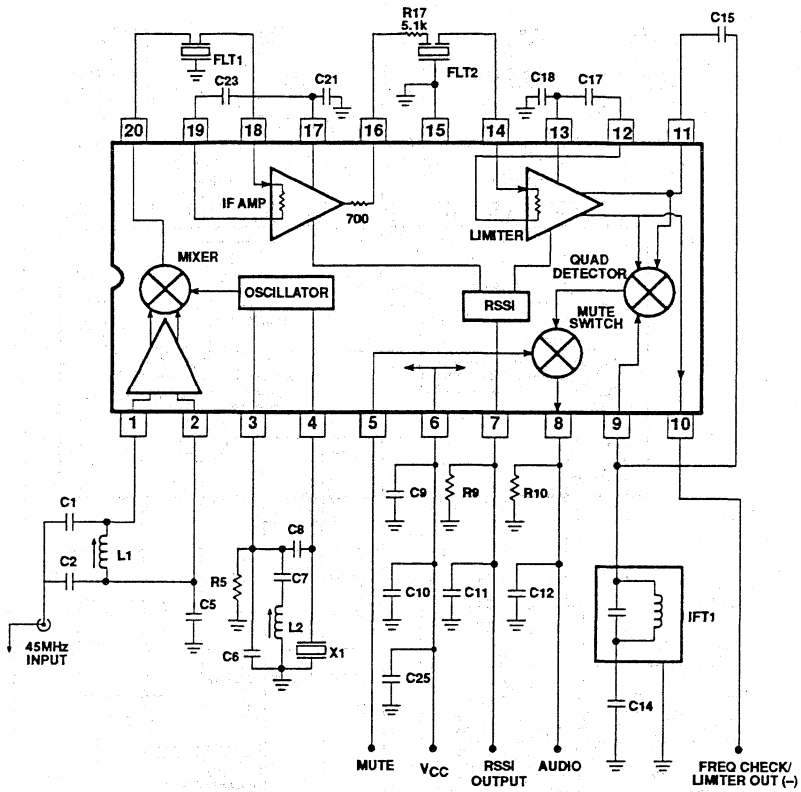


Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C9	100nF ±10% Monolithic Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C10	10μF Tantalum (minimum)	L2	0.8μH nominal Toko 292CNS–T1038Z
C11	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C12	15nF ±10% Ceramic	R9	100k ±1% 1/4W Metal Film
C13	0.1μF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C14	100nF ±10% Monolithic Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C15	10pF NPO Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R12	3kΩ ±5% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA627 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA627 45MHz Application Circuit

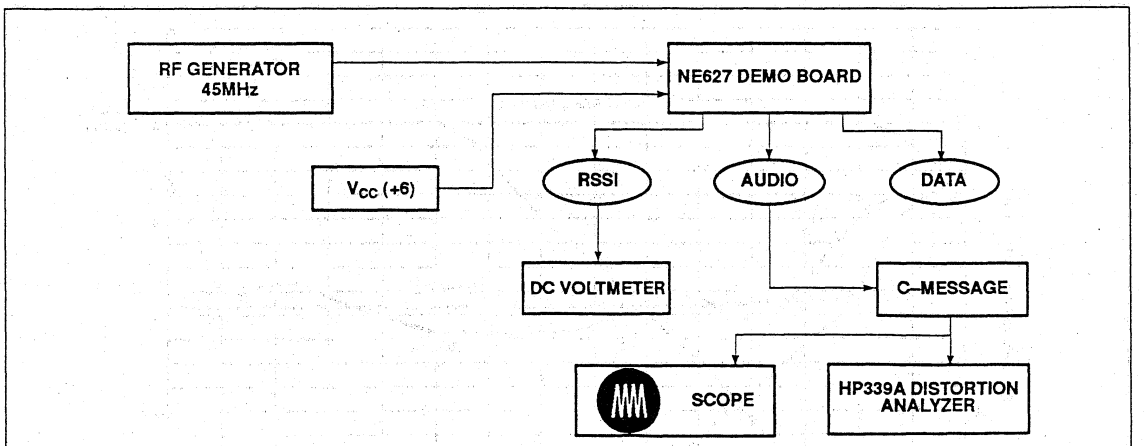


Figure 3. NE/SA627 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

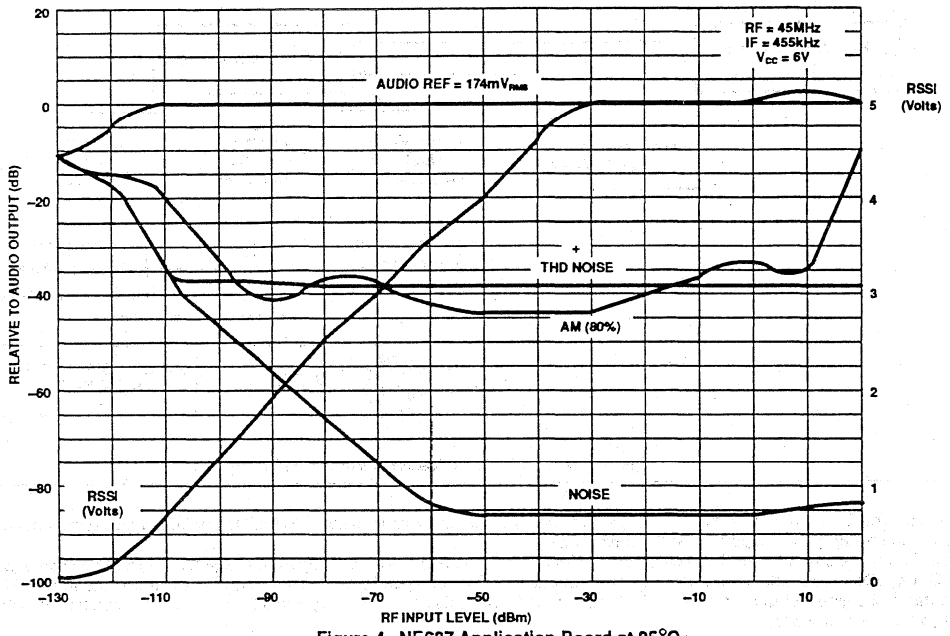


Figure 4. NE627 Application Board at 25°C

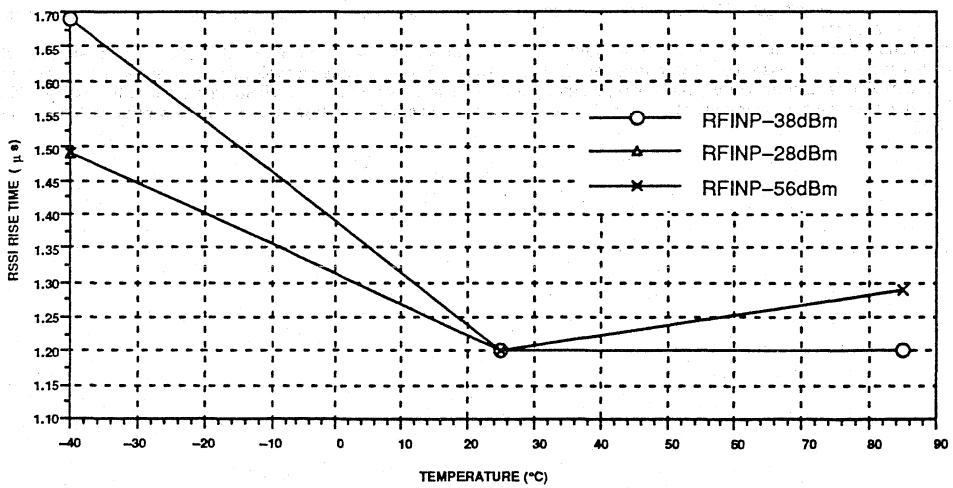


Figure 5. NE/SA627 Rise Time 455kHz IF Frequency

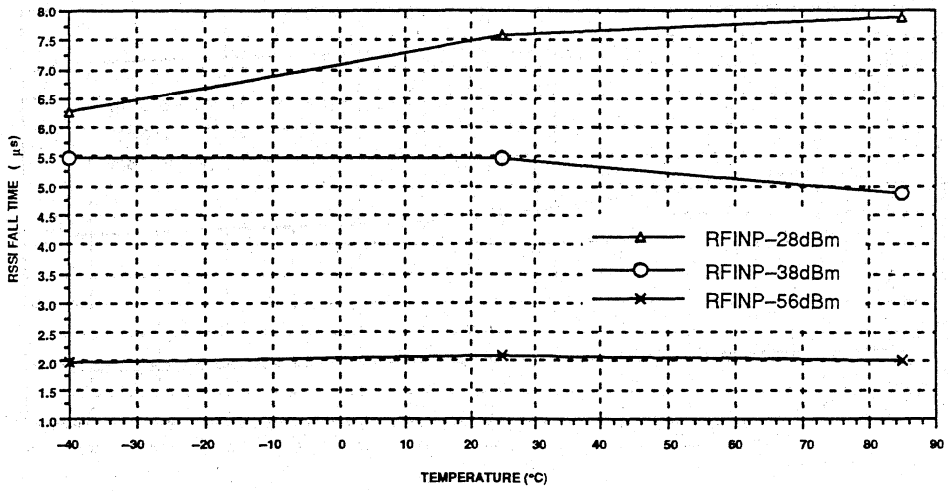


Figure 6. NE/SA627 Fall Time 455kHz IF Frequency

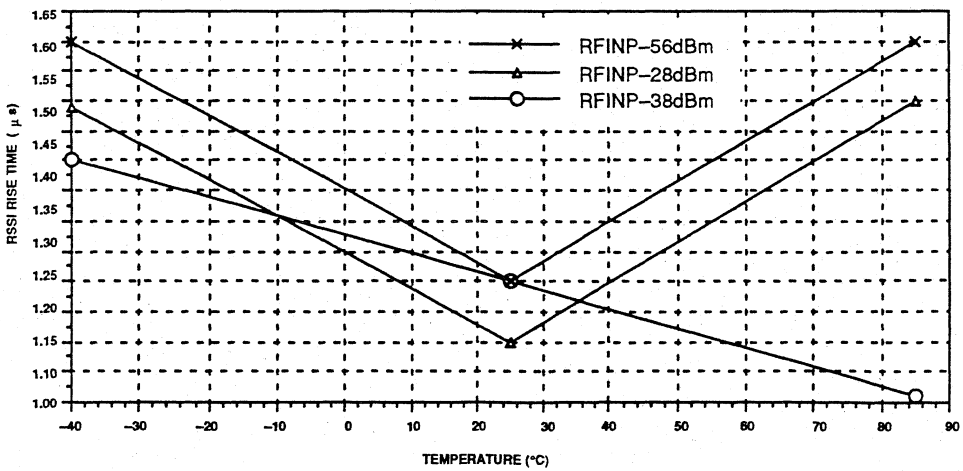


Figure 7. NE/SA627 Rise Time 10.7MHz IF Frequency

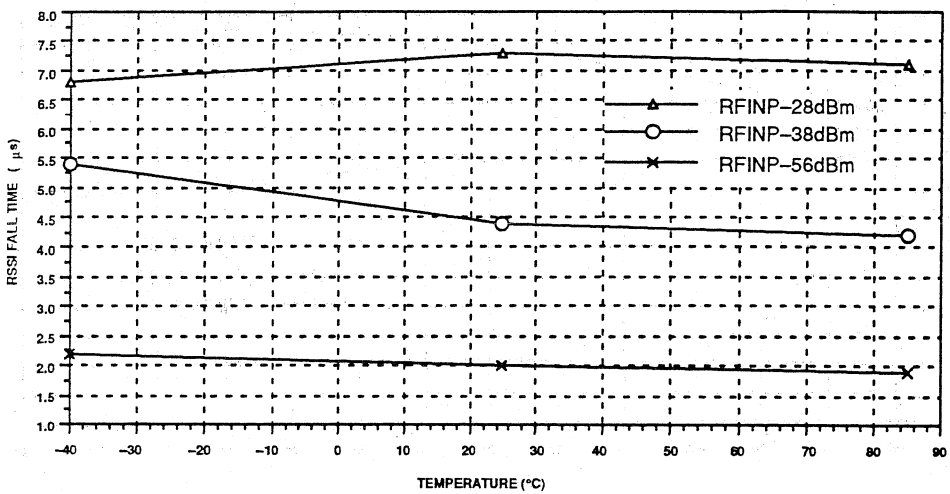


Figure 8. NE/SA627 Fall Time 10.7MHz IF Frequency

Single pole double throw (SPDT) switch

NE/SA630

DESCRIPTION

The NE630 is a wideband RF switch fabricated in BiCMOS technology and incorporating on-chip CMOS/TTL compatible drivers. Its primary function is to switch signals in the frequency range DC - 1GHz from one 50Ω channel to another. The switch is activated by a CMOS/TTL compatible signal applied to the enable channel 1 pin (ENCH1).

The extremely low current consumption makes the NE/SA630 ideal for portable applications. The excellent isolation and low loss makes this a suitable replacement for PIN diodes.

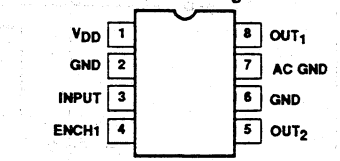
The NE/SA630 is available in an 8-pin dual in-line plastic package and an 8-pin SO (surface mounted miniature) package.

FEATURES

- Wideband (DC - 1GHz)
- Low through loss (1dB typical at 200MHz)
- Unused input is terminated internally in 50Ω
- Excellent overload capability (1dB gain compression point +18dBm at 300MHz)
- Low DC power (170μA from 5V supply)
- Fast switching (20ns typical)
- Good isolation (off channel isolation 60dB at 100MHz)
- Low distortion (IP_3 intercept +33dBm)
- Good 50Ω match (return loss 18dB at 400MHz)
- Full ESD protection
- Bidirectional operation

PIN CONFIGURATION

D and N Packages



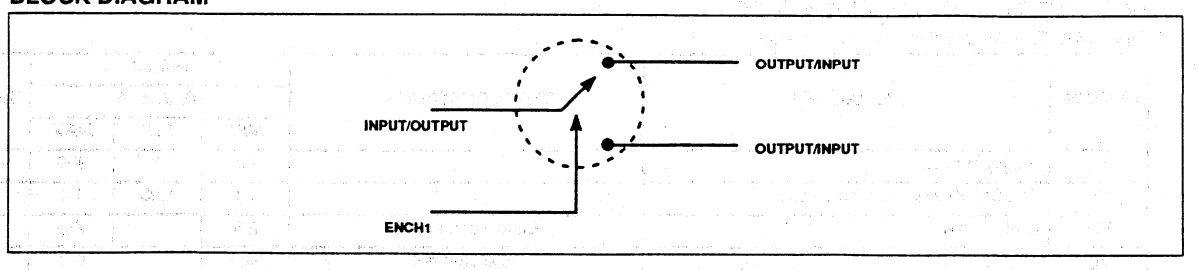
APPLICATIONS

- Digital transceiver front-end switch
- Antenna switch
- Filter selection
- Video switch
- FSK transmitter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to 70°C	NE630N
8-Pin Plastic SO (Surface-mount)	0 to 70°C	NE630D
8-Pin Plastic DIP	-40 to +85°C	SA630N
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA630D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	-0.5 to +5.5	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 8-Pin Plastic DIP 8-Pin Plastic SO	 1160 780	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	-65 to +150	°C

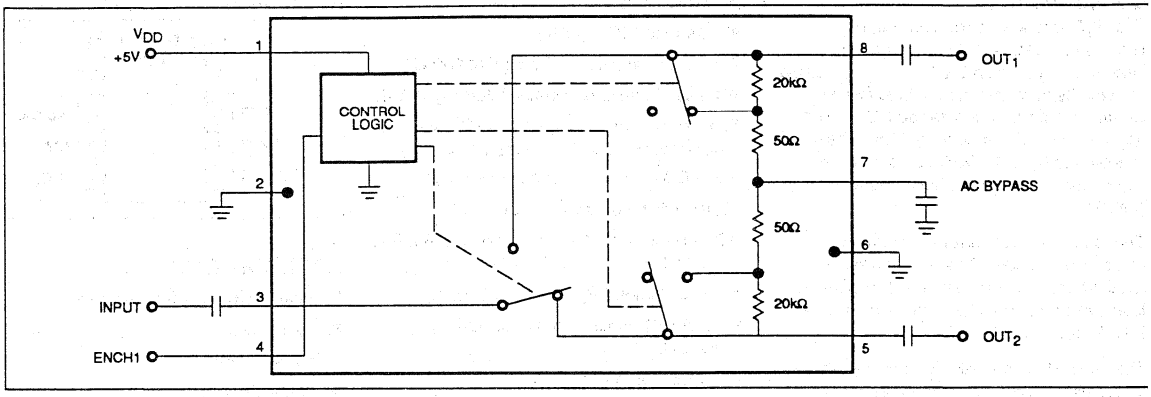
NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin DIP: θ_{JA} = 108°C/W
   8-Pin SO: θ_{JA} = 158°C/W

Single pole double throw (SPDT) switch

NE/SA630

EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	3.0 to 5.5V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			U
			NE/SA630			
			MIN	TYP	MAX	
I_{DD}	Supply current		40	170	300	
V_T	TTL/CMOS logic threshold voltage[1]		1.1	1.25	1.4	
V_{IH}	Logic 1 level	Enable channel 1	2.0		V_{DD}	
V_{IL}	Logic 0 level	Enable channel 2	-0.3		0.8	
I_{IL}	ENCH1 input current	ENCH1 = 0.4V	-1	0	1	
I_{IH}	ENCH1 input current	ENCH1 = 2.4V	-1	0	1	

NOTE:
1. The ENCH1 input must be connected to a valid Logic Level for proper operation of the NE/SA630.

AC ELECTRICAL CHARACTERISTICS[1] - D PACKAGE

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA630 MIN	LIMITS NE/SA630 TYP	LIMITS NE/SA630 MAX	UNITS
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2	 2.8	dB
S_{21}, S_{12}	Isolation (OFF channel)[2]	10MHz 100MHz 500MHz 900MHz	70 24	80 60 50 30		dB
S_{11}, S_{22}	Return loss (ON channel)	DC - 400MHz 900MHz		20 12		dB
S_{11}, S_{22}	Return loss (OFF channel)	DC - 400MHz 900MHz		17 13		dB
t_D	Switching speed (on-off delay)	50% TTL to 90/10% RF		20		ns
t_r, t_f	Switching speeds (on-off rise/fall time)	90%/10% to 10%/90% RF		5		ns
	Switching transients			165		mV_{P-P}
P_{-1dB}	1dB gain compression	DC - 1GHz		+18		dBm
IP_3	Third-order intermodulation intercept	100MHz		+33		dBm
IP_2	Second-order intermodulation intercept	100MHz		+52		dBm
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.0		dB

NOTE:
1. All measurements include the effects of the D package NE/SA630 Evaluation Board (see Figure 1B). Measurement system impedance is 50Ω.
2. The placement of the AC bypass capacitor is critical to achieve these specifications. See the applications section for more details.

AC ELECTRICAL CHARACTERISTICS[1] - N PACKAGE

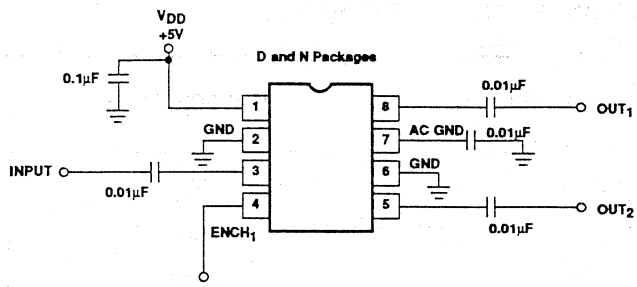
V_{DD} = +5V, T_A = 25°C; all other characteristics similar to the D-Package, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA630 MIN	LIMITS NE/SA630 TYP	LIMITS NE/SA630 MAX	UNITS
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2.5		dB
S_{21}, S_{12}	Isolation (OFF channel)	10MHz 100MHz 500MHz 900MHz	58	68 50 37 15		dB
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.5		dB

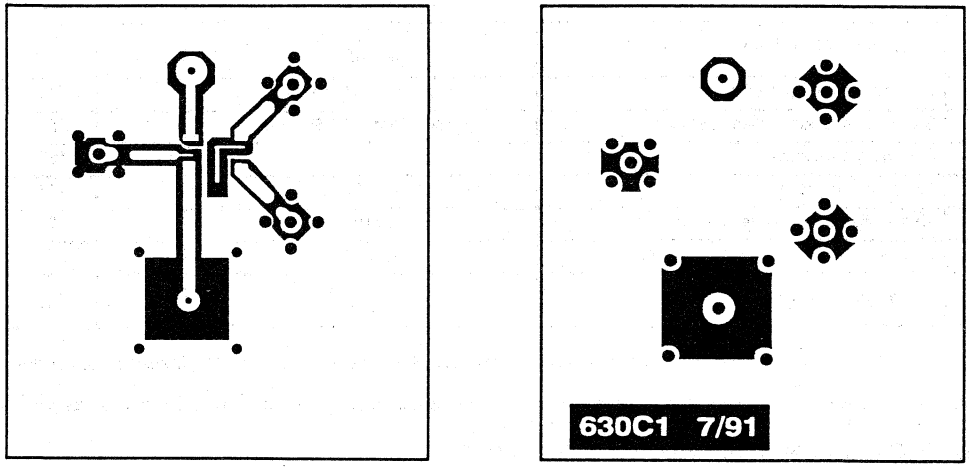
NOTE:
1. All measurements include the effects of the N package NE/SA630 Evaluation Board (see Figure 1C). Measurement system impedance is 50Ω.

APPLICATIONS

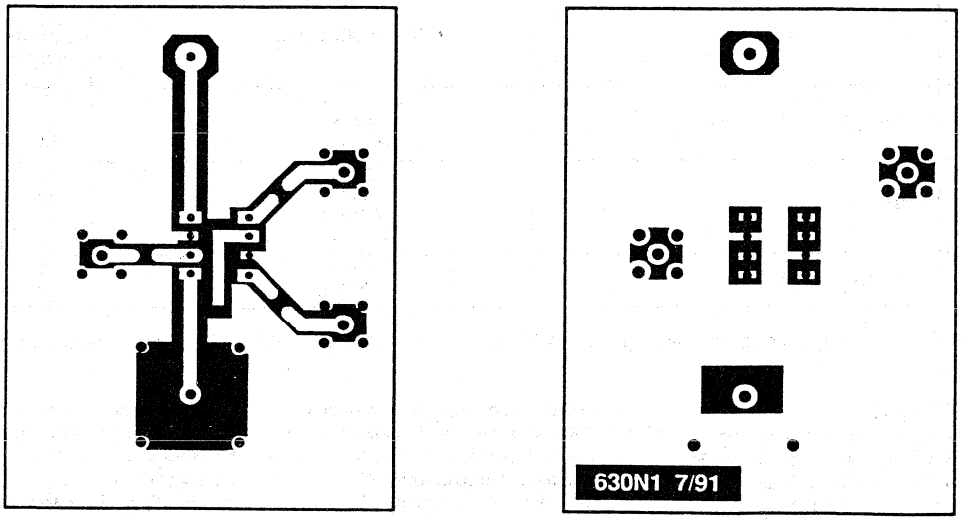
The typical applications schematic and printed circuit board layout of the NE/SA630 evaluation board is shown in Figure 1. The layout of the board is simple, but a few cautions need to be observed. The input and output traces should be 50Ω. The placement of the AC bypass capacitor is *extremely critical* if a symmetric isolation between the two channels is desired. The trace from Pin 7 should be drawn back towards the package and then be routed downwards. The capacitor should be placed straight down as close to the device as practical. For better isolation between the two channels at higher frequencies, it is also advisable to run the two output/input traces at an angle. This also minimizes any inductive coupling between the two traces. The power supply bypass capacitor should be placed close to the device. Figure 7 shows the frequency response of the NE/SA630. The loss matching between the two channels is excellent to 1.2GHz as shown in



a. NE/SA Evaluation Board Schematic



b. NE/SA630 D-Package Board Layout



c. NE/SA630 N-Package Board Layout

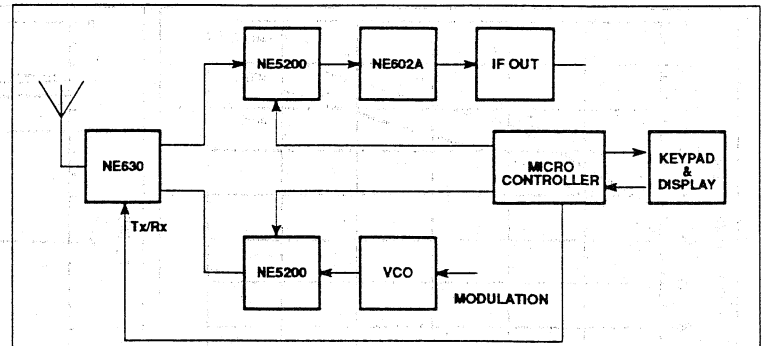
Figure 1

Figure 10. The isolation and matching of the two channels over frequency is shown in Figure 12 and Figure 14, respectively.

The NE630 is a very versatile part and can be used in many applications. Figure 2 shows a block diagram of a typical Digital RF transceiver front-end. In this application the NE630 replaces the duplexer which is typically very bulky and lossy. Due to the low power consumption of the device, it is ideally suited for handheld applications such as in CT2 cordless telephones. The NE630 can also be used to generate Amplitude Shift Keying (ASK) or On-Off Keying (OOK) and Frequency Shift Keying (FSK) signals for digital RF communications systems. Block diagrams for these applications are shown in Figure 3 and Figure 4, respectively.

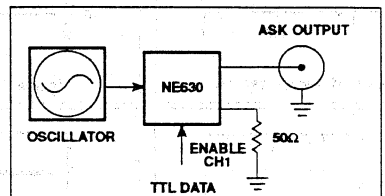
For applications that require a higher isolation at 1GHz than obtained from a single NE630, several NE630s can be cascaded as shown in Figure 5. The cascaded configuration will have a higher loss but greater than 35dB of isolation at 1GHz and greater than 65dB @ 500MHz can be obtained from this configuration. By modifying the enable control, an RF multiplexer/ de-multiplexer or antenna selector can be constructed. The simplicity of NE630 coupled with its ease of use and high performance lends itself to many innovative applications.

The NE/SA630 switch terminates the OFF channel in 50Ω. The 50Ω resistor is internal and is in series with the external AC bypass capacitor. Matching to impedances other than 50Ω can be achieved by adding a resistor in series with the AC bypass capacitor (e.g., 25Ω additional to match to a 75Ω environment).



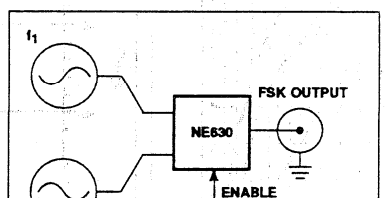
A TYPICAL TDMA/DIGITAL RF TRANSCEIVER SYSTEM FRONT-END

Figure 2



AMPLITUDE SHIFT KEYING (ASK) GENERATOR

Figure 3



FREQUENCY SHIFT KEYING (FSK) GENERATOR

Figure 4

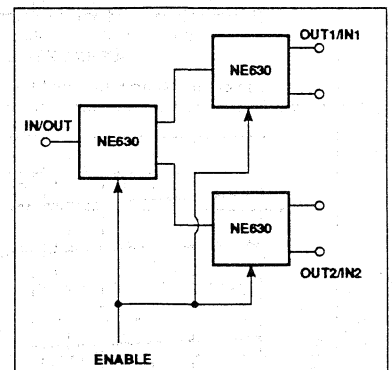


Figure 5

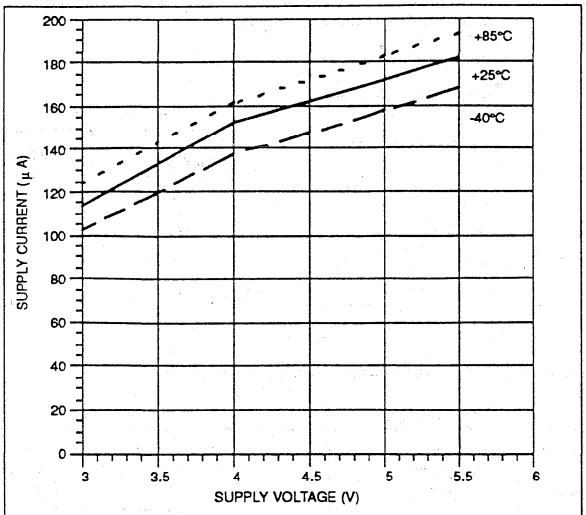


Figure 6 Supply Current vs. V_{DD} and Temperature

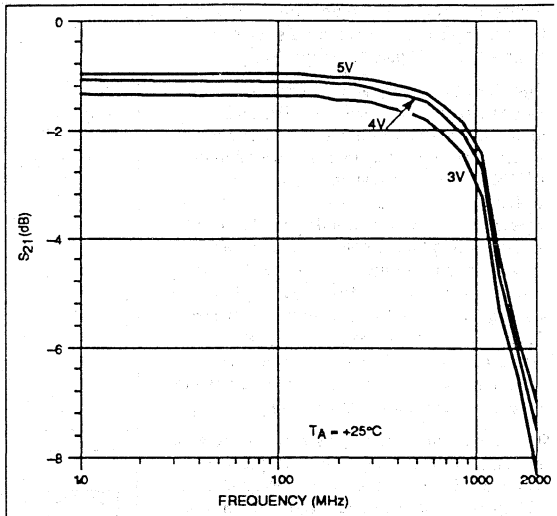


Figure 7 Loss vs. Frequency and V_{DD} for D-Package

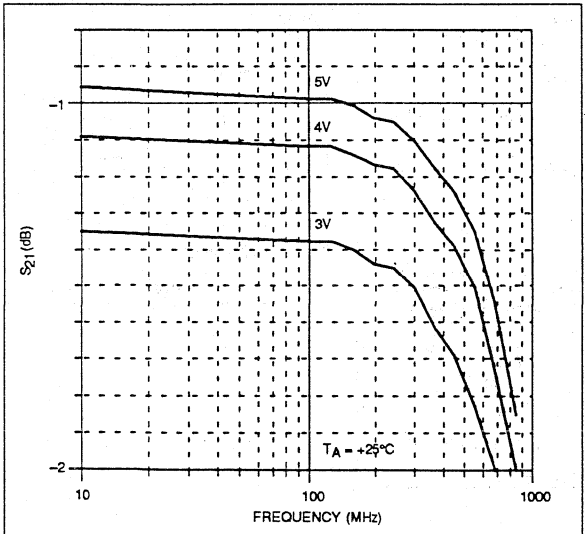


Figure 8 Loss vs. Frequency and V_{DD} for D-Package -Expanded Detail-

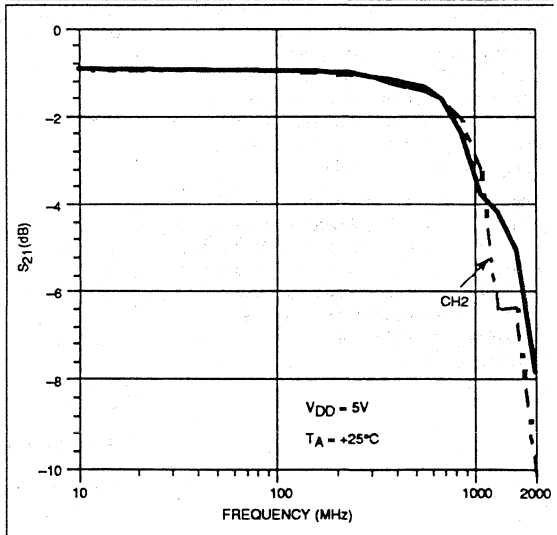


Figure 9 Loss Matching vs. Frequency for N-Package (DI

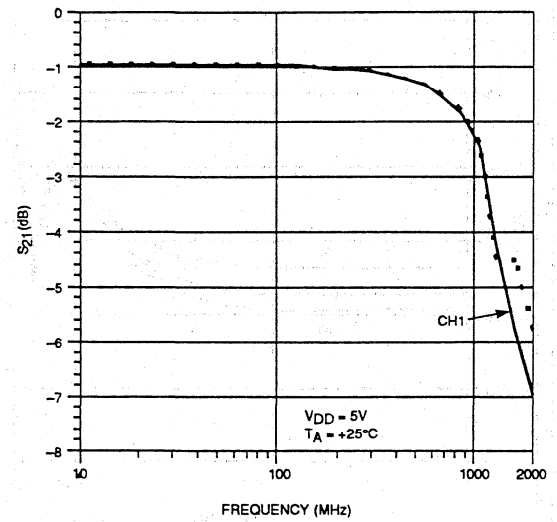


Figure 10 Loss Matching vs. Frequency; CH1 vs. CH2 for D-Pakage

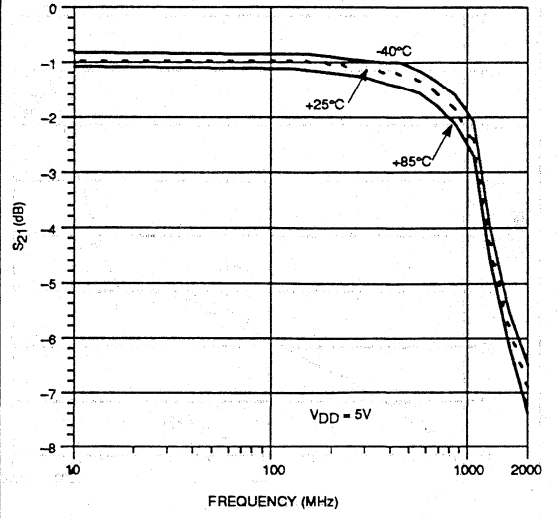


Figure 11 Loss vs. Frequency and Temperature for D-Package

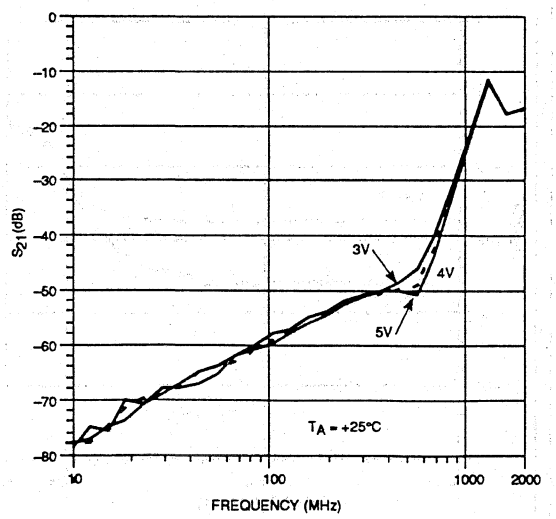


Figure 12 Isolation vs. Frequency and V_{DD} for D-Package

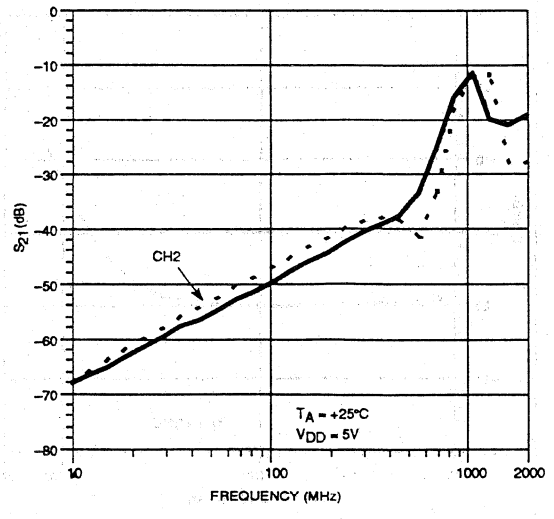


Figure 13 Isolation Matching vs. Frequency for N-Package (DIP)

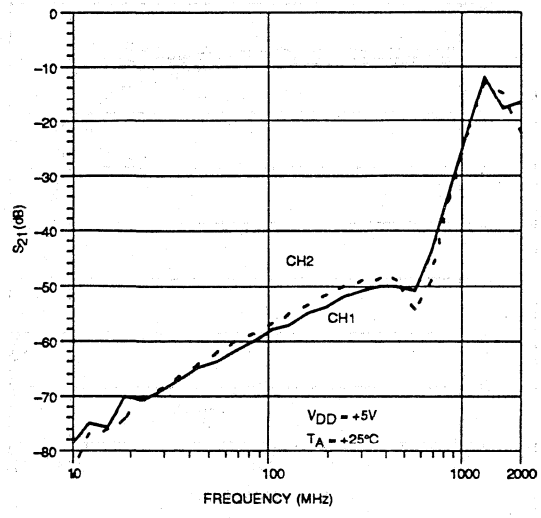


Figure 14 Isolation Matching vs. Frequency; CH1 vs. CH2 for D-Package

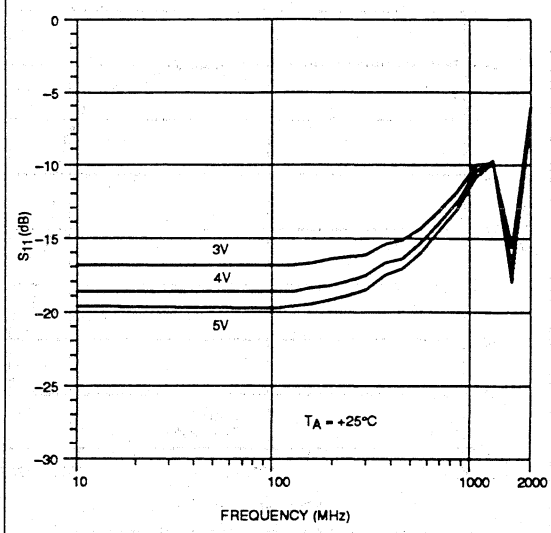


Figure 15 Input Match On-Channel vs. Frequency and V_{DD}

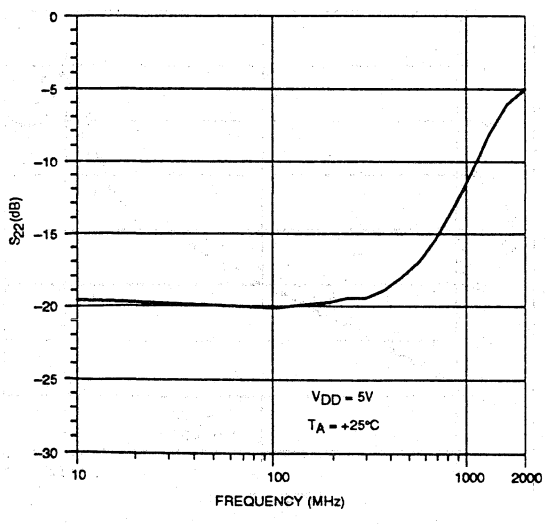


Figure 16 Output Match On-Channel vs. Frequency

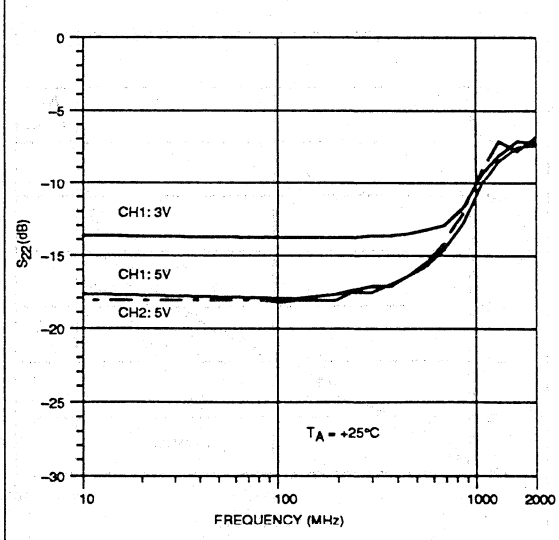


Figure 17 OFF-Channel Match vs. Frequency and V_{DD}

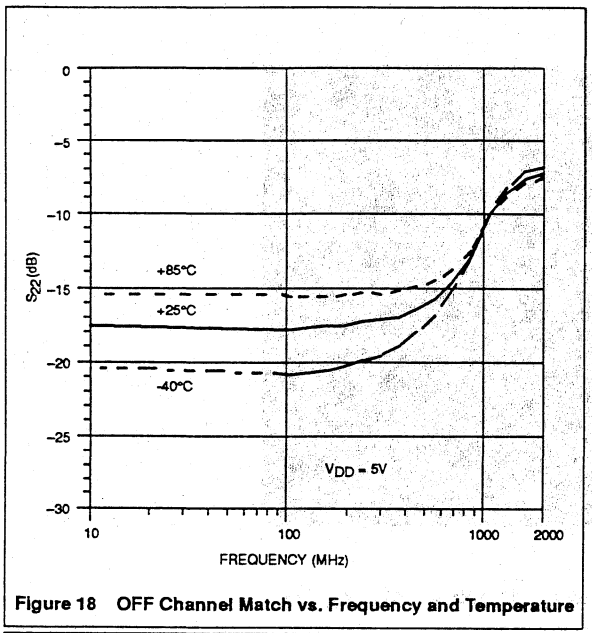


Figure 18 OFF Channel Match vs. Frequency and Temperature

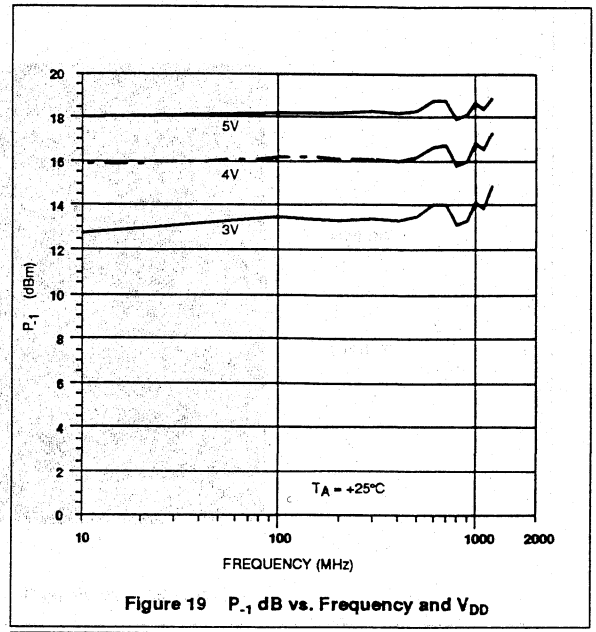


Figure 19 P_{-1} dB vs. Frequency and V_{DD}

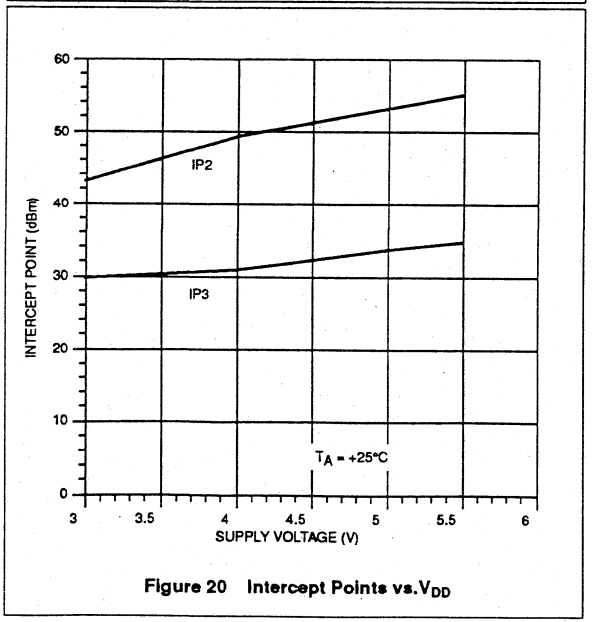


Figure 20 Intercept Points vs.V_{DD}

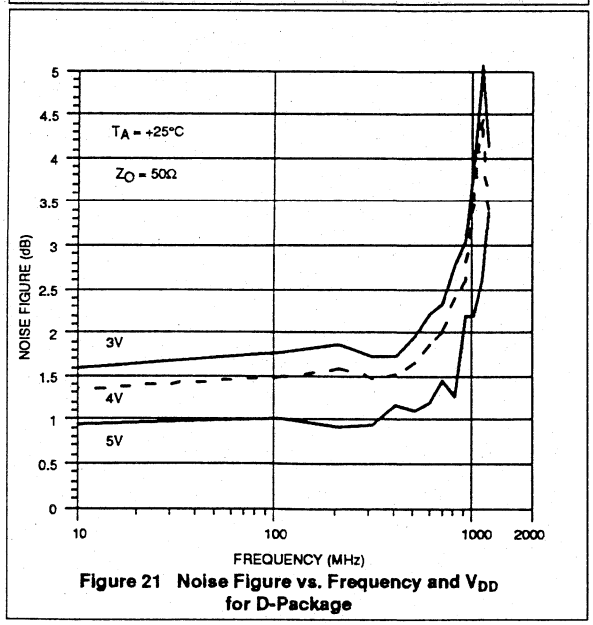


Figure 21 Noise Figure vs. Frequency and V_{DD} for D-Package

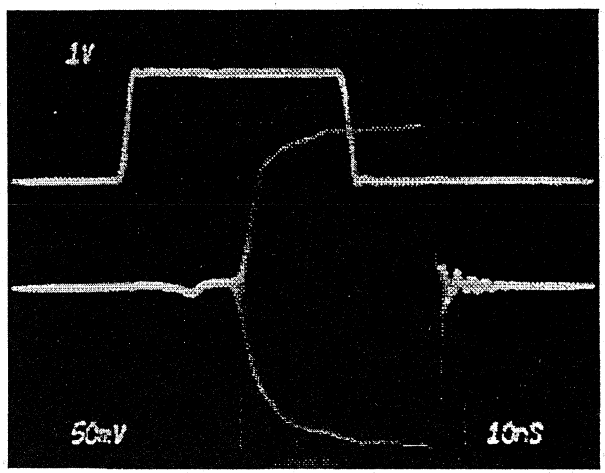


Figure 22 Switching Speed; f_{IN} = 100MHz at -6dBm, V_{DD} = 5V

Tone decoder/phase-locked loop NE/SA567

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

DESCRIPTION

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

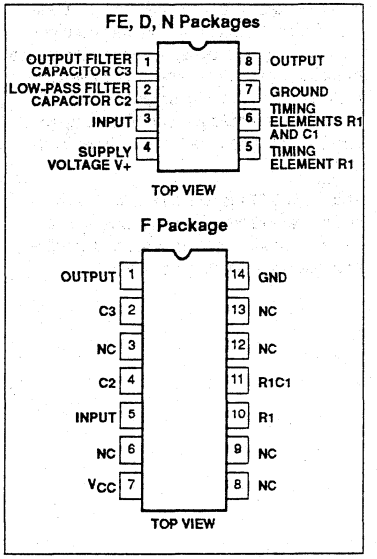
FEATURES

- Wide frequency range (.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14%)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20-to-1 range with an external resistor
- Military processing available

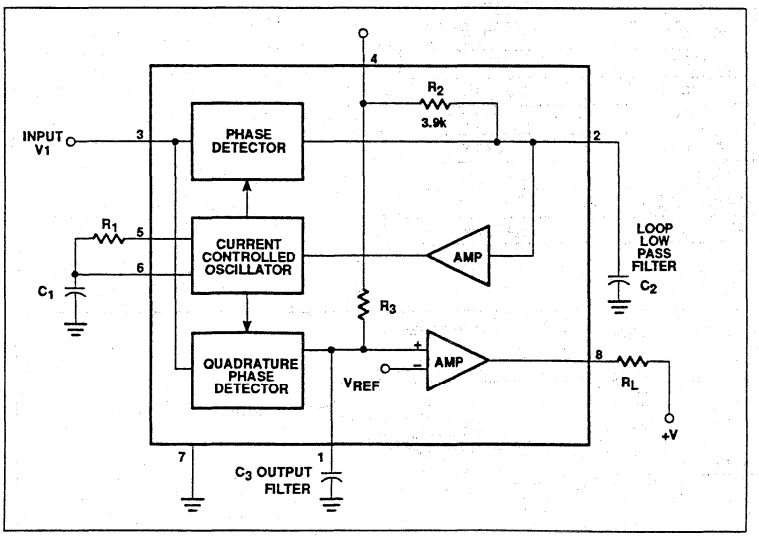
APPLICATIONS

- Touch-Tone® decoding
- Carrier current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

PIN CONFIGURATIONS



BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT&T.

Compandor | NE570/571/SA571

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

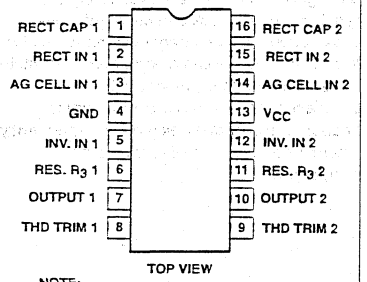
The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

FEATURES

- Complete compressor and expandor in one IChip
- Temperature compensated
- Greater than 110dB dynamic range
- Operates down to 6VDC
- System levels adjustable with external components
- Distortion may be trimmed out
- Dynamic noise reduction systems
- Voltage-controlled amplifier

PIN CONFIGURATION

D, F, and N Packages[1]



TOP VIEW

NOTE:
1. SOL - Released in Large SO Package Only.

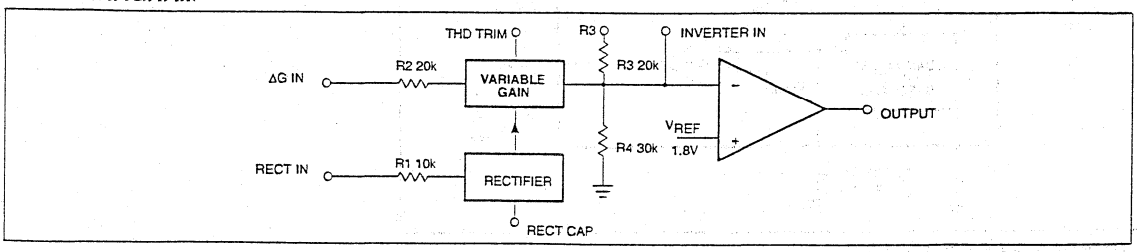
APPLICATIONS

- Cellular radio
- Telephone trunk compandor—570
- Telephone subscriber compandor—571
- High level limiter
- Low level expandor—noise gate
- Dynamic filters
- CD Player

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE570D
16-Pin Cerdip	0 to +70°C	NE570F
16-Pin Plastic DIP	0 to +70°C	NE570N
16-Pin Plastic SOL	0 to +70°C	NE571D
16-Pin Cerdip	0 to +70°C	NE571F
16-Pin Plastic DIP	0 to +70°C	NE571N
16-Pin Plastic SOL	-40 to +85°C	SA571D
16-Pin Cerdip	-40 to +85°C	SA571F
16-Pin Plastic DIP	-40 to +85°C	SA571N

BLOCK DIAGRAM



Digital post-detection filter for FSK data receivers

OM4031T

FEATURES

- External clock frequency 30 to 80 kHz (typ. 38.4 kHz)
- Supported data rates 600, 1200, 2400 and 4800 bits/s (typ.)
- Double bandwidth option (not for 4800 bits/s)
- Schmitt-triggered inputs for optimum slope tolerance
- Enable input for power-down mode
- Open-drain output (3-state in power-down mode)
- No external components required
- Single supply voltage from 1.8 to 6.0 V
- Very low operating current (1.5 µA typ.)
- Operating temperature from −10 to +70 °C.

APPLICATIONS

- Telemetry data receivers
- RF security systems
- Low-bit-rate radio data links
- Paging applications of UAA2080 and UAA2082 with software decoding.

GENERAL DESCRIPTION

The OM4031T is intended for performance enhancement of FSK data receivers that do not have a built-in post-detection filter.

It contains a digital moving average filter to remove noise from the demodulated data. When operated from a 38.4 kHz external clock it can handle data rates of 600, 1200 and 2400 bits/s at an oversampling rate of 16. The filter bandwidth can be doubled to ease the search for bit synchronization on the output data.

To allow for jitter in the input data, a 12-bit sample is taken for the majority decision. Doubling the filter bandwidth is realised by taking the majority out of 6 samples (2400 bits/s) or by doubling the sampling rate (600 and 1200 bits/s).

An input data rate of 4800 bits/s is supported at 8 times oversampling and normal bandwidth.

All inputs are Schmitt-triggered to ensure reliable operation even at signals with long rise/fall times.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.8	–	6.0	V
I_{DDPD}	power-down supply current	CE = V_{SS}	–	1.0	10.0	µA
I_{DD}	operating supply current	CE = V_{DD}; note 1	–	1.5	20.0	µA
$P_{i(ref)}$	sensitivity improvement at 3% bit error rate	note 2				
		600 bits/s, 250 µs slope	–	5.3	–	dB
		1200 bits/s, 250 µs slope	–	3.6	–	dB
		2400 bits/s, 125 µs slope	–	2.0	–	dB
T_{amb}	operating ambient temperature		−10	–	+70	°C

Notes

1. V_{DD} = 2.0 V; DOUT open-circuit; input data at 20 kHz random pattern.
2. Bench evaluated for UAA2080H at 470 MHz, not factory tested.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM4031T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Digital post-detection filter for FSK data receivers

OM4031T

BLOCK DIAGRAM

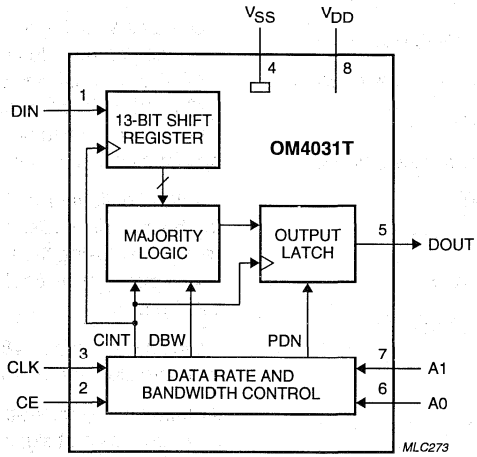


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DIN	1	data input
CE	2	chip enable input
CLK	3	external clock input
V_{SS}	4	negative supply voltage
DOUT	5	data output (open-drain)
A0	6	data rate and bandwidth control input 0 (see Table 1)
A1	7	data rate and bandwidth control input 1 (see Table 1)
V_{DD}	8	positive supply voltage

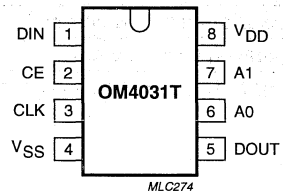


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The OM4031T digital post-detection filter oversamples the noisy binary data stream at input DIN (pin 1), and outputs a noise-reduced data stream via open-drain output DOUT (pin 5). The filter bandwidth can be doubled to ease the search for bit synchronization on the data output signal.

Input sampling takes place at 16 times the data rate. For a typical clock frequency of 38.4 kHz the nominal data rates are 600, 1200 and 2400 bits/s. A data rate of 4800 bits/s can be handled at an oversampling rate of 8 and at normal bandwidth only.

Using a different clock frequency will produce bit rates equal to the clock frequency divided by 64, 32 or 16. When the clock frequency is not an integer multiple of the data rate some edge jitter will be introduced in the output data.

The clock frequency is not very critical for the noise filtering performance: a clock frequency of 32.768 kHz could be used at 512, 1200 and 2400 bits/s without loss of performance.

Since no on-chip oscillator is available an external clock signal is required at input CLK (pin 3). Two control inputs A0 and A1 (pins 6 and 7) are used for selection of the data rate and the filter bandwidth.

A separate enable input CE (pin 2) allows the circuit to be powered down. In power-down mode (CE = LOW) the system clock is inhibited and the data output DOUT is made 3-state and remains static.

Moving average noise filter

Noise reduction is achieved by applying a moving average filter on N samples of the input data signal. In principle N can be odd or even, but in the OM4031T an even number is used (N = 12). When there is no absolute majority (equal number of ones and zeroes) the previous majority output is maintained.

An odd value for N would always produce an absolute majority and not require decision feedback. However the noise performance is worse for odd values of N, because the output can toggle at every clock (e.g. when a 101010... pattern is clocked in). For even values of N the output polarity can only change once every 3 clocks and does not toggle at all for a 101010... or a 11001100... pattern.

Using 12 out of 16 samples for the majority decision produces a filter which combines good noise reduction with a large tolerance for data jitter (maximum $\frac{1}{8}$-bit duration).

Filter implementation

The moving average filter is implemented using a 13-bit register and two state machines (COUNT and CLOCK) for the majority decision. The first stage of the shift register is used for input synchronization.

The CLOCK state machine generates the internal clock signal CINT and the bandwidth selection signal DBW in accordance with the logic levels on control lines CE, A0 and A1.

The majority decision is taken by state machine COUNT based on the contents of the input shift register and the previous decision in the output latch.

The doubled bandwidth is achieved by increasing the sampling rate by a factor of 2 for 600 and 1200 bits/s. For 2400 bits/s the number of samples for the majority decision is halved, controlled by the DBW signal. This signal is derived from the control signals as follows:

$$DBW = CE \bullet A0 \bullet \overline{A1}$$

Filter characteristic

The frequency characteristic of the moving average filter in the OM4031T is given in Fig.3 for N = 12 and N = 6.

The horizontal axis shows the normalized frequency f_N which is the ratio of the frequency f and the sampling frequency f_s. The value for f_s is given in Table 1 for the various data rates and filter bandwidths.

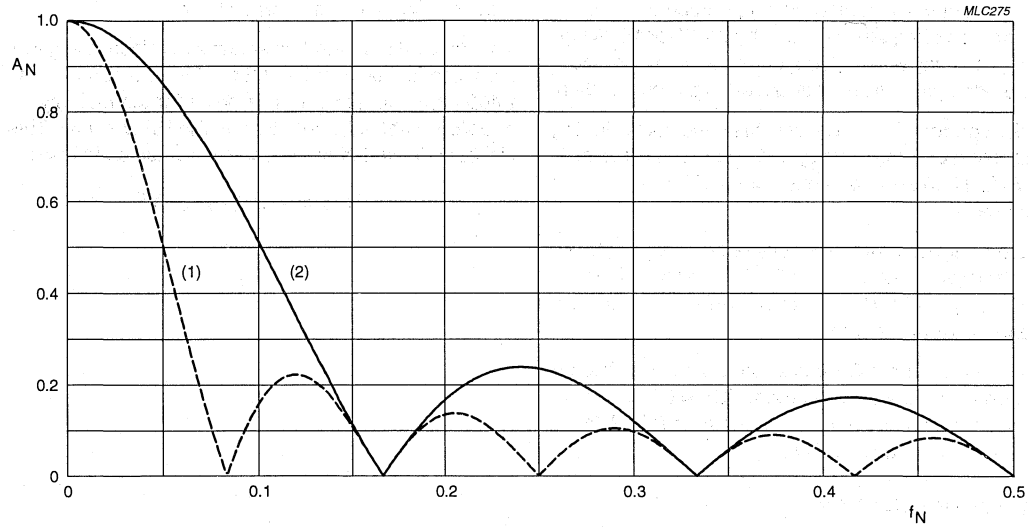
The vertical axis shows the normalized amplitude A_N.

At normal bandwidth the oversampling rate is 16, except for 4800 bits/s where it is 8. At double bandwidth the oversampling rate is 32, except for 2400 bits/s, where it is 16.

The 3 dB cut-off frequency is calculated as follows:

N = 12: $f_{co} = 0.0371 \times f_s$

N = 6: $f_{co} = 0.0748 \times f_s$



(1) N = 12.
(2) N = 6.

Fig.3 Filter transfer function of the OM4031T.

Noise reduction

The performance of the OM4031T was bench tested by measuring the sensitivity improvement (3% BER) of the UAA2080H pager receiver at various bit rates using a stand-alone pager receiver board (OM4647 at 470 MHz). The results are given in Chapter "AC Characteristics".

The OM4031T was also tested in a POCSAG pager application using software decoding together with the UAA2080H receiver.

For 12-digit numeric messages at 1200 bits/s the typical sensitivity for 80% call success rate improved by 2.8 dB, as shown in Fig.4.

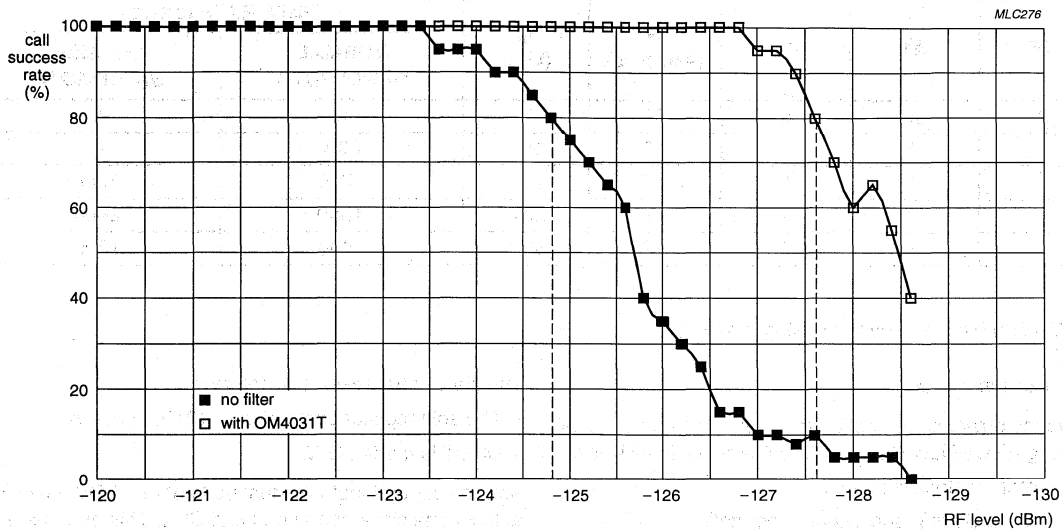


Fig.4 Paging call success rate improvement; 1200 bits/s, 12-digit numeric message.

OPERATING INSTRUCTIONS

Control signals

The operation of the OM4031T is determined by 3 control signals (CE, A0 and A1) and the clock frequency at input CLK. Table 1 shows the various possibilities for a typical clock frequency of 38.4 kHz.

The parameter N is the number of samples used in the calculation of the average bit value.

The parameter f_s is the input sampling frequency, assuming a 38.4 kHz external clock signal.

The logic levels on A0 and A1 can be changed while CE = HIGH, except to select or deselect 2400 bits/s with doubled bandwidth (A1 = LOW, A0 = HIGH). This mode must be entered or left while CE = LOW to avoid data errors on DOUT.

Table 1 Data rate and filter bandwidth selection

CE	A1	A0	N (samples)	f_s (kHz)	DATA RATE (bits/s)	
					NORMAL BANDWIDTH	DOUBLE BANDWIDTH
0	X	X	X	X	X	X
1	0	0	12	9.6	600	–
1	1	0	12	19.2	1200	600
1	0	1	6	38.4	4800(1)	2400
1	1	1	12	38.4	2400	1200

Note

1. At 4800 bits/s the oversampling rate is 8.

Power-down mode

To reduce power consumption the filter can be disabled by applying a LOW level to input CE. The result is as follows:

- The internal clock is inhibited
- Output DOUT is made 3-state and static.

Reset

The OM4031T is reset internally when power-down mode is left by applying a HIGH level to input CE. The actual reset takes place on the second falling edge on input CLK after CE = HIGH.

The status after reset is as follows:

- The shift register contains a 101010... pattern
- DOUT is made LOW.

After power-up input CE must be kept at a LOW level for at least one clock period on input CLK. This ensures a successful reset when CE is made HIGH.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	7.0	V
V_I	input voltage on any pin	−0.5	V_{DD} + 0.5	V
I_I	DC input current all pins	–	20	mA
I_O	DC output current all pins	–	20	mA
P_{tot}	total power dissipation	–	150	mW
T_{amb}	operating ambient temperature	−10	+70	°C
T_{stg}	storage temperature	−55	+125	°C

DC CHARACTERISTICS

V_{DD} = 1.8 to 6.0 V; V_{SS} = 0 V; T_{amb} = −10 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		1.8	–	6.0	V
I_{DDPD}	power-down supply voltage	CE = V_{SS}; note 1	–	1.0	10.0	µA
I_{DD}	operating supply current	CE = V_{DD}; notes 1 and 2	–	1.5	20.0	µA
Inputs A0, A1, CLK and CE						
V_{IL}	LOW level input voltage		−0.5	–	+0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = V_{DD} or V_I = V_{SS}	–	–	1.0	µA
C_I	input capacitance	tested on sample basis	–	2.0	–	pF
Output DOUT						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1.0	–	–	mA
I_{LO}	output leakage current	V_{OH} = V_{DD}	–	–	1.0	µA

Notes

1. V_{DD} = 2.0 V; V_{IL} = V_{SS}; V_{IH} = V_{DD}; DOUT is open-circuit; clock signal at input CLK; f_{clk} = 38.4 kHz, amplitude: V_{SS} to V_{DD}; data signal at input DIN: random pattern at 20 kHz to simulate 2400 bits/s data with noise; t_r = t_f = 5 ns.
2. The operating current will be higher than specified when the input signal amplitude is less than 100% (equals V_{SS} to V_{DD}) or when longer rise/fall times are used. This is caused by the Schmitt-trigger circuits drawing extra current.

AC CHARACTERISTICS

V_{DD} = 1.8 to 6.0 V; V_{SS} = 0 V; T_{amb} = −10 to +70 °C; f_{clk} = 38.4 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
External clock						
f_{clk}	external clock frequency		30	38.4	80	kHz
Filter bandwidth (note 1)						
f_{co}	cut-off frequency (−3 dB)	normal bandwidth				
		600 bits/s	–	356	–	Hz
		1200 bits/s	–	712	–	Hz
		2400 bits/s	–	1425	–	Hz
		4800 bits/s	–	2872	–	Hz
		double bandwidth				
		600 bits/s	–	712	–	Hz
		1200 bits/s	–	1425	–	Hz
		2400 bits/s	–	2872	–	Hz
Noise reduction (note 2)						
$P_{i(ref)}$	sensitivity improvement at 3% bit error rate	note 3				
		600 bits/s, 250 µs slope	–	5.3	–	dB
		1200 bits/s, 250 µs slope	–	3.6	–	dB
		2400 bits/s, 125 µs slope	–	2.0	–	dB

Notes

1. Filter bandwidth is guaranteed by design. Values supplied are simulation results.
2. Noise reduction is not factory tested, only bench evaluated.
3. Sensitivity improvement was bench tested on the UAA2080H demonstration board OM4747. Test signal: preamble (101010...), f_{iRF} = 469.950 MHz, deviation = ±4.0 kHz, slope = 10 to 90% of amplitude, V_P = 2.05 V, T_{amb} = 25 °C. See *"UAA2080 data sheet, AC characteristics"*.

APPLICATION INFORMATION

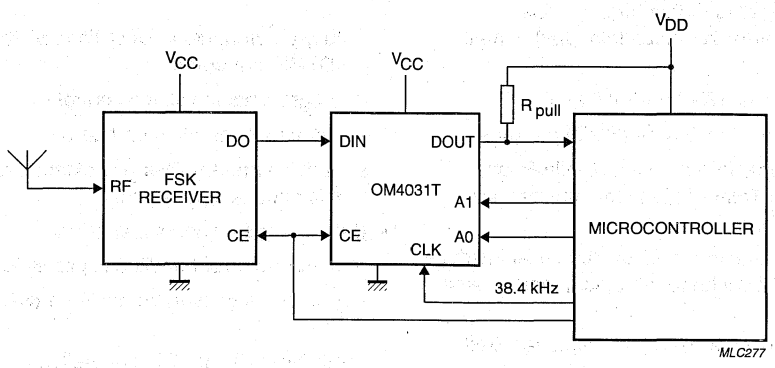


Fig.5 Typical application example.

The OM4031T will generally operate from the same power supply (V_{CC}) as the FSK data receiver providing its input data. The open-drain data output allows level shifting of the data to suit a microcontroller operating at a higher power supply voltage (V_{DD}).

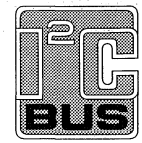
The value of the pull-up resistor R_{pull} on output DOUT is determined by the type and number of input circuits to be driven. The required signal rise time must be balanced against the current drawn by the pull-up.

For the highest rate (2400 bits/s) the signal rise time should preferably be below 50 µs.

For a single CMOS input with a 10 pF capacitance R_{pull} = 1 MΩ gives a rise time of approximately 30 µs ($3 \times t_{RC}$). At V_{DD} = 2.0 V this corresponds with a current of 2 µA.

AMPS/TACS hybrid baseband module OM5300

FEATURES



- Low-voltage operation (3.0 to 5.5 V)
- Low-current consumption (various current saving modes)
- Separate supply lines for Audio Amplifier and APROC, offering the possibility to switch off these ICs independently, in order to reduce (standby) current consumption
- Very small dimensions (25.4 × 43 × 5 mm)
- 66 pins Surface Mounted Device (SMD) package
- Software programmable Advanced Mobile Phone Service (AMPS) or Total Access Communications System (TACS) mode
- Easy and direct interfacing to RF system, user interface (keypad, buzzer, microphone, earpiece), and external program memory
- Minimum number of external components required
- Two 8-bit Analog-to-Digital Converter (ADC) inputs for e.g. Received Signal Strength Indicator (RSSI) and supply voltage measurements
- Low-pass filtered Pulse Width Modulation (PWM) output for RF power control
- External communication via:
  - I^2C interface
  - full duplex Universal Asynchronous Receiver and Transmitter (UART)
- System control:
  - on-board 83CL580 low-voltage microcontroller
  - direct interfacing to external memory
  - on-board 256 bytes Electrical Erasable Programmable Read Only Memory (EEPROM) for system parameter storage and memory dial capabilities
  - fixed operating frequency using crystal oscillator from 9.6 to 12 MHz
- Audio processing:
  - voice operated transmission (VOX) capability
  - bypass noise cancellor in order to enable data transmission or hands-free operation
  - includes all required compandor and de-/pre-emphasis filtering
  - fully programmable transmit and receive audio/data path (no external manual adjustments required during assembly)
  - fully programmable Dual Tone Multi-Frequency (DTMF) generator
  - programmable volume control
  - sidetone generation on-board
  - variable pre-amplifier (via external resistor) for microphone input signal
- Data processing and supervision
  - complete error handling capabilities
  - robust Supervisory Audio Tone (SAT) transponder loop
  - Signalling Tone (ST) generation.

GENERAL DESCRIPTION

The AMPS/TACS baseband hybrid module is a fully programmable system, integrating all audio and data processing functionality for the AMPS and TACS analog cellular radio. It includes the SA5752 and SA5753 Audio Processing (APROC) ICs, TDA7050 audio amplifier, the UMF1000LT Data Processor (DPROC), the 83CL580 microcontroller and the ST25C02A 256 bytes EEPROM. Together with an external PSD312L, this module offers a 'two-chip' implementation of the AMPS/TACS baseband functionality.

BLOCK DIAGRAM

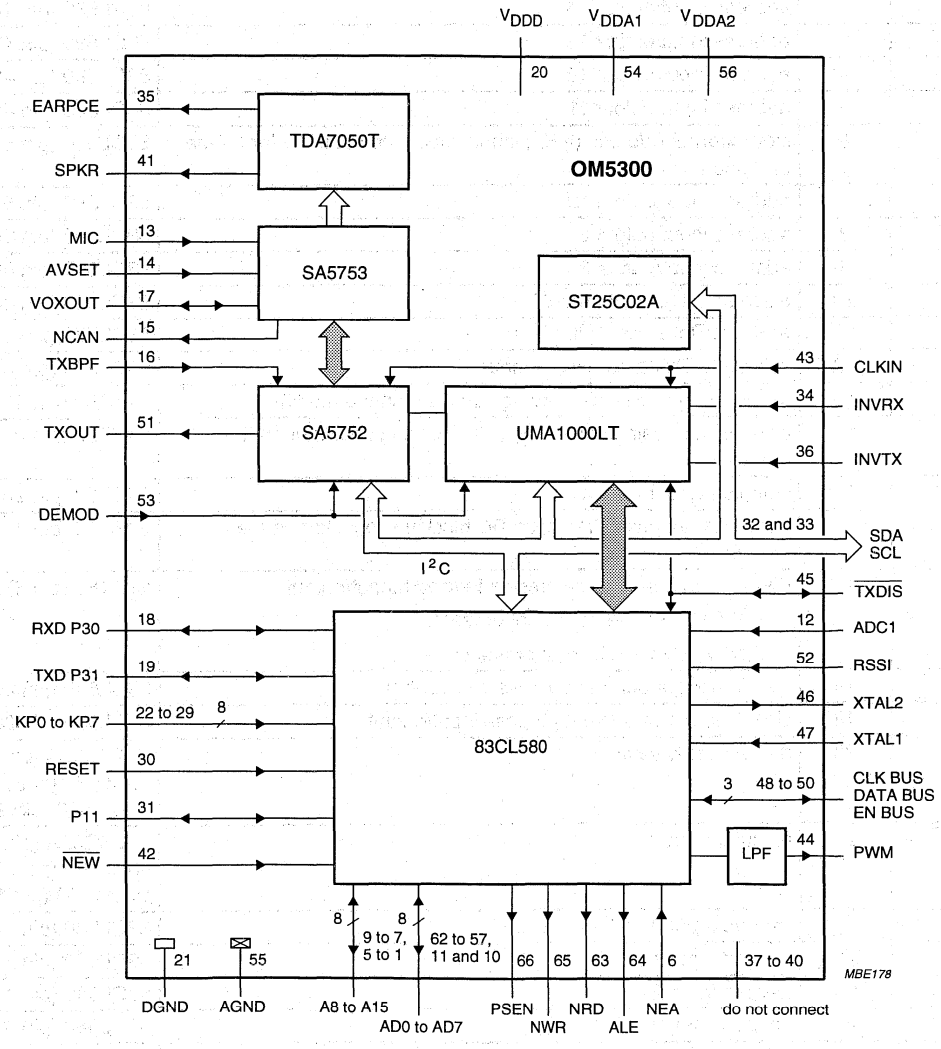


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	INTERNALLY CONNECTED TO
A15	1	address input/output 15	83CL580 (pin 45)
A14	2	address input/output 14	83CL580 (pin 46)
A13	3	address input/output 13	83CL580 (pin 47)
A12	4	address input/output 12	83CL580 (pin 48)
A11	5	address input/output 11	83CL580 (pin 49)
NEA	6	Not External Address (NEA) input; should be set LOW for normal operation	83CL580 (pin 51)
A10	7	address input/output 10	83CL580 (pin 54)
A9	8	address input/output 9	83CL580 (pin 55)
A8	9	address input/output 8	83CL580 (pin 56)
AD7	10	Address/Data input/output 7	83CL580 (pin 44)
AD6	11	Address/Data input/output 6	83CL580 (pin 43)
ADC1	12	Analog-to-Digital Converter input 1	83CL580 (pin 61)
MIC	13	microphone input; DC blocking capacitor on the module	SA5752 (pin 1)
AVSET	14	pre-amplifier gain setting input; DC blocking capacitor on the module	SA5752 (pin 2)
NCAN	15	noise cancellor output	SA5752 (pin 20)
TXBPF	16	transmit bandpass filter input; DC blocking capacitor on the module	SA5753 (pin 1)
VOXOUT	17	if VOX is enabled, voice present indicator input/output: VOXOUT = LOW; voice not present. VOXOUT = HIGH; voice present.	SA5752 (pin 5)
RXD P30	18	UART input or general purpose input/output	83CL580 (pin 27)
TXD P31	19	UART output or general purpose input/output	83CL580 (pin 28)
V_{DDD}	20	digital supply voltage	ST25C02A (pin 8); 83CL580 (pin 57); UMA1000 (pin 28)
DGND	21	digital ground	ST25C02A (pin 4); 83CL580 (pin 26); UMA1000 (pin 14)
KP0	22	keypad input 0	83CL580 (pin 1)
KP1	23	keypad input 1	83CL580 (pin 2)
KP2	24	keypad input 2	83CL580 (pin 4)
KP3	25	keypad input 3	83CL580 (pin 5)
KP4	26	keypad input 4	83CL580 (pin 6)
KP5	27	keypad input 5	83CL580 (pin 7)
KP6	28	keypad input 6	83CL580 (pin 8)
KP7	29	keypad input 7	83CL580 (pin 10)
RESET	30	reset input for the module; active HIGH	83CL580 (pin 11)
P11	31	general purpose input/output	83CL580 (pin 13)

SYMBOL	PIN	DESCRIPTION	INTERNALLY CONNECTED TO
SDA	32	I²C-bus serial data line; pull-up resistor on the module	83CL580 (pin 21); SA5753 (pin 17); UMA1000 (pin 24)
SCL	33	I²C-bus serial clock line; pull-up resistor on the module	83CL580 (pin 20); SA5753 (pin 16); UMA1000 (pin 25)
INVRX	34	inverts sense of received data stream if input = HIGH	UMA1000 (pin 7)
EARPCE	35	earpiece output; DC blocking capacitors on module	TDA7050 (pin 6)
INVTX	36	inverts sense of transmitted data stream if input = HIGH	UMA1000 (pin 21)
DEMOD IN	37	demodulated input signal; do not connect this pin	
DATA IN	38	data/SAT/ST output from DPROC to APROC; do not connect this pin	SA5753 (pin 19); UMA1000 (pin 4)
TXMUTE	39	TXMUTE signal from DPROC to APROC; do not connect this pin	SA5753 (pin 18); UMA1000 (pin 11)
RXMUTE	40	RXMUTE signal from DPROC to APROC; do not connect this pin	SA5753 (pin 12); UMA1000 (pin 5)
SPKR	41	audio output to speaker; DC blocking capacitors on module	TDA7050 (pin 6)
$\overline{NEW}$	42	enable watchdog timer input; active LOW	83CL580 (pin 23)
CLKIN	43	1.2 MHz clock input for APROC and DPROC	SA5753 (pin 14); UMA1000 (pin 12)
PWM	44	Low-Pass Filter (LPF) PWM output	83CL580 (pin 22)
$\overline{TXDIS}$	45	transmitter disable signal input/output; with pull-up resistors on the module; active LOW	83CL580 (pin 14); UMA1000 (pin 20)
XTAL2	46	inverting amplifier output that form the oscillator; must be left open when an external oscillator is used	83CL580 (pin 24)
XTAL1	47	inverting amplifier input that form the oscillator and internal clock generator input; receives the external oscillator signal when an external oscillator is used	83CL580 (pin 25)
CLK BUS	48	3-wire interface clock signal input/output	83CL580 (pin 31)
DATA BUS	49	3-wire interface data signal input/output	83CL580 (pin 32)
EN BUS	50	3-wire interface enable signal input/output	83CL580 (pin 30)
TXOUT	51	output signal to be transmitted	SA5753 (pin 20)
RSSI	52	analog-to-digital converter input	83CL580 (pin 62)
DEMOD	53	demodulated signal input	SA5753 (pin 11); UMA1000 (pin 3)
V_{DDA1}	54	analog supply voltage for APROC	SA5753 (pin 4); SA5752 (pin 9)
AGND	55	analog ground	SA5752 (pin 7); SA5753 (pin 15); TDA7050 (pin 5)
V_{DDA2}	56	analog supply voltage for audio amplifier	TDA7050 (pin 8)
AD5	57	Address/Data pin 5 input/output	83CL580 (pin 42)
AD4	58	Address/Data pin 4 input/output	83CL580 (pin 41)

SYMBOL	PIN	DESCRIPTION	INTERNALLY CONNECTED TO
AD3	59	Address/Data input/output 3	83CL580 (pin 40)
AD2	60	Address/Data input/output 2	83CL580 (pin 39)
AD1	61	Address/Data input/output 1	83CL580 (pin 38)
AD0	62	Address/Data input/output 0	83CL580 (pin 37)
NRD	63	not read output	83CL580 (pin 34)
ALE	64	address latch enable output	83CL580 (pin 52)
NWR	65	not write output	83CL580 (pin 33)
PSEN	66	program store enable output	83CL580 (pin 53)

MECHANICAL INFORMATION

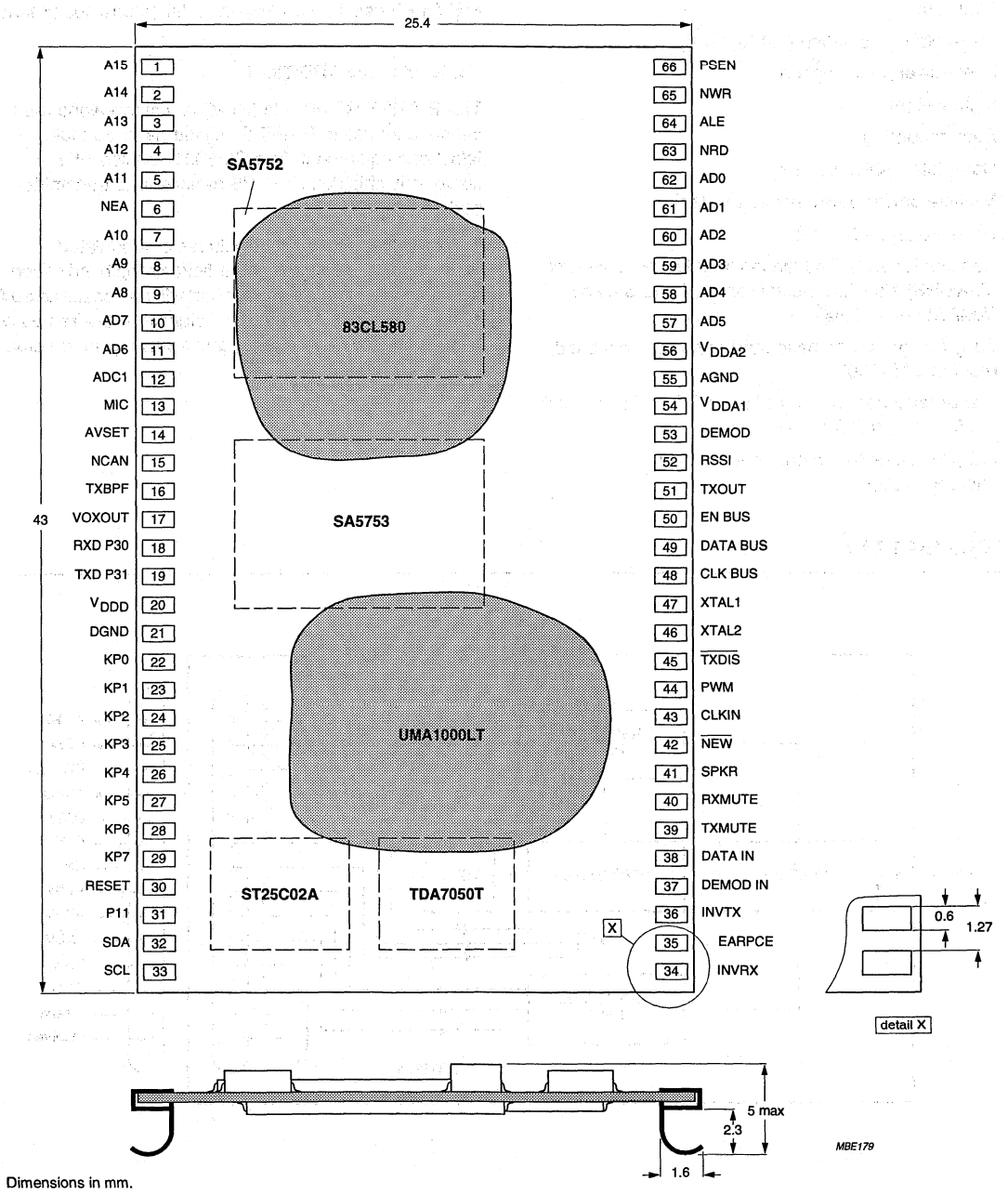


Fig.2 Mechanical data.

E-AMPS Radio Frequency Module (RFM) OM5301

FEATURES

- Low cost
- Low-voltage operation (4.4 to 6.4 V)
- Low-power consumption
- Light weight
- Easy mounting
- Completely shielded box
- Multiple power-down modes available
- Small volume (29 cm^3)
- Besides Extended-Advanced Mobile Phone Service (E-AMPS) also Advanced Mobile Phone Service (AMPS) compatible
- Easy design-in with baseband part (e.g. baseband module OM5300)
- Power level control possibility via DC or Pulse Width Modulated (PWM) signal
- 9.6 MHz clock signal output available for microcontroller.

APPLICATION

- E-AMPS cellular hand-portable telephone equipment.

GENERAL DESCRIPTION

This E-AMPS RF Module (RFM) is a stand-alone module intended for use in E-AMPS cellular hand-portable telephone equipment. The OM5301 consists of a completely shielded E-AMPS receiver and transmitter part.

Output of the receiver part includes demodulated (baseband) audio signal and a field strength indication signal. Input to the transmitter part will be baseband audio signal and output power control signals. A 3-wire bus will be used to provide frequency and switching information to the RFM.

BLOCK DIAGRAM

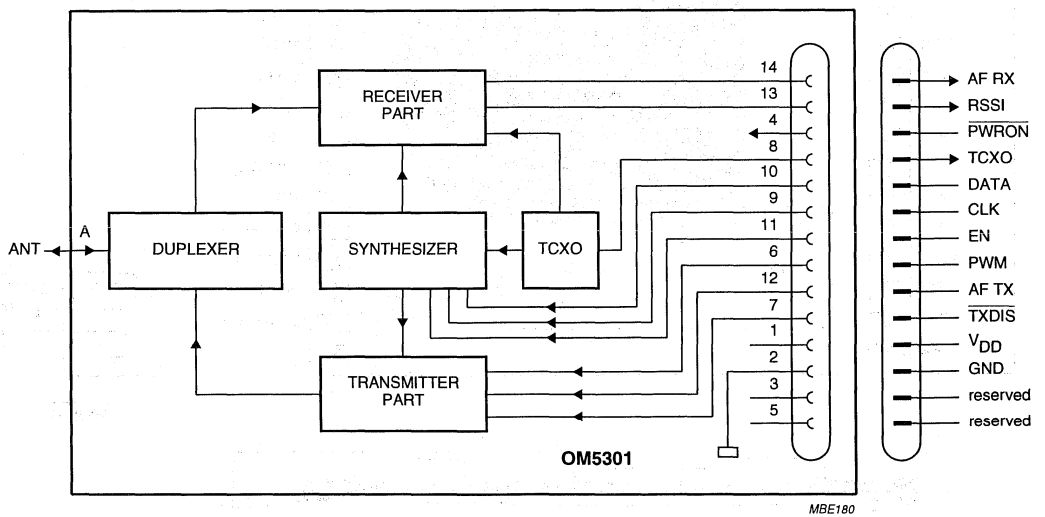


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD}	1	supply voltage (battery)
GND	2	ground
Reserved	3	reserved for future use e.g. receiver disable (RXDIS)
$\overline{\text{PWRON}}$	4	module power-on input; active LOW
Reserved	5	reserved for future use e.g. 1.2 MHz output
PWM	6	Pulse Width Modulation input
$\overline{\text{TXDIS}}$	7	transmitter disable input; active LOW
TCXO	8	TCXO output (9.6 MHz)
CLK	9	3-wire bus clock input
DATA	10	3-wire bus data input
EN	11	3-wire bus enable input
AF TX	12	transmitter audio input
RSSI	13	received signal strength indication output
AF RX	14	receiver demodulated audio output
ANT	A	antenna input/output
MT1	MT1	mounting tab 1
MT2	MT2	mounting tab 1
MT3	MT3	mounting tab 3
MT4	MT4	mounting tab 4

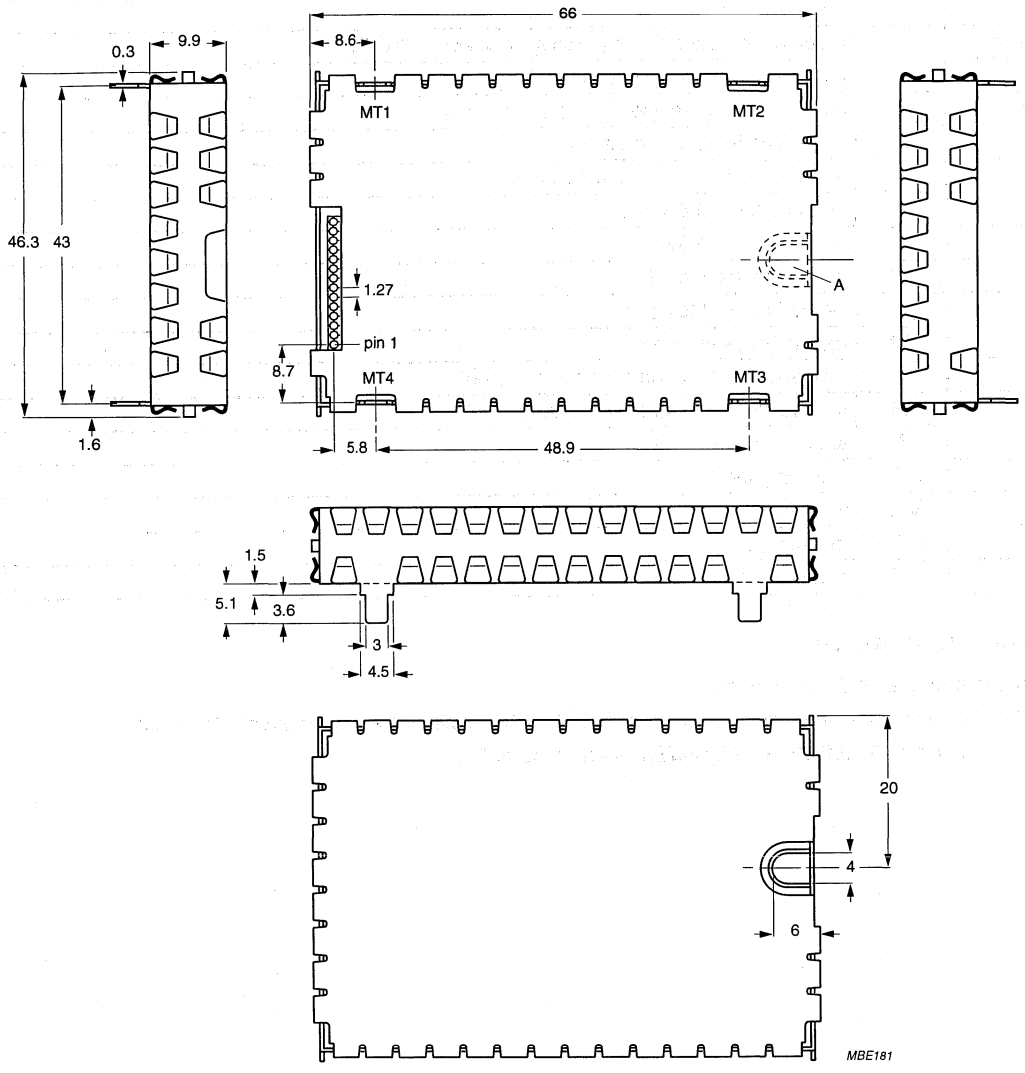
REFERENCE DOCUMENTS

The applicable reference documents are:

"EIA/IS-19-B. Recommended minimum standards for 800 MHz cellular subscriber units", May 1988.

"Data sheet OM5300, AMPS/TACS hybrid baseband module."

MECHANICAL INFORMATION



Dimensions in mm; maximum volume 29 cm^3.
I/O connector: 14 pins female 1.27 mm (0.05 inch) pitch single row.
RF connection (A): soldering island 3 mm^2 with through plated hole.

Fig.2 Mechanical data.

E-TACS Radio Frequency Module (RFM) OM5302

FEATURES

- Low cost
- Low-voltage operation (4.4 to 6.4 V)
- Low-power consumption
- Light weight
- Easy mounting
- Completely shielded box
- Multiple power-down modes available
- Small volume (29 cm^3)
- Easy design-in with baseband part (e.g. baseband module OM5300)
- Power level control possibility via DC or Pulse Width Modulated (PWM) signal
- 9.6 MHz clock signal output available for microcontroller.

APPLICATION

- E-TACS cellular hand-portable telephone equipment.

GENERAL DESCRIPTION

This Extended-Total Access Communication System (E-TACS) RF Module (RFM) is a stand-alone module intended for use in E-TACS cellular hand-portable telephone equipment. The OM5302 consists of a completely shielded E-TACS receiver and transmitter part.

Output of the receiver part includes demodulated (baseband) audio signal and a field strength indication signal. Input to the transmitter part will be baseband audio signal and output power control signals. A 3-wire bus will be used to provide frequency and switching information to the RFM.

BLOCK DIAGRAM

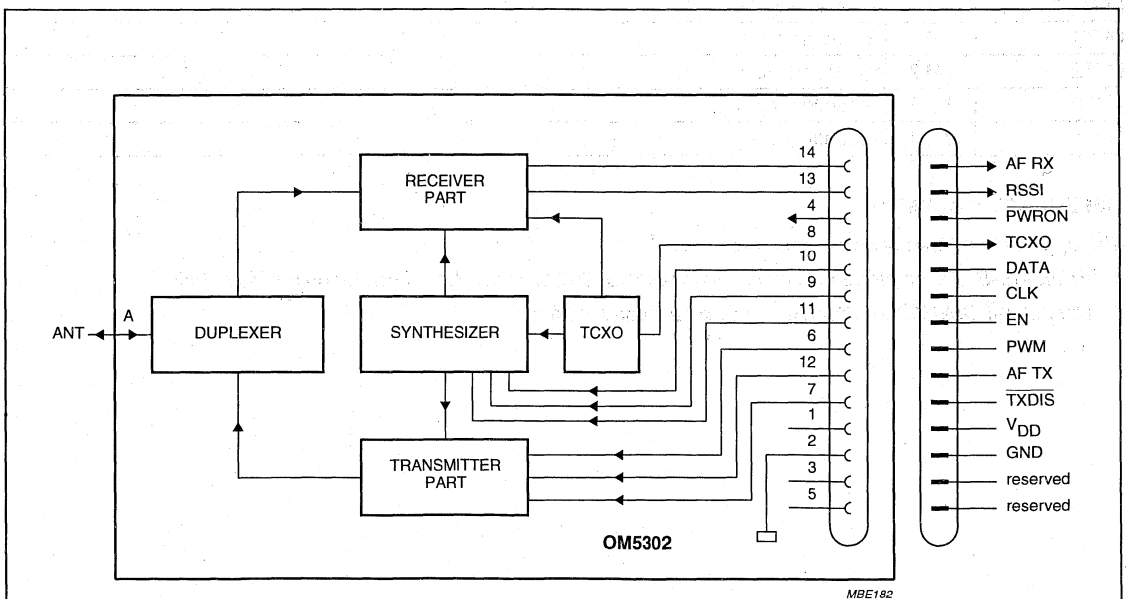


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD}	1	supply voltage (battery)
GND	2	ground
Reserved	3	reserved for future use e.g. receiver disable (RXDIS)
$\overline{PWRON}$	4	module power-on input; active LOW
Reserved	5	reserved for future use e.g. 1.2 MHz output
PWM	6	Pulse Width Modulation input
$\overline{TXDIS}$	7	transmitter disable input; active LOW
TCXO	8	TCXO output (9.6 MHz)
CLK	9	3-wire bus clock input
DATA	10	3-wire bus data input
EN	11	3-wire bus enable input
AF TX	12	transmitter audio input
RSSI	13	received signal strength indication output
AF RX	14	receiver demodulated audio output
ANT	A	antenna input/output
MT1	MT1	mounting tab 1
MT2	MT2	mounting tab 1
MT3	MT3	mounting tab 3
MT4	MT4	mounting tab 4

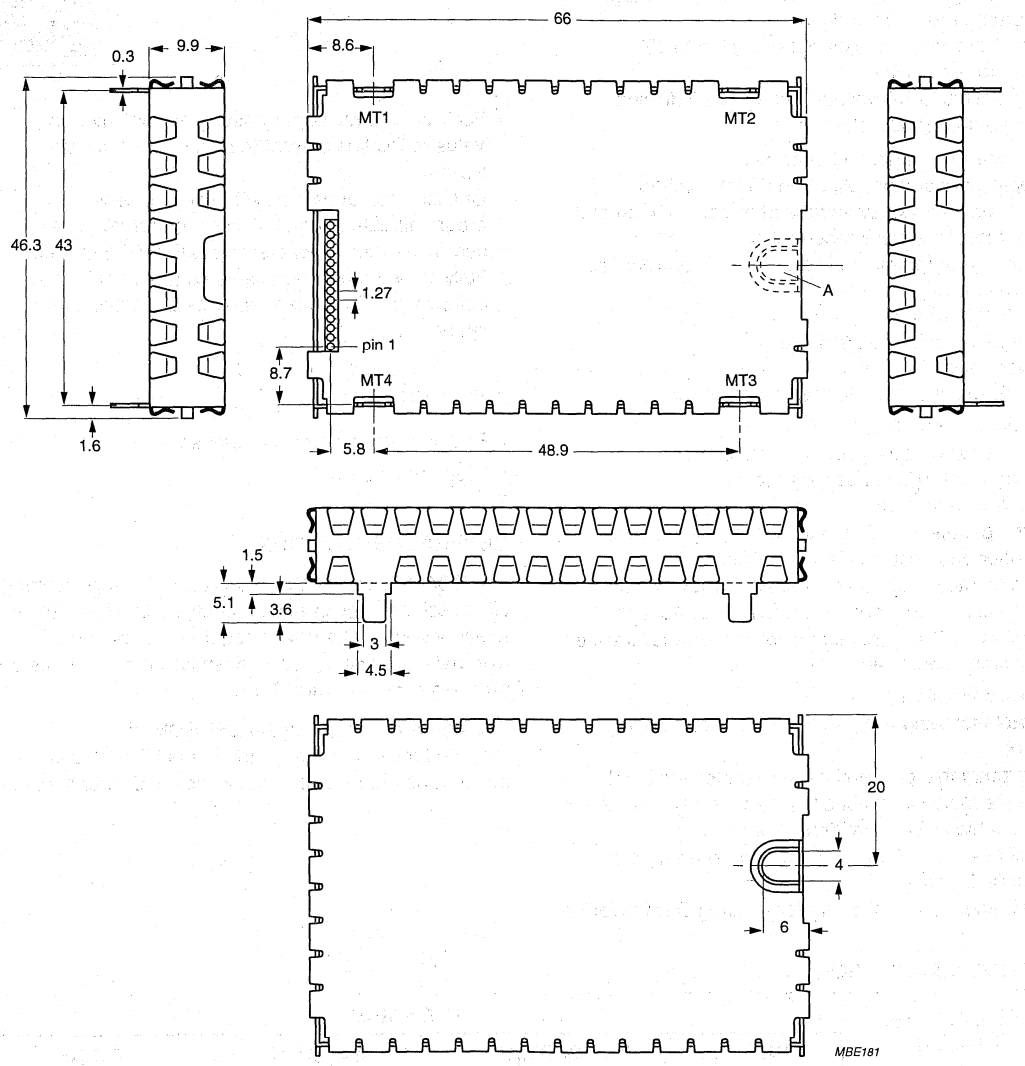
REFERENCE DOCUMENTS

The applicable reference documents are:

"EIA/IS-19-B. Recommended minimum standards for 800 MHz cellular subscriber units", May 1988.

"Data sheet OM5300, AMPS/TACS hybrid baseband module."

MECHANICAL INFORMATION



Dimensions in mm; maximum volume 29 cm^3.
I/O connector: 14 pins female 1.27 mm (0.05 inch) pitch single row.
RF connection (A): soldering island 3 mm^2 with through plated hole.

Fig.2 Mechanical data.

Programmable analog CMOS transmission IC

PCA1070

FEATURES

- Line interface with:
  Voltage regulator with programmable DC voltage drop
  Programmable set impedance
  Output to control an external switching MOS transistor for pulse dialling
  Programmable DC voltage duting pulse dialling
  Circuitry for fast DC start-up
- Interface to peripheral circuits with:
  Supply for microcontroller and DTMF diallers
  Input to sense supply voltage of microcontroller and output for reset of microcontroller
  I²C-bus (programming of parameters, control of all logic signals)
  DTMF signal input
  Input for external oscillator signal
  Power down via I²C-bus
  Stabilized supply for electret microphones
- Microphone amplifier:
  Suitable for various types of microphones
  Symmetrical high impedance inputs
  Programmable gain
  Sending mute via I²C-bus to disable microphone amplifier and enable DTMF amplifier
  Sending mute also to be used as privacy switch
  Dynamic limiting (speech controlled) to prevent distortion of line signal and sidetone; programmable maximum sending level
- Receive amplifier
  Suitable for various types of earpieces (including piezo)
  Programmable gain and hearing protection level
  Receive mute via I²C-bus to disable receive amplifier and enable DTMF confidence tone
  On-chip anti-sidetone circuit with programmable sidetone balance
  Confidence tone in the earpiece during DTMF dialling
- Faciltity to regulate parameters with line current:
  Value of DC line current (bit code) readable via I²C-bus
  Line loss compensation with fully software programmable characteristics (control range, stop current) of microphone/earpiece/DTMF amplifiers
  Fully software programmable control of sidetone balance and DC voltage drop as a function of line length

APPLICATIONS

- Requires few external components
- Programming via I²C-bus

GENERAL DESCRIPTION

The PCA1070 is a CMOS integrated circuit performing all speech and line interface functions in fully electronic telephone sets. The device requires a minimum of external components. The transmission parameters are programmable via the I²C-bus.

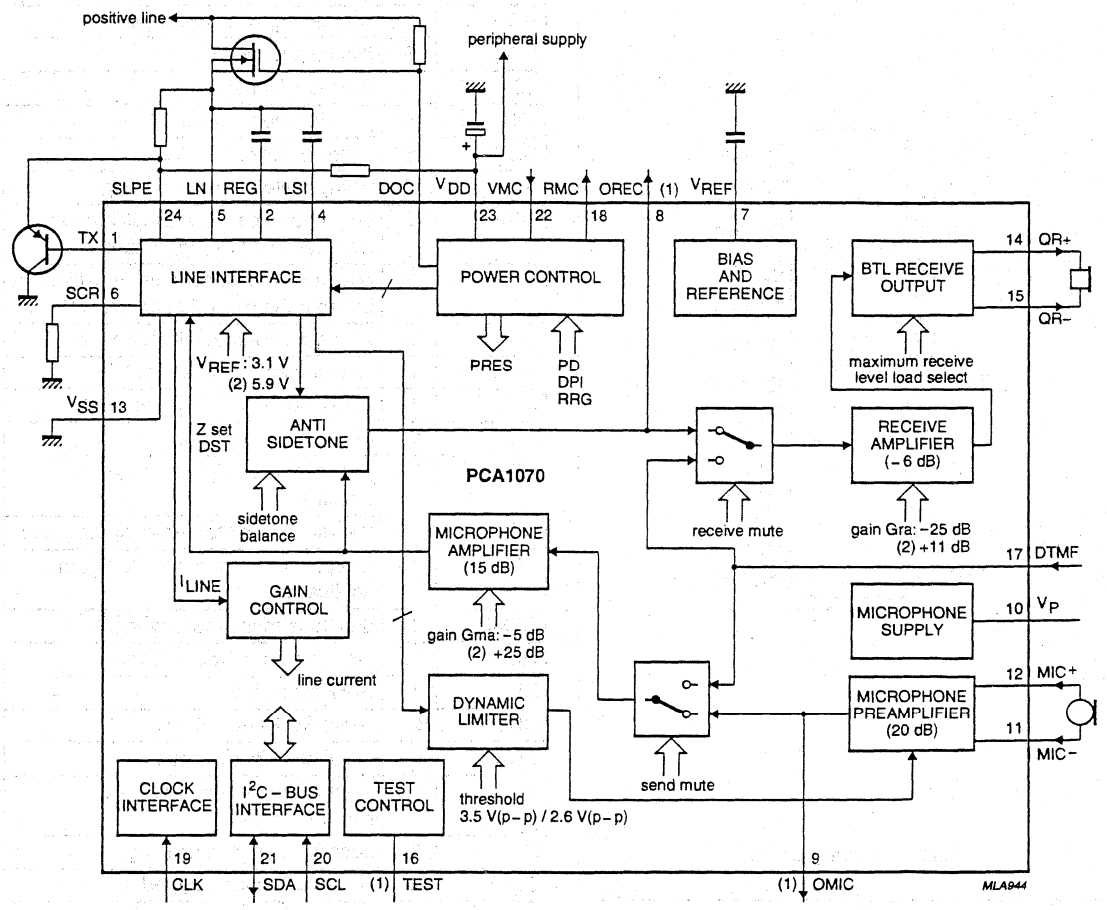
The values are stored in the EEPROM of a microcontroller and are loaded in the PCA1070 during the start-up phase of the transmission IC after hook-off.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA1070P	24	DIL	plastic	SOT101
PCA1070T	24	mini-pack	plastic	SO24; SOT137A

Programmable analog CMOS transmission IC

PCA1070



(1) Test pins.
(2) Default value.

Fig.1 Block diagram.

Programmable analog CMOS transmission IC

PCA1070

PINNING

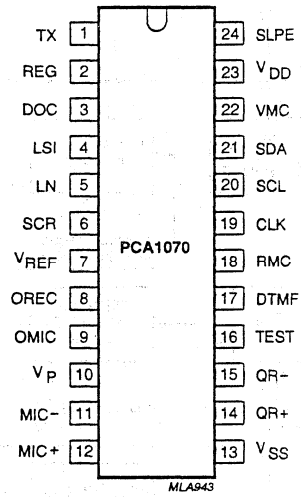


Fig.2 Pin configuration.

SYMBOL	PIN	DESCRIPTION
TX	1	drive output
REG	2	voltage regulator decoupling
DOC	3	dial output connection
LSI	4	line signal input
LN	5	positive line terminal
SCR	6	sending current resistor
V_{REF}	7	voltage reference decoupling
OREC	8	output for receive preamplifier; to be left open-circuit in application
OMIC	9	output for microphone preamplifier; to be left open-circuit in application
V_P	10	supply for electret microphones
MIC–	11	inverting microphone input
MIC+	12	non-inverting microphone input
V_{SS}	13	negative line terminal
QR+	14	non-inverting output for receiving amplifier
QR–	15	inverting output for receiving amplifier
TEST	16	test pin; to be connected to V_{SS} in application
DTMF	17	dual tone multi-freqency input
RMC	18	reset output for microcontroller
CLK	19	clock signal input
SCL	20	serial clock line; I²C-bus
SDA	21	serial data line; I²C-bus
VMC	22	input to sense supply voltage microcontroller
V_{DD}	23	positive supply decoupling
SLPE	24	slope (DC resistance) adjustment

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Paging decoder PCA5000AT

GENERAL DESCRIPTION

The PCA5000AT is a fully integrated decoder for the CCIR Radio Paging Code number 1 (POCSAG-code). It supports two basic modes of operation:

Alert-Only-Pager. This is a stand-alone mode in which the PCA5000AT scans inputs from three external switches that relate to the states ON, OFF and SILENT. Only a few external components are required to build an Alert-Only pager.

Display-Pager. In this mode, received calls and messages are transferred via the IC's serial communication interface to an external microcontroller. A built-in voltage converter can double the supply voltage output and perform level shifting on the interface signals.

Call-alert cadences are generated when valid calls and messages are received, and status cadences to indicate the present state of the decoder are generated following a status interrogation. An on-chip 5 x 9-bit static RAM with battery back-up is provided for programming two user-addresses and for special functions. Synchronization of the input data stream is achieved by the built-in ACCESS algorithm which allows data to be synchronized without preamble detection and minimizes battery power consumption by receiver-enable control. One of three error correction algorithms is applied to received code words to optimize the call success rate.

The PCA5000AT is fabricated in SACMOS-technology to ensure low power consumption at low supply voltages. Typical applications are alert-only pagers, numeric/alphanumeric display pagers, cellular radio and data/telemetry decoders.

Features

- Wide operating supply voltage range (1.7 to 6.0 V)
- Very low supply current (15 μA typ.)
- Decodes CCIR Radio Paging Code number 1
- Data rate: 512 bits/s
- Powerful 'ACCESS' synchronisation algorithm
- Supports two user addresses
- Four cadences per user address
- Silent call storage, up to four different calls
- Interfaces directly to the UAA2033 digital paging receiver
- Directly drives a 2 kHz bleeper
- High-level alert facility requires only a single external transistor
- Receiver-enable control for battery economy
- On-chip static RAM, non-volatile with battery back-up
- On-chip voltage converter
- Level-shifted microcontroller interface
- Battery-low alert
- Out-of-range indication (optional)

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A.)

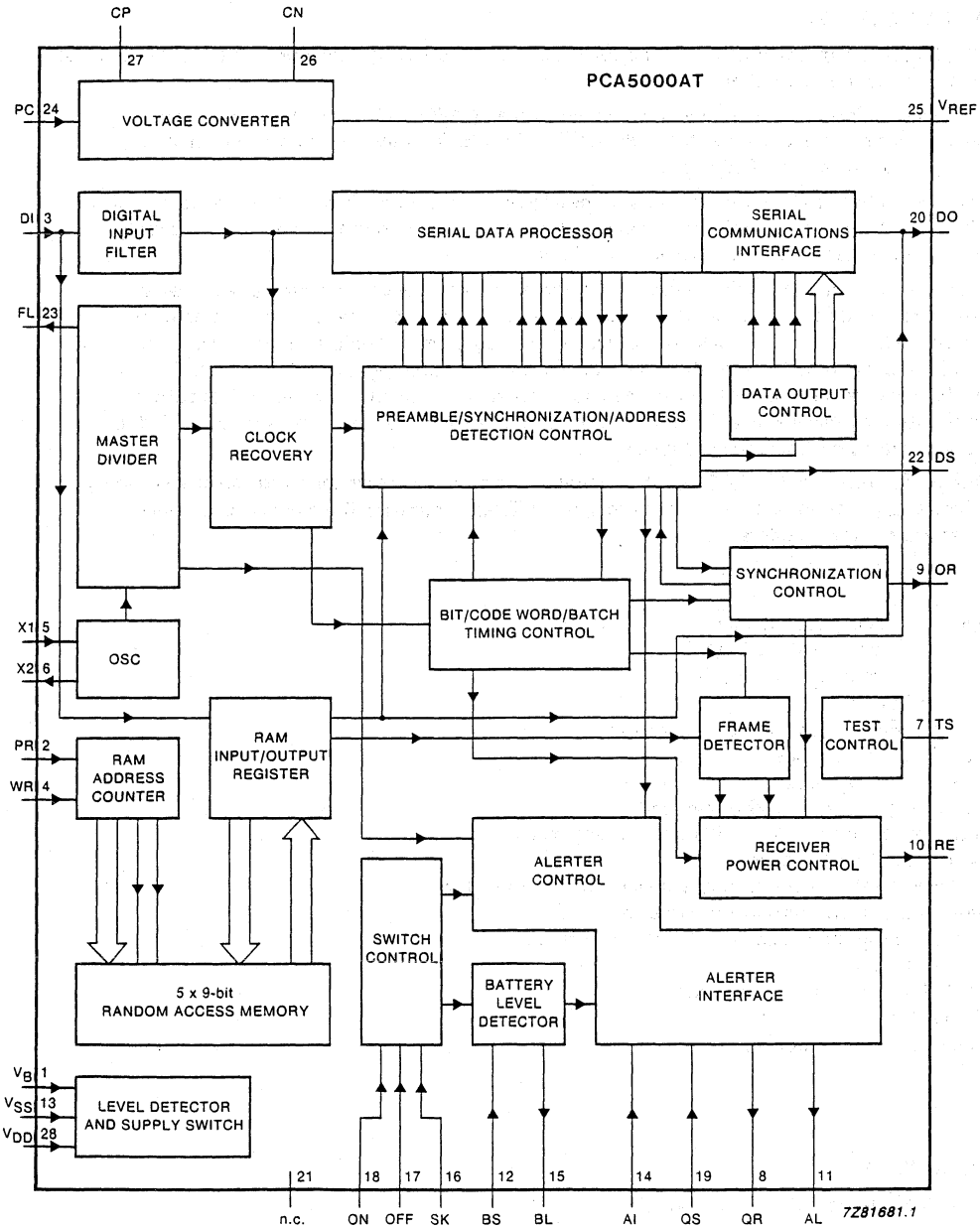


Fig. 1 Block diagram.

PINNING

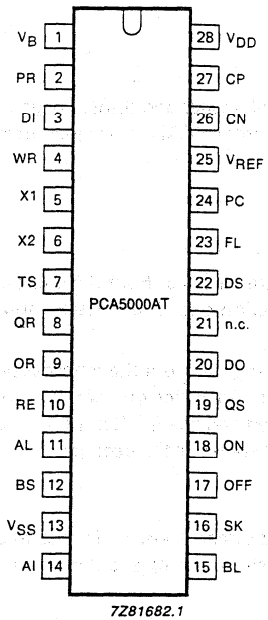


Fig. 2 Pinning diagram.

pin	mnemonic	description
1	V_B	RAM back-up negative supply voltage
2	PR	programming enable input
3	DI	serial data input
4	WR	programming WRITE input
5	X1	oscillator input
6	X2	oscillator output
7	TS	test mode enable input
8	QR	alert high-level output/vibrator output
9	OR	out-of-range output
10	RE	receiver enable output
11	AL	alert low-level output
12	BS	battery sense input
13	V_{SS}	negative supply voltage
14	AI	alarm input
15	BL	battery-low output
16	SK	silent key/mute input
17	OFF	off key/reset input
18	ON	on key/on-off input
19	QS	vibrator enable input
20	DO	received data output
21	n.c.	not connected
22	DS	received data strobe output
23	FL	frequency reference output
24	PC	power control input to voltage converter
25	V_{REF}	microcontroller interface negative reference voltage
26	CN	voltage converter external capacitor (negative)
27	CP	voltage converter external capacitor (positive)
28	V_{DD}	positive supply voltage (common)

FUNCTIONAL DESCRIPTION

Operating modes

The decoder has two basic operating modes; alert-only-pager and display-pager. There is also a programming mode in which the contents of the internal RAM are programmed or verified. The RAM holds two user-addresses and special function bits.

Alert-Only-Pager

No external microcontroller is required in this mode.

Tone-alert cadences are generated when valid calls are received. Four different alert cadences are available and are called by combinations of the function bits. The voltage doubler is disabled in this mode.

The decoder continually scans the inputs ON, OFF and SK from the external switches ON, OFF and SILENT that determine the internal operating status. Operating one of the switches first causes the cadence of the existing internal status to be generated and then, after 1.5 s switch operation, generation of a cadence to indicate the new internal status of the decoder.

Display-Pager

In this mode the decoder receives calls/messages and directs those addressed to one of the two stored user addresses to an external microcontroller for post-processing and display. Tone-alert cadences are generated when valid calls are received.

The decoder provides a doubled supply voltage output to the microcontroller and associated hardware, and the interface signals are level-shifted to allow direct coupling to the microcontroller.

The internal state of the decoder is determined by the logic levels on the static inputs ON and SK.

Internal states

If the decoder is in one of the two operating modes, its internal status is always one of the following:

OFF state. This is the power-saving inactive state in which no decoding takes place and the paging receiver is disabled. Scanning of the ON, OFF and SK inputs is maintained to allow state-changes to be effected.

ON state. This is the normal active state of the decoder. Received calls and messages are compared with the two user addresses stored in the RAM. When the validity of incoming calls is confirmed, appropriate cadences are generated and data is shifted out via the serial microcontroller interface.

SILENT state. This is the same as the ON state except that alert cadences are not generated following valid calls. Instead, if programmed as an alert-only pager, the decoder stores up to four different calls. The appropriate alert cadences are generated after the decoder has been returned to the ON-state. However, special silent override calls will cause generation of alert cadences.

POCSAG code structure

A transmission using the CCIR Radio Paging Code No. 1 (POCSAG code) is structured according to the following rules (see Fig. 3)

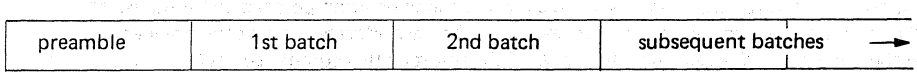
The transmission is started by sending a preamble which is a sequence of at least 576 continually alternating bits (01010101 . . .). The preamble precedes a number of batch blocks. The transmission is terminated after the last batch.

Every batch comprises a synchronisation code word with a fixed 32-bit pattern followed by eight frames (numbered 0 to 7). Only complete batches are transmitted.

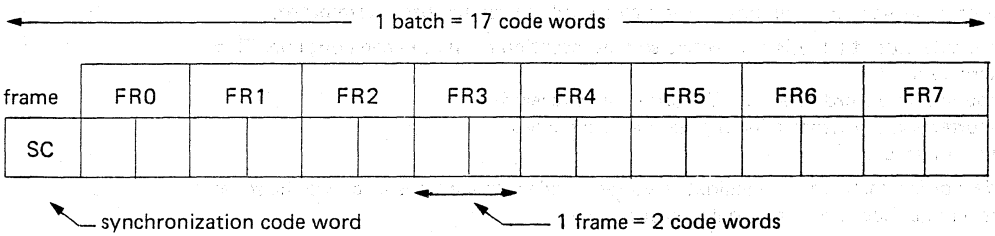
A frame comprises two code words, each 32 bits long. A code word is either an address, message or an idle code word. Idle code words are transmitted to fill empty batches or to separate messages.

An address code word is coded as shown in Fig. 3; 18 bits of the 21-bit user address are coded in the code word and are protected against transmission errors by a CRC check word (bits 22 to 31). The other three bits of the user address are coded in the number of the frame in which the address code word is transmitted. Two function bits (bits 20 and 21) allow distinction between four different calls to one user address.

A message code word contains 20 bits of any information, these are also protected by a check word.



a) Call structure



b) Batch structure

bit

1	2 to 19	20	21	22 to 31	32
0	user address	FC	FC	parity check	

c) Address code word structure (FC are function code bits)

bit

1	2 to 21	22 to 31	32
1	message	parity check	

d) Message code word structure

Fig. 3 POCSAG coding structure.

FUNCTIONAL DESCRIPTION (continued)

Decoding

The POCSAG-coded input data is first noise-filtered by a digital filter. A sampling clock, synchronous to the 512 bits/s data rate, is derived from the filtered data.

Synchronization is performed on the POCSAG code structure using the ACCESS algorithm, which is a five-stage state mechanism.

The decoder first searches the data stream for preamble or synchronization code word patterns. Before synchronism can be achieved, the decoder must ascertain that synchronization code words are correctly positioned at the beginning of each batch. When the correct structure is detected, the decoder switches to the 'receive mode'. (The receiver enable output (RE) is active before input data is required.) Error correction algorithms are applied to the data.
If synchronization is lost (i.e. no synchronization code word found at the beginning of the next batch) the decoder enters a two-step recovery mechanism. In the first step, over the next 15 batches, the decoder attempts to resynchronize by bit-wise shifting its frame window. A 'carrier off' state is entered in the second step, in this the data stream is tested convolutionally for a preamble or synchronization code word at every effective bit position within a continuous stream of at least 17 batches. When synchronization is regained, the decoder returns to the 'receive mode'.

In the 'receive mode', the input data stream is sampled at the frame position pointed to by the RAM program and the sampled code words are error-corrected. If they are address code words, they are compared with the two user addresses from the RAM. If the result of this comparison is 'true', the following actions take place:

- a store is set for a call-alert cadence. The cadence will relate to the combination of the function bits in the accepted code word but will not be generated until the call has been terminated;
- the receiver enable output (RE) is held active so that reception of the call can continue. This condition remains until
  - another address code word or an IDLE instruction is received
  - the error-correction algorithm fails to generate a code word
  - synchronisation is lost;
- message code words attached to the validated address code word are transferred via the serial communication interface to the external microcontroller.

Programming

The on-chip RAM is organized in five 9-bit words (Fig. 4). It is used to store two user addresses (receiver identification codes) and six programmed special function bits. A lithium back-up battery maintains data retention when the main power supply is removed.

	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
word 0	A08	A07	A06	A05	A04	A03	A02	A01	A00
word 1	A17	A16	A15	A14	A13	A12	A11	A10	A09
word 2	B08	B07	B06	B05	B04	B03	B02	B01	B00
word 3	B17	B16	B15	B14	B13	B12	B11	B10	B09
word 4	FR2	FR1	FR0	SP6	SP5	SP4	SP3	SP2	SP1

where:

AXX are 18 bits of user address 'A'
BXX are 18 bits of user address 'B'
FR2 to FR0 are frame number bits common to both addresses 'A' and 'B'
SP6 to SP1 are special function bits.

Fig. 4 RAM organization.

A user address in POCSAG code comprises 21 bits, three of which are coded in the frame number. In the PCA5000AT the frame number is common to both user addresses.

The special function bits are programmable to select from the following:

bit SP1: 0 alert-only-pager mode; silent override enabled on address 'B'
1 display-pager mode

SP2: 0 enable voltage converter (SP1 = 1)
1 disable voltage converter (SP1 = 1); cadence 1 also for FC = 11

SP3: 0 1-bit error-correction on message code words
1 4-bit burst error-correction on message code words on address 'B' (FC = 00 or 11)

SP4: free for user-application

SP5: 0 silent override enabled on address 'B' (FC = 01 or 10)
1 silent override enabled on address 'B' (FC = 00 or 11)

SP6: 0 silent override disabled on address 'A' (FC = 10)
1 silent override enabled on address 'A' (FC = 10)

The programming mode is entered by holding input PR at V_{DD} during power-on; exit from the programming mode is made by removing the main power supply. The back-up battery must remain connected to the PCA5000AT to keep the RAM contents when the main power supply is removed. During programming, inputs ON, OFF and SK must not all be '1' at the same time.

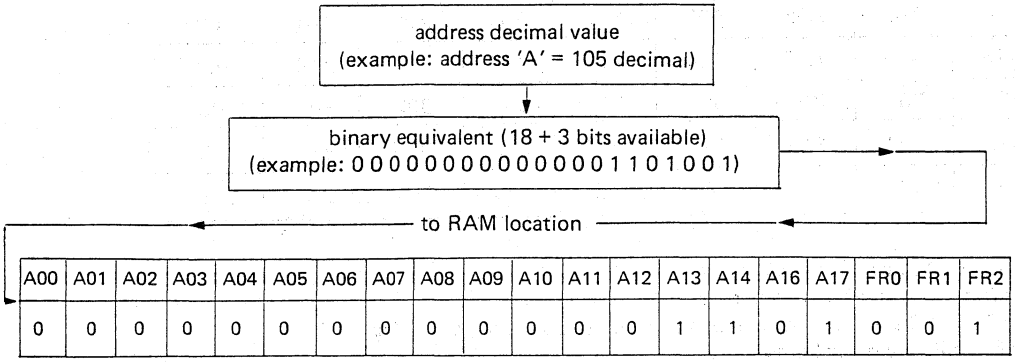
Programming of the RAM and verifying its contents is performed in a sequence starting with word 0, bit 0 and progressing through each of the five words in turn. Input and output is a serial operation; X1 is the shift clock input and DI, DO are respectively the data input and output.

During the RAM programming operation, a negative-going pulse first on WR and then on PR copies the 9 bits just shifted in into the RAM and switches to the next word (see Fig. 10).

During the RAM verify operation, reading the first word is triggered by a negative-going pulse on PR, which also switches to the next word in the sequence after 9 bits have been read (see Fig. 11).

Exit from the programming mode should be made after programming or verification of the RAM contents has been performed on all five words.

FUNCTIONAL DESCRIPTION (continued)



A00	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A16	A17	FR0	FR1	FR2
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1

Fig. 5 Example of bit conversion in user address programming.

Generation of output signals

Alerter interface

The alerter interface provides for the acoustic signalling of calls received (Fig. 8) and of changes of pager status (Fig. 9).

When valid calls are received and the pager is in the ON state, the decoder generates 2 kHz squarewave output signals to produce tone alert cadences via a magnetic or piezoceramic 2 kHz bleeper. The cadence signals differ in modulation according to the two function bits FC in the address code word (Fig. 6b). The PCA5000AT supports two levels of alerter loudness: during the first four seconds, cadences are generated at low intensity (output AL active, output QR inactive); during the following twelve seconds, the intensity is increased (outputs AL and QR both active).

The alert tone generation is automatically terminated after sixteen seconds. Alert cadences are also terminated by an ON, OFF or SILENT input when in alert-only-pager mode, or by pulsing the status/reset input in display-pager mode.

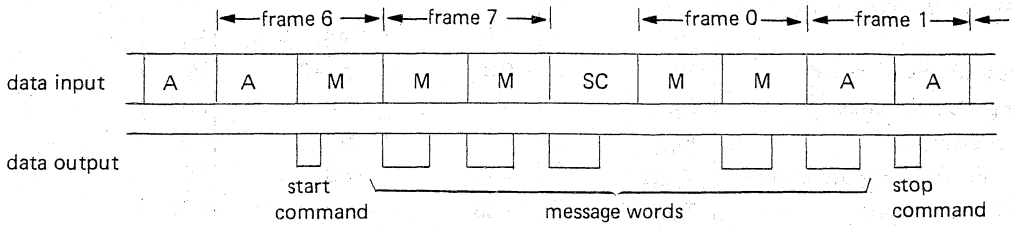
If the call is a message with subsequent message code words, alert cadence generation begins after the message has been terminated.

The alerter generates cadences to indicate the present internal status when interrogated and, when the main supply is low, gives a battery-low indicator output and generates an alarm tone.

Serial communication interface

This interface facilitates communication with an external microcontroller. Data is transmitted serially in the format shown in Fig. 6.

After receiving a valid address code word, transmission commences by sending a start command. The start command contains function data from the RAM, user address called (A or B) and function control bits FC from the address code word. The transmission continues with message words that contain the data from the received message code words. The end of a message transfer is marked by the sending of a stop command or another start command. In a stop command, bit 2 indicates that the call was successfully terminated.



a) Message format

bit	0	1	2	3	4	5	6	7
	0	1	SP3	SP6	SP5	user address A or B	address bit 20 (FC)	address bit 21 (FC)

b) Start command format

bit	0	1	2	3	4 to 23
	1	1	1	1	message code word bits 2 to 21 as received

c) Message word format

bit	0	1	2	3	4	5	6	7
	0	0	successful termination	$\overline{QS}$ input	SP4	SP2	not used	not used

d) Stop command format

Fig. 6 Serial communication interface.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
V_{DD} is referred to as 0 V (ground)

parameter	symbol	min.	max.	unit
Supply voltage	$V_{SS} = V_{13-28}$	+ 0.5	−7.0	V
RAM back-up supply voltage	V_B	V_{SS} + 0.8	−6.0	V
Input voltage on pins ON, OFF, SK, AI, PC, FL, BL, DS, DO	V_I	0.8	V_{REF}−0.8	V
Input voltage on any other pin	V_I	0.8	V_{SS}−0.8	V
Power dissipation per output	P_O	–	100	mW
Total power dissipation	P_{tot}	–	250	mW
Operating ambient temperature range	T_{amb}	−10	+ 60	°C
Storage temperature range	T_{stg}	−55	+ 125	°C

CHARACTERISTICS: Alert-Only-Pager (SP1 = 0)

V_{DD} = 0 V; V_{SS} = −2.7 V; V_{REF} = −2.7 V; V_B = −3.0 V; T_{amb} = 25 °C; quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 12) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	−2.7	−6.0	V
Operating supply current	all outputs open; all inputs at V_{SS}; voltage converter off	I_{SS}	–	–	−22.0	μA
Level at which RAM switches to V_B		$V_{SS(sw)}$	−1.0	–	−1.7	V
Supply current; peak value	AL = LOW	I_{SSM}	–	–	−45.0	mA
Input voltage LOW PR, DI, BS, QS, WR, TS		V_{IL}	0.7 V_{SS}	–	–	V
AI, ON, OFF, SK, PC		V_{IL}	0.7 V_{REF}	–	–	V
Input voltage HIGH PR, DI, BS, QS, WR, TS		V_{IH}	–	–	0.3 V_{SS}	V
AI, ON, OFF, SK, PC		V_{IH}	–	–	0.3 V_{REF}	V

CHARACTERISTICS: Alert-Only-Pager (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input current						
PR, TS, BS	$V_I = V_{DD}$	I_I	7.0	–	18.0	μA
WR	$V_I = V_{SS}$	I_I	−9.0	–	−28.0	μA
DI	$V_I = V_{DD}$; $V_{RE} = V_{SS}$	I_I	6	–	16	μA
PR, TS, BS, DI, QS, PC	$V_I = V_{SS}$	I_I	–	–	−0.1	μA
WR, QS, PC	$V_I = V_{DD}$	I_I	–	–	0.1	μA
AI, ON, OFF, SK,	$V_I = V_{DD}$	I_I	6.0	–	16.0	μA
AI, ON, OFF, SK	$V_I = V_{SS}$	I_I	–	–	−0.1	μA
Input capacitance						
BS, DI, PR, WR, QS, TS		C_I	–	–	5	pF
AI, ON, OFF, SK, PC		C_I	–	–	5	pF
X1		C_I	–	–	5	pF
Output current LOW						
RE, OR, QR	$V_{OL} = -1.35$ V	I_{OL}	10.0	–	–	μA
DO, DS, BL, FL	$V_{OL} = -1.35$ V	I_{OL}	10.0	–	–	μA
AL	$V_{OL} = -1.5$ V	I_{OL}	17.5	–	41.5	mA
Output current HIGH						
RE	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	–	–	μA
OR, QR	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	540	750	μA
DO, DS, BL, FL	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	–	–	μA
AL	AL = high impedance	$-I_{OH}$	–	–	0.2	μA
Output capacitance						
X2		C_O	19	–	23	pF

CHARACTERISTICS: Dispiay-pager; alphanumeric mode (SP1 = 1, SP2 = 1)

CN and CP open circuit;
$V_{DD} = 0$ V; $V_{SS} = -3.0$ V; $V_{REF} = -6.0$ V; $T_{amb} = 25$ °C; quartz crystal f = 32.768 kHz,
$R_{Smax} = 40$ kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	–	−3.0	V
Microcontroller interface negative reference		V_{REF}	V_{SS}	–	−6.0	V
Input current AI, ON, OFF, SK	$V_I = V_{REF}$ or V_{DD}	I_I	–	–	0.1	μA

CHARACTERISTICS: Display-pager; numeric mode (SP1 = 1, SP2 = 0)

220 nF capacitor connected to CN, CP;
V_{DD} = 0 V; V_{SS} = −3.0 V; T_{amb} = 25 °C;
quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	–	−3.0	V
Voltage converter V_{REF} output:						
output voltage	V_{SS} = −3.0 V; no load	V_{REF}	−5.95	–	−6.0	V
	V_{SS} = −2.0 V; I_{VREF} = 150 μA; PC = 0	V_{REF}	−2.7	–	–	V
	V_{SS} = −2.0 V; I_{VREF} = 45 μA; PC = 1	V_{REF}	−2.7	–	–	V
output current	V_{SS} = −2.0 V; PC = 0	I_{VREF}	−150	–	–	μA
	V_{SS} = −2.0 V; PC = 1	I_{VREF}	−45	–	–	μA
Input current AI, ON, OFF, SK	V_I = V_{REF} or V_{DD}	I_I	–	–	0.1	μA

TIMING: Display-pager (SP1 = 1)

V_{DD} = 0 V; V_{SS} = −2.7 V; T_{amb} = 25 °C;
quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency		f_{osc}	–	32.768	–	kHz
Alerter frequency		f_{alert}	–	2048	–	Hz
Data input rate		f_{DI}	–	512	–	bits/s
Frequency reference FL output		f_{FL}	–	16.384	–	kHz
Data input transition time		t_{TDI}	–	–	100	μs
Preamble duration			1125	–	–	ms
Batch duration		t_{BAT}	–	1062.5	–	ms
Bit period		t_{BIT}	–	1.9531	–	ms
Data output rate		f_{DO}	–	512	–	bit/s
Data output transition time	C_L = 5 pF	t_{DTO}	–	–	100	ns
Data strobe clock period		t_{DS}	–	1.9531	–	ms
Data output set-up time		t_{DOS}	–	1.77	–	ms
Data strobe pulse width		t_{DSW}	61	122	–	μs
Data hold time		t_{DH}	30.5	61	–	μs
Call alert period		t_{ALT}	–	16	–	s
Call alert (low level) AL output only		t_{ALL}	–	4.0	–	s
Call alert (high level) QR and AL outputs		t_{ALH}	–	12.0	–	s

parameter	conditions	symbol	min.	typ.	max.	unit
Call alert cycle period		t_{ALC}	–	1.0	–	s
Call alert pulse period		t_{ALP}	–	125	–	ms
Status pulse set-up time		t_{STP}	10.0	330	–	µs
Status pulse duration		t_{STD}	10.0	330	–	µs
Status alert period		t_{STON}	–	62.5	–	ms
Status alert delay		t_{STOF}	–	62.5	–	ms
Receiver control RE transition time	C_L = 5 pF	t_{RXT}	–	–	100	ns
RE establishment time		t_{RXON}	–	31.2	–	ms
Programming:						
data clock period		t_{PDC}	–	100	–	µs
data settling time		t_{PDS}	20.0	–	–	µs
write set-up time		t_{WSU}	20.0	–	–	µs
write pulse width		t_{WP}	10.0	–	–	µs
program input pulse width		t_{PR}	10.0	–	–	µs
program input settling time		t_{PRS}	20	–	–	µs
Power-on reset pulse width		t_{POR}	7.5	–	–	µs
Program start delay time		t_{CSU}	20.0	–	–	µs
Program data hold time		t_{PDE}	10.0	–	–	µs
Data clock period LOW		t_{X1}	10.0	50.0	–	µs

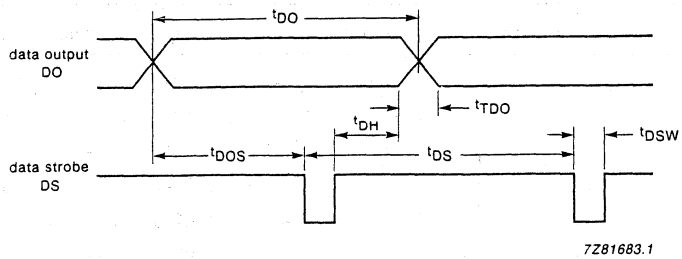


Fig. 7 Serial communications interface timing.

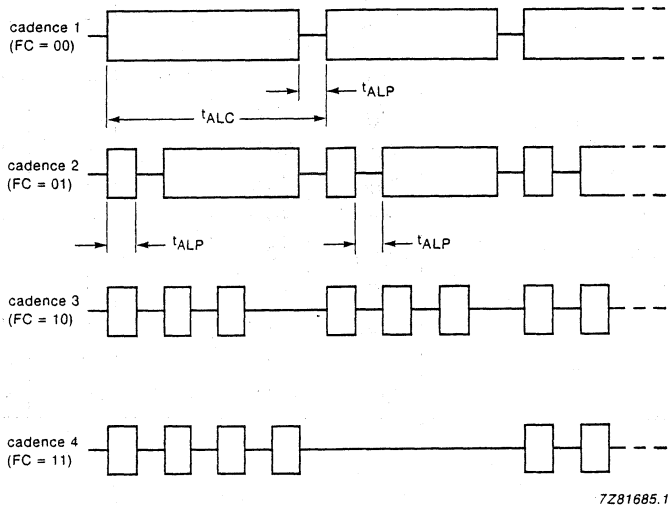


Fig. 8 Call alert cadences; FC refers to function control bits 20 and 21 in the address code word.

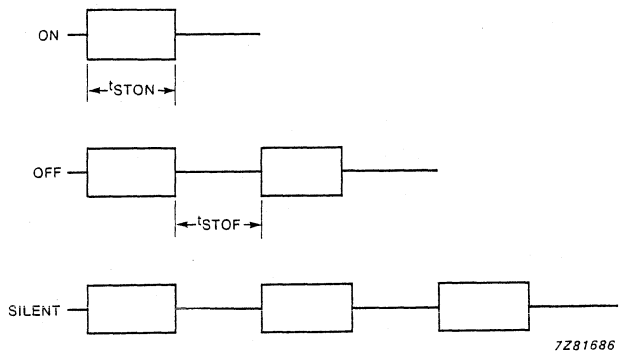


Fig. 9 Status indication cadences.

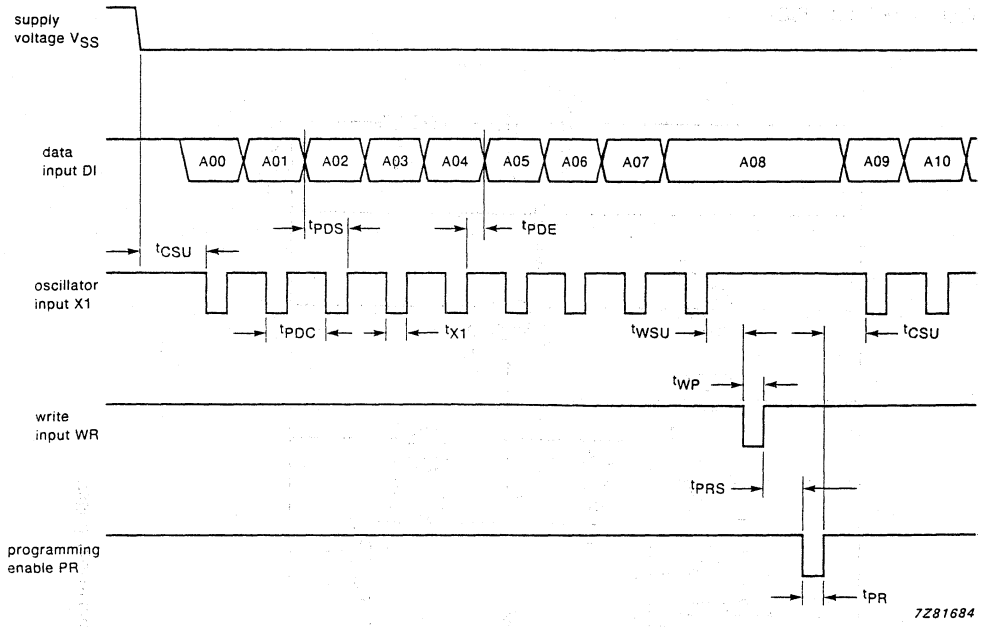


Fig. 10 Timing of RAM programming operation.

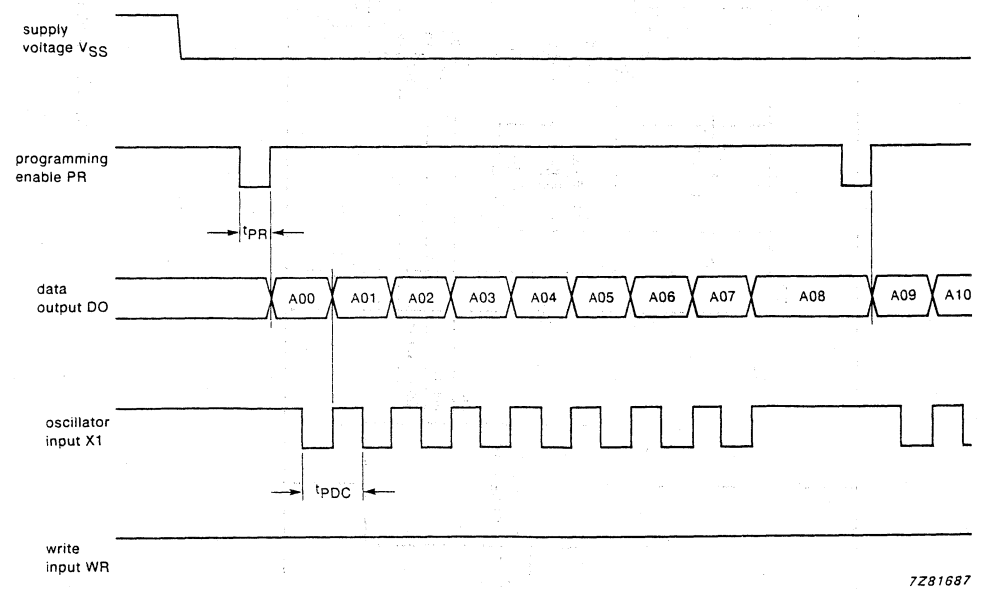


Fig. 11 Timing of RAM verify operation.

APPLICATION INFORMATION

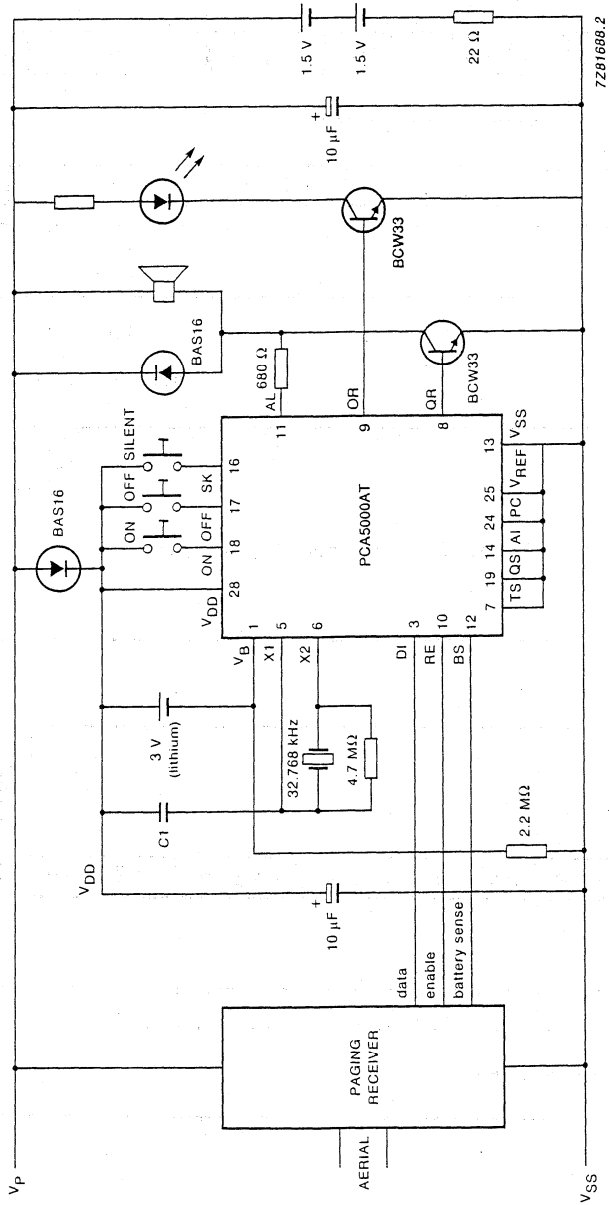


Fig. 12 Example of alert-only pager.

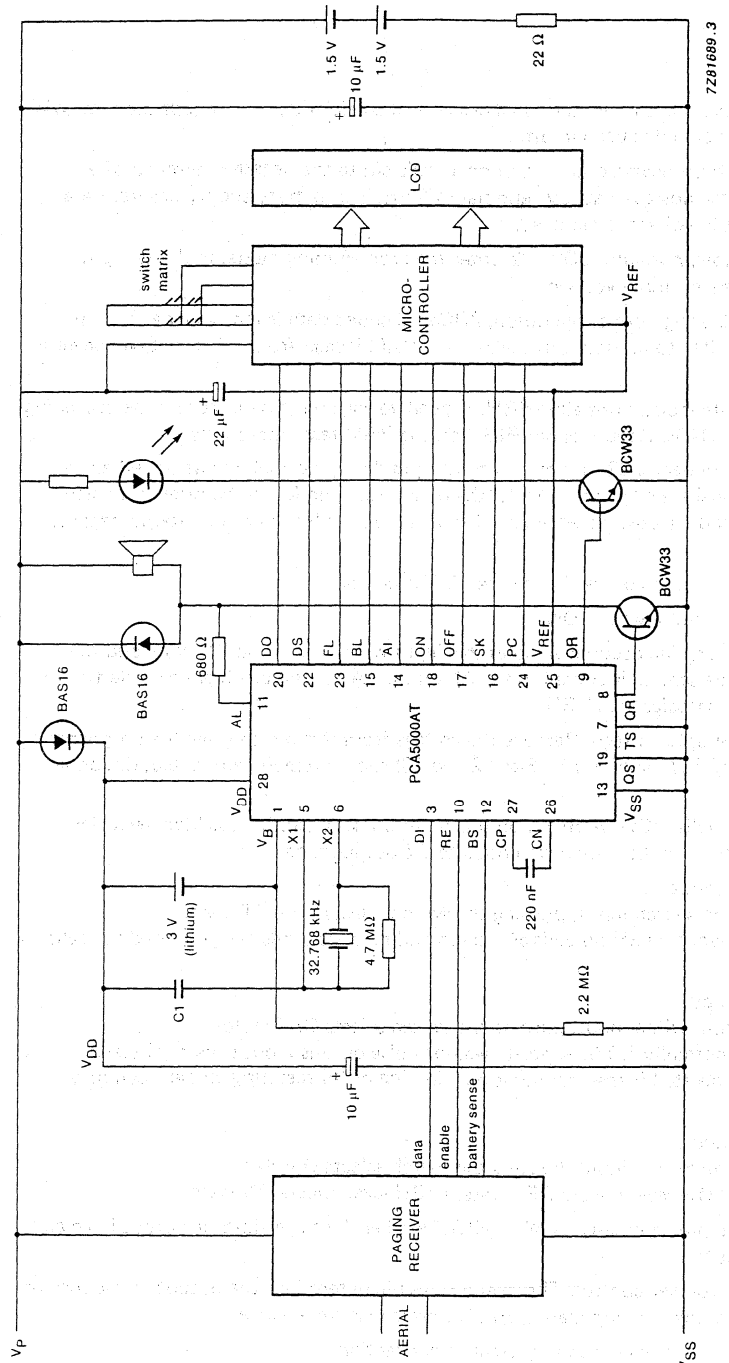


Fig. 13 Example of display-pager in alphanumeric mode with voltage converter enabled.

Application notes

Input pins

The programming control inputs have internal biasing resistors of sufficiently low impedance to provide safe operation even if the pins are left open circuit.

Pin 1 (V_B): RAM back-up battery negative supply. Connect this pin to the negative terminal of a lithium battery and connect the positive battery terminal to V_{DD}. This battery supply ensures data retention when the main supply voltage is removed.

Pin 2 (PR): programming enable, normally LOW. To enter the programming mode, pull this input HIGH when connecting the main supply voltage.

Pin 3 (DI): serial data input. During normal operation, POCSAG-coded data is received via this pin. When in programming mode, data to be stored in the internal RAM is read from this input whenever a pulse on X1 occurs.

Pin 4 (WR): programming write input, normally HIGH. A positive edge on this pin copies the preceding word shifted into the internal RAM. Keep this pin HIGH during RAM-read operations.

Pin 5 (X1): oscillator input. Connect a 32 kHz crystal to this pin during normal operation. When in programming write mode, a positive edge on X1 shifts the data present on DI to the internal register. When in programming read mode, a positive edge on X1 moves the next bit from the internal register to DO.

Pin 6 (X2): oscillator output. Return connection to the 32 kHz crystal.

Pin 7 (TS): test mode enable input, **always** LOW.

Pin 12 (BS): battery sense input. The decoder samples this input when it is in the ON state and the receiver is enabled. Every single sample is copied to the BL output. A continuous high-level alert tone is generated if four sequential samples are HIGH.

Pin 13 (V_{SS}): main negative supply voltage. Remove the voltage from this pin to leave the programming mode. The RC combination of 22 Ω and 10 μF (Figs 12 and 13) should remain connected; disconnect the battery only.

Pin 14 (AI): alarm input, normally LOW. A HIGH on this input causes a continuous high-level alert tone to be generated. The input may be pulsed to modulate the output tone.

Pin 16 (SK): silent key/mute input.
Alert-Only-Pager: push-button switch input, pushing the switch selects SILENT state.
Display-Pager: static input, when HIGH no calls are stored and no alert tones are generated for calls received.

Pin 17 (OFF): off key/reset input.
Alert-Only-Pager: push-button switch input, pushing the switch selects OFF state.
Display-Pager: static input, normally LOW. A positive-going pulse on this input causes (a) status indication cadences to be generated if the decoder is not alerting or (b) resetting an alert call or a battery-low alert if active.

Pin 18 (ON): on key/on-off input.
Alert-Only-Pager: push-button switch input. Pushing the switch selects ON state.
Display-pager: static input. LOW level selects OFF state, HIGH level selects ON state.

Pin 19 (QS): vibrator enable input, normally LOW. A HIGH level enables the vibrator output logic and switches QR to vibrator output.

Pin 24 (PC): voltage converter power control. The level on this pin determines the output impedance of the voltage converter. LOW selects low impedance, HIGH selects high impedance.

Pin 26 (CN): voltage converter external capacitor, negative connection.

Input pins (continued)

Pin 27 (CP): voltage converter external capacitor, positive connection.

Pin 28 (V_{DD}): main positive supply input. This pin is common to all supply voltages and is referred to as GROUND.

Output pins

Pin 8 (QR): alert high-level output/vibrator output. This output can directly drive an external bipolar transistor to control a vibrator-type alerter if QS is set HIGH, or supports high-level alerting in conjunction with AL.

Pin 9 (OR): out-of-range output, active HIGH. If the decoder detects 'carrier-off', an output is generated for the duration of the synchronization scan period. Connecting OR to QR provides alert tone generation during 'carrier-off'.

Pin 10 (RE): receiver enable output, active HIGH. Connect the radio paging receiver power control input to this pin to minimize power consumption. Whenever no input data is required, the PCA5000AT will disable the paging receiver to conserve power.

Pin 11 (AL): alert low-level output, active LOW. The low-level alert tone is generated via this output; the alert becomes high-level in conjunction with QR.

Pin 15 (BL): battery-low output, active HIGH. Every time the PCA5000AT samples the BS input, data sensed is output on this pin.

Pin 20 (DO): received data output. During normal operation, accepted calls and possibly subsequent message code words are output via this pin at a rate of 512 bits/s. When in programming read mode, data read from the internal RAM is presented bit-by-bit on this pin.

Pin 22 (DS): received data strobe output, active LOW. In normal operation, every time this output goes LOW, the next bit on the DO output is valid.

Pin 23 (FL): frequency reference output. If the decoder is programmed as a Display-Pager, a 16 kHz squarewave reference is output from this pin.

Pin 25 (V_{REF}): microcontroller interface negative reference voltage. The LOW level of pins FL, BL, DO, DS, AI, ON, OFF, SK and PC is related to the voltage on V_{REF}.
Alert-Only-Pager: Connect V_{REF} output to V_{SS}.
Display-Pager: The doubled negative supply voltage generated by the internal voltage converter is output from V_{REF}. The V_{REF} pin may also be driven from an external supply if the capacitor across CN/CP is removed and CN/CP are left open circuit.

128 × 8-bit EEPROM with I²C-bus interface PCA8581; PCA8581C

FEATURES

- Operating supply voltage:
  - 4.5 to 5.5 V (PCA8581)
  - 2.5 to 6.0 V (PCA8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current; maximum 10 µA
- 8-byte page write mode
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for minimum 10000 write cycles per byte
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582
- Operating temperature: −25 to +85 °C.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

GENERAL DESCRIPTION

The PCA8581 and PCA8581C are low power CMOS EEPROMs with standard and wide operating voltages:

4.5 to 5.5 V (PCA8581)

2.5 to 6.0 V (PCA8581C).

In the following text, the generic term 'PCA8581' is used to refer to both types in all packages except when otherwise specified.

The PCA8581 is organized as 128 words of 8-bytes.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to 8 bytes can be written in one operation, reducing the total write time per byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage				
	PCA8581		4.5	5.5	V
	PCA8581C		2.5	6.0	V
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	10	µA
T_{amb}	operating ambient temperature		−25	+85	°C
T_{stg}	storage temperature	without EEPROM retention	−65	+150	°C
		with EEPROM retention	−65	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA8581P	8	DIP	plastic	SOT97-1
PCA8581CP	8	DIP	plastic	SOT97-1
PCA8581T	8	SO8	plastic	SOT96-1
PCA8581CT	8	SO8	plastic	SOT96-1

BLOCK DIAGRAM

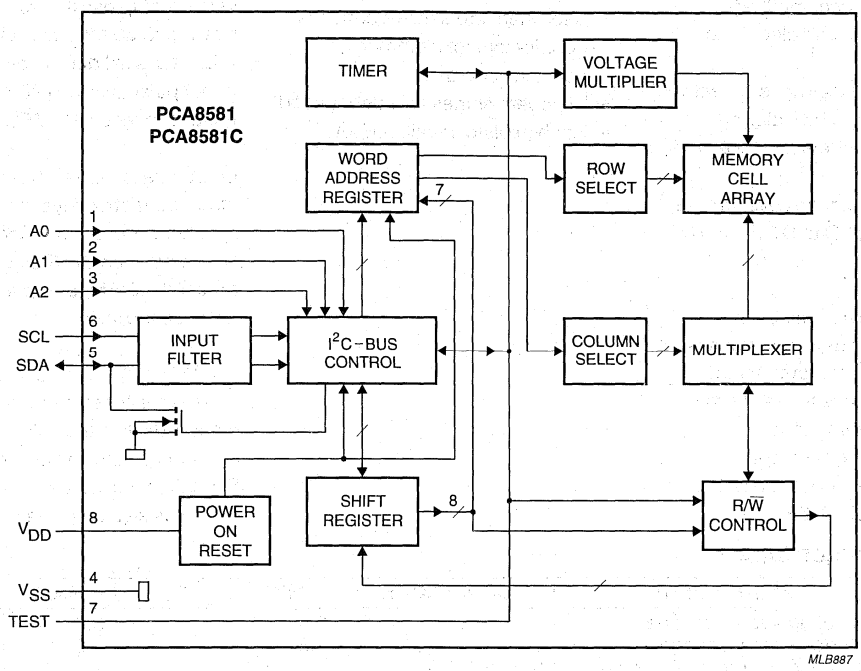


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output can be connected to V_{SS}, V_{DD} or left open-circuit
V_{DD}	8	positive supply

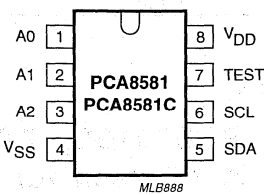


Fig.2 Pin configuration.

Pulse and DTMF dialler with redial PCD3310 family

FEATURES

- Pulse and DTMF dialling
- 23-digit capacity for redial operation (cursor method)
- Memory clear and electronic notepad
- Mixed-mode dialling: start with PD and end with DTMF dialling
- Dual redial buffers for PABX and public calls
- Four extra function keys; program, flash, redial, PD to DTMF (mixed dialling)
- DTMF timing:
  manual dialling - minimum duration for bursts and pauses
  re-dialling - calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3.58 MHz (tv colour burst) crystal or piezo resonator
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

GENERAL DESCRIPTION

The PCD3310 family are single-chip silicon gate CMOS integrated circuits with on-chip oscillators suitable for use with 3.58 MHz crystals. They are dual-standard dialling circuits for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either DP or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time. For data communication mix mode dialling is also possible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		2.5	-	6.0	V
V_{DDO}	standby supply voltage		1.8	-	6.0	V
I_{DDO}	low standby current (on hook)	V_{DDO} = 1.8 V	-	-	2	µA
	operating currents	V_{DD} = 3.0 V				
I_{DDC}	conversation mode		-	-	150	µA
I_{DDP}	pulse dialling mode		-	-	200	µA
I_{DDF}	DTMF dialling mode		-	-	0.9	µA
	DTMF output voltage level		-	192	-	mV
$V_{HG(rms)}$	HIGH group		-	150	-	mV
$V_{LG(rms)}$	LOW group					
ΔV_G	pre-emphasis of group		-	2.1	-	dB
THD	total harmonic distortion		-	–25	-	dB
Tamb	operating ambient temperature range		–25	-	+ 70	°C

Note:

the PCD3310C, PCD3310E, PCD3310F and PCD3310H are not to be used for new design-ins.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3310XP*	20	DIL	plastic	SOT146
PCD3310XT*	28	SO28	plastic	SO28; SOT136A

* When ordering 'X' is replaced by one of the letters A, C, E, F, G, H or nothing.

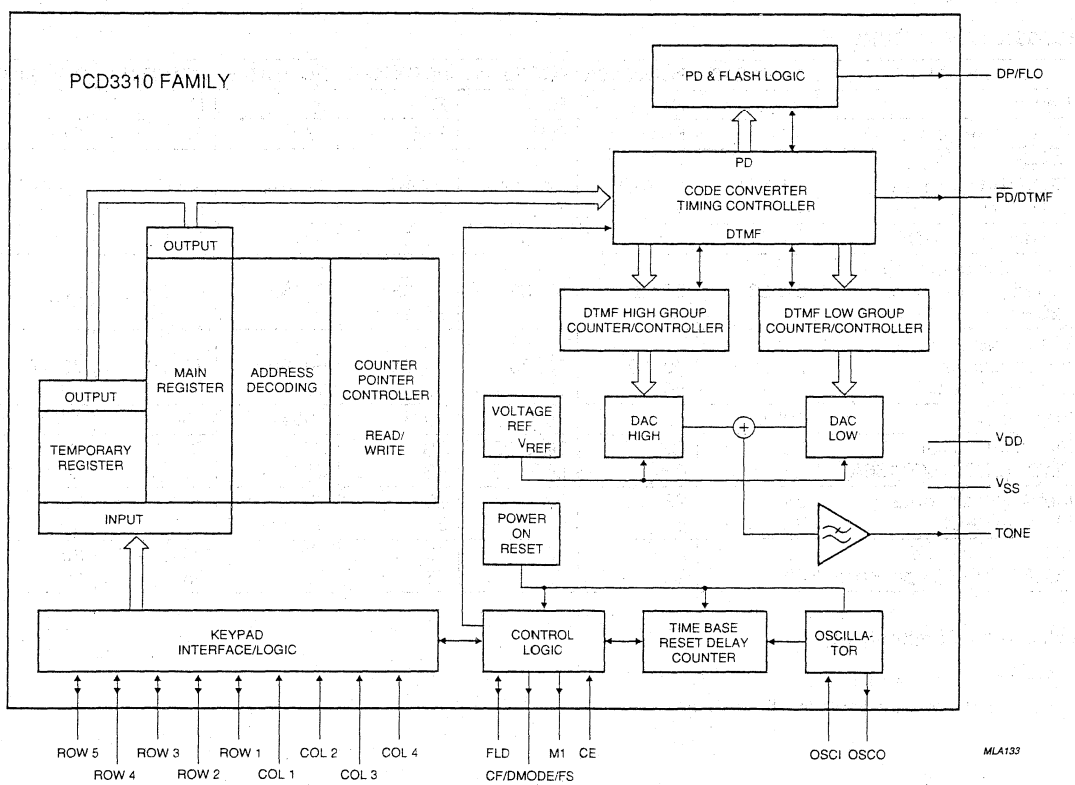


Fig.1 Block diagram.

Table 1 The PCD3310 family of ICs.

PCD3310	P/T dialler with redial, notepad, 4 x 5 keypad, flash, mark/space ratio 2:1, PABX register, automatic access pause control access to the cursor method.
PCD3310A	item PCD3310 with 3:2 mark/space ratio
PCD3310C	item PCD3310 with dialling mode output
PCD3310E	item PCD3310 with also 20 Hz pulse dialling
PCD3310F	item PCD3310 with DTMF timing of 60/90 ms
PCD3310G	item PCD3310 during switch over to data mode the '*' and '#' keys do not send out their corresponding tones
PCD3310H	item PCD3310 M1 replaced by M2

PCD3310 FAMILY SURVEY

FUNCTION	PCD3310	PCD3310A	PCD3310C	PCD3310E	PCD3310F	PCD3310G	PCD3310H
Redial key	R	R	R	R	R	R	R
Notepad keys; note 1	P/R	P/R	P/R	P/R	P/R	P/R	P/R
Mixed mode entry PD-DTMF + tone PD-DTMF no tone	 * # A-D >	 * # A-D >	 * # A-D >	 * # A-D >	 * # A-D >	 A-D > * #	 * # A-D >
Keypad (4x5, A-D)	3 x 5	3 x 5	3 x 5	3 x 5	3 x 5	3 x 5	3 x 5
Pulse dial; break/make 10 Hz, t_{id} = 840 ms 20 Hz, t_{id} = 504 ms	 67, 33	 60, 40	 67, 33	 67, 33 34, 17	 67, 33	 67, 33	 67, 33
DTMF dial: tone/pause (ms) mute hold-over	 70, 70 80	 70, 70 80	 70, 70 80	 70, 70 80	 60, 90 100	 70, 70 80	 70, 70 80
Flash (ms)	100+	100+	100+	100+	100+	100+	100+
Pin 15 (SOT146) Pin 20 (SO28; SOT136A)	CF CF	CF CF	DMODE DMODE	FS FS	CF CF	CF CF	CF CF
Memory main, data Memory PABX	23 5	23 5	23 5	23 5	23 5	23 5	23 5
SOT146 package SO28/SOT136A package	20 28	20 28	20 28	20 28	20 28	20 28	20 -

Notes to the Family survey

1. P = program, R = dial.
2. PCD3310H only available in DIL package.

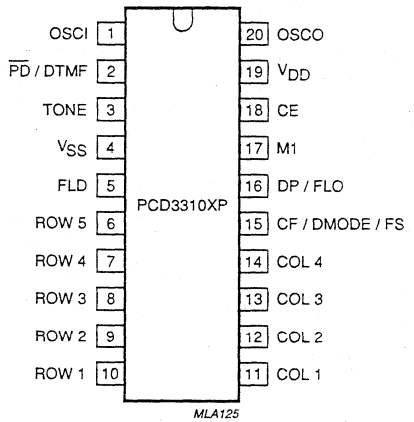


Fig.2 Pinning diagram; PCD3310XP.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input
$\overline{PD}$/DTMF	2	select pin; pulse or DTMF dialling
TONE	3	single or dual tone frequency output
V_{SS}	4	negative supply
FLD	5	flash duration control input/output
ROW 5	6	scanning row keyboard input/output
ROW 4	7	scanning row keyboard input/output
ROW 3	8	scanning row keyboard input/output
ROW 2	9	scanning row keyboard input/output
ROW 1	10	scanning row keyboard input/output
COL 1	11	sense column keyboard input
COL 2	12	sense column keyboard input
COL 3	13	sense column keyboard input
COL 4	14	sense column keyboard input
CF/DMODE/FS	15	confidence tone output, dialling mode output, frequency select
DP/FLO	16	dialling pulse and flash output
M1	17	muting output
CE	18	chip enable input
V_{DD}	19	positive supply
OSCO	20	oscillator output

Note: COL1 to COL4 have internal pull-ups.

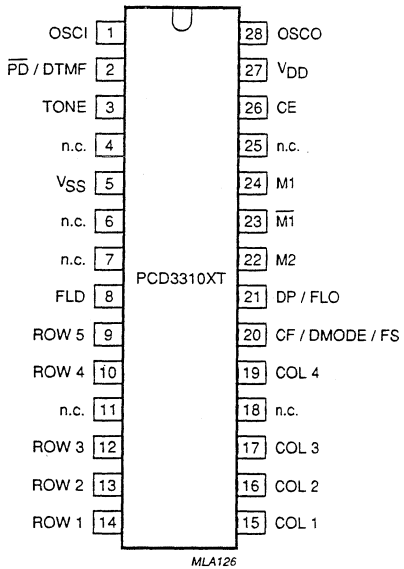


Fig.3 Pinning diagram for PCD3310XT.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input
$\overline{PD}$/DTMF	2	select pin; pulse or DTMF dialling
TONE	3	single or dual tone frequency output
n.c.	4	not connected
V_{SS}	5	negative supply
n.c.	6	not connected
n.c.	7	not connected
FLD	8	flash duration control input/output
ROW 5	9	scanning row keyboard input/output
ROW 4	10	scanning row keyboard input/output
n.c.	11	not connected
ROW 3	12	scanning row keyboard input/output
ROW 2	13	scanning row keyboard input/output
ROW 1	14	scanning row keyboard input/output
COL 1	15	sense column keyboard input
COL 2	16	sense column keyboard input
COL 3	17	sense column keyboard input
n.c.	18	not connected
COL 4	19	sense column keyboard input
CF/DMODE/FS	20	confidence tone output, dialling mode output, frequency select
DP/FLO	21	dialling pulse and flash output
M2	22	strobe; active HIGH during transmission
$\overline{M1}$	23	inverted mute output
M1	24	muting output
n.c.	25	not connected
CE	26	chip enable input
V_{DD}	27	positive supply
OSCO	28	oscillator output

Note: COL1 to COL4 have internal pull-ups.

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the DC characteristics. To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters. If V_{DD} drops below the minimum standby supply voltage of 1.8 V the power-on reset circuit inhibits re-dialling after hook-off. The power-on reset signal has the highest priority; it blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI; OSCO)

The time base for the circuit for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3.58 MHz crystal or ceramic resonator between the OSCI and OSCO pins.

Recommended resonator type:

- 3.58 MHz PXE - Murata; CSA 3.58MG310VA.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the device.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) and Temporary WriteAddress Counter (TWAC) which point to the last entered digit (see Fig.6). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO\ (min)}$. The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or re-dialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for longer than time period t_{rd} (see Fig.10a, Fig.10b and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system changes to the static standby state. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse mode is selected. Entries of non-numeric keys are neglected, they are neither stored in the redial register nor transmitted.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each non-function key activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations. Harmonic content is filtered out thus meeting the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual key depression time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Mixed mode

When the $\overline{PD}$/DTMF pin is open-circuit the mixed mode is selected. After activation of CE or FL (Flash) the circuit starts as a pulse dialler and remains in this state until a non-numeric key (A, B, C, D, *, # or >) is activated. The circuit then changes to DTMF dialling for data communication and remains in this state until FL is activated or after a static standby condition when CE is re-activated.

A connection between the $\overline{PD}$/DTMF pin and V_{DD} also initiates DTMF dialling. Chip enable, FL or a connection of $\overline{PD}$/DTMF pin to V_{SS} sets the circuit back to pulse dialling.

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 5 of the circuit are connected to the keyboard as shown in Fig.4. All keyboard entries are debounced on both the leading and trailing edges for approximately time period t_e as shown in Fig.11. Each entry is tested for validity. When a key is depressed, keyboard scanning starts and only returns to the sense mode after release of that key.

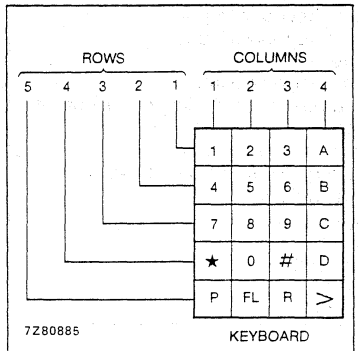


Fig.4 Keyboard organization.

Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall
- R redial
- > change of dial mode from PD to DTMF in mixed dialling mode

In pulse dialling mode the valid keys are the 10 numeric keys (0 to 9). The non-numeric keys (A, B, C, D, *, #) have no effect on the dialling or the redial storage. Valid function keys are P, R and FL.

In DTMF mode all non-function keys are valid. They are transmitted as a dual tone combination and at the same time stored in the redial register. Valid function keys are P, L and R.

In mixed mode all key entries are valid and executed accordingly.

Flash duration control (FLD)

Flash (or register recall) is activated by the FL key and can be used in DTMF and pulse dialling modes. Pressing the FL key will produce a timed line-break of 100 ms (min.) at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. The flash pulse duration (t_{FL}) is calibrated and can be prolonged with an external resistor and capacitor connected to the FLD input/output (see Fig.5). The flash pulse resets the Read Address Counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number). The counter of the reset delay time is held during the period of t_{FL}.

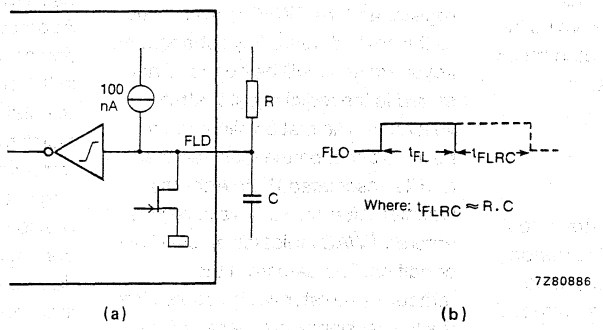


Fig.5 Flash pulse duration setting.

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter. Hence, the total harmonic distortion of the DTMF tones meets the CEPT CS 203 recommendations. The tone output has following states:

- tone OFF; 3-state
- tone ON; the associated frequencies are superimposed on a DC level of 1/2 V_{DD}.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS} and Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

Table 1 Frequency tolerance of the output tones for DTMF signalling; f_{XTAL} = 3.579545 MHz.

ROW/ COLUMN	STANDARD FREQUENCY (Hz)	TONE OUTPUT FREQUENCY (Hz)	FREQUENCY DEVIATION	
			%	Hz
Row 1	697	607.90	+ 0.13	+ 0.90
Row 2	770	770.46	+ 0.06	+ 0.46
Row 3	852	850.45	−0.18	−1.55
Row 4	941	943.23	+ 0.24	+ 2.23
Col 1	1209	1206.45	−0.21	−2.55
Col 2	1336	1341.66	+ 0.42	+ 5.66
Col 3	1477	1482.21	+ 0.35	+ 5.21
Col 4	1633	1638.24	+ 0.32	+ 5.25

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. It is also active HIGH during flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD3310P it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break or make time in pulse dialling, or during tone ON/OFF in DTMF dialling. It is an open drain p-channel output.

DIALLING PROCEDURES
(see Figs.8 to 10)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig.6). By entering the first valid digit, the Temporary Write Address Counter (TWAC) will be set to the first address, the decoded digit will be stored in the register and the TWAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. The first 5 valid entries have no effect on the main register and its associated Write Address Counter. After the sixth valid digit is entered TWAC indicates an overflow condition. The data from the temporary register will be copied into the 5 least significant places of the main register and TWAC into the WAC. All following digits (including the sixth digit) will be stored in the main register (a total of not more than 23). If more than 23 digits are entered redial will be inhibited. If not more than 5 digits are entered only the temporary register and the associated TWAC are affected. Allentries are debounced on both the leading and trailing edges for at least time period t_e as shown in Fig.11. Each entry is tested for validity before being stored in the redial register.

- In DTMF mode all non-function keys are valid
- In PD mode only numeric keys are valid

Simultaneous to their acceptance and corresponding to the selected mode (PD, DTMF or mixed), the entries are transmitted as PD pulse-trains or as DTMF frequencies in accordance with postal requirements. Non-numeric entries are neglected during pulse dialling, they are neither stored nor transmitted.

Re-dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The circuit is in the conversation mode. If "R" is the first keyboard entry the circuit starts re-dialling the contents of the temporary register. If the overflow flag of the TWAC was set in the previous dialling, the re-dialling continues in the main register. If the flag was not set, the number residing in the temporary register will only be redialled until the temporary read and write registers are equal.

Before pressing "R" a dialling sequence with up to 4 digits is possible. If the digits are equal to the corresponding ones in the main register, then redial starts in the main register until the last digit stored is transmitted.

Timing in the DTMF mode is calibrated for both tone bursts and pauses.

In mixed mode only the first part entered (the pulse dialled part of the stored number) can be redialled.

During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of re-dialling. No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory clear ("P" without successive data entry)
- Memory overflow (more than 23 valid data entries)

Notepad

The redial register can also be used as a notepad. In conversation mode a number with up to 23 digits can be entered and stored for re-dialling. By activating the program key (P) the WAC and TWAC pointers are reset. This acts like a memory clear (redial is inhibited). Afterwards, by entering and storing any digits, re-dialling will be possible after flash or hook on and off.

During notepad programming the numbers entered will neither be transmitted nor is the mute active, only the confidence tone is generated.

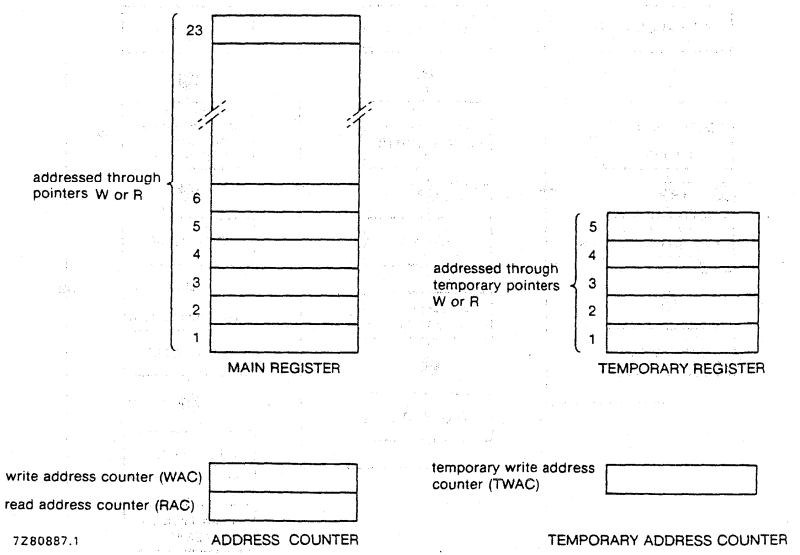


Fig.6 Program memory map.

Note to Fig.6

1). If [access digit(s) + external number] ≤ 23 digits.

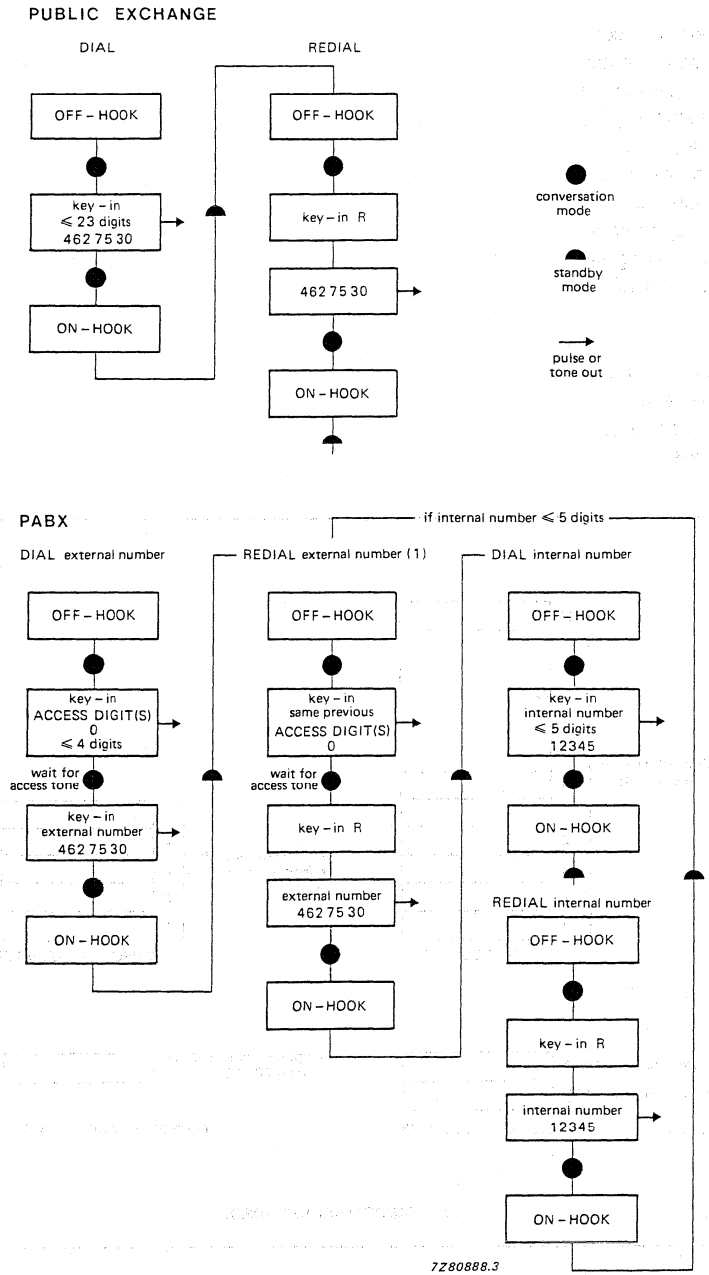


Fig.7 PD or DTMF dialling mode.

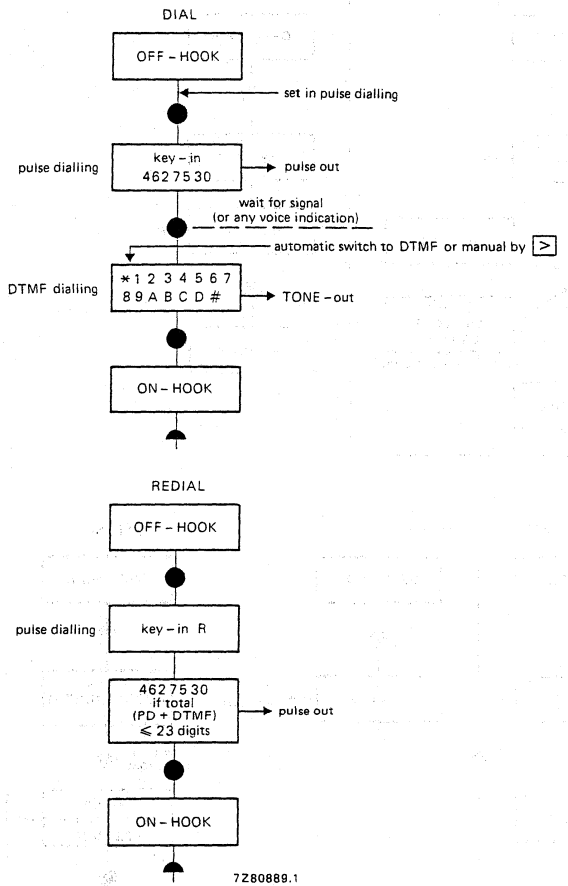


Fig.8 PD/DTMF mixed-mode dialling.

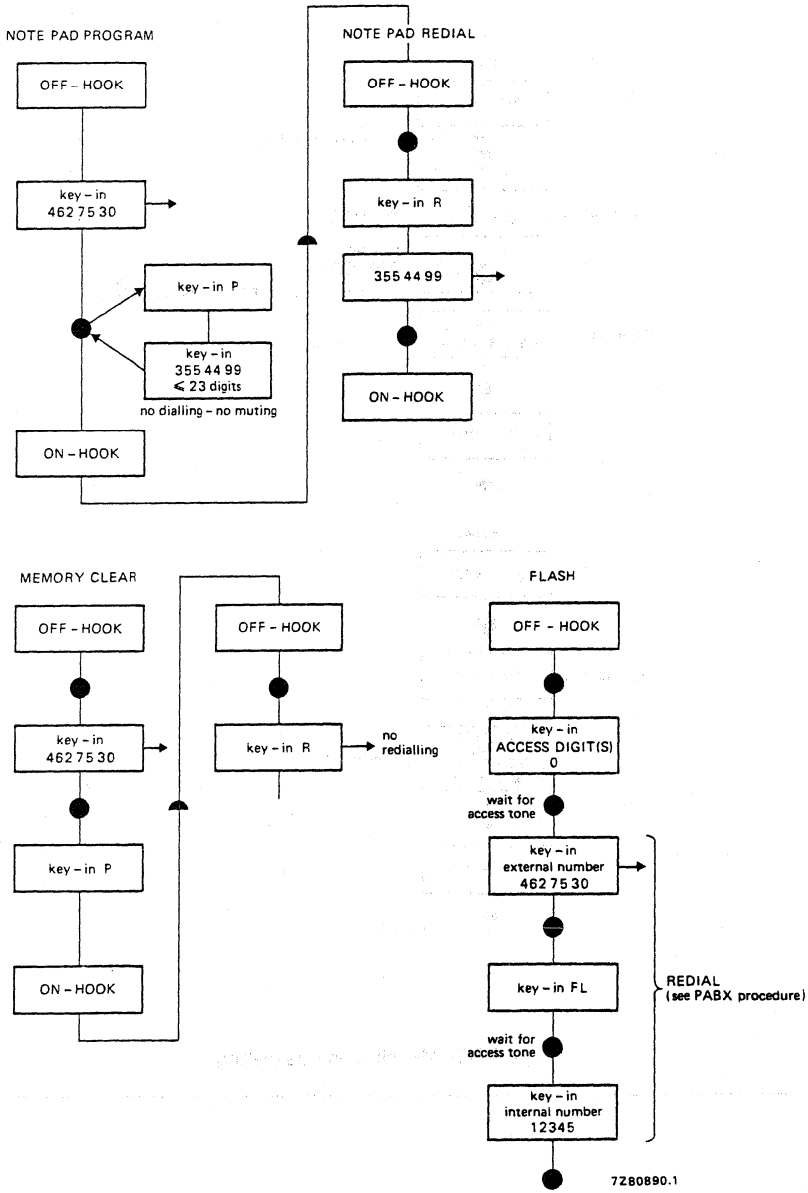


Fig.9 Notepad, memory clear, flash; independent of dialling mode

TIMING

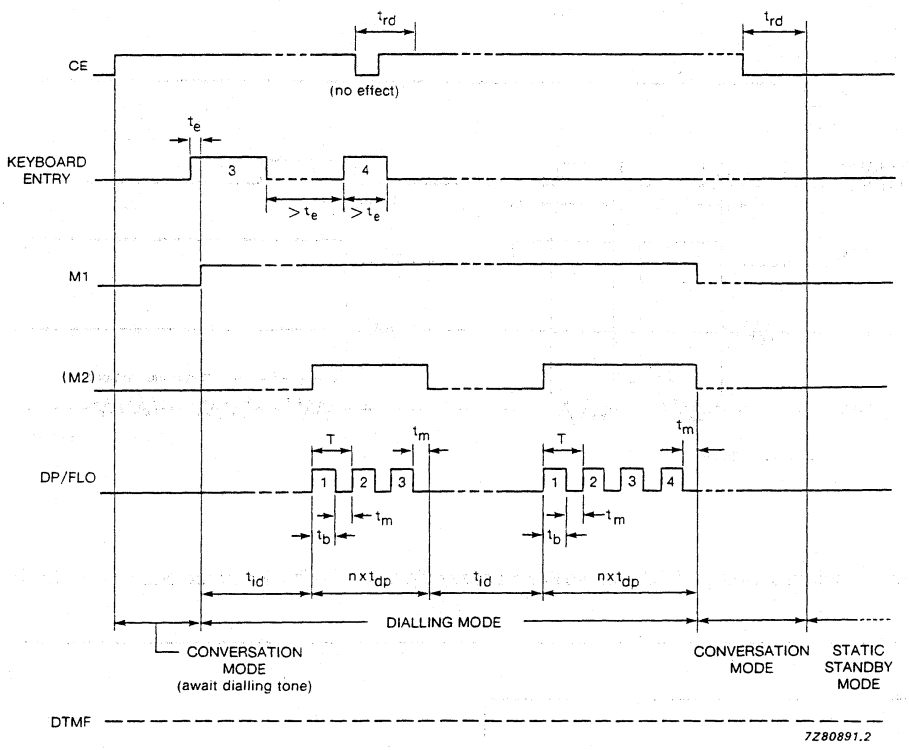


Fig.10a Timing diagram for pulse dialling ($\overline{PD}$/DTMF = V_{SS})

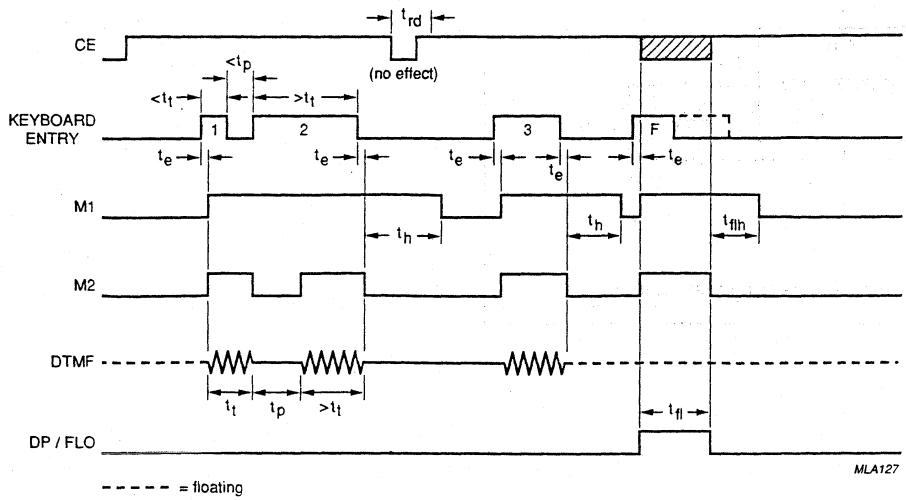


Fig.10b Timing diagram for DTMF dialling ($\overline{PD}$/DTMF = V_{DD})

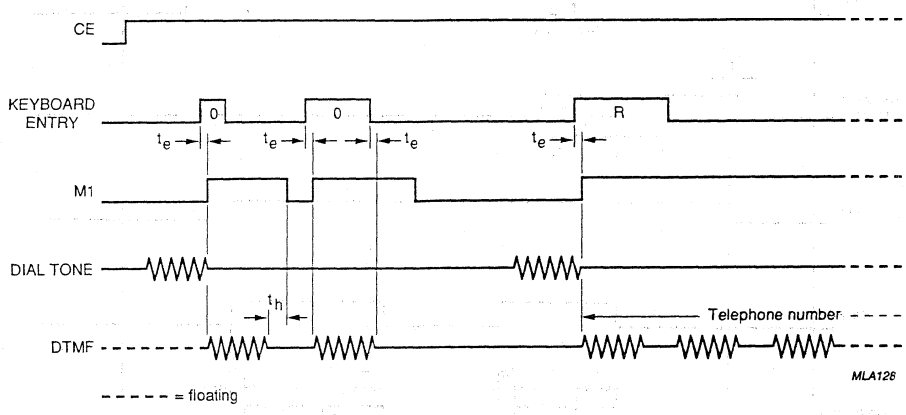


Fig.11 Timing diagram showing REDIAL where PABX access digits are the first keyboard entries in DTMF dialling mode.

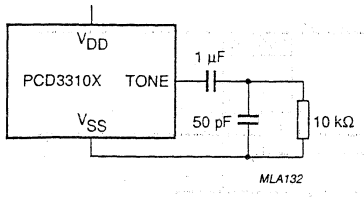


Fig.12 Tone output test circuit.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	−0.8	8	V
I_{DD}	supply current		50	mA
$\pm I_I, \pm I_O$	DC current into any input or output		10	mA
V_I	all input voltages	−0.8	V_{DD} + 0.8	V
P_{tot}	total power dissipation	-	300	mW
P_o	power dissipation per output	-	50	mW
T_{stg}	storage temperature range	−65	+ 150	°C
T_{amb}	operating ambient temperature range	−25	+ 70	°C

DC CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3.579545 MHz; T_{amb} = −25 to + 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		2.5	-	6.0	V
V_{DDO}	standby supply voltage		1.8	-	6.0	V
	Operating supply current					
I_{DDC}	conversation mode	oscillator ON	-	-	150	µA
I_{DDP}	pulse dialling or flash		-	-	200	µA
I_{DDF}	DTMF dialling	tone ON	-	0.6	0.9	mt
I_{DDF}	DTMF dialling	tone OFF	-	-	200	µA
I_{DDO}	standby supply current	V_{DD} = 1.8 V oscillator OFF; note 1	-	-	2	µA
Inputs						
V_{IL}	input voltage LOW (any pin)		0	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH (any pin)		0.7 V_{DD}	-	V_{DD}	V
$\lvert I_{IL} \rvert$	input leakage current; CE		-	-	1	µA
Keyboard inputs						
R_{KON}	keyboard ON resistance		-	-	2	kΩ
R_{KOFF}	keyboard OFF resistance		1	-	-	MΩ
Outputs						
	output sink current	V_{OL} = V_{SS} + 0.5 V				
I_{OL}	M1, $\overline{M1}$, DP/FLO, CF, FLD		0.7	-	-	mA
I_{OL}	$\overline{PD}$/DTMF	note 2	-	-	1	mA
	output source current	V_{OH} = V_{DD} − 0.5 V				
$-I_{OH}$	M1, $\overline{M1}$, DP/FLO, CF, M2		0.6	-	-	mA
$-I_{OH}$	$\overline{PD}$/DTMF	note 2	-	-	1	mA
$-I_{OH}$	FLD	note 3	-	60	-	nA
Timing and frequency						
t_{on}	clock start-up time		-	4	-	ms
t_e	debounce time		-	12	-	ms
t_{rd}	reset delay time		-	160	-	ms
Tone output (see Fig.12)						
	DTMF output voltage levels	V_{DD} = 2.5 to 6 V				
$V_{HG(rms)}$	HIGH group		158	192	205	mV
$V_{LG(rms)}$	LOW group		125	150	160	mV
Δf/f	frequency deviation		−0.6	-	+ 0.6	%
V_{DC}	DC voltage level		-	1/2 V_{DD}	-	V
$\lvert Z_O \rvert$	output impedance		-	0.1	0.5	kΩ
ΔV_G	pre-emphasis of group		1.85	2.1	2.35	dB
THD	total harmonic distortion	T_{amb} = 25 °C, note 4	-	−25	-	dB

Notes to the DC characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. < |10 mA| dynamic current to set/reset $\overline{PD}$/DTMF pin (mixed mode).
3. Flash inactive; V_{OH} = V_{SS}.
4. Related to the level of the LOW group frequency component (CEPT CS 203).

TYPE NUMBER DEPENDENT CHARACTERISTICS

PCD3310

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	redialling	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

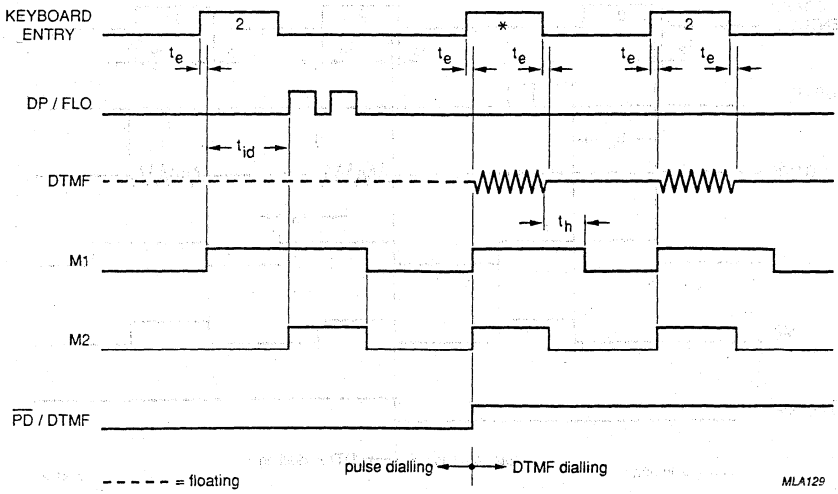


Fig.13 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310A

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	redialling	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	59	60	61	ms
t_m	make time	39	40	41	ms

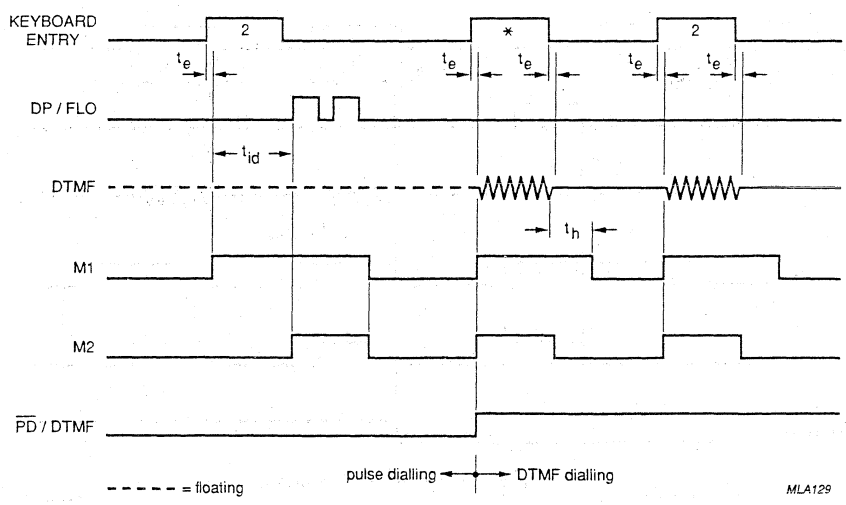


Fig.14 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310C

Dialling mode output (DMODE)

The dialling mode output is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

The DMODE output represents the actual dialling status of the dialler. In pulse mode the output is LOW and in DTMF mode the output is HIGH.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	redialling	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

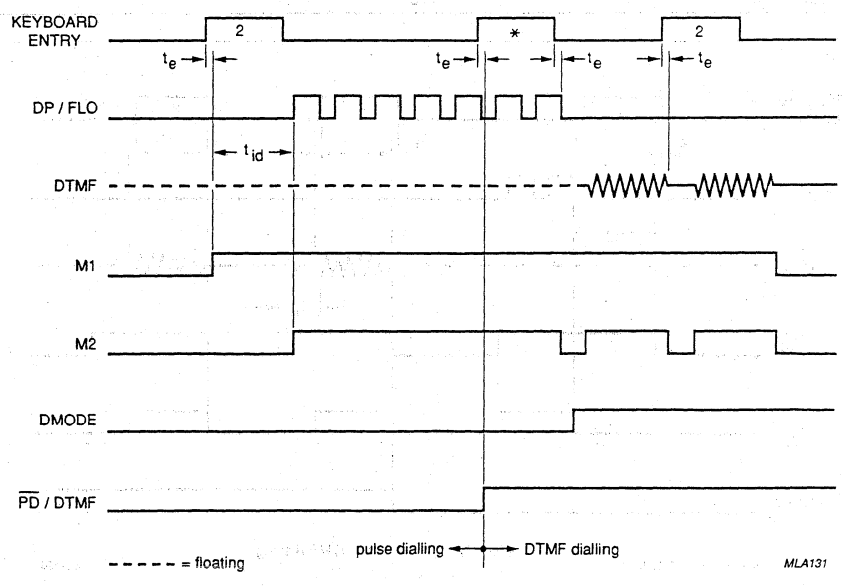


Fig.15 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310E

Pulse dialling frequency select (FS)

The frequency select pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT146 package.

If FS = V_{SS}; 10 Hz dialling selected. If FS = V_{DD}; 30 HZ dialling selected.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	retailing	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling @ 10 Hz					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms
Pulse dialling @ 20 Hz					
f_{dp}	dialling pulse frequency	19.6	20	20.8	Hz
t_{id}	inter-digit pause	496	504	512	ms
t_b	break time	33	34	35	ms
t_m	make time	16	17	18	ms

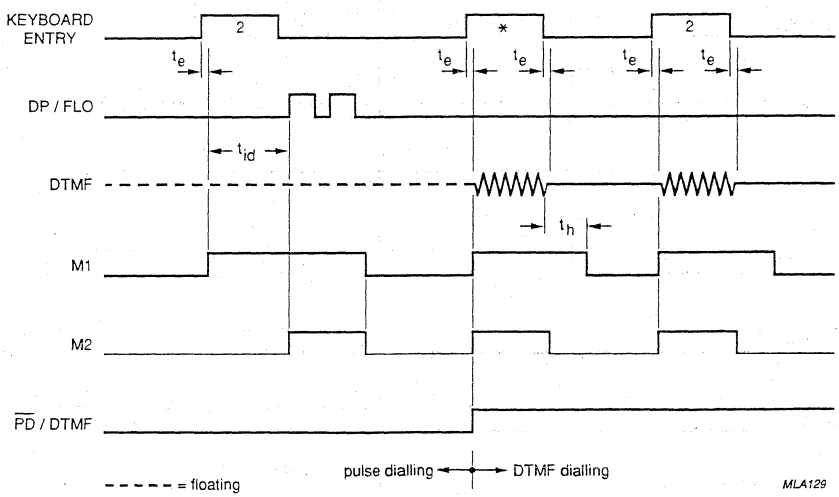


Fig.16 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310F

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t	manual dialling	59	-	-	ms
t_p		89	-	-	ms
t_t	retailing	59	60	61	ms
t_p		89	90	91	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	99	100	101	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

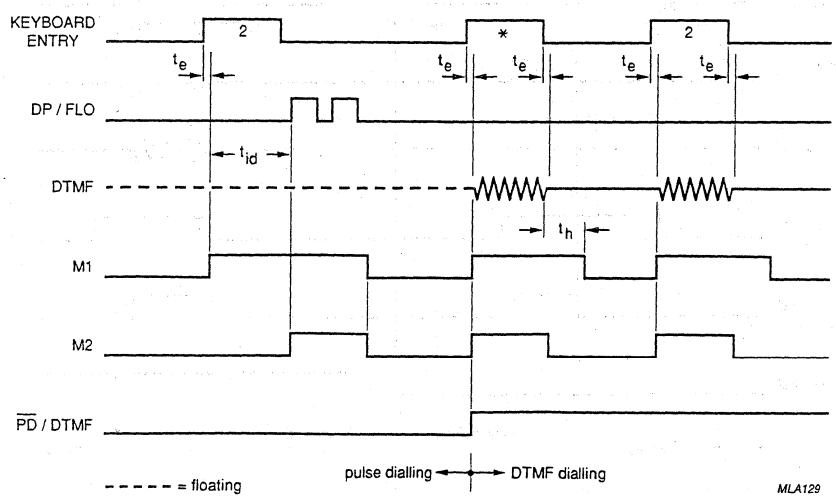


Fig.17 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310G

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

In mixed mode dialling the switch-over from pulse to DTMF mode can be activated by the * and # keys without sending out its corresponding frequencies when activated for the first time.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	retailing	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

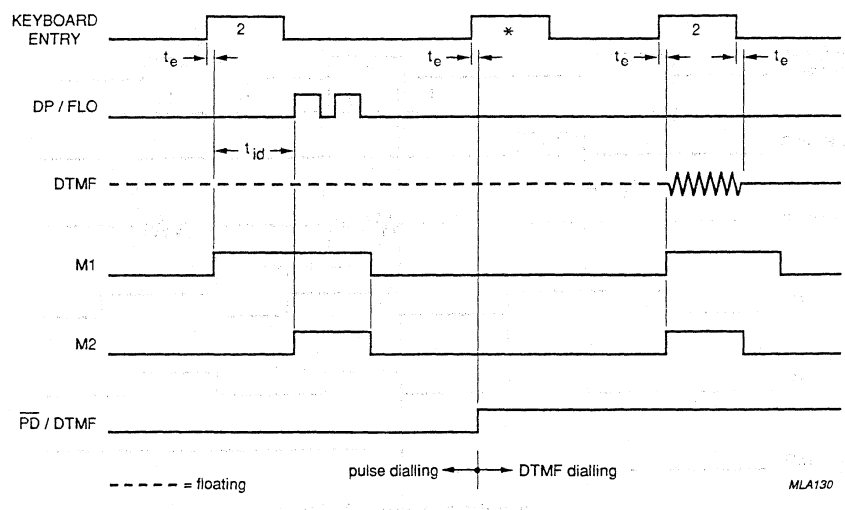


Fig.18 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

APPLICATION INFORMATION

1. Automatic line compensation obtained by connecting R6 to V_{SS}.
2. The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA 1060/61.

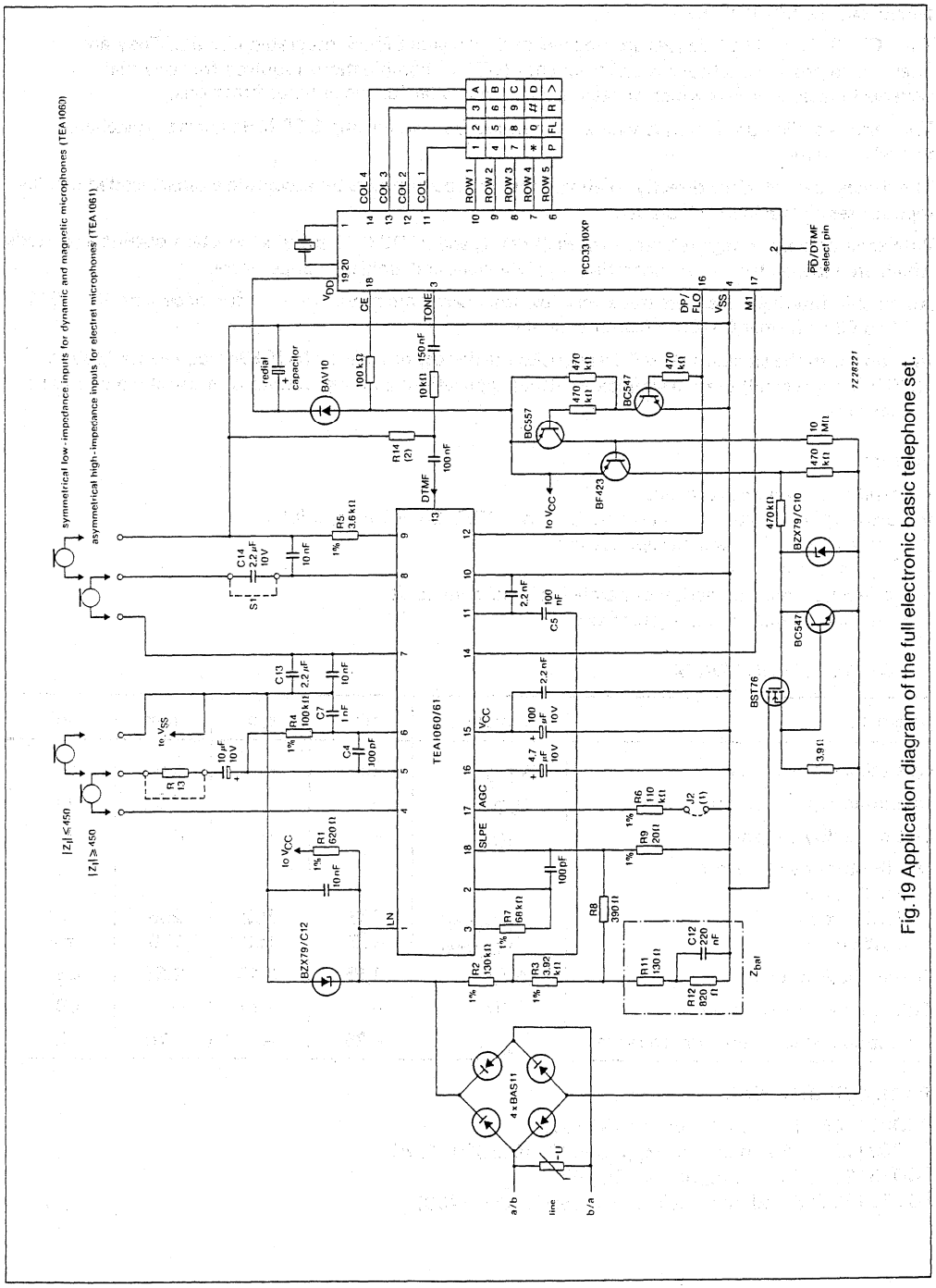


Fig.19 Application diagram of the full electronic basic telephone set.

GENERAL DESCRIPTION

The PCD3311C and PCD3312C are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C-bus).

With their on-chip voltage reference the PCD3311C and PCD3312C provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT T/CS46-03 (= former CS203) recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C-bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	0,9	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (RMS values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	–25	–	dB
Operating ambient temperature range	T_{amb}	–25	–	+70	°C

PACKAGE OUTLINES

PCD3311CP: 14-lead DIL; plastic (SOT27).
PCD3311CT: 16-lead mini-pack; plastic (SO16L; SOT162A).
PCD3312CP: 8-lead DIL; plastic (SOT97).
PCD3312CT: 8-lead mini-pack; plastic (SO8L; SOT176C).

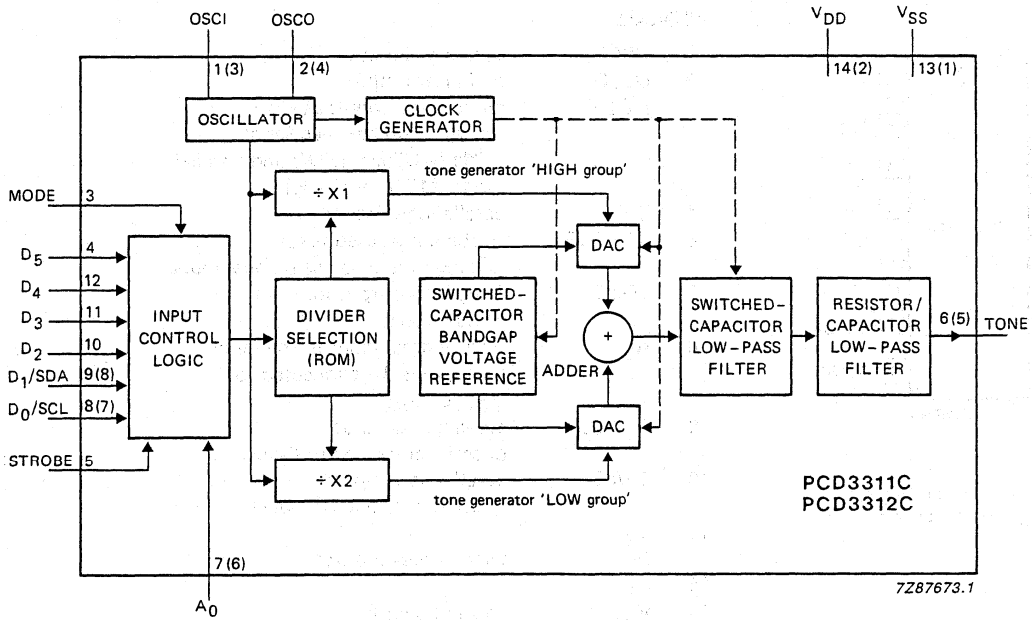


Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312C.

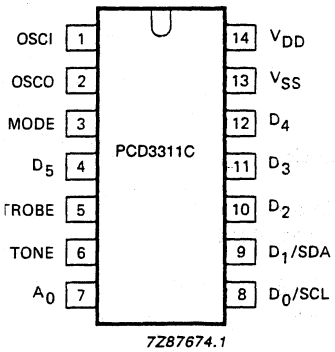


Fig. 2 Pinning diagram for the PCD3311CP.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C-bus)
9	D_1/SDA	parallel data input* or serial data line (I^2C-bus)
10	D_2	parallel data inputs*
11	D_3	
12	D_4	
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

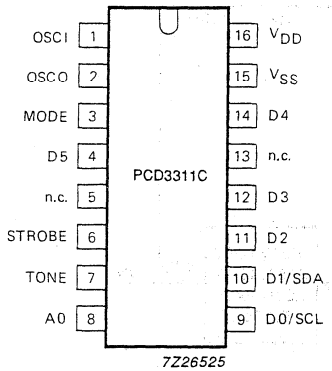


Fig. 3 Pinning diagram for the PCD3311CT.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
6	STROBE	strobe input; used for the loading of data in the parallel mode
7	TONE	frequency output for single or dual tones
8	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
9	D_0/SCL	parallel data input* or serial clock line (I^2C-bus)
10	D_1/SDA	parallel data input* or serial data line (I^2C-bus)
11	D_2	parallel data inputs*
12	D_3	
14	D_4	
15	V_{SS}	negative supply
16	V_{DD}	positive supply
5; 13	n.c.	not connected

* MODE = HIGH.

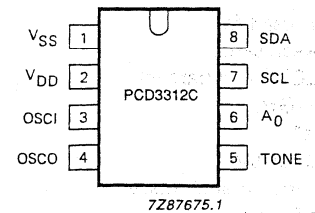


Fig. 4 Pinning diagram for the PCD3312C.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I^2C bus)
8	SDA	serial data line (I^2C bus)

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311C and PCD3312C is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311C), or, when connected to V_{SS} or left open, data can be received via the serial I^2C-bus (for both PCD3311C and PCD3312C).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

FUNCTIONAL DESCRIPTION (continued)

Data inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Table 1 D_5 and D_4 in accordance with the selected application

D_5	D_4	application
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	melody tones

1 = H = HIGH voltage level
0 = L = LOW voltage level

Note: Tables 2, 3, 4 and 5 show all input codes and their corresponding output frequencies.

Strobe input (STROBE, only for the PCD3311C)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311C by setting MODE input LOW.

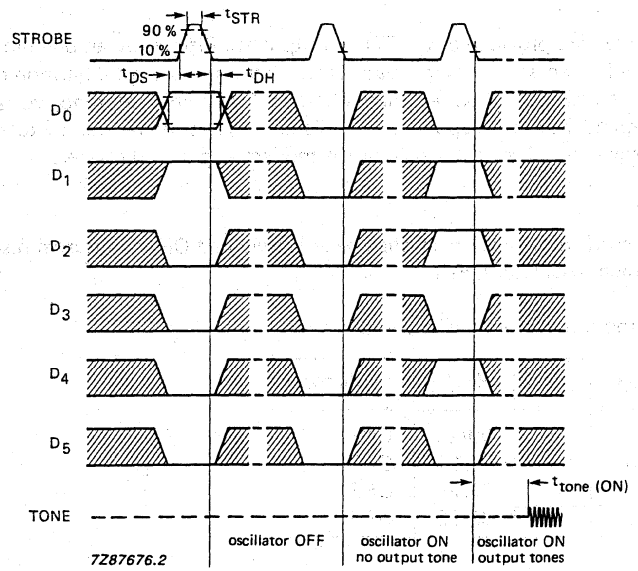


Fig. 5 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1 respectively. For the PCD3311C the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I²C-bus specification (see "CHARACTERISTICS OF THE I²C-BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311C or PCD3312C devices are connected to the same I²C bus. In any case A_0 must be connected to V_{DD} or V_{SS}.

I²C bus data configuration (see Fig. 6)

The PCD3311C and PCD3312C are always slave receivers in the I²C-bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311C as well as for the PCD3312C, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

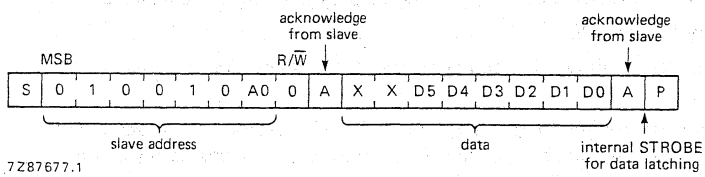


Fig. 6 I²C-bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS46-03 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

Table 2 Input data for control (no output tone; TONE in 3-state)

D_5	D_4	D_3	D_2	D_1	D_0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	symbol	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Table 4 Input data for MODEM frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz	remarks
1	0	0	1	0	0	24	1300	1296,94	−0,24	−3,06	V.23
1	0	0	1	0	1	25	2100	2103,14	+ 0,15	+ 3,14	
1	0	0	1	1	0	26	1200	1197,17	−0,24	−2,83	Bell 202
1	0	0	1	1	1	27	2200	2192,01	−0,36	−7,99	
1	0	1	0	0	0	28	980	978,82	−0,12	−1,18	V.21
1	0	1	0	0	1	29	1180	1179,03	−0,08	−0,97	
1	0	1	0	1	0	2A	1070	1073,33	+ 0,31	+ 3,33	Bell 103
1	0	1	0	1	1	2B	1270	1265,30	−0,37	−4,70	
1	0	1	1	0	0	2C	1650	1655,66	+ 0,34	+ 5,66	V.21
1	0	1	1	0	1	2D	1850	1852,77	+ 0,15	+ 2,77	
1	0	1	1	1	0	2E	2025	2021,20	−0,19	−3,80	Bell 103
1	0	1	1	1	1	2F	2225	2223,32	−0,08	−1,68	

* Tone output frequency when using a 3,579 545 MHz crystal.

= H = HIGH voltage level

= L = LOW voltage level

Table 5 Input data for melody tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	note	standard frequency Hz*	tone output frequency Hz**
1	1	0	0	0	0	30	D#5	622,3	622,5
1	1	0	0	0	1	31	E5	659,3	659,5
1	1	0	0	1	0	32	F5	698,5	697,9
1	1	0	0	1	1	33	F#5	740,0	741,1
1	1	0	1	0	0	34	G5	784,0	782,1
1	1	0	1	0	1	35	G#5	830,6	832,3
1	1	0	1	1	0	36	A5	880,0	879,3
1	1	0	1	1	1	37	A#5	932,3	931,9
1	1	1	0	0	0	38	B5	987,8	985,0
1	1	1	0	0	1	39	C6	1046,5	1044,5
1	1	1	0	1	0	3A	C#6	1108,7	1111,7
1	0	1	0	0	1	29	D6	1174,7	1179,0
1	1	1	0	1	1	3B	D#6	1244,5	1245,1
1	1	1	1	0	0	3C	E6	1318,5	1318,9
1	1	1	1	0	1	3D	F6	1396,9	1402,1
0	0	1	1	1	0	0E	F#6	1480,0	1482,2
1	1	1	1	1	0	3E	G6	1568,0	1572,0
1	0	1	1	0	0	2C	G#6	1661,2	1655,7
1	1	1	1	1	1	3F	A6	1760,0	1768,5
0	0	0	1	0	0	04	A#6	1864,7	1875,1
0	0	0	1	0	1	05	B6	1975,5	1970,0
1	0	0	1	0	1	25	C7	2093,0	2103,1
1	0	1	1	1	1	2F	C#7	2217,5	2223,3
0	0	0	1	1	0	06	D7	2349,3	2358,1
0	0	0	1	1	1	07	D#7	2489,0	2470,4

* Standard scale based on A4 = 440 Hz.

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level

0 = L = LOW voltage level

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

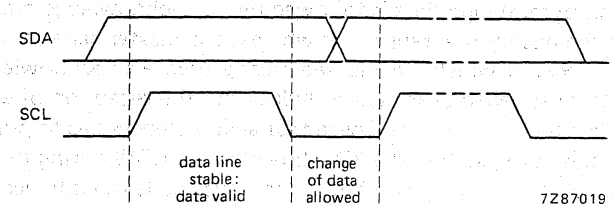


Fig. 7 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

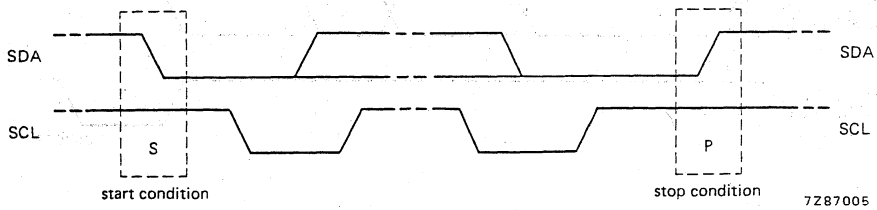


Fig. 8 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

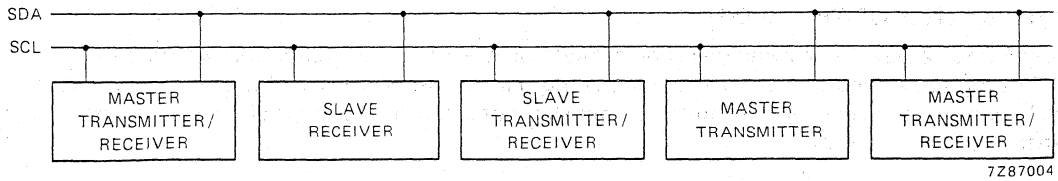


Fig. 9 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

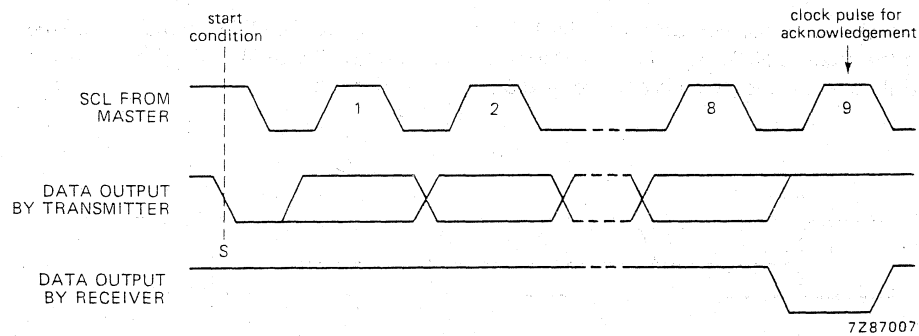


Fig. 10 Acknowledgement on the I^2C-bus.

CHARACTERISTICS OF THE I²C-BUS (continued)

Timing specifications

Within the I²C-bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 11.

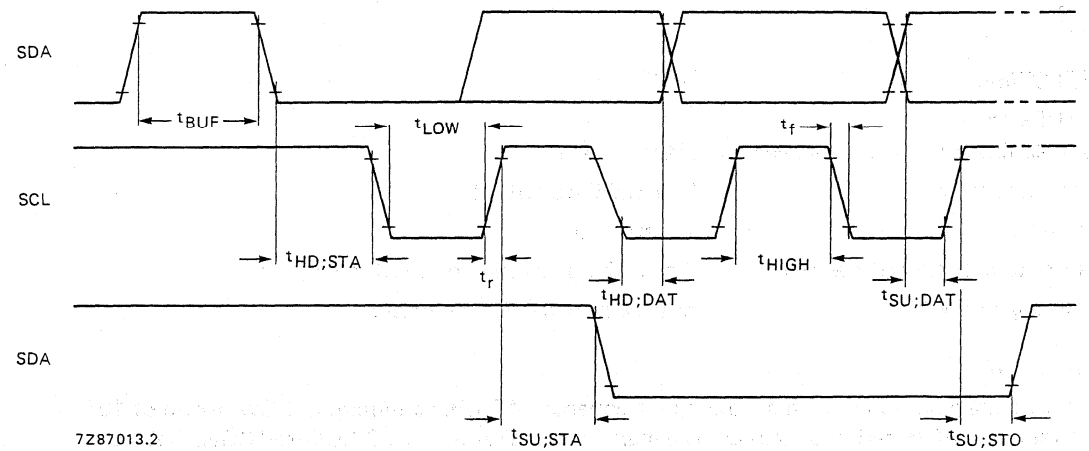


Fig. 11 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

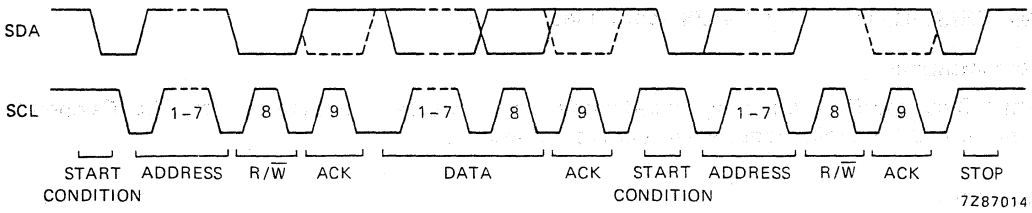


Fig. 12 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 13.

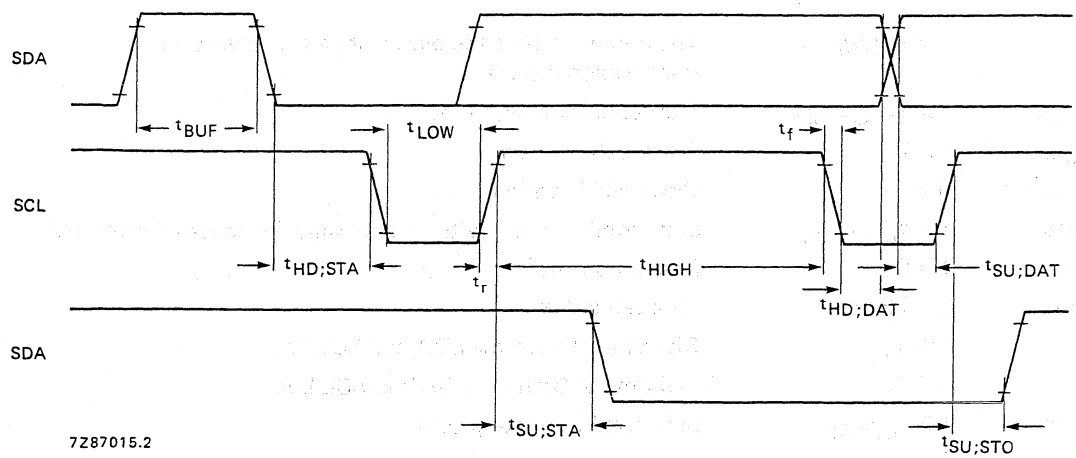


Fig. 13 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

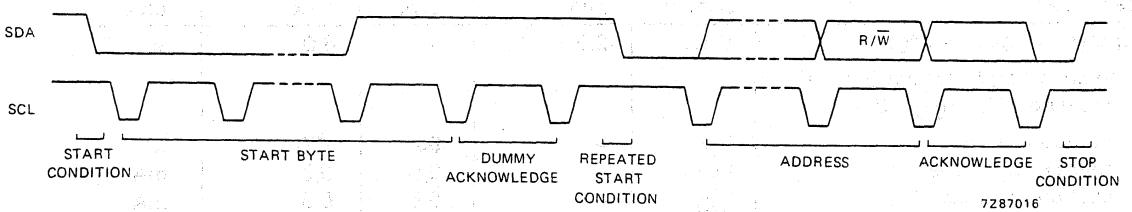


Fig. 14 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Power dissipation per output	P_O	–	50	mW
Total power dissipation per package	P_{tot}	–	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 50 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	–	50	100	μA
single output tone	I_{DD}	–	0,5	0,8	mA
dual output tone	I_{DD}	–	0,6	0,9	mA
Static standby current oscillator OFF; note 1	I_{DDO}	–	–	3	μA
Inputs/outputs (SDA)					
D_0 to D_5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
D_2 to D_5; MODE; STROBE; A_0					
Pull-down input current $V_I = V_{DD}$	$-I_{IL}$	30	150	300	nA
SCL (D_0); SDA (D_1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Clock frequency (see Fig. 11)	f_{SCL}	–	–	100	kHz
Input capacitance; $V_I = V_{SS}$	C_I	–	–	7	pF
Allowable input spike pulse width	t_I	–	–	100	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 15)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
DC voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	−25	–	dB
modem tone, note 3	THD	–	−29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS46-03).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

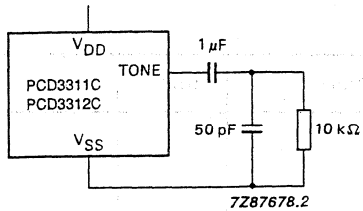


Fig. 15 TONE output test circuit.

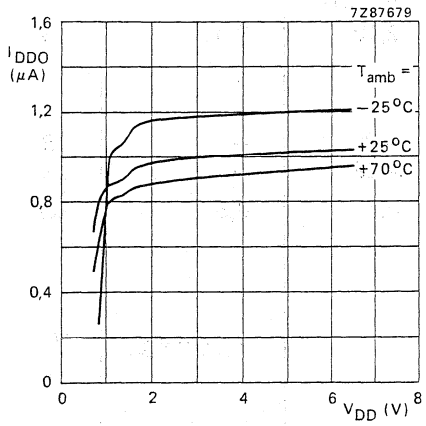


Fig. 16 Standby supply current as a function of supply voltage; oscillator OFF.

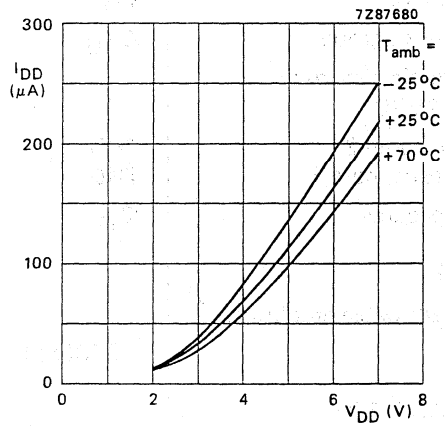


Fig. 17 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

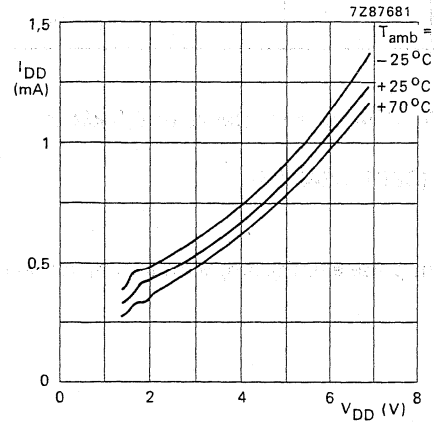


Fig. 18 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

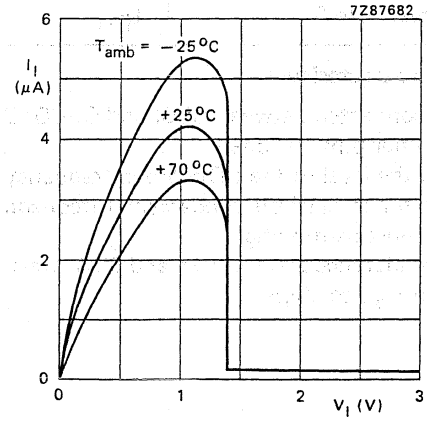


Fig. 19 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

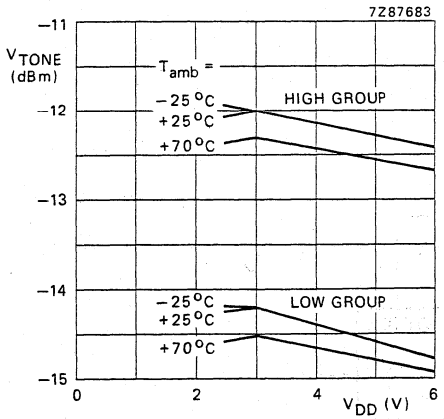


Fig. 20 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

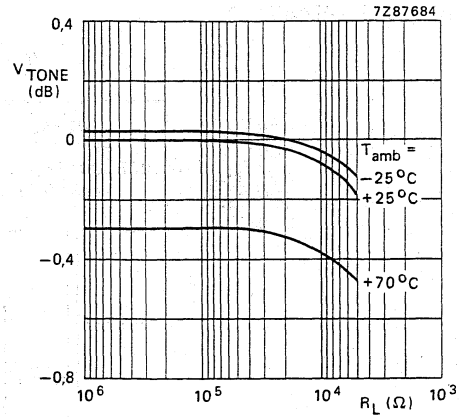


Fig. 21 Dual tone output voltage level as a function of output load resistance.

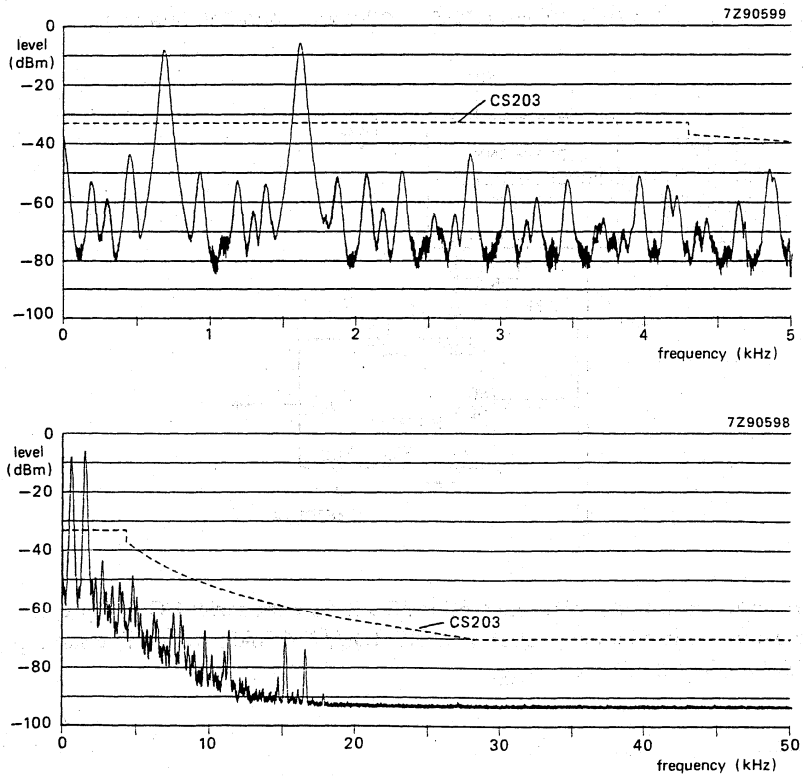


Fig. 22 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

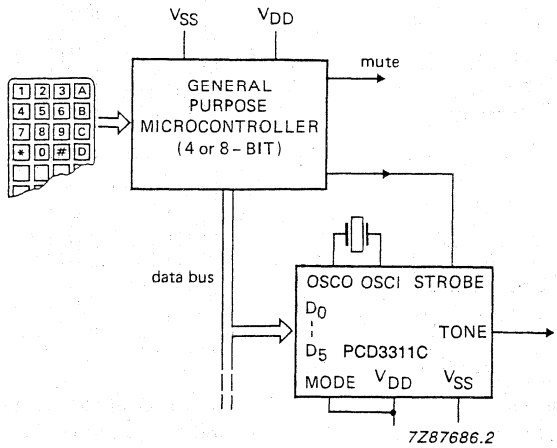


Fig. 23 PCD3311C driven by a microcontroller with parallel data bus.

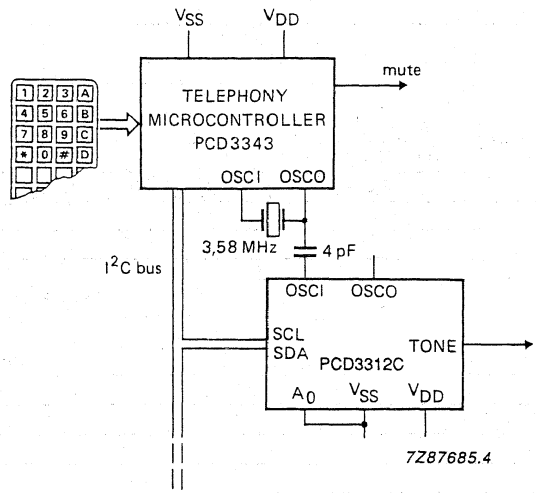


Fig. 24 PCD3312C driven by telephony microcontroller PCD3343 with serial I/O (I^2C-bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes. The same application is possible with the PCD3311C with MODE = V_{SS}.

CONTENTS

1 FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 1536 bytes ROM
- 160 bytes RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 2 single-level vectored interrupts:
  - external
  - 8-bit programmable timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- Power-on reset
- Stop and Idle modes
- Logic supply voltage: V_{DD} = 1.8 to 6 V
- Low stand-by voltage: V_{DD} = 1 V
- Low stand-by current: I_{DD} = 1.2 µA typical at 1.8 V and 25 °C
- Clock frequency: 1 to 16 MHz
- Operating temperature: −25 to +70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3315A. The shared characteristics of the PCD33XXA family of microcontrollers are described in the *"PCD33XXA family data sheet"* which should be read in conjunction with this publication.

The PCD3315A is a microcontroller intended for telecom applications. It provides 1.5 kbytes of program memory, 160 bytes of RAM and 20 I/O lines. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3315AP	28	DIP	plastic	SOT117-1
PCD3315AT	28	SO28L	plastic	SOT136-1

4 BLOCK DIAGRAM

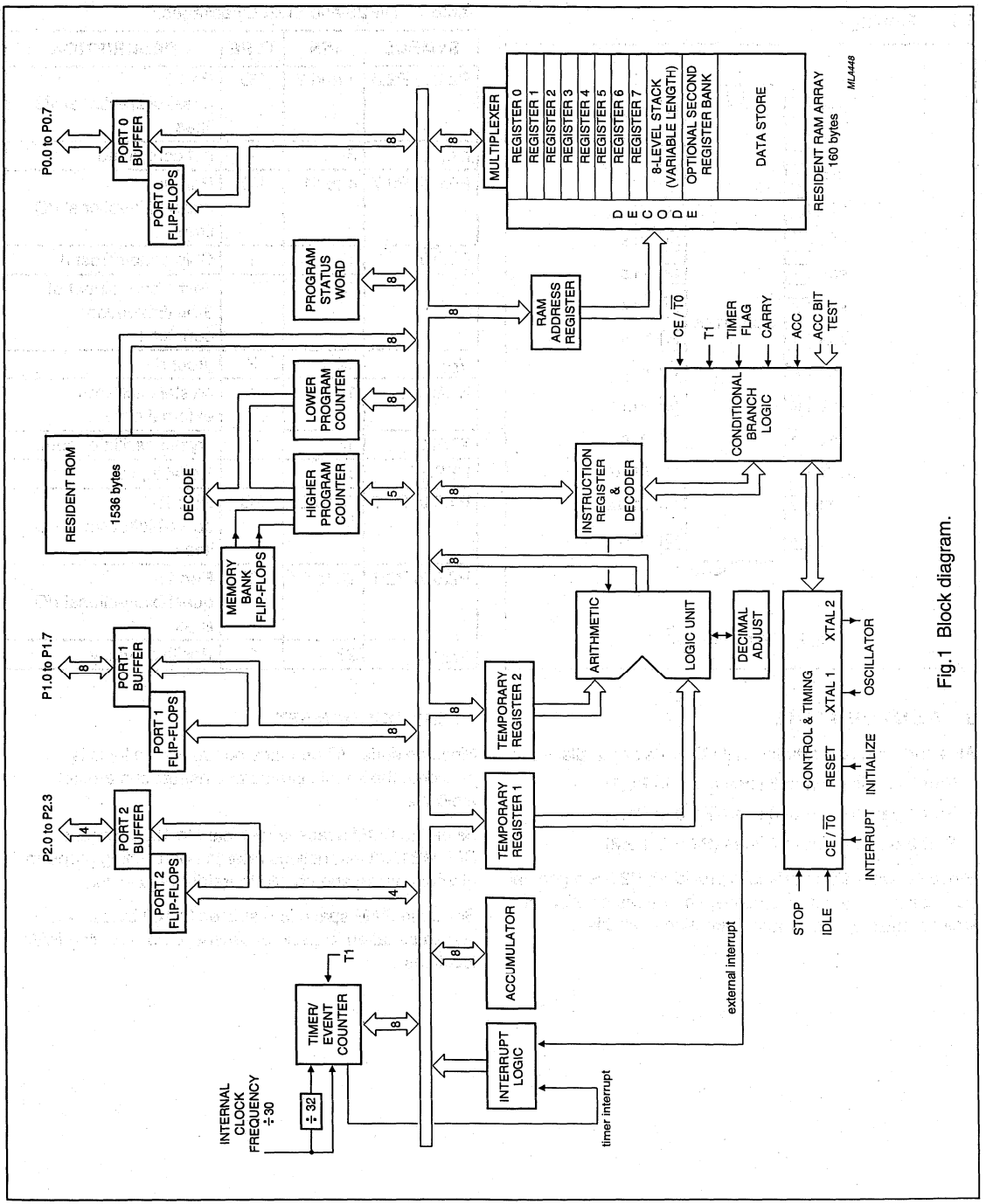


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

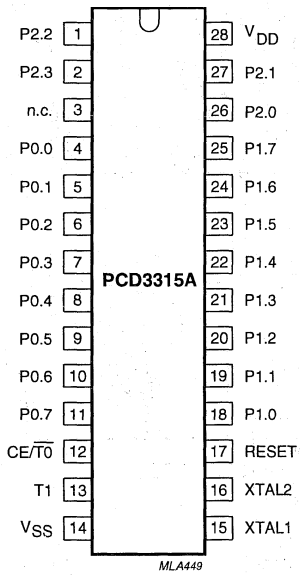


Fig.2 Pin configuration.

5.2 Pin description

Table 1 DIP28 and SO28L packages.

SYMBOL	PIN	TYPE	DESCRIPTION
P2.2 to P2.3	1 and 2	I/O	Port 2: quasi-bidirectional I/O lines
n.c.	3	–	not connected
P0.0 to P0.7	4 to 11	I/O	Port 0: quasi-bidirectional I/O lines
CE/$\overline{T0}$	12	I	Chip enable/Test 0
T1	13	I	Test 1/count input of 8-bit timer/event counter 1
V_{SS}	14	P	ground
XTAL1	15	I	crystal oscillator/ external clock
XTAL2	16	O	crystal oscillator output
RESET	17	I	Reset input
P1.0 to P1.7	18 to 25	I/O	Port 1: quasi-bidirectional I/O lines
P2.0 to P2.1	26 to 27	I/O	Port 2: quasi-bidirectional I/O lines
V_{DD}	28	P	Positive supply

6 PARALLEL PORTS

All standard quasi-bidirectional I/O ports are available:

- Port 0 parallel port of 8 lines (P0.0 to P0.7)
- Port 1 parallel port of 8 lines (P1.0 to P1.7)
- Port 2 parallel port of 4 lines (P2.0 to P2.3)

Since no serial I/O interface is provided, P2.3 is a general purpose line without restrictions, i.e. the reset option as well as mask options 1 and 3 are also available.

7 INSTRUCTION SET

Since no serial I/O interface nor derivative logic is provided, the serial input/output instructions are not available.

Since the ROM space is restricted to 1536 bytes, the SEL MB1/2/3 instructions refer to non-existing program memory banks and should therefore be avoided.

Since the RAM space is restricted to 160 bytes, care should be taken to avoid accesses to non-existing RAM locations.

8 SUMMARY OF MASK OPTIONS

Table 2 Port mask options (see *"PCD33XXA family data sheet"*).

PORT	PORT OUTPUT[1]			PORT STATE AFTER RESET	
	OPTION 1	OPTION 2	OPTION 3	SET	RESET
P0.0 to P0.7	X	X	X	X	X
P1.0 to P1.7	X	X	X	X	X
P2.0 to P2.3	X	X	X	X	X

Note

1. Option 1: normal port
   Option 2: open drain
   Option 3: push-pull.

Table 3 Mask options.

FEATURE	DESCRIPTION
ROM Code: program/data	Any mix of instructions and data up to ROM size of 1536 bytes.
Power-on reset voltage level: V_{ref}	1.2 to 3.6 V in increments of 100 mV; OFF
Oscillator transconductance: g_m	LOW transconductance: g_{mL}
	MEDIUM transconductance: g_{mM}
	HIGH transconductance: g_{mH}

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	7	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_{DD}	positive supply current	−50	+50	mA
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	–	90	°C

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

11 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.579545 MHz (g_{mL}); $R_X \leq 100\ \Omega$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 3 to 6)						
V_{DD}	operating supply voltage	note 1	1.8	–	6	V
V_{DD}	RAM data retention Stop mode		1.0		6	V
I_{DD}	operating supply current	V_{DD} = 3 V; f_{xtal} = 3.579545 MHz (g_{mL}); note 1	–	0.3	0.6	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL}); note 1	–	1.1	3.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM}); note 1	–	1.7	5.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); note 1	–	2.5	6.0	mA
$I_{DD(ID)}$	supply current Idle mode	V_{DD} = 3 V; f_{xtal} = 3.579545 MHz (g_{mL}); note 1	–	0.2	0.4	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL}); note 1	–	0.8	1.6	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM}); note 1	–	1.2	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); note 1	–	1.7	5.0	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 2	–	1.2	2.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 °C; note 2	–	–	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	Input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	µA
Outputs (see Figs 7 to 9)						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V	0.7	8	–	mA
I_{OH}	HIGH level port pull-up source current	V_{DD} = 3 V; V_O = 2.7 V	–10	–20	–	µA
		V_{DD} = 3 V; V_O = 0 V	–	–100	–300	µA
I_{OH}	HIGH level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	–0.7	–4	–	mA
ΔV_{POR}	power-on reset level variation around chosen V_{POR}	note 3	–0.5	0	+0.5	V

Notes

1. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; all other outputs open. Maximum values: external clock at XTAL1; XTAL2 open. Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; RESET, T1 and CE/$\overline{T0}$ at V_{SS}; crystal connected between XTAL1 and XTAL2; all other outputs open.
3. V_{POR} is an option chosen by the user. Depending on its value, it may restrict the supply voltage range.

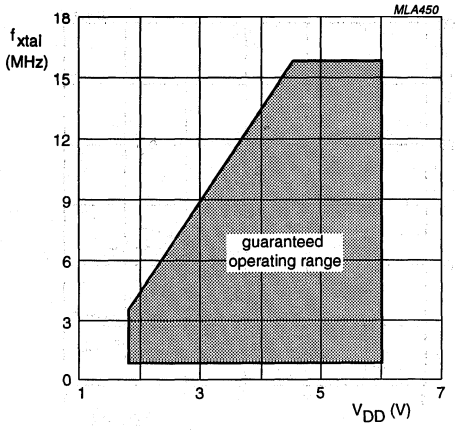


Fig.3 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

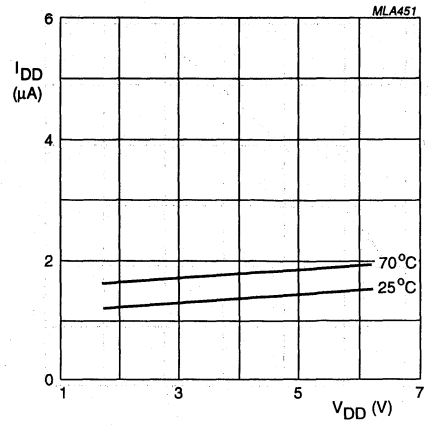


Fig.4 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).

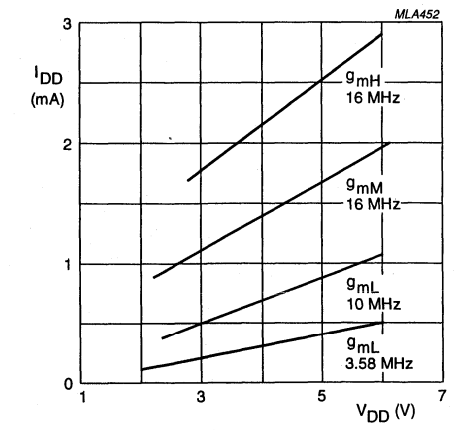


Fig.5 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).

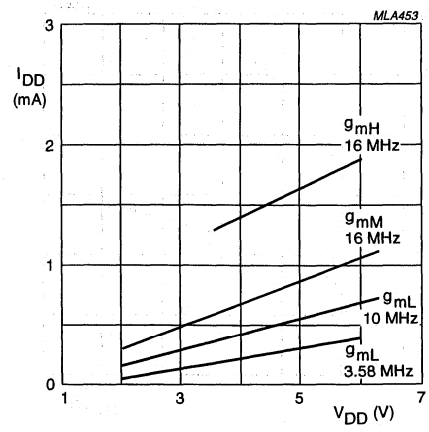
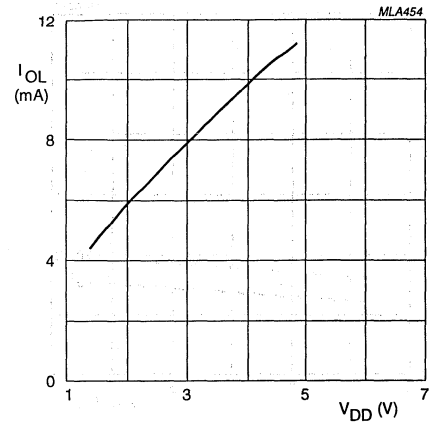


Fig.6 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



$V_O = 0.4$ V.

Fig.7 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

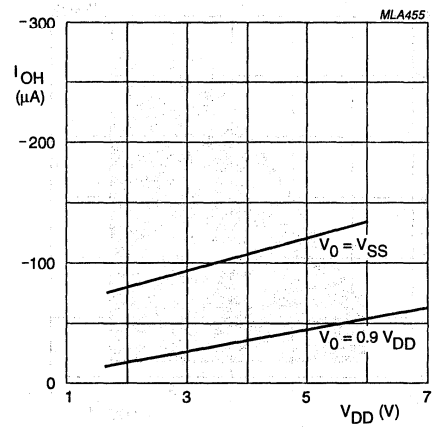
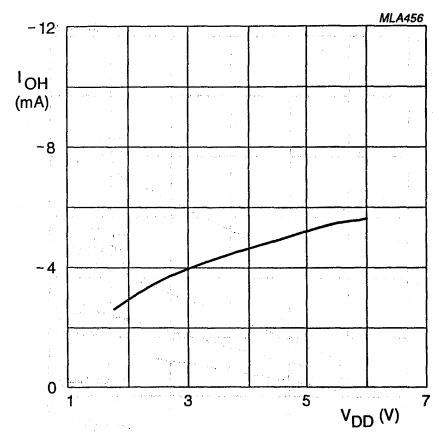


Fig.8 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.9 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

12 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; all other outputs open. Maximum values: external clock at XTAL1; XTAL2 open. Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
f_{xtal}	clock frequency	see Fig.3	1	–	16	MHz
Oscillator (see Fig.10)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance	V_{DD} = 5 V	0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance	V_{DD} = 5 V	3.0	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

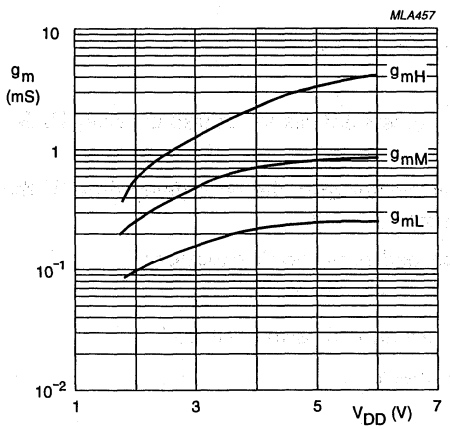


Fig.10 Typical transconductance as a function of supply voltage (V_{DD}) for the options g_{mL}, g_{mM} and g_{mH}.

Pulse dialler circuits with redial PCD332XC family

GENERAL DESCRIPTION

The PCD332XC family comprises seven CMOS pulse dialler circuits with redial. Each circuit converts 3 x 4 matrix keyboard entries into correctly-timed line current interruptions. For redial, the last-dialled number (up to 23 digits) is stored in an on-chip RAM. A RAM overflow is handled by inhibiting the redial but manual dialling of more than 23 digits still can be made. The circuits include a delayed reset for line power breaks to ensure correct operation.

Most ICs of the family regenerate an access pause during redial. Insertion of the access pause during the original entry is either automatic or via the '*' key. Termination of the regenerated access pause during redial is via the '#' key, after a built-in delay or controlled by an external tone recognizer. Other differences between the circuits are selections of pulse dialling frequency, mark/space ratio, regenerated access pause duration, mute, hold/access pause output control and oscillator frequency.

Features

- Operating supply voltage range: 2.0 to 6.0 V
- Static supply voltage (with redial memory data retention): down to 1.5 V
- Low operating supply current: typ. 60 μA
- Low static standby supply current: typ. 0.65 μA
- On-chip RAM capacity: 23 keyboard entries (digits and access pauses)
- Redial inhibited after memory overflow
- Manual dialling can continue beyond 23 keyboard entries (excess entries are stored at lower RAM addresses)
- (Re)dialling procedure is not affected by line interruptions shorter than the reset delay time (if the supply voltage does not fall below the static standby voltage)
- Line interruptions longer than the reset delay time are regarded as on-hook situations
- Hold facility for lengthening the inter-digit period
- On-chip oscillator for 3.58 MHz crystal (type for ceramic resonator is also available)
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard
- Pull-up or pull-down circuits at all inputs except CE
- Electrostatic discharge protection at all inputs
- High input noise immunity
- Test mode in which the dialling frequency is increased.

Note:

the PCD3320C, PCD3322C, PCD3324C and PCD3325C are not to be used for new design-ins

Pulse dialler circuits with redial PCD332XC family

The PCD332XC family of ICs comprises the following types:

PCD3320C dialler with several mute signals
PCD3321C dialler with two automatic access pauses
PCD3322C variant of PCD3320C
PCD3324C dialler with one automatic access pause
PCD3325C dialler with manual access pause control
PCD3326C variant of PCD3321C
PCD3327C variant of PCD3325C for ceramic resonator with automatic reset of access pause

functional survey	PCD . . .						
	3320C	3321C	3322C	3324C	3325C	3326C	3327C
Number of pins	18	18	18	18	18	18	18
Dialling frequency 10 Hz	●	●	●	●	●	●	●
selectable with F01, F02 16, 20 Hz		●		●	●	●	●
Mark/space ratio 3 : 2	●	●	●	●	●	●	●
selectable with M/S 2 : 1		●		●	●		●
Access pauses repeated during redial		●		●	●	●	●
Manual insertion of access pauses		●		●	●	●	●
Automatic access pause insertion							
1 max				●			
2 max		●				●	
Access pause duration 32 x T_{DP}		●		●		●	●
selectable with APD 64 x T_{DP}						●	
not automatically terminated					●		
$\overline{M1}$, inverted mute output	●		●				
M2, strobe output			●				
M3, AND function of mute (M1) and inverted dialling pulse (DP) outputs	●						
HOLD, dialling-interrupt input	●		●				
APO + HOLD, internally connected		●		●	●	●	●

T_{DP} = dialling pulse period

* PCD3327C for ceramic resonator

Features common to all PCD332XC family

OSC IN, OSC OUT: on-chip oscillator input and output
C1 to C3: column keyboard inputs with on-chip pull-up
R1 to R4: row keyboard outputs with on-chip pull-down
CE: chip enable input
DP: dialling pulse output to external line-switching transistor or relay
M1: mute output

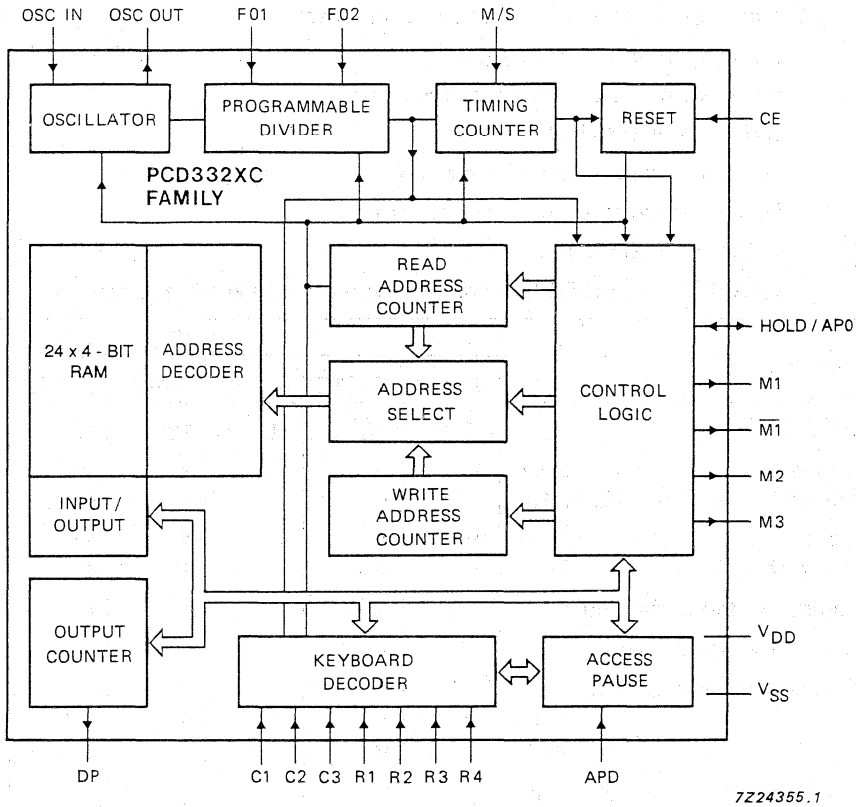


Fig.1 Block diagram.

PACKAGE OUTLINES

PCD3320CP
PCD3321CP
PCD3322CP
PCD3324CP
PCD3325CP
PCD3326CP
PCD3327CP
: 18-lead DIL; plastic (SOT102G).

PCD3320CD
PCD3321CD
: 18-lead DIL; ceramic (SOT133B).

PCD3321CT
PCD3322CT
PCD3327CT
: 20-lead mini-pack; plastic (SOT163A).

PCD3327U: uncased chip in tray.

PINNING

pin	purpose	PCD . . .						
		3320C	3321C	3322C	3324C	3325C	3326C	3327C
Supplies								
V_{DD}	positive supply	●	●	●	●	●	●	●
V_{SS}	negative supply	●	●	●	●	●	●	●
Inputs								
M/S	controls mark/space ratio of the line pulses		●		●	●		●
F01	define the dialling pulse frequency	●	●	●	●	●	●	●
F02			●		●	●	●	●
CE	Chip enable: used to initialize the system, to select between operating and static standby mode and to handle line power breaks	●	●	●	●	●	●	●
C1	keyboard column inputs with on-chip pull-up	●	●	●	●	●	●	●
C2								
C3								
ADP	Access Pause Duration: selects the maximum duration of an access pause if no external APR appears						●	
R1	keyboard row outputs with on-chip pull-down	●	●	●	●	●	●	●
R2								
R3								
R4								
HOLD	interrupts dialling after completion of the current digit or immediately during an inter-digit pause	●		●				
Outputs								
DP	Dialling Pulse: drive of the external switching transistor or relay	●	●	●	●	●	●	●
M1	Muting: normally used for muting during the dialling sequence	●	●	●	●	●	●	●
$\overline{M1}$	inverted output of M1	●		●				

pin	purpose	PCD . . .						
		3320C	3321C	3322C	3324C	3325C	3326C	3327C
M2	strobe; HIGH during pulsing of each digit, LOW during an inter-digit pause			●				
M3	AND-function with $\overline{DP}$ and M1 as inputs; for direct drive of a switching transistor for dialling pulses and muting	●						
Oscil-lator								
OSC IN	input and output of the on-chip oscillator	●	●	●	●	●	●	●
OSC OUT		●	●	●	●	●	●	●
Input/ outputs								
HOLD/ APO	The HOLD and APO features are connected together at this pin, normally an output pin but can be forced as an input		●		●	●	●	●

PINNING (continued)

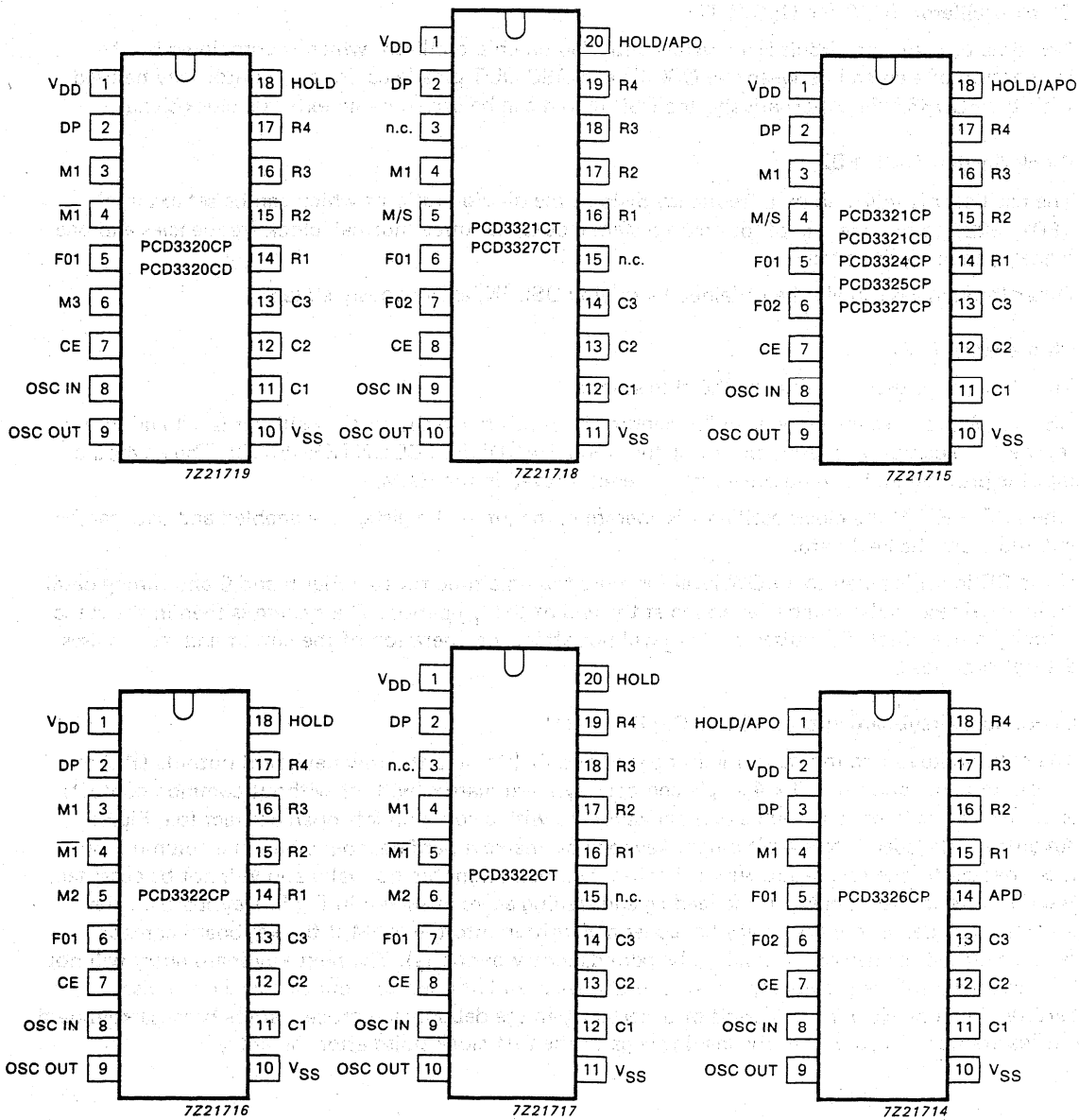


Fig.2 Pinning diagrams.

FUNCTIONAL DESCRIPTION

Clock oscillator (OSC IN, OSC OUT)

The time base for the circuit is a crystal-controlled on-chip oscillator which is completed by the connection of a crystal between the OSC IN and OSC OUT pins (a ceramic resonator may be used with the PCD3327C). Alternatively, the OSC IN pin can be driven by an external clock signal.

Clock divider (F01, F02)

The oscillator is followed by a frequency divider, the division ratio of which can be set externally (F01, F02) to provide one of four chip system clocks, i.e. three 'normal' clock frequencies and one higher frequency for testing.

Other frequencies can also be obtained by driving OSC IN, as previously stated.

Chip enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped at reset, excepting the WRITE ADDRESS COUNTER (WAC). The keyboard input is prohibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

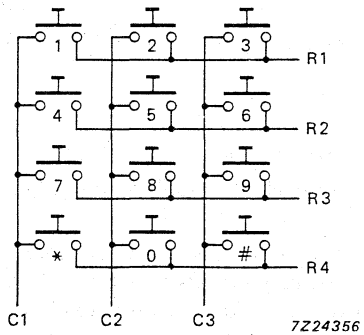
Debouncing keyboard entries (C1 to C3; R1 to R4)

The column keyboard inputs to the integrated circuits(Cn) and the row keyboard outputs (Rn) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig.3, or to a double contact keyboard with a common left open contact (see Fig.4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input. Any other input combinations are not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig.5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for five or six clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been left open for four or five clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the leading edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 codes are written into the RAM, memory overflow results and the access keycodes replace the data in the lower-numbered locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly-timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset (see 'Access Pause System'). During redial, no keyboard entry will be accepted and stored in the RAM. But, when all numbers stored in the RAM have been pulsed out, new keyboard entries will be accepted and stored in the RAM position after the last digit code of the original entry and converted into correctly-timed dialling pulses.



* Access pause set.
\# Redial or access pause reset.

Fig.3 Single contact keyboard.

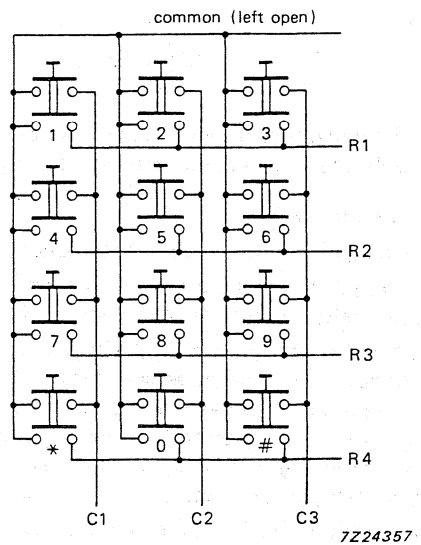


Fig.4 Double contact keyboard.

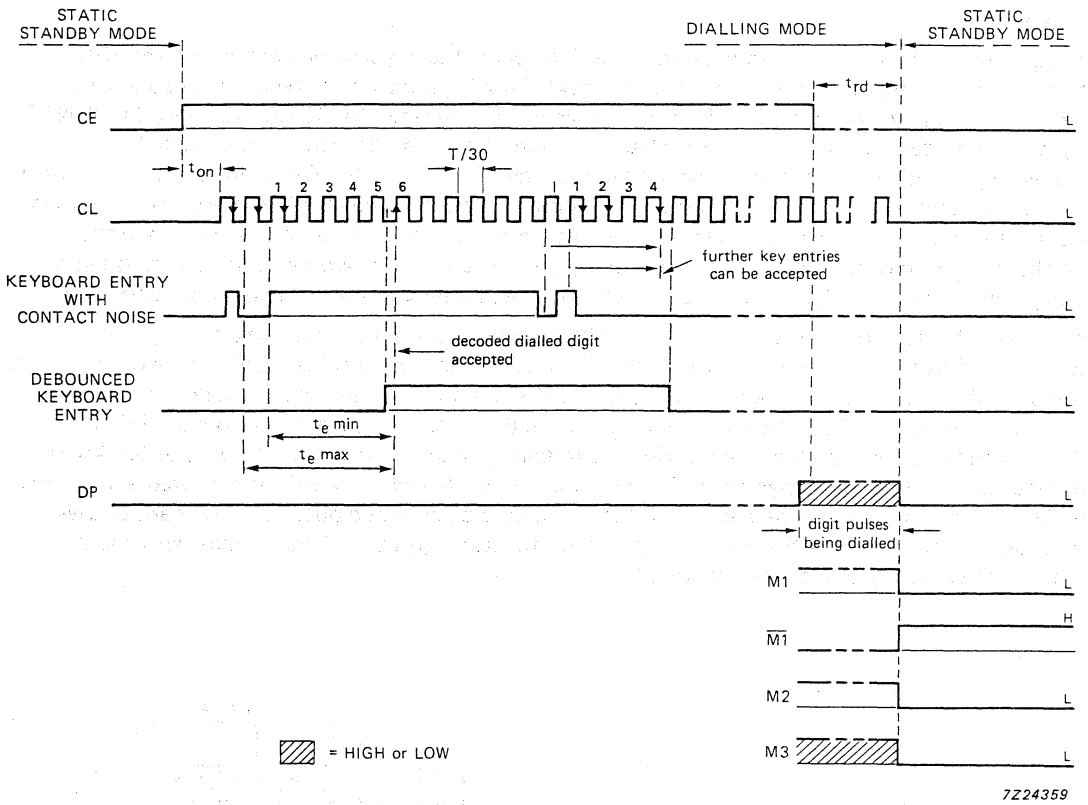


Fig.5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig.6.

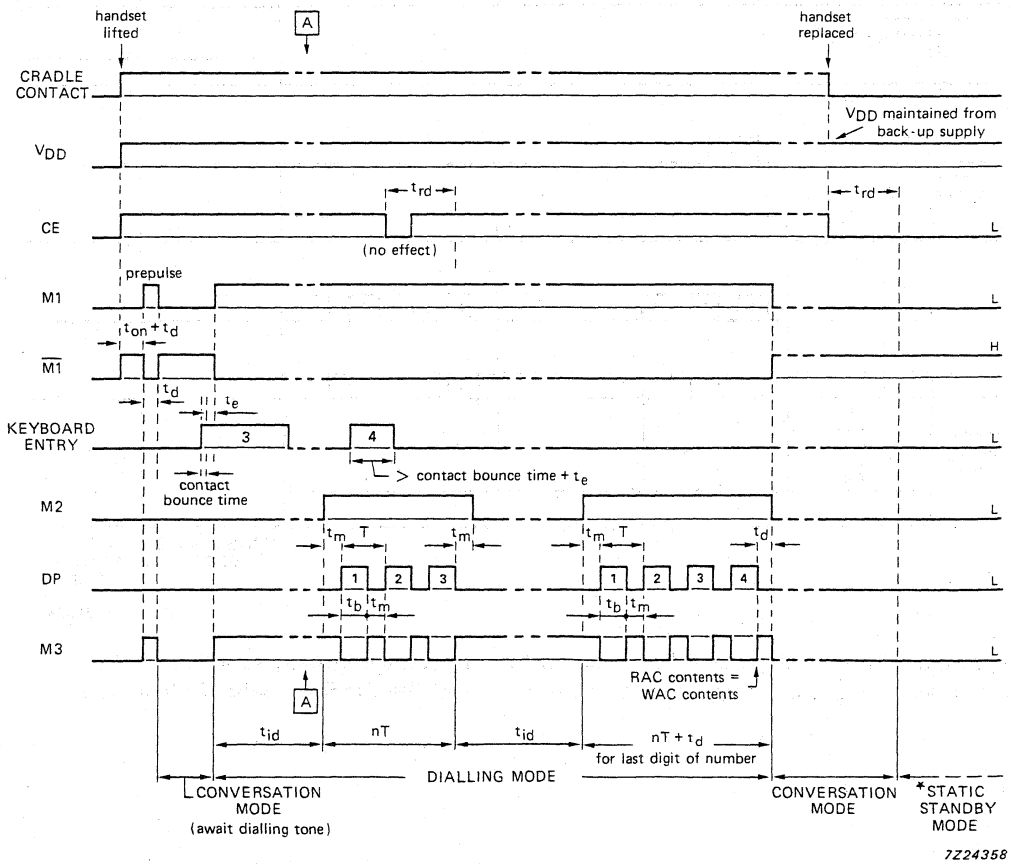
Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and ten clock pulse periods later a prepulse with a duration of ten clock pulse periods (t_d) appears at outputs M1 and M3. This prepulse ensures that if a polarized muting relay with two stable positions is used it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (see Fig.7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes high, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

Dialling sequence (continued)

Referring to Fig.6, when the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1.6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above the level V_{DD0} = 1.5 V, which is detected by the power-on reset circuit.



* Oscillator off; all registers reset; keyboard input inhibited; number stored in RAM until $V_{DD} < 1.5$ V.

Fig.6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts).

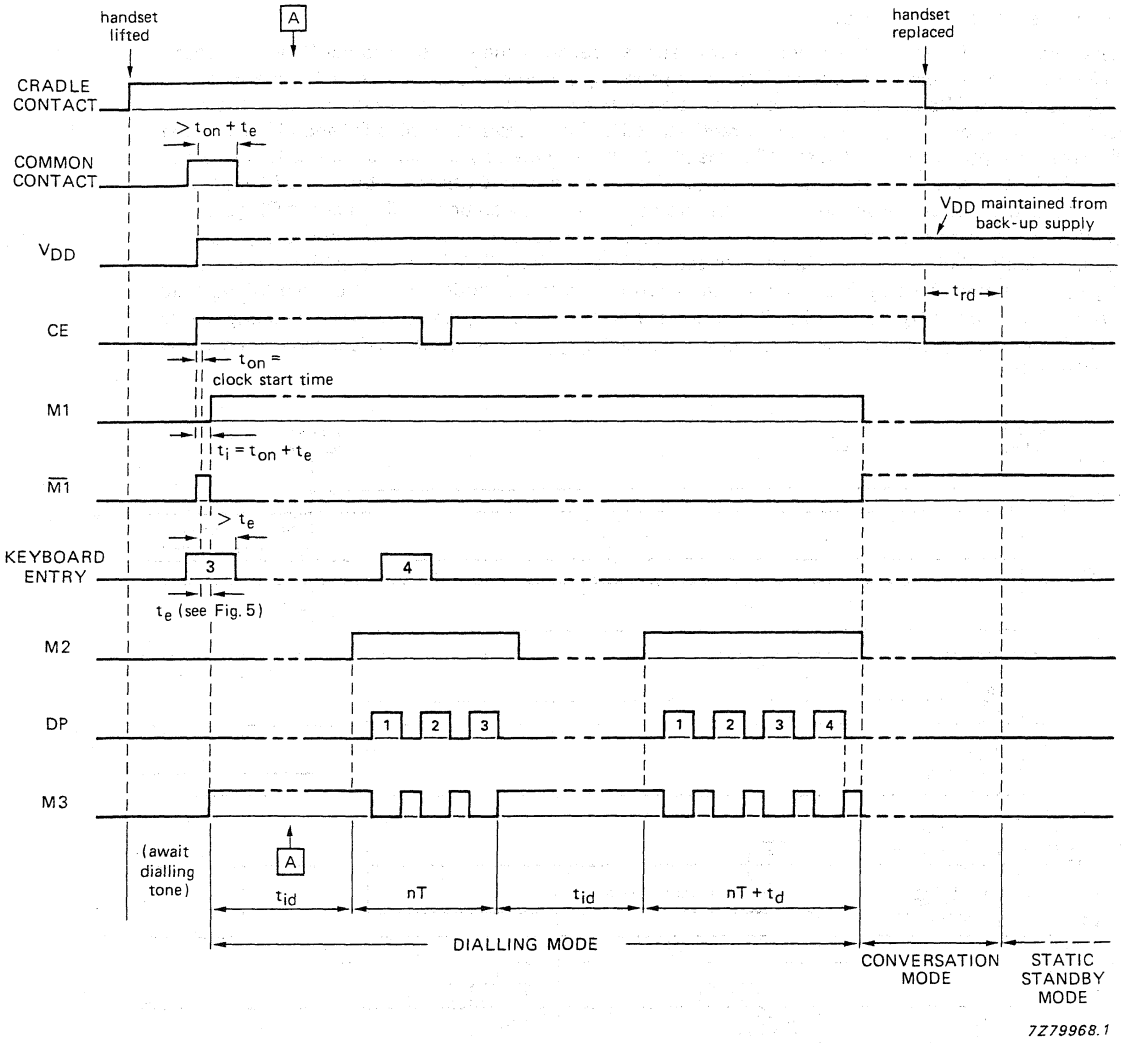


Fig.7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig.6 for pulse timings after point A.

Hold function (HOLD)

As shown in Fig.8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM to be converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

HOLD can be controlled by the Access Pause Output (see section "Access pause system).

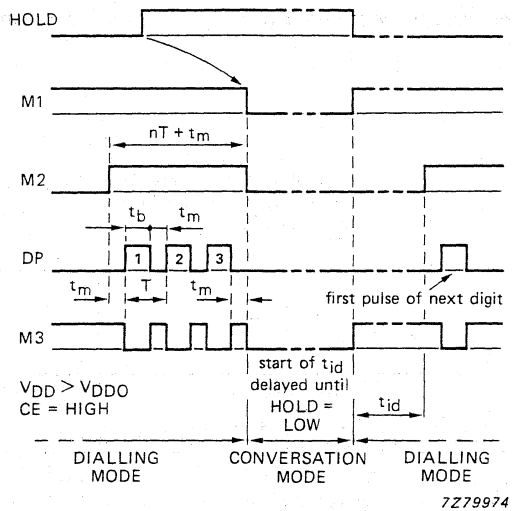


Fig.8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses.

Access pause system (HOLD/APO)

The PCD3320C and PCD3322C only have the HOLD input and therefore these devices cannot reproduce the access pauses during redial (the access pause system is disabled). In all the other devices the HOLD input is internally connected to the APO output. This pin (HOLD/APO) can be used as an output, or forced as an input (e.g. by an external tone recognizer). Access pauses can be stored at appropriate positions in the RAM during the original entry of a number. As soon as the access pause code is read from the RAM, the access pause output (HOLD/APO) goes HIGH and dialling is interrupted.

Storing access pauses during dialling

Access pauses can be stored by one or both of the following ways:

- Manually by pressing the access pause key (*). The number of access pauses that can be stored in this way is limited only by the capacity of the RAM (digits + access pauses $\leqslant$ 23).
- In some ICs of the family an access pause is stored automatically in the RAM (see Fig.9) during the original entry after all the digits so far entered have been transmitted (when M1 goes LOW, see Fig.6). The maximum number of access pause codes that can be entered in this manner is either one or two, depending on the type of IC.

Note: that when access pauses are manually inserted into ICs with automatic insertion of access pauses, the circuit automatically adds an access pause code after the number. This increases the RAM digit-count by one and reduces the maximum number of digits to 22 (including actual access pauses). The same would happen if the maximum number of access pauses for automatic entry is not reached before the end of the number.

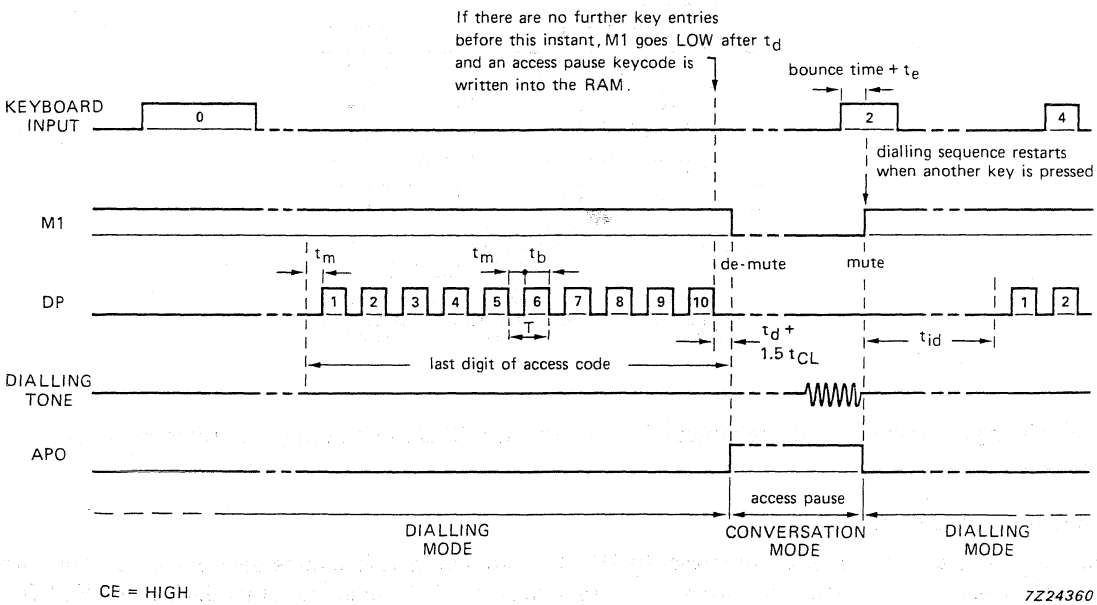


Fig.9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Terminating access pauses during redial (APD)

If APO is connected to HOLD, there are three ways of terminating access pauses during redial (see Fig.10):

- Manually by pressing the redial key before t_{ap} expires.
- Automatically if the built-in time t_{ap} expires; APO, and also HOLD, then go LOW so that the next digit will be dialled. With the Access Pause Delay (APD) select input, t_{ap} can be set to one of two values. With ICs that do not terminate access pauses in this way, t_{ap} is virtually infinity.
- By forcing HOLD/APO LOW (e.g. with an external tone recognizer).

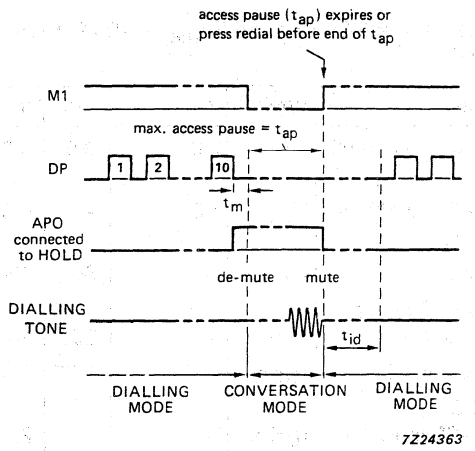
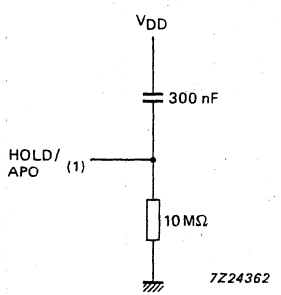


Fig.10 Timing diagram showing access pause reset.

For types with automatic reset of the access pause it is possible to lengthen the access pulse duration with external components (see Fig.11).



(1) $\Delta t_{ap} \approx 2$ s.

Fig.11 External circuit required to lengthen the access pause for ICs with automatic reset of the access pause.

FAMILY RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0.5	8.0	V
Voltage on any pin		V_I	V_{SS}−0.3	V_{DD}+0.3	V
Operating ambient temperature range		T_{amb}	−25	+70	°C
Storage temperature ramge		T_{stg}	−55	+125	°C

FAMILY CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters f_{osc} = 3.58 MHz and R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage	T_{amb} = −25 to +70 °C	V_{DD}	2.0	3.0	6.0	V
Standby supply voltage (note 1)	T_{amb} = −25 to +70 °C	V_{DDO}	1.5	–	6.0	V
Operating supply current	CE = V_{DD}; notes 2 and 3	I_{DD}	–	60	120	μA
	V_{DD} = 6 V; CE = V_{DD}; notes 2 and 3	I_{DD}	–	200	400	μA
Standby supply current	CE = V_{SS}; note 2	I_{DDO}	–	0.65	2.0	μA
	V_{DD} = 1.8 V; T_{amb} = −25 to +70 °C	I_{DDO}	–	–	2	μA
Input voltage LOW	1.8 V ⩽ V_{DD} ⩽ 6 V	V_{IL}	–	–	0.3 x V_{DD}	V
Input voltage HIGH	1.8 V ⩽ V_{DD} ⩽ 6 V	V_{IH}	0.7 x V_{DD}	–	–	V
CE input leakage current						
LOW	CE = V_{SS}	$-I_{IL}$	–	–	50	nA
HIGH	CE = V_{DD}	I_{IH}	–	–	50	nA
M/S pull-up input current	V_I = V_{SS}	$-I_{IL}$	30	100	300	nA
F01, F02, HOLD/APO APD pull-down input current	V_I = V_{DD}	I_{IH}	30	100	300	nA
Matrix keyboard operation						
Keyboard current	Cn connected to Rn; CE = HIGH	I_K	–	30	–	μA
Keyboard 'ON' resistance	contact 'ON'; note 4	R_{KON}	–	–	2	kΩ
Keyboard 'OFF' resistance	contact 'OFF'; note 4	R_{KOFF}	1	–	–	MΩ

FAMILY CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Matrix keyboard operation (continued)						
Outputs R_1 to R_4						
sink current		I_O	–	3	–	mA
source current		$-I_O$	–	40	–	μA
Outputs M1, $\overline{M1}$, M2, M3, DP						
sink current	V_{OL} = 0.5 V	I_{OL}	0.7	2.0	4.0	mA
source current	V_{OH} = 2.5 V	$-I_{OH}$	0.65	1.8	3.6	mA
Outputs HOLD/APO						
source current	V_{OH} = 2.5 V	$-I_{OH}$	0.7	2.0	4.0	mA

Notes to family characteristics

1. V_{DDO} = 1.5 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between OSC IN and OSC OUT pins < 3 pF.
4. Guarantees correct keyboard operation.

FAMILY TIMING DATA

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 3.58 MHz

parameter	conditions	symbol	min.	typ.	max.	unit
Clock start-up time	CE: from V_{SS} to V_{DD} note 1	t_{on}	–	4	–	ms

Note to family timing data

1. Stray capacitance between OSC IN and OSC OUT < 3 pF.

FAMILY CURVES

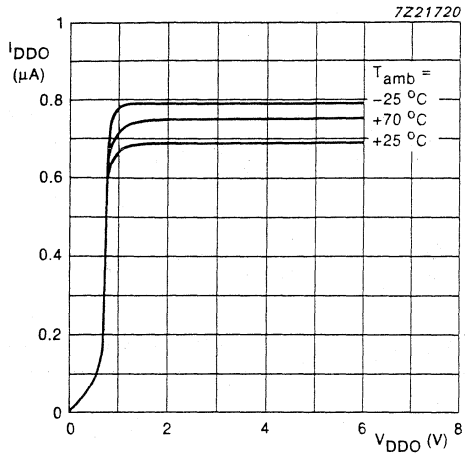


Fig.12 Standby supply current as a function of standby supply voltage.

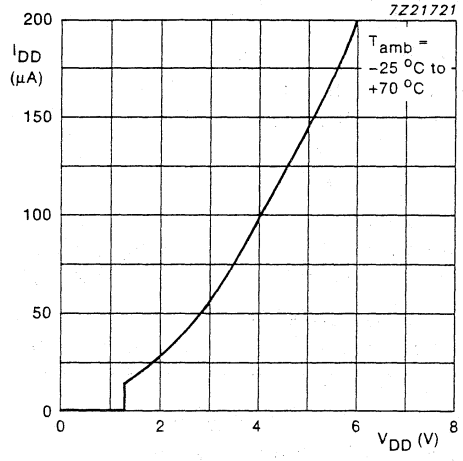


Fig.13 Operating supply as a function of operating supply voltage.

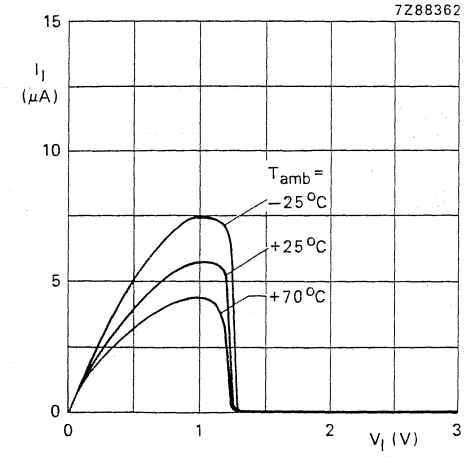


Fig.14 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

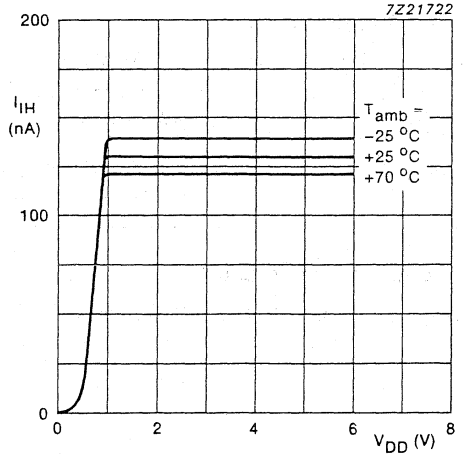


Fig.15 Pull-down input current as a function of supply voltage, $V_I = V_{DD}$.

FAMILY CURVES (continued)

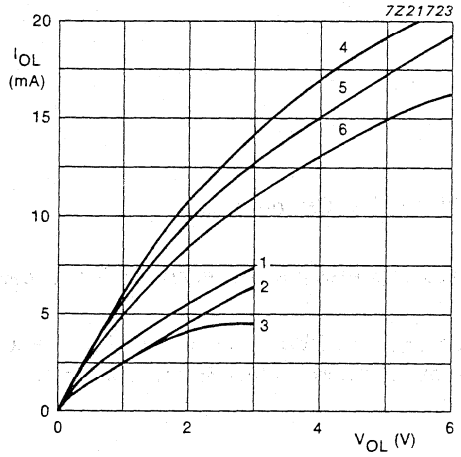


Fig.16 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M2, M3 and DP.

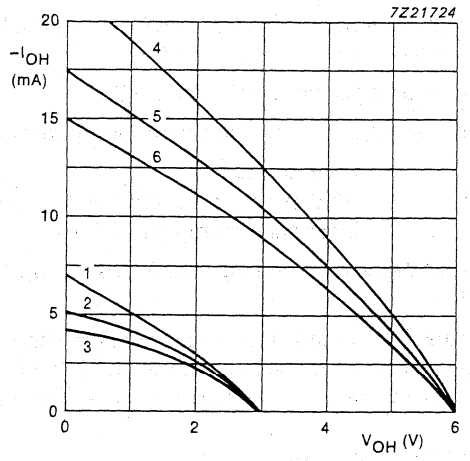


Fig.17 Output (P-channel) source characteristics for M1, $\overline{M1}$, M2, M3 and DP.

Key to Figs 16 and 17

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	curve 1	curve 4
+25 °C	curve 2	curve 5
+70 °C	curve 3	curve 6

CHARACTERISTICS PER TYPE

PCD3320C specification

Inputs that are not available are defined internally as follows:
F02 = APD = LOW and M/S = HIGH

Outputs not available are M2 and APO.

Features additional to the common family specification are:

$\overline{M1}$	inverted mute output
M3	AND-function of mute (M1) and inverted dialling pulse (DP) outputs
HOLD	input that interrupts dialling

Redial of the last entered number is possible up to 23 digits; access pauses are not generated. Mark/space ratio is 3:2.

Using the F01 input it is possible to select either normal mode (F01 = LOW) or test mode (F01 = HIGH). In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

PCD3320C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.58 MHz

parameter	conditions	symbol	FO1 = LOW (dialling)	unit
Dialling pulse frequency	note 1	f_{DP}	10.13	Hz
Dialling pulse period; $1/f_{DP}$	see Fig. 6 and 7	T_{DP}	98.7	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	Hz
Break time; 3/5 x T_{DP}	see Fig. 6	t_b	59.2	ms
Make time; 2/5 x T_{DP}	see Fig. 6	t_m	39.5	ms
Inter-digit pause; 8 x T_{DP}	see Figs 6 and 7	t_{id}	790	ms
Reset delay time; 1.6 x T_{DP}	see Figs 5, 6 and 7	t_{rd}	158	ms
Prepulse duration; 1/3 x T_{DP}	see Figs 6 and 7	t_d	33	ms
Debounce time;				
min. 5/30 x T_{DP}	see Fig. 5	$t_{e\,min}$	16.45	ms
max. 6/30 x T_{DP}	see Fig. 5	$t_{e\,max}$	19.74	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22	ms

Note to the PCD3320C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.

CHARACTERISTICS PER TYPE (continued)

PCD3321C specification

The PCD3321C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for Private Automatic Branch Exchange (PABX) systems. Two access pauses can be stored automatically during the original entry of a number, or several made via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are defined internally as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02 inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

HOLD/APO input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)

M/S input for M/S ratio selection to 3:2 or 2:1

PCD3321C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CL}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39.5	25.8	20.6	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65.8	42.9	34.3	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32.9	21.5	17.2	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Access pause time; 32 x T_{DP}-t_m-$1/f_{CL}$		t_{ap}	3.12	2.03	1.63	s

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time; min. 5/30 x T_{DP}		t_e min	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		t_e max	19.74	12.88	10.30	ms
Initial data time (typ.); $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3321C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

CHARACTERISTICS PER TYPE (continued)

PCD3322C specification

Inputs that are not available are defined internally as follows:

F02 = APD = LOW and M/S = HIGH

Outputs not available are M3 and APO.

Features additional to the common family specification are:

$\overline{M1}$	inverted mute output
M2	strobe; HIGH during pulsing of a digit, LOW during an inter-digit pause
HOLD	input that interrupts dialling

Redial of the last entered number is possible up to 23 digits; access pauses are not generated. Mark/space ratio is 3:2.

Using the F01 input it is possible to select either normal mode (F01 = LOW) or test mode (F01 = HIGH). In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

PCD3322C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.58 MHz

parameter	conditions	symbol	F01 = LOW (dialling)	unit
Dialling pulse frequency	note 1	f_{DP}	10.13	Hz
Dialling pulse period; $1/f_{DP}$	see Figs 6 and 7	T_{DP}	98.7	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	Hz
Break time; 3/5 x T_{DP}	see Fig.6	t_b	59.2	ms
Make time; 2/5 x T_{DP}	see Fig. 6	t_m	39.5	ms
Inter-digit pause; 8 x T_{DP}	see Figs 6 and 7	t_{id}	790	ms
Reset delay time; 1.6 x T_{DP}	see Figs 5,6 and 7	t_{rd}	158	ms
Prepulse duration; 1/3 x T_{DP}	see Figs 6 and 7	t_d	33	ms
Debounce time;				
min. 5/30 x T_{DP}	see Fig. 5	$t_{e\ min}$	16.45	ms
max. 6/30 x T_{DP}	see Fig. 5	$t_{e\ max}$	19.74	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22	ms

Note to the PCD3322C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.

PCD3324C specification

The PCD3324C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for PABX systems. One access pause can be stored automatically during the original entry of a number, or several made via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
M/S	input for M/S ratio selection to 3:2 or 2:1.

CHARACTERISTICS PER TYPE (continued)

PCD3324C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW HIGH LOW FO2: LOW HIGH HIGH			unit
Dialling pulse frequency $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse period: $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39.5	25.8	20.6	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65.8	42.9	34.3	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32.9	21.5	17.2	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time ; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Access pause time; 32 T_{DP}-t_m-$1/f_{CL}$		t_{ap}	3.12	2.03	1.63	s
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time; min. 5/30 x T_{DP}		$t_{e\ min}$	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		$t_{e\ max}$	19.74	12.88	10.30	ms
Initial data entry time (typ.) $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3324C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

PCD3325C specification

The PCD3325C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for PABX systems. Access pauses can be stored via the keyboard during the original entry of a number (there is no automatic storage of access pauses). The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either via the keyboard or with an external dial tone recognizer.

Inputs that are not available are defined internally as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02 inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

HOLD/APO input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected).

M/S input for M/S ratio selection to 3:2 or 2:1.

CHARACTERISTICS PER TYPE (continued)

PCD3325C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse perid; $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39.5	25.8	20.6	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65.8	42.9	34.3	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32.9	21.5	17.2	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time min. 5/30 x T_{DP}		$t_{e\ min}$	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		$t_{e\ max}$	19.74	12.88	10.30	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3325C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

PCD3326C specification

The PCD3326C includes many additional features that make it ideal for PABX systems. Two access pauses can be stored automatically during the original entry of a number, or several stored via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

M/S = HIGH

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
APD	input for selecting access pause duration.

CHARACTERISTICS PER TYPE (continued)

PCD3326C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	note 2	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	note 2	t_m	39.5	25.8	20.6	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Access pause time	APD = LOW;					
32 x T_{DP}-t_m-$1/f_{CL}$	or n.c.; note 3	t_{ap}	3.12	2.03	1.63	s
64 x T_{DP}-t_m-$1/f_{CL}$	APD = HIGH	t_{ap}	6.28	4.09	3.28	s
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time; min. 5/30 x T_{DP}		$t_{e\,min}$	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		$t_{e\,max}$	19.74	12.88	10.33	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3326C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. Mark/space ratio = 3:2.
3. In the n.c. (not connected) condition, the input is drawn to the LOW state by the internal pull-down current.

PCD3327C specification

The PCD3327C contains an oscillator with sufficient gain to provide oscillation when using an inexpensive 455 kHz ceramic resonator. Two additional capacitors are required as shown in Fig.18. Alternatively, the OSC IN pin may be driven from an external 455 kHz clock signal.

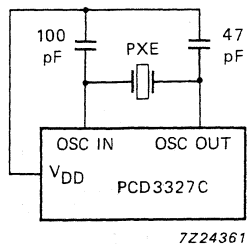


Fig.18 PCF3327 oscillator circuit.

This IC is pin-compatible with the DF320 and MT4320 types and includes additional features that make it ideal for PABX systems. The circuit allows several access pauses to be stored via the keyboard and regenerates the access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02 inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

HOLD/APO input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected).

M/S input for M/S ratio selection to 3:2 or 2:1.

CHARACTERISTICS PER TYPE (continued)

PCD3327C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 455 kHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.3	15.8	19.7	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	97	63	51	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	309	474	592	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	58	38	30	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39	25	20	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65	42	34	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32	21	17	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	776	506	405	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	155	101	81	ms
Access pause time; 32 x T_{DP}-t_m-$1/f_{CL}$		t_{ap}	3.12	2.03	1.63	s
Prepulse duration; 1/3 x T_{DP}		t_d	32	21	17	ms
Debounce time; min. 5/30 x T_{DP}		$t_{e\ min}$	16.18	10.54	8.45	ms
max. 6/30 x T_{DP}		$t_{e\ max}$	19.41	12.66	10.13	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3327C timing data

1. f_{DP} is 10 Hz when a 441.6 PXE ceramic resonator is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

Multistandard repertory dialler/ringer with EEPROM

PCD3330-1

FEATURES

Pulse/DTMF dialling

- Pulse dialling
- DTMF dialling
- Mixed mode dialling
- Number of digits per call is infinite (FIFO register)
- Flash or register recall
- Connect a/b to Earth function
- Mute functions
- Disconnect function
- Standard 4 x 4 keyboard for: 0 to 9 and *, #, A, B, C and D
- Function keys for: Flash, Hook, Mute, Tone and Disconnect
- On-hook dialling control
- Country specifications which can be stored in EEPROM are:
  Will * and/or # be transmitted when switching over to DTMF dialling mode
  Mark-to-space ratio (3 : 2 or 2 : 1)
  6 Tone time selections (60/90, 70/70, 80/80, 100/100, 100/140 or 140/140 ms)
  4 Flash time selections (100, 115, 270 or 600 ms)
  Mute output type selection (M1, $\overline{M1}$, M2 or $\overline{M2}$)
  DTMF keys or Function keys selection
- On-chip voltage reference for stabilized supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)

Number storage

- Redial Cursor method (maximum 24 digits) stored in internal EEPROM
- Storage for 13 repertory dial numbers (16 digits each) or 10 repertory dial numbers (20 digits each) in internal EEPROM
- Access pause generation and termination: manually or by Atlanta procedure
- Function keys for: LNR, Memory recall, Store, Access Pause and 1 key repertory
- Country specifications which can be stored in EEPROM are:
  Access pause time selection (1.5/1.0, 2.5/1.5, 3.0/3.5 or 6.0/6.0 s)
  10 Number repertory dialler selection (1 or 2 key)
  Two repertory number programming procedures (General or Germany)
  Repertory length (16 or 20 digits)

Ringer

- Ringer input frequency detection
- Function key for: Program Ringer
- Three-tone ringer with 4 different ringer frequencies
- Ringer melody generation with four signal speeds and four output volume steps, keypad controlled
- Country specifications which can be stored in EEPROM are:
  Ringer input frequency detection selection
  Ringer output selection (via DTMF or special RTO output)
  4 possible ringer melodies
  4 possible ringer repetition rates
  4 possible ringer volumes

General

- On-chip oscillator uses low-cost 3.58 MHz (TV colour burst) crystal or PXE resonator
- On-chip power-on reset (typically 2.0 V)
- Supply voltage range 1.8 to 6.0 V (2.5 to 6.0 V in EEPROM erase/write and DTMF and ringer mode)

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3330-1P	28	DIL	plastic	SOT117
PCD3330-1T	28	mini-pack	plastic	SO28; SOT136A

GENERAL DESCRIPTION

The PCD3330-1 is a mixed-mode multistandard repertory dialler/ringer IC frabricated in a low threshold voltage CMOS technology and is a member of the Philips family of telecommunication ICs.

The (maximum 13) repertory numbers, redial and various country specifications are stored in EEPROM so that memory retention is guaranteed for 10 years without using a battery back-up.
Therefore, different models can be created by changing the contents of some EEPROM bytes.

The various country specifications can be fulfilled by changing a few bytes in EEPROM which contain the different telephone timing and dialling procedures.

The two on-chip tone generators are used for Dual Tone Multi-Frequency (DTMF) dialling, and for generating a melody during ringing, which is activated when a correct incoming ringer frequency is detected.

As an output transducer for the ringer, a loudspeaker (ringer out via tone output) or a PXE (ringer out via the special ringer output which generates square wave ringer tones with a peak-to-peak voltage of V_{DD} to V_{SS}) can be used.

The operating supply voltage is 1.8 V (2.5 V in EEPROM erase/write and DTMF and ringer mode) to 6.0 V with a low current consumption in all operating modes: standby, conversation, dialling, programming and ringer.

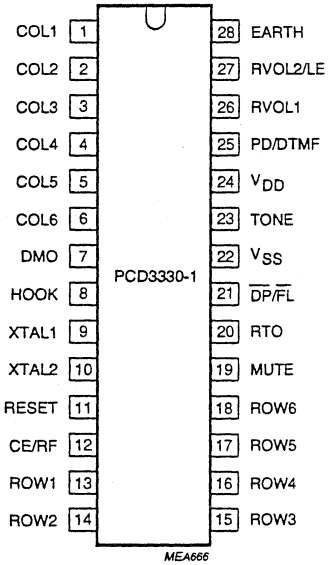


Fig.1 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
COL1	1	sense column keyboard input/programming EEPROM
COL2	2	sense column keyboard input/programming EEPROM
COL3	3	sense column keyboard input/programming EEPROM
COL4	4	sense column keyboard input/programming EEPROM
COL5	5	sense column keyboard input
COL6	6	sense column keyboard input
DMO	7	dial mode output
HOOK	8	cradle contact input
XTAL1	9	crystal/PXE oscillator input
XTAL2	10	crystal/PXE oscillator output
RESET	11	reset input
CE/RF	12	chip enable and zero crossing for ringer input
ROW1	13	scanning row keyboard output
ROW2	14	scanning row keyboard output
ROW3	15	scanning row keyboard output
ROW4	16	scanning row keyboard output
ROW5	17	scanning row keyboard output
ROW6	18	scanning row keyboard output
MUTE	19	mute output
RTO	20	ringer melody output
$\overline{DP/FL}$	21	dial pulse/flash inverted output
V_{SS}	22	negative supply
TONE	23	DTMF tones or ringer melody output
V_{DD}	24	positive supply
PD/DTMF	25	pulse/DTMF dial selection
RVOL1	26	ringer volume output 1
RVOL2/LSE	27	ringer volume output 2/loudspeaker enable output
EARTH	28	earth output

Multistandard pulse/tone repertory dialler/ringer

PCD3332-1

FEATURES

- Pulse and DTMF mixed mode dialling
- 10 number repertory dial up to 32 digits
- Last number redial up to 32 digits
- Flash and Earth register recall
- Access pause generation and termination
- Function keys for: Program, Memory recall, Flash, LNR, pause and Tone
- Strap functions:
  Mark-to-space ratio (3 : 2 or 2 : 1)
  Tone burst times
  Access pause time
  Pulse or DTMF switch
  Register recall Flash or Earth
  Parcifier tones select
  Ringer frequency select
- Ringer tone generation
- Ringer input frequency discriminator (20 to 54 Hz)
- Ringer sound selection via keypad
- Memory monitor
- Parcifier tones

GENERAL DESCRIPTION

The PCD3332-1 is a mixed-mode multistandard repertory dialler/ringer IC fabricated in a low threshold voltage CMOS technology and is a member of the Philips family of telecommunication ICs.

Dial parameters of this IC can be set by diode options to specific country requirements.

The on-chip tone generators are used for DTMF dialling and ringer melody generation.

A discriminator input enables the tone output only if a correct ringer frequency is applied.

The memory contents of a repertory dial location can be up to 32 digits with a maximum total of 254 digits.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3332-1P	28	DIL	plastic	SOT117
PCD3332-1T	28	mini-pack	plastic	SO28; SOT136A

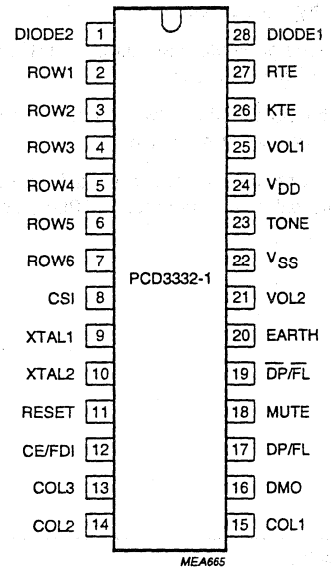


Fig.1 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
DIODE2	1	diode 2 option row
ROW1	2	row keyboard output
ROW2	3	row keyboard output
ROW3	4	row keyboard output
ROW4	5	row keyboard output
ROW5	6	row keyboard output
ROW6	7	row keyboard output
CSI	8	cradle switch input
XTAL1	9	oscillator input
XTAL2	10	oscillator output
RESET	11	reset input
CE/FDI	12	chip enable/frequency discriminator
COL3	13	column keyboard input
COL2	14	column keyboard input
COL1	15	column keyboard input
DMO	16	dial mode output
DP/FL	17	dial pulse/flash output
MUTE	18	mute output
$\overline{DP/FL}$	19	dial pulse/flash inverted
EARTH	20	earth recall output
VOL2	21	volume 2 output
V_{SS}	22	negative supply
TONE	23	tone generator output
V_{DD}	24	positive supply
VOL1	25	volume 1 output
KTE	26	key tone enable
RTE	27	ringer tone enable
DIODE1	28	diode 1 option row

Multi-standard pulse/tone repertory dialler/ringers

PCD3332-2; PCD3332-S

FEATURES

- Pulse and Dual Tone Multi-Frequency (DTMF) mixed mode dialling
- 13 number repertory dial up to 32 digits
  - 10 direct accessible or 3 direct plus 10 two-touch
- Last number redial up to 32 digits
- Repertory and redial memory integrity check (memory contents check)
- Notepad memory function
- Flash and earth register recall
- Access pause generation and termination
- On-chip power-on-reset
- Function keys for:
  - program
  - memory recall
  - flash
  - Last Number Redial (LNR)
  - pause
  - tone
- Strap functions:
  - mark-to-space ratio (3 : 2 or 2 : 1)
  - tone burst times
  - access pause time
  - pulse or DTMF switch
  - register recall flash or earth
  - pacifier tones select
  - ringer frequency select
- Ringer tone generator
- Ringer input frequency discriminator (20 to 54 Hz)
- Ringer sound selection via keypad
- Volume control for loudspeaking phones
- Pacifier tones
- On-hook dialling.

GENERAL DESCRIPTION

The PCD3332-2 and PCD3332-S are mixed-mode multi-standard repertory dialler/ringer ICs, fabricated in a low-threshold voltage CMOS technology and are members of the Philips Semiconductors family of telecom ICs. Dial parameters of these ICs can be set by diode options to specific country requirements. The on-chip tone generators are used for DTMF dialling and ringer melody generation. A discriminator input enables the tone output only if a correct ringer frequency is applied. The memory contents of a repertory dial location can be up to 32 digits with a maximum of 250 digits total.

Differences between the two devices are to be found on in Chapter "Ordering information".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3332-2P; PCD3332-SP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3332-2T; PCD3332-ST	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

PINNING

SYMBOL	PIN	DESCRIPTION
ROW2	1	row 2 keyboard output
ROW3	2	row 3 keyboard output
ROW4	3	row 4 keyboard output
ROW5	4	row 5 keyboard output
DIODE	5	diode option
MUTE	6	mute output
EARTH	7	earth recall
CSI	8	cradle switch input
XTAL1	9	oscillator input
XTAL2	10	oscillator output
RESET	11	reset input
CE/FDI	12	chip enable/frequency discriminator input
COL6	13	column 6 input
COL5	14	column 5 input
COL4	15	column 4 input
COL3	16	column 3 input
COL2	17	column 2 input
COL1	18	column 1 input
DPN/FLN	19	dial pulse/flash output
LFE	20	low-frequency amplifier enable
VOL2	21	volume 2 output
V_{SS}	22	supply ground
TONE	23	tone generator output
V_{DD}	24	supply voltage
VOL1	25	volume 1 output
DMO/KTE	26	dial mode output (pulse or DTMF)/keytone enable
HF/RTE	27	hands-free/ringer tone enable
ROW1	28	row 1 keyboard output

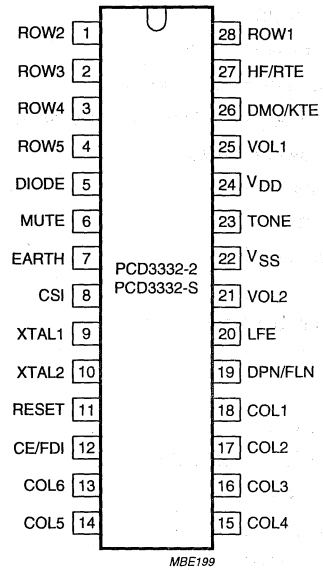


Fig.1 Pin configuration.

Telecom microcontroller with serial I/O interface

PCD3343A PCD3348A

CONTENTS

Telecom microcontroller with serial I/O interface

PCD3343A PCD3348A

1 FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 3 kbytes ROM, 224 bytes RAM (PCD3343A)
- 8 kbytes ROM, 256 bytes RAM (PCD3348A)
- Serial I/O interface with multi-master capability
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts:
  - external
  - 8-bit programmable timer/event counter 1
  - SIO/derivative
- Two test inputs, one of which also serves as the external interrupt input
- Power-on reset
- Stop and Idle modes
- Logic supply voltage: V_{DD} = 1.8 to 6 V
- Low stand-by voltage: V_{DD} = 1 V
- Low stand-by current: I_{DD} = 2 μA typical
- Clock frequency: 1 to 16 MHz
- Oscillator with output drive for peripherals (e.g. PCD3312 DTMF generator)
- Operating temperature: –25 to +70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3343A and PCD3348A. The shared characteristics of the PCD33XXA family of microcontrollers are described in the *"PCD33XXA family data sheet"*, which should be read in conjunction with this publication.

The PCD3343A and PCD3348A are microcontrollers intended for telecom applications. They provide 3 and 8 kbytes of program memory and 224 and 256 bytes of RAM, respectively. In addition to 20 I/O port lines, the microcontrollers provide an on-chip serial I/O interface.

This two-line serial bus extends the microcontroller capabilities when implemented with the powerful I^2C-bus devices of the PCF85XX, PCD33XX and 'Clips' peripheral families. These include liquid crystal display drivers, pulse and/or DTMF diallers, ringers, AD/DA converters, clock/calendar circuits, EEPROM and RAM.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3343AP	28	DIP	plastic	SOT117-1
PCD3348AP	28	DIP	plastic	SOT117-1
PCD3343AT	28	SO28L	plastic	SOT136-1
PCD3348AT	28	SO28L	plastic	SOT136-1

4 BLOCK DIAGRAM

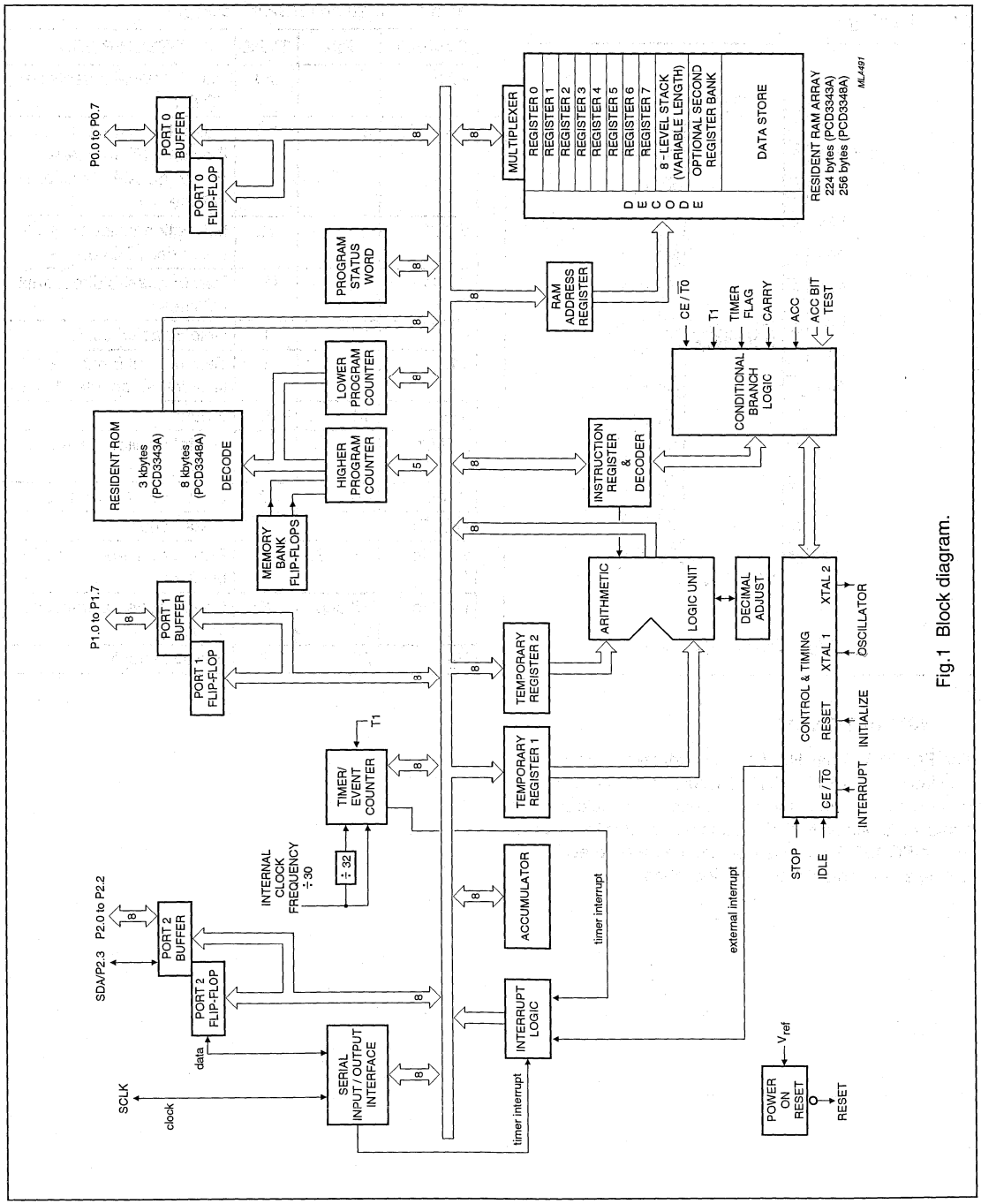


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

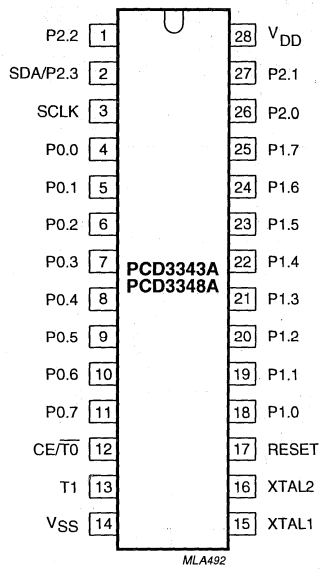


Fig.2 Pin configuration.

5.2 Pin description

Table 1 DIP28 and SO28L packages.

SYMBOL	PIN	TYPE	DESCRIPTION
P2.2	1	I/O	Port 2: quasi-bidirectional I/O line
SDA/P2.3	2	I/O	bidirectional data line of the serial I/O interface/ Port 2: quasi-bidirectional I/O line
SCLK	3	I/O	bidirectional clock line of the serial I/O interface
P0.0 to P0.7	4 to 11	I/O	Port 0: quasi-bidirectional I/O lines
CE/$\overline{T0}$	12	I	Chip Enable/Test 0
T1	13	I	Test 1/count input of 8-bit timer/event counter 1
V_{SS}	14	P	ground
XTAL1	15	I	crystal oscillator/external clock
XTAL2	16	O	crystal oscillator output
RESET	17	I	Reset input
P1.0 to P1.7	18 to 25	I/O	Port 1: quasi-bidirectional I/O lines
P2.0 to P2.1	26 and 27	I/O	Port 2: quasi-bidirectional I/O lines
V_{DD}	28	P	positive supply

6 INSTRUCTION SET

The PCD3343A has ROM space restricted to 3 kbytes. The instructions SEL MB1/2/3 would therefore define non-existing program memory banks and should be avoided. Additionally, RAM space is restricted to 224 bytes for the PCD3343A, so care should be taken to avoid accesses to non-existing RAM locations.

7 SUMMARY OF MASK OPTIONS

Table 2 Port mask options (see *"PCD33XXA family data sheet"*).

PORT	PORT OUTPUT[1]			PORT STATE AFTER RESET	
	OPTION 1	OPTION 2	OPTION 3	SET	RESET
P0.0 to P0.7	X	X	X	X	X
P1.0 to P1.7	X	X	X	X	X
P2.0 to P2.3	X	X	X	X	X
SDA /P2.3	–	X	–	X	–

Note

1. Option 1: normal port
   Option 2: open drain
   Option 3: push-pull.

Table 3 Mask options.

FEATURE	DESCRIPTION
ROM Code: program/data	Any mix of instructions and data up to ROM size of 3 kbytes (PCD3343A) and 8 kbytes (PCD3348A).
Power-on reset voltage level: V_{ref}	1.2 to 3.6 V in increments of 100 mV; OFF
Oscillator transconductance: g_m	LOW transconductance: g_{mL}
	MEDIUM transconductance: g_{mM}
	HIGH transconductance: g_{mH}

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+7	V
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	–50	+50	mA
T_{stg}	storage temperature	–65	+150	°C
T_j	operating junction temperature	–	90	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

10 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.579545 MHz (g_{mL}); $R_X \leq 100\ \Omega$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 3 to 8)						
V_{DD}	operating supply voltage	note 1	1.8	–	6	V
V_{DD}	RAM data retention Stop mode		1.0		6	V
I_{DD}	operating supply current	V_{DD} = 3 V; note 1	–	0.3	0.6	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL}); note 1	–	1.1	3.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM}); note 1	–	1.7	5.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); note 1	–	2.5	6.0	mA
$I_{DD(ID)}$	supply current Idle mode	V_{DD} = 3 V; note 1	–	0.2	0.4	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL}); note 1	–	0.8	1.6	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM}); note 1	–	1.2	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); note 1	–	1.7	5.0	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 2	–	1.2	2.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 °C; note 2	–	–	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	+1	µA
Outputs (see Figs 9 to 12)						
I_{OL}	LOW level port sink current except SDA/P2.3 and SCLK	V_{DD} = 3 V; V_O = 0.4 V	0.7	8	–	mA
I_{OL}	LOW level SIO sink current SDA/P2.3 and SCLK	V_{DD} = 3 V; V_O = 0.4 V	1.5	8	–	mA
I_{OH}	HIGH level port pull-up source current	V_O = 2.7 V; V_{DD} = 3 V	−10	−20	–	µA
		V_O = 0 V; V_{DD} = 3 V	–	−100	−300	µA
I_{OH}	HIGH level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	−0.7	−4	–	mA
ΔV_{POR}	power-on reset level variation around chosen V_{POR}	note 3	−0.5	0	+0.5	V

Notes

1. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; all other outputs open. Maximum values: external clock at XTAL1; XTAL2 open. Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; RESET, T1 and CE/$\overline{T0}$ at V_{SS}; crystal connected between XTAL1 and XTAL2; all other outputs open.
3. V_{POR} is an option chosen by the user. Depending on its value, it may restrict the supply voltage range.

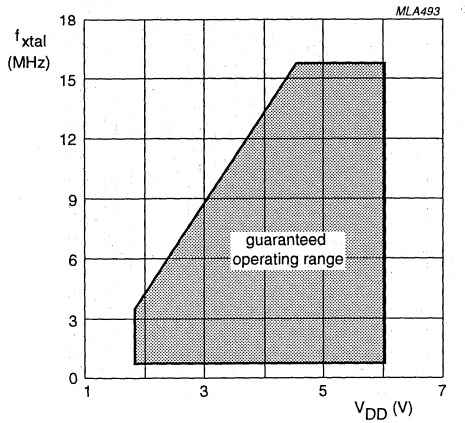


Fig.3 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

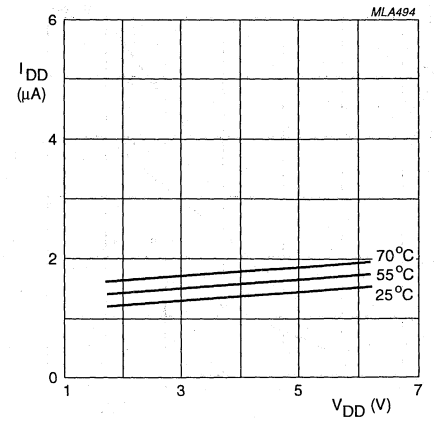


Fig.4 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).

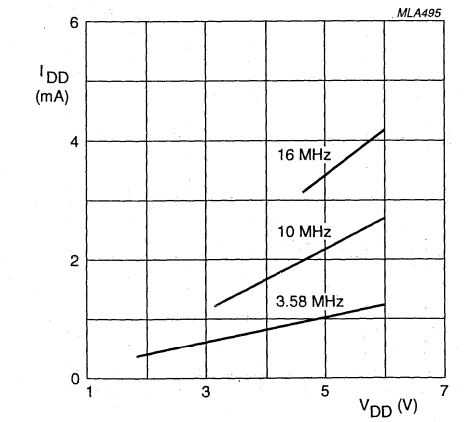


Fig.5 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).

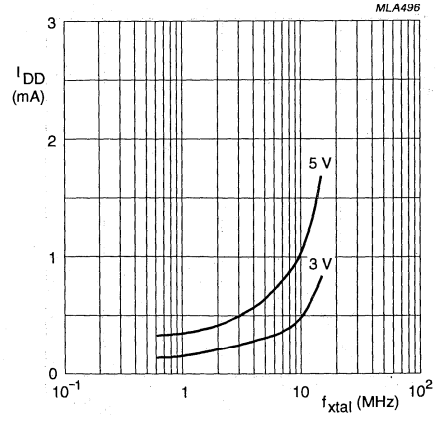


Fig.6 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).

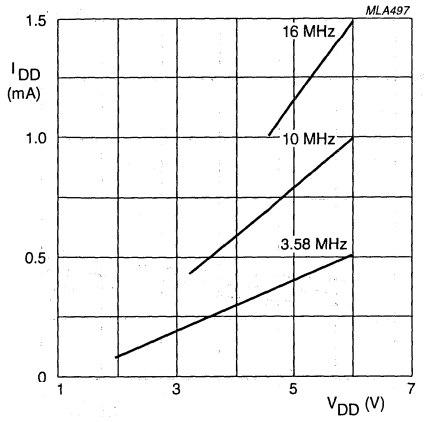


Fig.7 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).

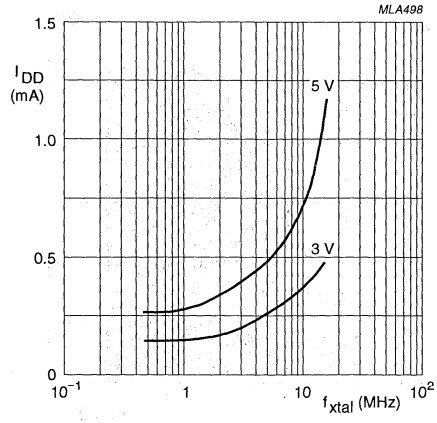
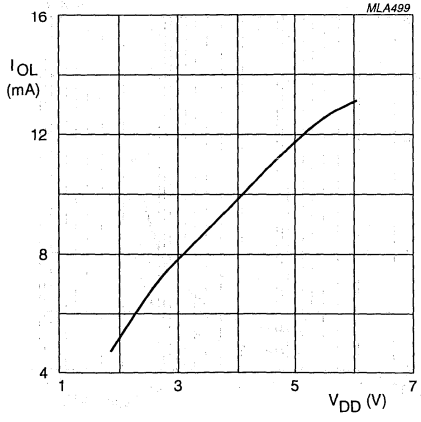
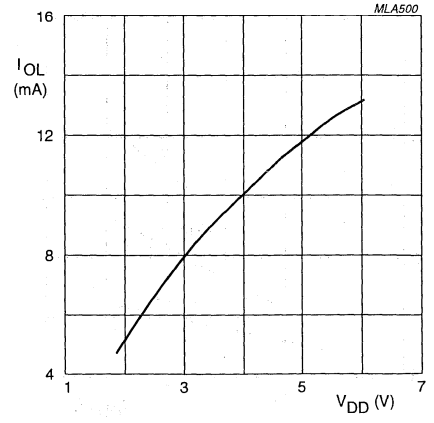


Fig.8 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).



V_O = 0.4 V.

Fig.9 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).



V_O = 0.4 V.

Fig.10 Typical SDA/P2.3 or SCLK LOW level output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

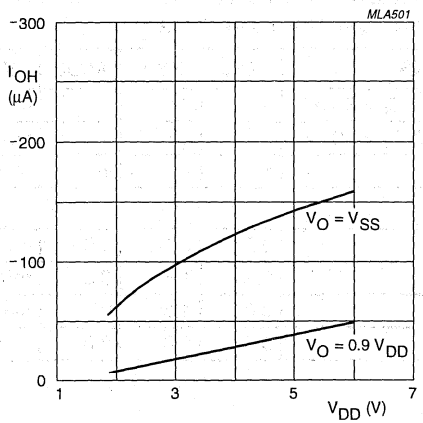
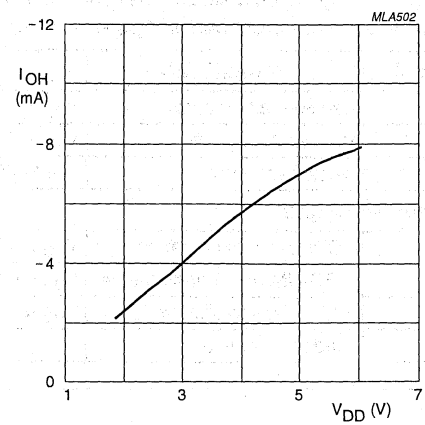


Fig.11 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.12 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

11 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; all other outputs open. Maximum values: external clock at XTAL1; XTAL2 open. Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
f_{xtal}	clock frequency	see Fig.3	1	–	16	MHz
Oscillator (see Fig.13)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance	V_{DD} = 5 V	0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance	V_{DD} = 5 V	3.0	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

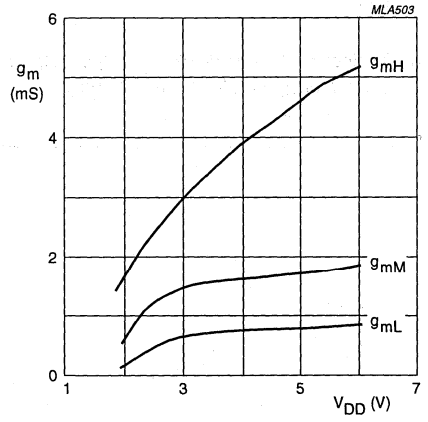


Fig.13 Typical transconductance as a function of supply voltage (V_{DD}) for the options g_{mL}, g_{mM} and g_{mH}.

11.1 I²C-bus interface characteristics

Table 4 I²C-bus timing.

SYMBOL	PARAMETER	INPUT (see Fig.14)	OUTPUT (see Fig.15; note 1)
SCLK			
$t_{HD;STA}$	START condition hold time	$\geq \frac{14}{f_{xtal}}$	$\frac{DF+9}{2 \times f_{xtal}}$
t_{LOW}	SCLK LOW time	$\geq \frac{17}{f_{xtal}}$	$\frac{DF-3}{2 \times f_{xtal}}$; note 2
t_{HIGH}	SCLK HIGH time	$\geq \frac{17}{f_{xtal}}$	$\frac{DF+3}{2 \times f_{xtal}}$; note 2
t_{RC}	SCLK rise time	≤ 1 µs	≤ 1 µs; note 3
t_{FC}	SCLK fall time	≤ 0.3 µs	≤ 0.1 µs; note 4
SDA			
t_{BUF}	bus free time	$\geq \frac{14}{f_{xtal}}$	≥ 4.7 µs; note 5
$t_{SU;DAT}$	data set-up time	≥ 250 ns	$\geq \frac{15}{f_{xtal}}$; note 6
$t_{HD;DAT}$	data hold time	≥ 0	$\geq \frac{9}{f_{xtal}}$
t_{RD}	SDA/P2.3 rise time	≤ 1 µs	≤ 1 µs; note 3
t_{FD}	SDA/P2.3 fall time	≤ 0.3 µs	≤ 0.1 µs; note 4
$t_{SU;STO}$	STOP condition set-up time	$\geq \frac{14}{f_{xtal}}$	$\frac{DF-3}{2 \times f_{xtal}}$

Notes

1. DF stands for divisor of f_{xtal} (see *"PCD33XXA family data sheet"*).
2. Values given for ASC = 0; for ASC =1: $t_{HIGH} = \frac{3(DF+1)}{4 \times f_{xtal}}$; $t_{LOW} = \frac{DF-3}{4 \times f_{xtal}}$.
3. Determined by I²C-bus capacitance (C_b) and external pull-up resistor.
4. At maximum allowed I²C-bus capacitance C_b = 400 pF.
5. Determined by program.
6. If $t_{LOW} < \frac{24}{f_{xtal}}$, $t_{SU:DAT} \geq \frac{t_{LOW}-9}{f_{xtal}}$, independent of ASC.

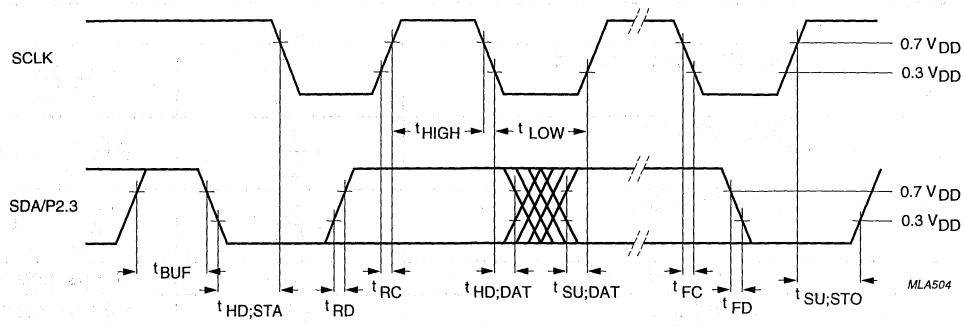


Fig.14 Slave SCLK and receiver SDA/P2.3 timing (SCLK and SDA/P2.3 are inputs).

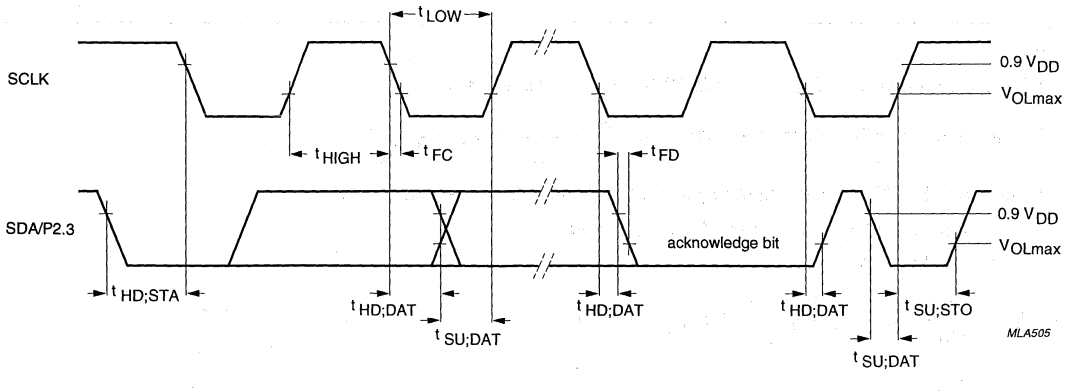
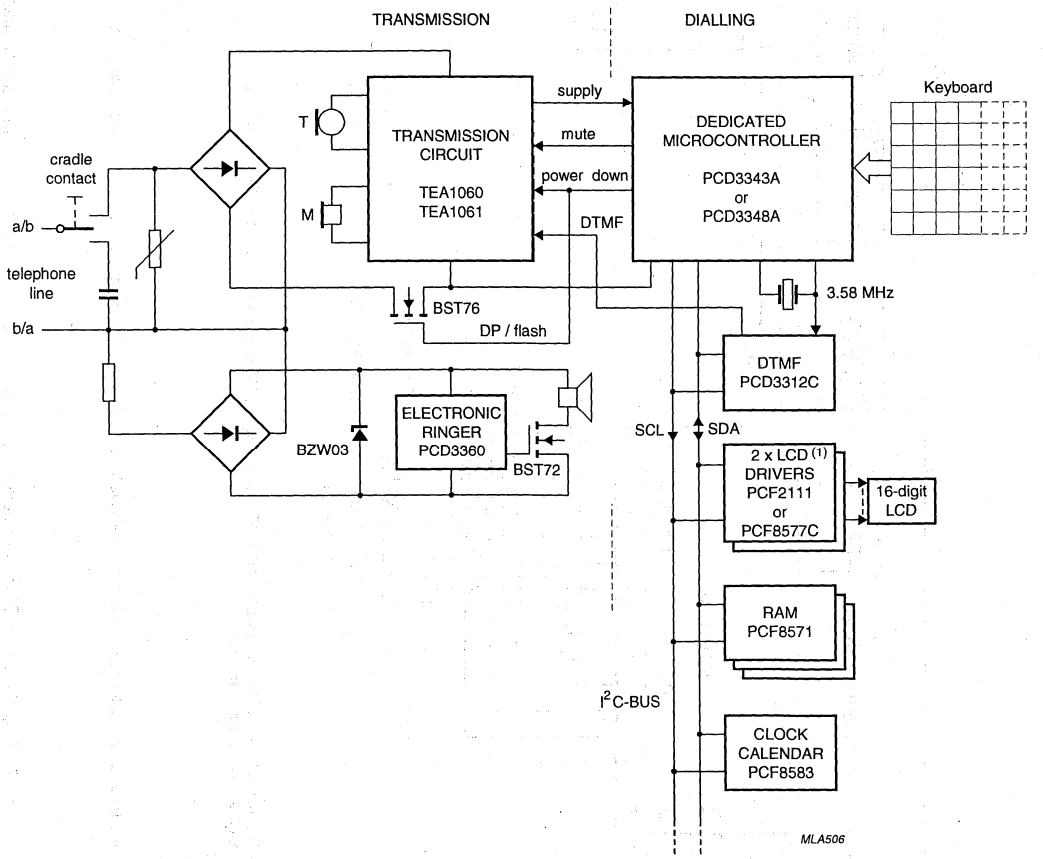


Fig.15 Master SCLK and transmitter SDA/P2.3 timing (SCLK and SDA/P2.3 are outputs).

12 APPLICATION INFORMATION

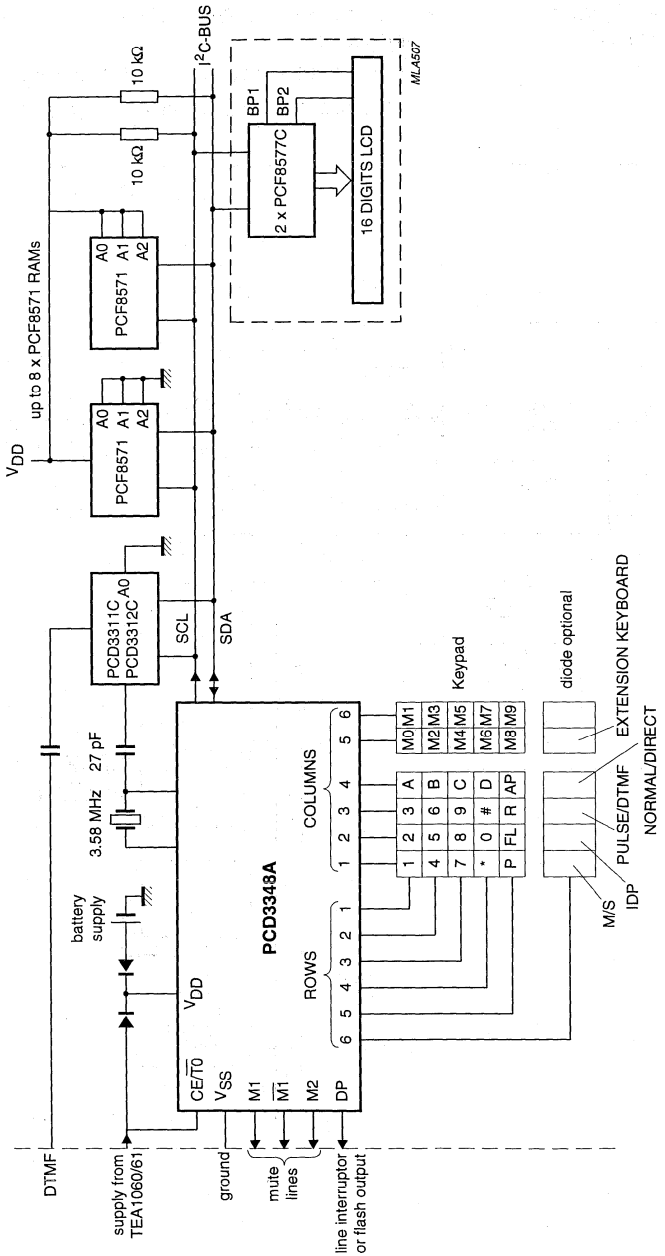
A block diagram of an electronic feature-phone built around the PCD3343A/48A is shown in Fig.16. It comprises the following dedicated telecom ICs:

- TEA1060/1061: transmission circuit for telephony
- PCD3312C: DTMF generator with I²C-bus interface
- PCF2111 or PCF8577C: 2 LCD drivers in LCD module MB7020160
- PCF8571: 1 kbyte RAMs with I²C-bus interfaces
- PCD3360/3361: programmable multi-tone ringer.



(1) Maximum 8.

Fig.16 Block diagram of an electronic feature-phone with common line interface.



A more detailed schematic of the PCD3343A/48A with: PCD3312 (DTMF), two PCF8571 (RAMs) and two PCF2111 (LCD drivers).
Row 5 of the keyboard contains the following special keys:
P: program and autodial
FL: flash or register recall
R: redial or extended redial
AP: access pause
Row 6 contains the different diode options. Columns 5 and 6 contain the keys M0 to M9 used as single name keys for repertory telephone numbers.

Fig.17 PCD3343A/PCD3348A application for an electronic feature-phone with associated keyboard.

Single-chip 8-bit Telecom Microcontroller

PCD3344A PCD3349A

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 2 k ROM bytes (PCD3344A)
- 4 k ROM bytes (PCD3349A)
- 224 bytes RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- Two single-level vectored interrupts: external, 8-bit programmable timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT CS203 compatible)
- Power-on reset
- Stop and idle modes
- Logic supply from 1.8 V to 6 V (DTMF tone output from 2.5 V)
- Low standby voltage of 1 V
- Low standby current of 2 μA (typ.)
- Clock frequency from 1 MHz to 16 MHz (3.58 MHz for DTMF suggested)
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3344A and PCD3349A. The shared characteristics of the PCD33XXA family of microcontrollers are described in the PCD33XXA family data sheet, which should be read in conjunction with this publication.
The PCD3344A and PCD3349A are microcontrollers which have been designed primarily for Telecom applications. They include an on-chip dual tone multi-frequency (DTMF) generator. The PCD3344A and the PCD3349A provide 2 k and 4 k bytes respectively of program memory, 224 bytes of RAM and 20 I/O lines. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	−0.5	+7.0	V
V_I	all input voltages	−0.5	V_{DD}+0.5	V
I_I,I_O	DC input or output current	−10	+10	mA
I_{SS}	ground supply current	−50	+50	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
T_{stg}	storage temperature range	−55	+150	°C
T_j	operating junction temperature	−	90	°C

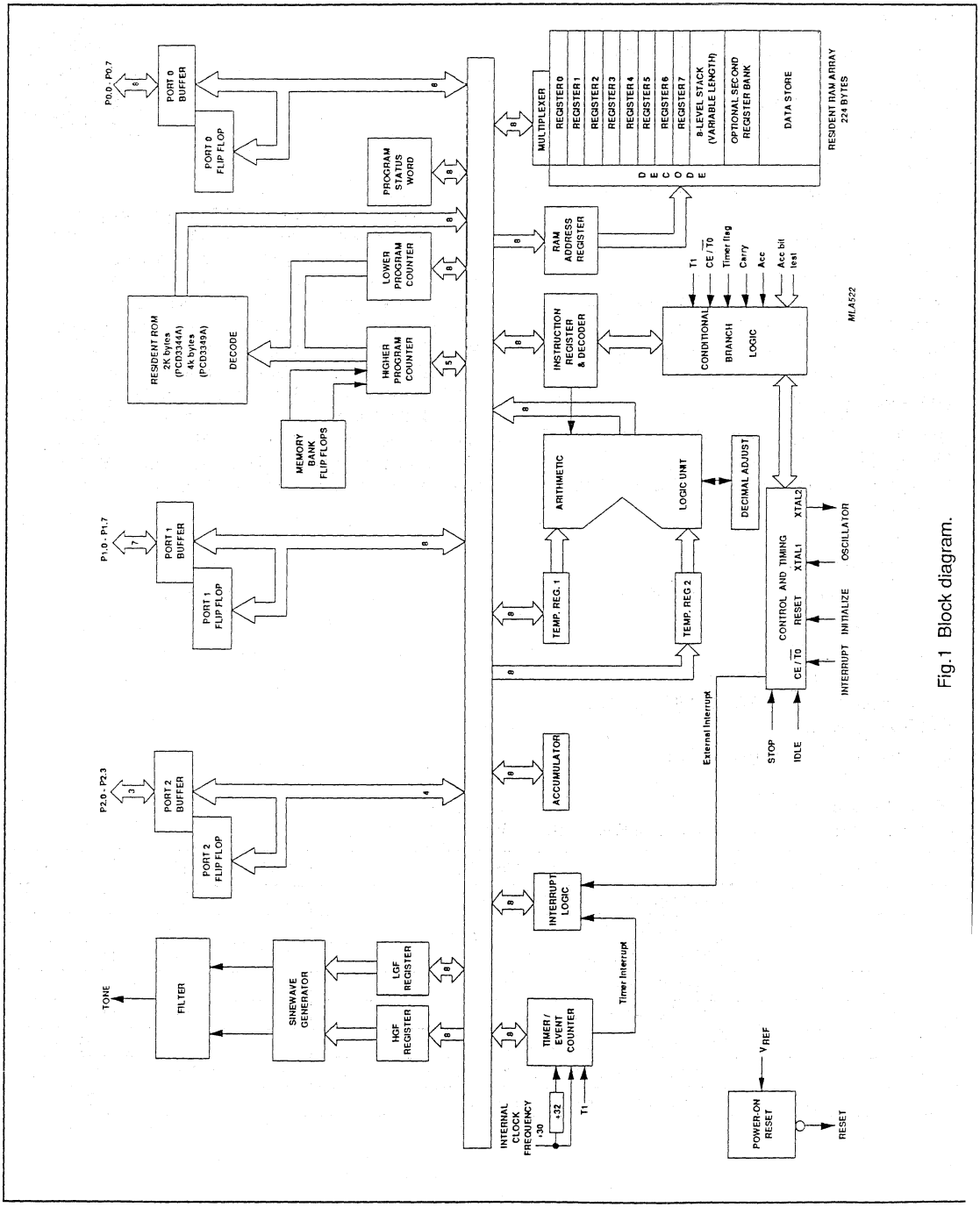


Fig.1 Block diagram.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3344AP/49AP	28	DIL	plastic	SOT117
PCD3344AT/49AT	28	mini-pack	plastic	SOT136A

Note to the Ordering Information

Full and up-to-date data for this device is available upon request via your Philips local sales office.

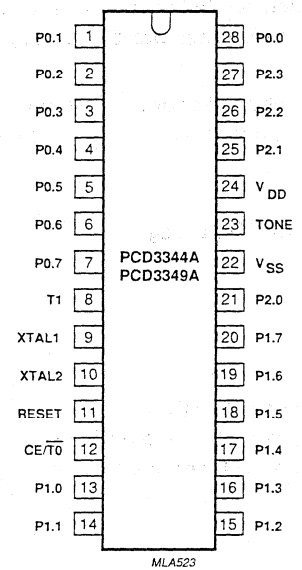


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
P0.1-P0.7	1-7	I/O	Port 0: quasi-bidirectional I/O lines
T1	8	I	test 1/count input of 8-bit timer/event counter 1
XTAL1	9	I	crystal oscillator/ external clock input
XTAL2	10	O	crystal oscillator output
RESET	11	I	reset input
$CE/\overline{T0}$	12	I	chip enable / test 0
P1.0-P1.7	13-20	I/O	Port 1: quasi-bidirectional I/O line
P2.0	21	I/O	Port 2: quasi-bidirectional I/O line
V_{SS}	22	P	ground
TONE	23	O	DTMF output
V_{DD}	24	P	positive supply voltage
P2.1-P2.3	25-27	I/O	Port 2: quasi-bidirectional I/O lines
P0.0	28	I/O	Port 0: quasi-bidirectional I/O line

Single-chip 8-bit microcontroller PCD3346

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The PCD3346 is a single-chip 8-bit microcontroller manufactured in CMOS technology. The PCD3346 is a member of the PCD33XX family and as such has special on-chip features for telephony applications.

The PCD3346 has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt circuit, two 8-bit timer event counters and on-board clock oscillator and clock circuits. The PCD3346 also incorporates 256 bytes of EEPROM permitting intermediate data storage without the need for battery back-up.

The instruction set is based on that of the MAB8048 and is instruction set compatible with the MAB8400 family. The PCD3346 has bit handling abilities for both binary and BCD arithmetic.

Features

- 8-bit CPU, ROM, EEPROM, RAM, I/O in a single 28-lead DIL or SO package
- 4 K ROM bytes
- 128 RAM bytes
- 256 bytes EEPROM
- 20 quasi-bidirectional I/O port lines
- 2 x 8-bit programmable timers
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter, serial I/O and derivative port
- I^2C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- Clock frequency 450 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2.5 V to 6.0 V
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals (e.g. PCD3312 DTMF generator)
- Individual mask configuration of all port lines for: pull-up, push-pull or open drain
- Power-on-reset circuit and low supply voltage detection
- Individual mask selection of reset state for all ports
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3346P: 28-lead DIL; plastic (SOT117).
PCD3346T: 28-lead mini-pack; plastic (SO28; SOT136A).

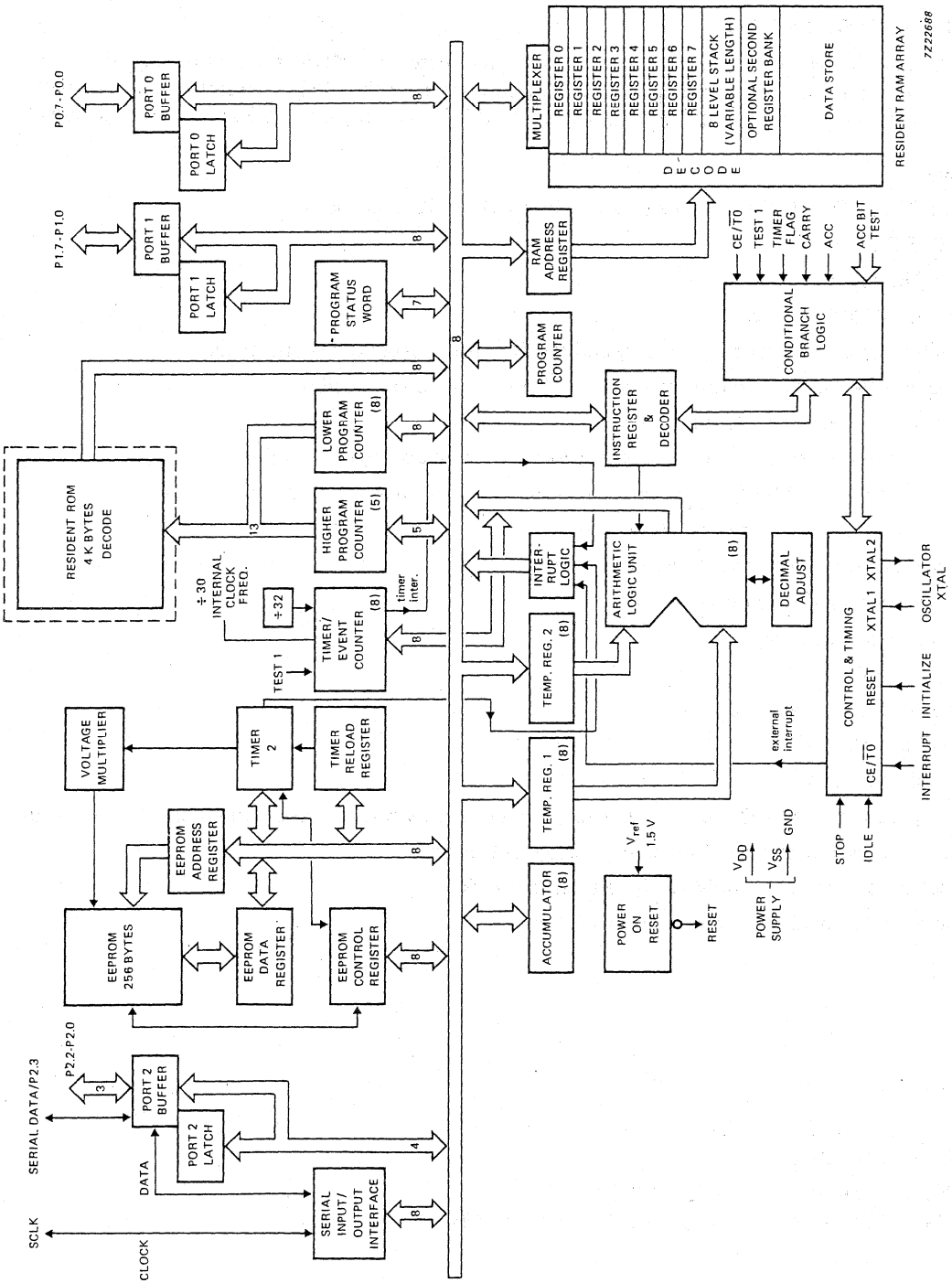


Fig. 1 Block diagram.

CMOS microcontroller with on-chip DTMF generator

PCD3347

GENERAL DESCRIPTION

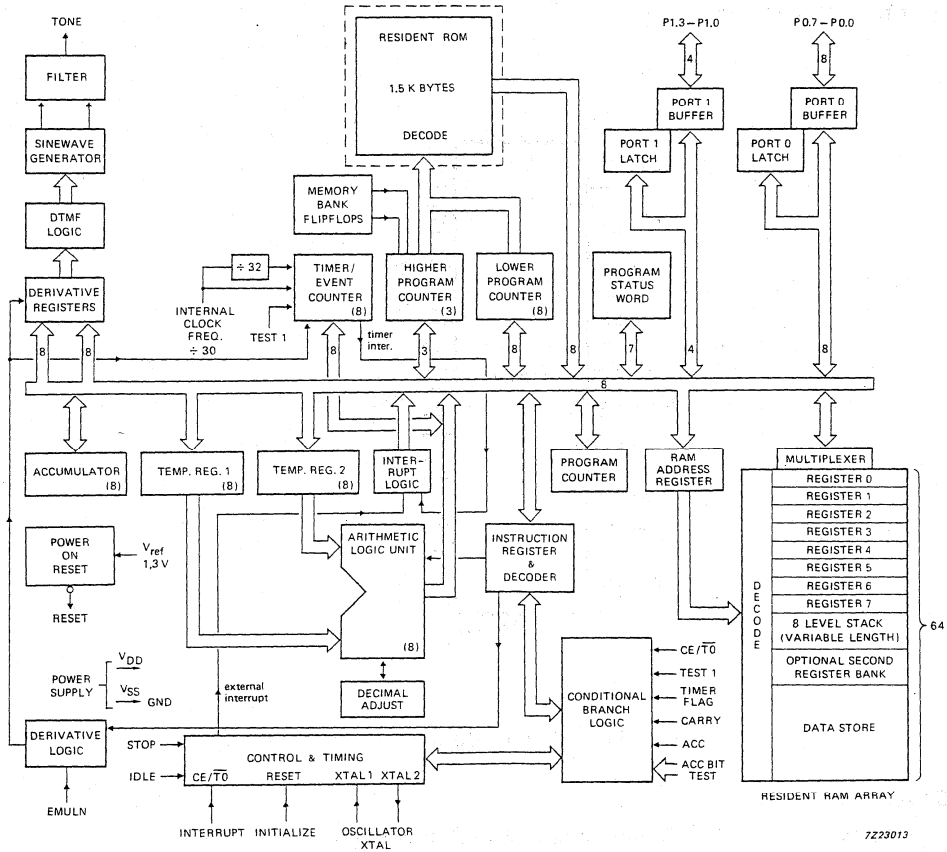
The PCD3347 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD33XX family. It has an on-chip dual tone multi-frequency (DTMF) generator and other features for application in telephone sets. For further detailed information, see PCD33XX family specification.

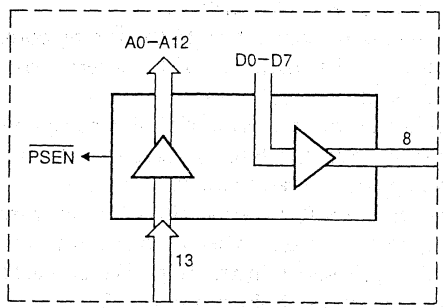
Features

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead DIL or SO package
- 1536 ROM bytes
- 64 RAM bytes
- On-chip DTMF tone generator
- On-chip voltage reference for supply and temperature-independent tone output
- On-chip filtering for low output distortion (CEPT CS203 compatible)
- 12 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles
- Clock frequency 3,58 MHz
- Single supply voltage from 2,5 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3347P: 20-lead DIL; plastic (SOT146).
PCD3347T: 20-lead mini-pack; plastic (SO20; SOT163A).





(a)

Fig. 1 PCD3347 block diagram: the function in the dotted outline is replaced as shown in (a) for the PCD3344B 'piggy-back' version.

PINNING (for normal operation)

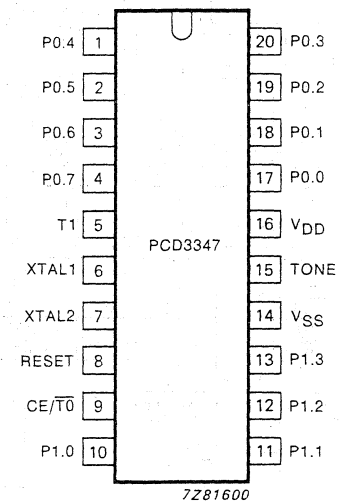


Fig. 2 Pinning diagram.

PIN DESIGNATION

17-20, 1-4	P0.0-P0.7	Port 0: 8-bit quasi-bidirectional I/O port.
5	T1	Test 1: test input, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter using the STRT CNT instruction.
6	XTAL1	Crystal input: connection to the timing component (crystal) which determines the frequency of the internal oscillator; is also the input for an external clock source.
7	XTAL2	Connection to other side of timing component.
8	RESET	Reset input (active HIGH): used to initialize the processor or output of the power-on-reset circuit.
9	CE/$\overline{T0}$	Interrupt/Test 0: external interrupt input (sensitive to positive-going edge)/test input pin. When used as a test input is directly tested by conditional branch instructions JT0 and JNT0.
10-13	P1.0-P1.3	Port 1: 4-bit quasi-bidirectional I/O port.
14	V_{SS}	Ground: circuit earth potentional.
15	TONE	Tone output: single or dual tone frequency output with on-chip filtering for low output distortion (CEPT CS203 compatible). This generator is controlled via the internal processor bus.
16	V_{DD}	Power supply: 2,5 to 6 V.

FUNCTIONAL DESCRIPTION

Program memory PCD3347

The program memory comprises 1536 bytes (8-bit words) in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 3 shows the program memory map.

Three program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine,
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

The program memory is divided into location 'pages', each of 256 bytes. This division applies only for conditional branches. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory PCD3347

Data memory consists of 64 bytes (8-bit words) of random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 4 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently-addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 5) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with next generated return address.

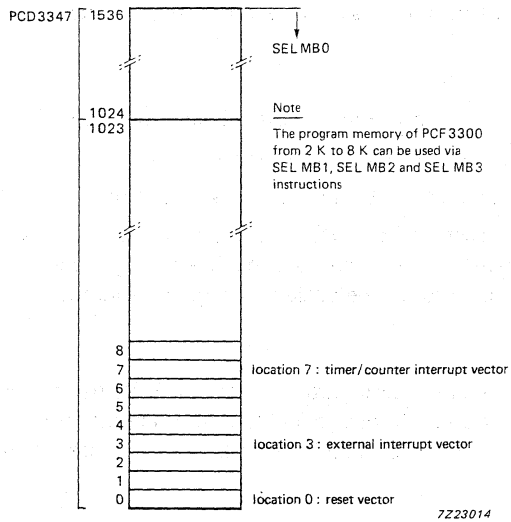


Fig. 3 Program memory map.

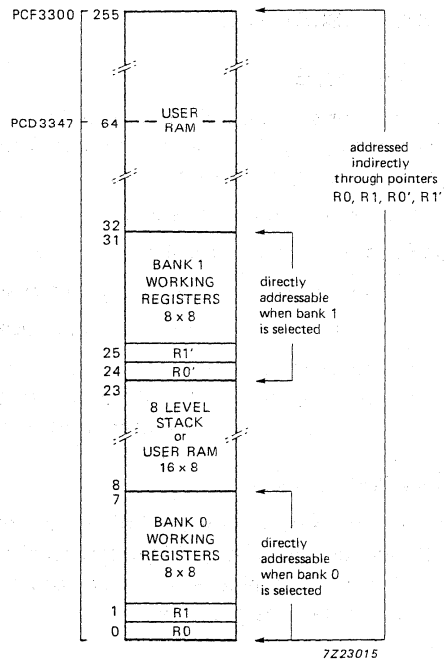


Fig. 4 Data memory map.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 64 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

FUNCTIONAL DESCRIPTION (continued)

Program counter stack (continued)

stack pointer									
1 1 1	----------								R23/22
1 1 0	----------								R21/20
1 0 1	----------								R19/18
1 0 0	----------								R17/16
0 1 1	----------								R15/14
0 1 0	----------								R13/12
0 0 1	----------								R11/10
0 0 0	PSW7	PSW6	PC12	PSW4	PC11	PC10	PC9	PC8	R9
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	R8

Fig. 5 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (H'01') the oscillator and timer/counter are kept running. The microcontroller exits from the IDLE mode by one of two interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 6).

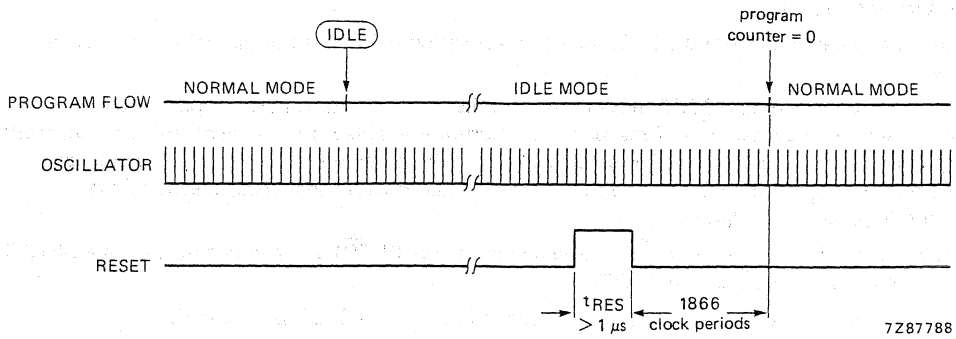


Fig. 6 Exit from IDLE mode via a RESET.

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW-to-HIGH transition on the external interrupt pin (CE/$\overline{T0}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{T0}$ will reactivate the microcontroller only in the STOP mode. Thus, if CE/$\overline{T0}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Fig. 7).

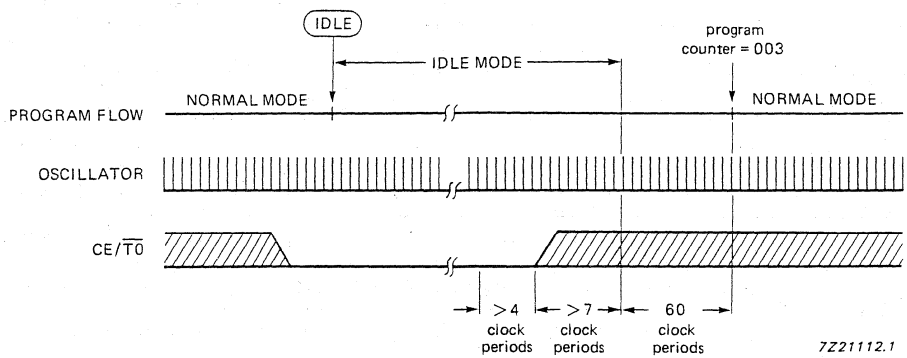


Fig. 7 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when CE/$\overline{T0}$ is LOW for 4 CP (clock periods) followed by a HIGH for 7 CP. After the initial forced CALL H'003' operation (60 CP) the program continues with the external interrupt service routine.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (H'22'). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 8).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin HIGH, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{T0}$ pin, and not by a LOW-to-HIGH transition as in a normal interrupt mechanism.

When the CE/$\overline{T0}$ level is active during the STOP instruction then no STOP is executed.

A HIGH level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

FUNCTIONAL DESCRIPTION (continued)

STOP mode (continued)

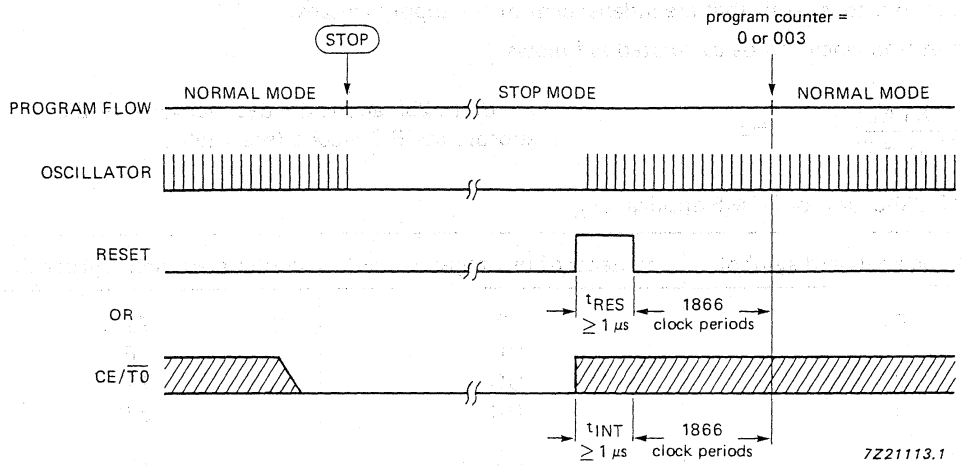


Fig. 8 Entering and exiting the STOP mode.

Tone output (DTMF mode)

Control of the sinewave generator

The on-chip sinewave oscillator is controlled by the 'derivative' registers Dx (x = H'O' to 'FF'). The instruction that controls the derivative registers is shown in Table 1.

Table 1 Derivative register control

mnemonic	opcode	description	function
MOV Dx,A	8D Dx	move accumulator contents to derivative register	(Dx) ← (A)

The instruction is 2 cycles/2 bytes. The second byte selects the derivative register to be addressed (H'O' to 'FF'). Register H'01' is for control of HIGH group frequencies, and register H'02' for control of LOW group frequencies. Thus data transport from accumulator to derivative register D01 is done by the 2-byte opcode 8D,01.

Generation of frequencies

The single and dual tones at the tone output are filtered by an on-chip switched-capacitor filter followed by an on-chip active RC low-pass filter. These ensure that the total harmonic distortion of the DTMF tones fulfil the CEPT CS 203 recommendations. An on-chip reference voltage provides output tone levels that are independent of the supply voltage.

The output frequency can be calculated as follows:

$$f_{out} = \frac{f_{XTAL}}{23\,(x + 2)} \quad \text{Hz}$$

x = 60 to 255 and is the decimal value of the appropriate ROM-code (see Table 2)

Table 2 ROM-codes for DTMF applications

telephone keyboard symbol	contents of low register (hex)	contents of high register (hex)
0	A3	72
1	DD	7F
2	DD	72
3	DD	67
4	C8	7F
5	C8	72
6	C8	67
7	B5	7F
8	B5	72
9	B5	67
A	DD	5D
B	C8	5D
C	B5	5D
D	A3	5D
*	A3	7F
#	A3	67

DTMF generation is stopped by loading H'00' into both derivative registers.

I/O facilities

The PCD3344 family has 14 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P0.0 to P0.7)
- Port 1 parallel port of 4 lines (P1.0 to P1.3)
- CE/$\overline{T0}$ external interrupt and test input. When used as a test input it can be directly tested by conditional branch instructions JT0 and JNT0.
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

FUNCTIONAL DESCRIPTION (continued)

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional. Output data written to a port is latched and remains unchanged until rewritten. Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one LS-TTL or CMOS load.

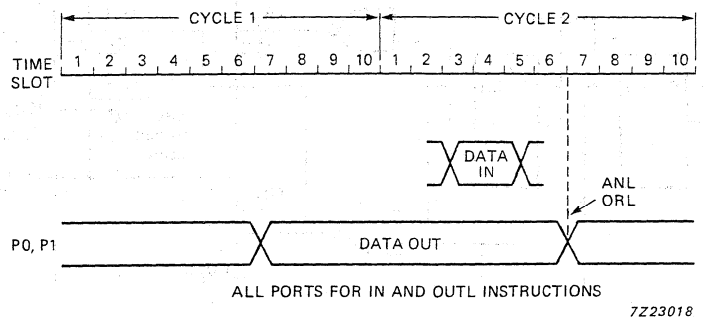


Fig. 9 Timing diagram of all ports on IN and OUTL instructions; for ANL and ORL instructions, the ports change on the time slot 7 of cycle 2.

Fig. 10 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source. Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current source provides sufficient current for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period) to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore the PCD3347 offers the possibility to select individually the 12 parallel port pins by the following mask options:

Option 1 – STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2 (2,5 mA). TR2 is active only during 1 clock cycle (0,28 μs at 3,58 MHz).

Option 2 – OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 11).

Option 3 – PUSH-PULL OUTPUT; drive capability of the output will be 2,5 mA (typ.) at V_{DD} = 3 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must be used only as outputs (Fig. 12).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2 or 3.

Option S-SET; after RESET this pin will be initialized to HIGH

Option R-RESET; after RESET this pin will be initialized to LOW.

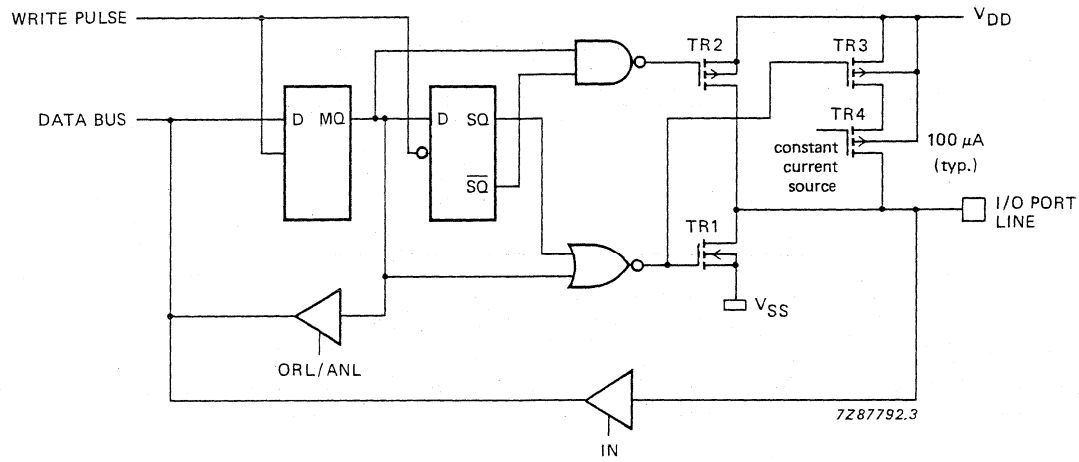


Fig. 10 Standard output with switched pull-up current source.

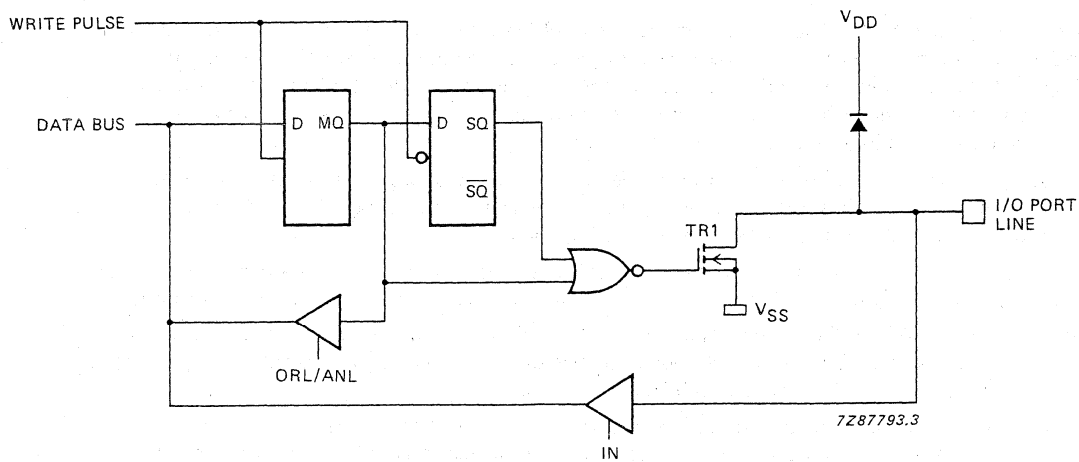


Fig. 11 Open drain output.

FUNCTIONAL DESCRIPTION (continued)

Parallel ports (continued)

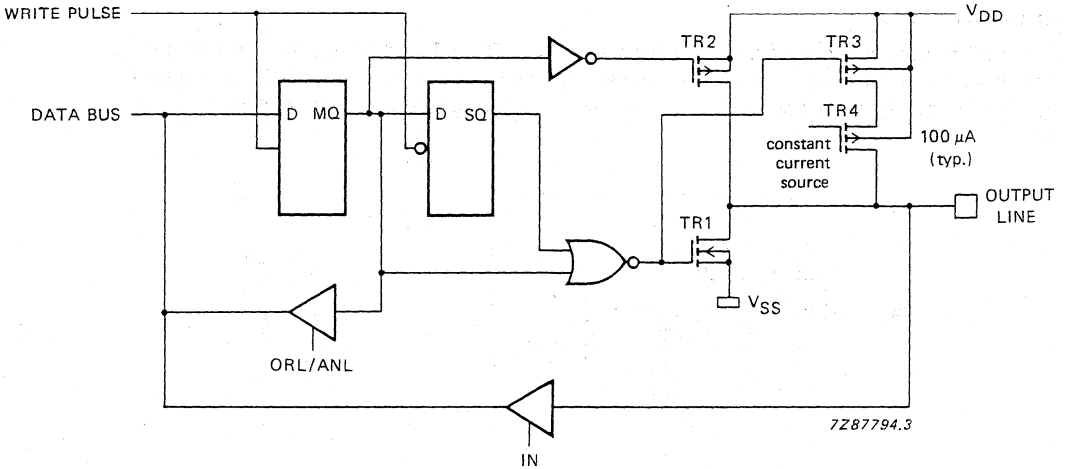


Fig. 12 Push-pull output.

Interrupts (see Fig. 13(a) and Fig. 13(b))

When an interrupt routine is entered, the contents of the program counter and bits 4, 6 and 7 of the PSW are saved in the program counter stack. The contents of the accumulator can only be saved by user software. Interrupt acknowledgement can be carried out by software via I/O ports. All interrupt routines must reside in memory bank 0; the SEL MB1, SEL MB2 and SEL MB3 instructions may not be used in an interrupt routine. An interrupt routine can only be terminated by the RETR (return and restore) instruction. During an interrupt routine, subroutine calls must be terminated by the RET instruction. Using the RETR instruction to terminate a subroutine called in an interrupt routine would terminate the interrupt routine prematurely and result in a wrong return address.

1. **External interrupt**

When the external interrupt is enabled, a HIGH-to-LOW transition on the CE/$\overline{TO}$ input initiates an external interrupt routine which forces a call to program memory location 3. The program counter points to the external interrupt vector address (003 H) between 2,6 and 3,6 machine cycles after the transition occurs. Interrupt latency depends on the instruction that is being executed when the transition occurs. External interrupts are latched in the External Interrupt Flag (EIF) even when they are not enabled. Execution of a DIS I instruction clears previously latched interrupts, the digital filter latch and the external interrupt flag.

2. **Timer/counter interrupt**

When the timer interrupt is enabled, a timer/counter overflow sets the Timer Interrupt Flag (TIF) and forces a CALL to location 7. The timer interrupts are only latched when they are enabled. The timer flag is set every time the timer/counter overflows and is not automatically reset when the timer/counter interrupt routine is called. It can only be cleared by the JTF and JNTF instructions or by a hardware RESET.

3. Simultaneous interrupts

If simultaneous interrupts occur their priority is as follows:

external (highest);
timer/counter (lowest).

An interrupt routine can only be interrupted by a hardware RESET and cannot be interrupted by other interrupts (which will be latched if enabled). When the interrupt routine is terminated by the RETR instruction, at least one instruction of the main program will be executed before another interrupt routine is entered.

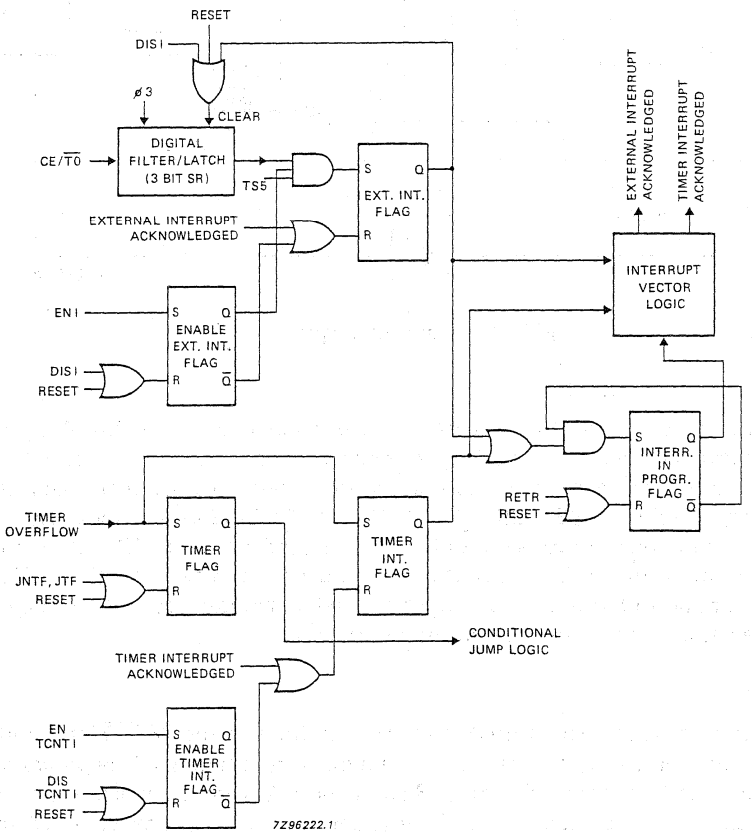


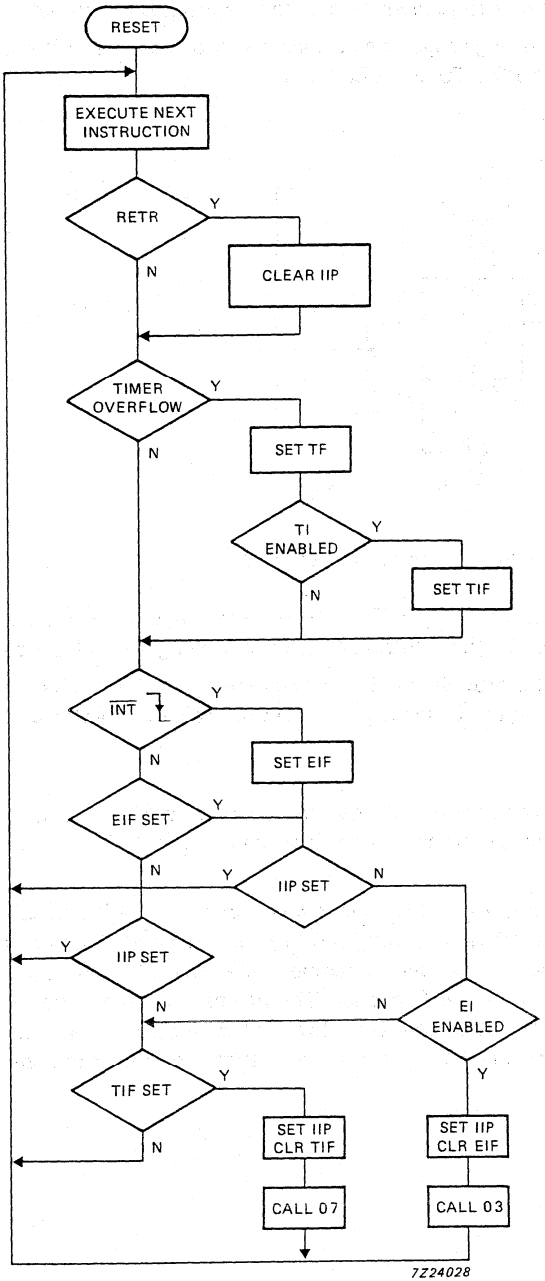
Fig. 13(a) Interrupt logic.

Notes to figure 13(a)

1. CE/$\overline{T0}$ positive edge is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when CE/$\overline{T0}$ is LOW for $>$ 4 CP followed by a HIGH for $>$ 7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.
5. For all flip-flops, RESET overrules SET.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (continued)



EI External Interrupt
TI Timer/counter Interrupt
EIF External Interrupt Flag
TF Timer Flag
IIP Interrupt In Progress flag

Fig. 13(b) Interrupt flowchart.

Oscillator (see Fig. 14)

The 3,58 MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-voltage condition is present to prevent discharge of a weak back-up battery.

Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at either the CE/$\overline{T0}$ or RESET pin.

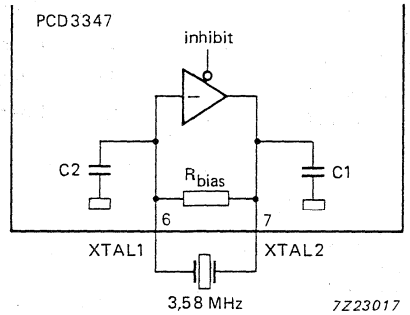


Fig. 14 Oscillator with integrated elements.

The oscillator has an output drive capability from pin 7 (XTAL2). An external clock can be applied to pin 6 (XTAL1). A machine cycle comprises 10 time slots, each time slot being 3 oscillator periods.

In telephony applications the 3,58 MHz crystal provides an 8,4 μs machine cycle. The range of the clock frequency is from 100 kHz up to a maximum which is a function of the supply voltage.

Timer/event counter (see Fig. 15)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 3 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 8 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (182,6 kHz for an 8,4 μs machine cycle). When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump if timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

FUNCTIONAL DESCRIPTION (continued)

Timer/event counter (continued)

Table 3 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.

** READ does not disturb the counting process.

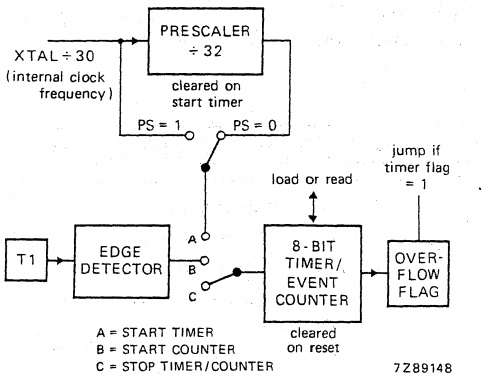


Fig. 15 Timer/event counter.

Program status word (see Fig. 16)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS);
  0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS);
  0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

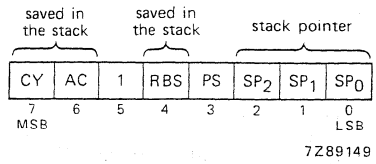


Fig. 16 Program status word.

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 17).

A 12-bit program counter is used to facilitate 8 K bytes of ROM being addressed. The arrangement of the bits is shown in Figure 17. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 12 bits are saved in the stack during CALL and interrupt routines.

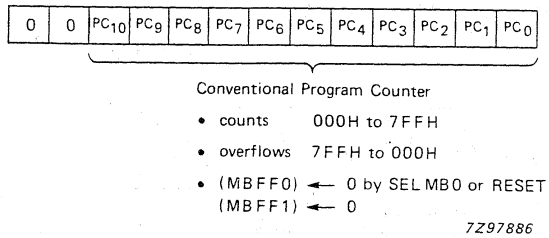


Fig. 17 Program counter.

Central processing unit

The PCD3347 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the CURRENT ROM page.

FUNCTIONAL DESCRIPTION (continued)

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program.
Table 4 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 4 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JNT0
	0	JT0*
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

* Because of the inverted interrupt input CE/$\overline{T0}$ the conditional jump JT0 is also inverted.

Test input T1 (pin 8)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for $>$ 4 CP, followed by a HIGH for $>$ 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100\ k\Omega$).
When T1 is not used pin 8 must be connected to V_{DD} or V_{SS}.

Reset (pin 11)

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external and timer)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports according to reset states
- Cancels IDLE and STOP mode

After the voltage is applied to RESET an internal delay of 1866 CP is introduced before the microcontroller commences operation.

Power-on reset

The internal power-on reset circuit monitors the supply voltage V_{DD}. As long as V_{DD} remains below the internal reference level V_{ref} (typically 1,3 V), the oscillator is inhibited and RESET (pin 8) has an undefined level. When V_{DD} rises above V_{ref}, the oscillator is released and RESET is pulled HIGH to V_{DD} by TR1 for a period t_D (typically 50 μs). Note that the start-up time of the oscillator is typically 10 ms because of the narrow bandwidth of the crystal.

Three modes of power-on reset are possible:

1. If V_{DD} has a fast rise time, i.e. V_{DD} reaches its minimum value before the RESET signal finishes (t_D), then no additional circuit is required (see Figs 18 and 19). Note that the first instruction is executed after the oscillator start-up time plus 1866 clock periods.
2. If V_{DD} has a slow rise time then the RESET signal should be stretched by an external CR circuit (see Figs 20 and 21). In the event of a short drop in V_{DD}, the diode path discharges the capacitor rapidly to ensure a reliable power-on reset. The RESET signal should reach at least 70% of the final value of V_{DD} to ensure a correct reset. Given that the RESET voltage and V_{DD} rise exponentially, the above requirement is satisfied when the time constant of the RESET pulse is > 8 times the time constant of V_{DD}. If V_{DD} rises linearly then a RESET time constant > 2 times the rise time of V_{DD} is required.

   When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods (see Fig. 21). If the oscillator starts up prior to the completion of RESET then program execution begins 1866 clock periods after RESET goes LOW.
3. Fig. 22 shows an external reset applied during power-on. The external reset signal must remain HIGH until V_{DD} has reached its minimum operating value corresponding to the selected oscillator frequency. When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods (see Fig. 23). If the oscillator starts up prior to the completion of RESET then program execution begins 1866 clock periods after RESET goes LOW.

FUNCTIONAL DESCRIPTION (continued)

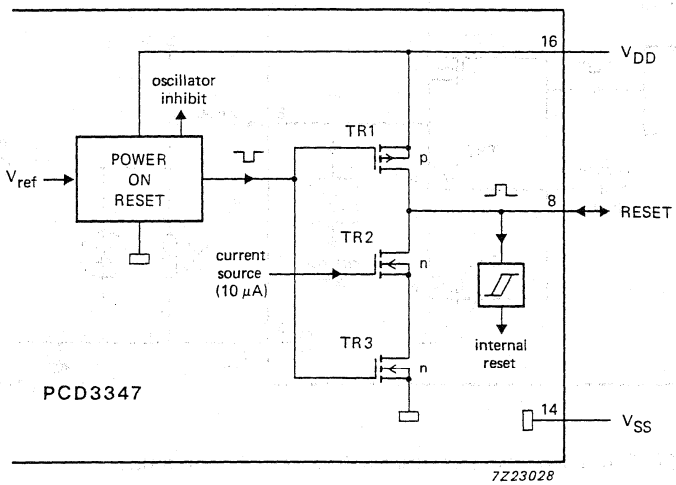


Fig. 18 Power-on reset configuration.

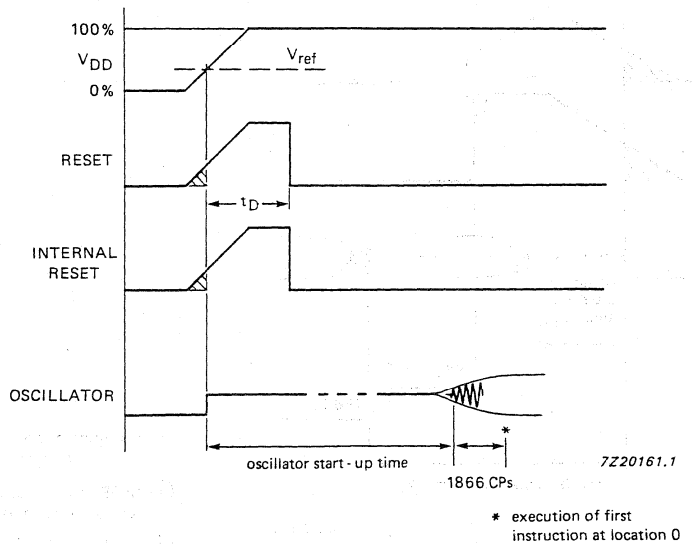


Fig. 19 Timing of power-on reset with fast rise time of V_{DD}.

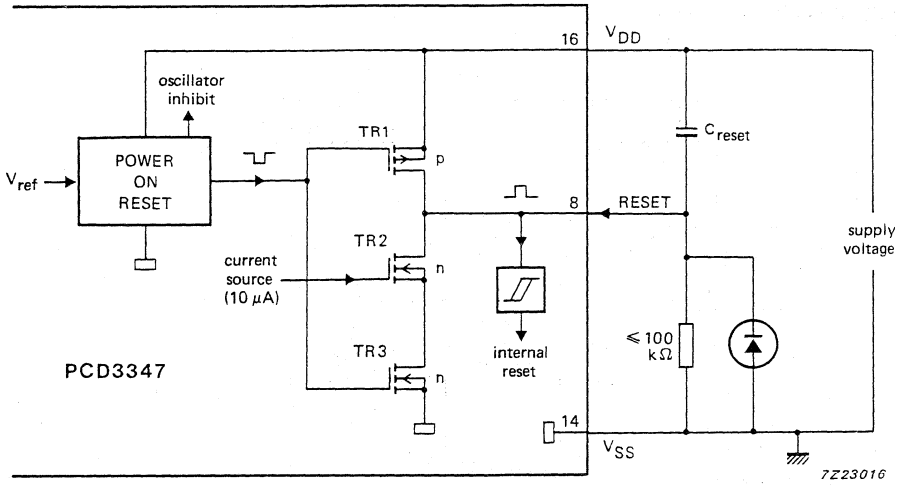


Fig. 20 Stretched power-on reset with external CR circuit.

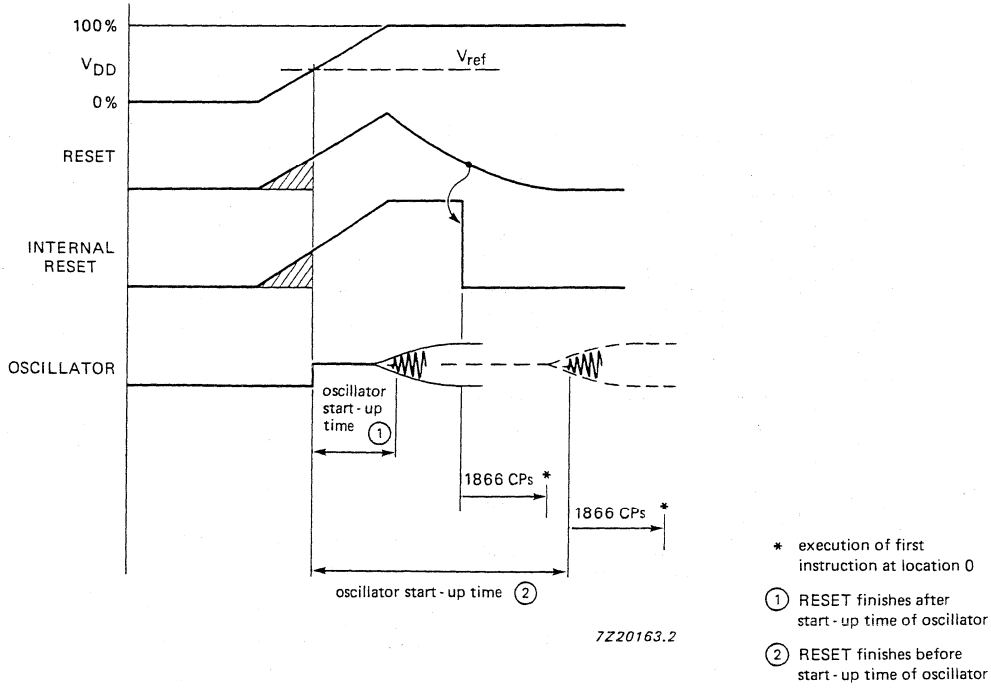


Fig. 21 Timing of power-on reset with a slowly rising V_{DD} and a stretched RESET pulse.

FUNCTIONAL DESCRIPTION (continued)

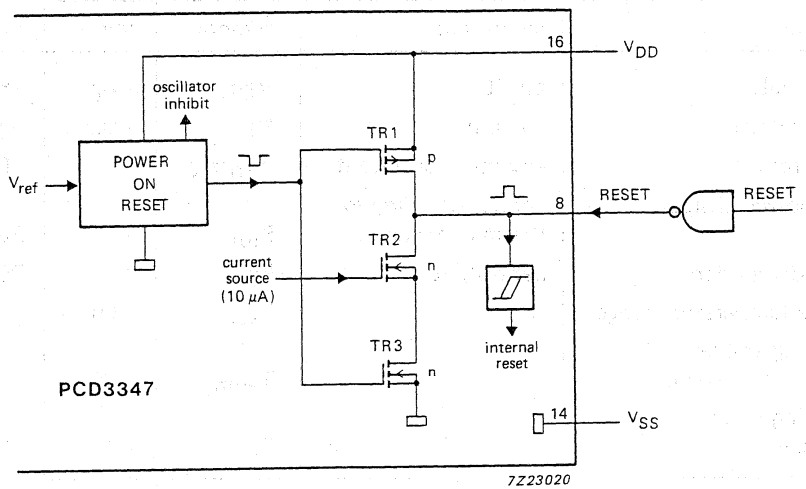


Fig. 22 External power-on reset configuration.

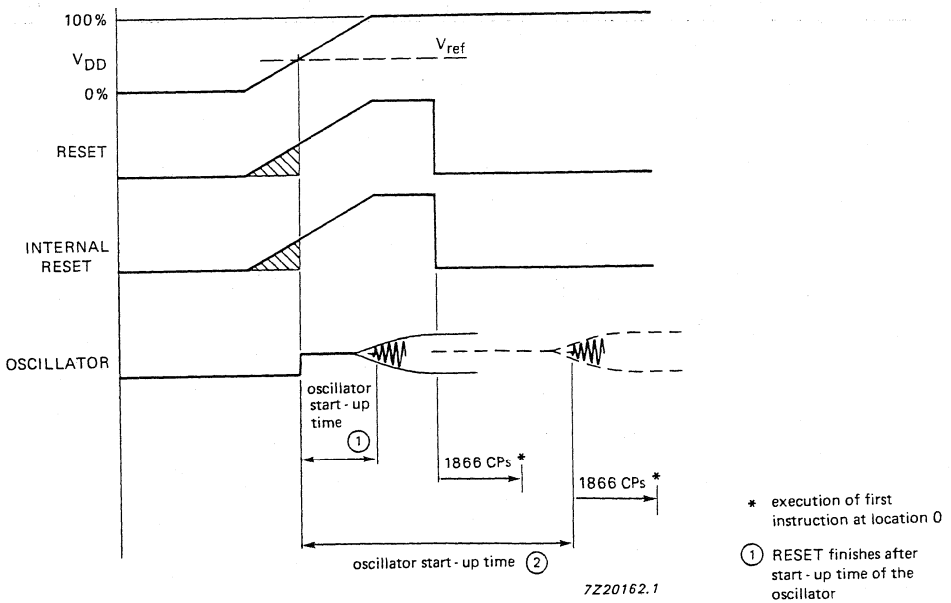


Fig. 23 Timing of external power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 16	V_{DD}	−0,8	+8	V
Input voltage	any pin	V_I	−0,8	V_{DD} + 0,8	V
DC current	any input or output	$\pm I_I, \pm I_O$	–	10	mA
Total power dissipation	derate according to thermal resistance	P_{tot}	–	500	mW
Power dissipation	per output	P_O	–	50	mW
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−25	+70	°C
Operating junction temperature		T_j	–	+125	°C
Thermal resistance junction to ambient	SOT146 SOT163A	$R_{th\ j\text{-}a}$ $R_{th\ j\text{-}a}$	– –	120 150	K/W K/W

DC CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 100 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage operating		V_{DD}	2,5	–	6	V
STOP mode for RAM data retention		V_{DD}	1,0	–	6	V
Supply current (Fig. 25) operating with tone generator on	V_{DD} = 3 V	I_{DD}	–	800	–	μA
operating without tone generator	V_{DD} = 3 V	I_{DD}	–	400	–	μA
IDLE mode (Fig. 26) with tone generator on	V_{DD} = 3 V	I_{DD}	–	600	–	μA
without tone generator	V_{DD} = 3 V	I_{DD}	–	200	–	μA
STOP mode (Fig. 27)	note 1; V_{DD} = 1,8 V					
	T_{amb} = 25 °C	I_{DD}	–	1,5	2,0	μA
	T_{amb} = 55 °C	I_{DD}	–	–	5	μA
	T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O						
Switching level		V_{RESET}	–	1,3	–	V
Sink current	$V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs						
Input voltage LOW		V_{IL}	0	–	0,3 V_{DD}	V
Input voltage HIGH		V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Input leakage current	$V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs						
Output voltage LOW	V_I = V_{SS} or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW for all remaining ports	V_{DD} = 3 V; V_O = 0,4 V	I_{OL}	1,5	2,5	–	mA
Pull-up output source current HIGH (Fig. 29)	V_{DD} = 3 V; V_O = 0,7 V_{DD}	$-I_{OH}$	10	–	–	μA
	V_O = V_{SS}	$-I_{OH}$	–	–	300	μA
Push-pull output source current HIGH	V_{DD} = 3 V; V_O = V_{DD} −0,4 V	$-I_{OH}$	0,6	1,5	–	mA

Note 1

Crystal connected between XTAL1 and XTAL2; CE and T1 at V_{SS}.

TONE GENERATOR CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 100 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Tone output (Fig. 24)						
DTMF output voltage levels (r.m.s. values)						
HIGH group		$V_{HG(rms)}$	158	192	205	mV
LOW group		$V_{LG(rms)}$	125	150	160	mV
Frequency deviation		$\Delta f/f$	−0,6	–	+ 0,6	%
DC voltage level		V_{dc}	–	½ V_{DD}	–	V
Output impedance		$\lvert Z_O \rvert$	–	0,1	0,5	kΩ
Load resistance		R_L	10	–	–	kΩ
Pre-emphasis of group		ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion	note 2; T_{amb} = 25 °C	THD	–	−25	–	dB

Note 2

Related to the level of the LOW group frequency component (CEPT CS 203)

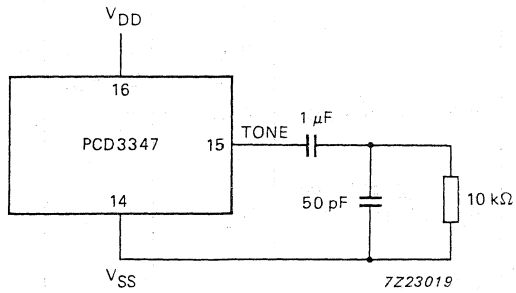


Fig. 24 Tone output test circuit.

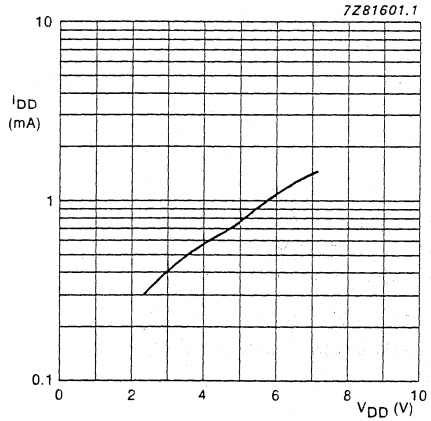


Fig. 25 Typical supply current (I_{DD}) in operating mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C; clock frequency = 3,58 MHz; I_{DD} is increased by approximately 0,6 mA when the DTMF function is operating.

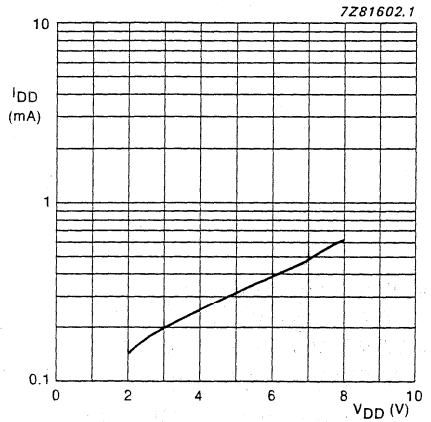
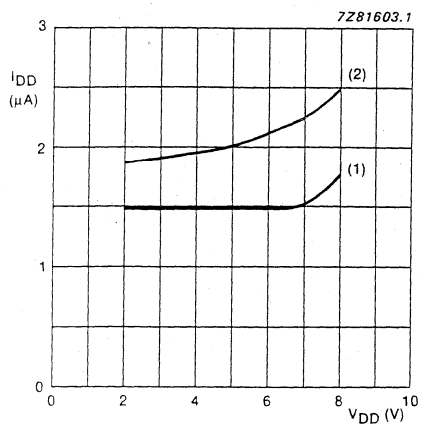
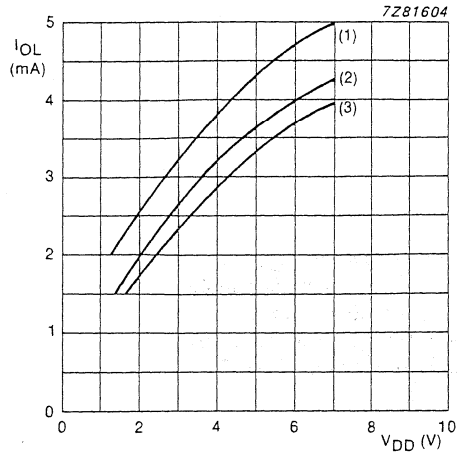


Fig. 26 Typical supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C; clock frequency = 3,58 MHz.



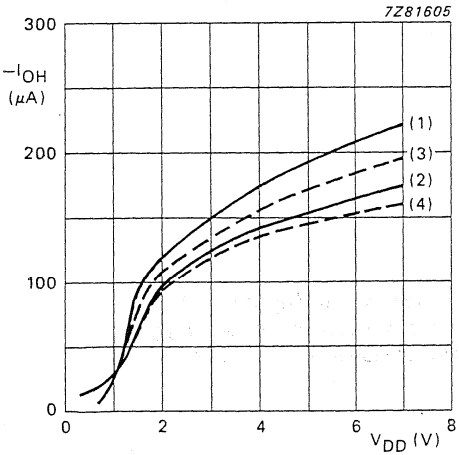
(1) T_{amb} = 25 °C
(2) T_{amb} = 70 °C

Fig. 27 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).



(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$
(3) $T_{amb} = 70\ ^{o}C$

Fig. 28 Output sink current LOW (I_{OL}), as a function of supply voltage (V_{DD}); $V_O = 0{,}4$ V.



(1) $T_{amb} = 25\ ^{o}C$; $V_O = V_{SS}$
(2) $T_{amb} = 25\ ^{o}C$; $V_O = 0{,}7\ V_{DD}$
(3) $T_{amb} = 70\ ^{o}C$; $V_O = V_{SS}$
(4) $T_{amb} = 70\ ^{o}C$; $V_O = 0{,}7\ V_{DD}$

Fig. 29 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).

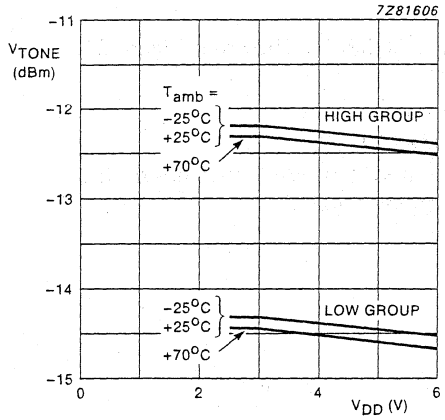


Fig. 30 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

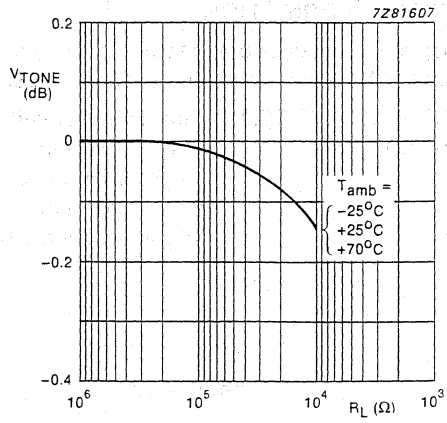


Fig. 31 Dual tone output voltage level as a function of output load resistance.

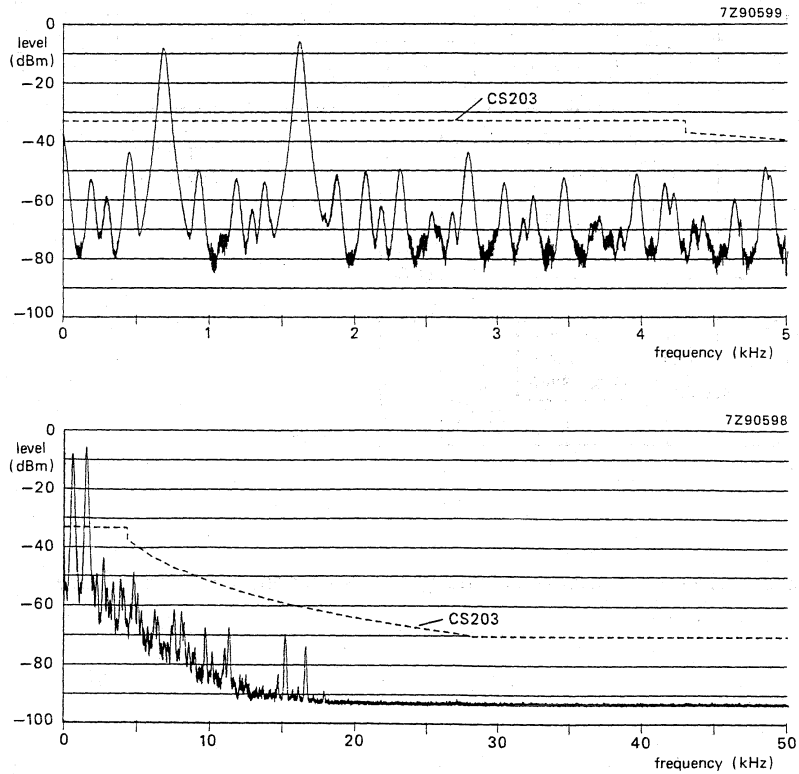


Fig. 32 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

A block diagram of an electronic featurephone built around the PCD3347 is shown in Figure 31. It comprises the following dedicated telephony ICs:

- TEA1060/1061/1067/1068 transmission circuit for telephony
- PCF8576 or PCF8577 2 LCD drivers in LCD module MB7020160
- PCF8571 1 K RAMs with Serial I/O; the number of RAMs depends on the required amount of stored telephone numbers
- PCD3360 programmable multi-tone ringer

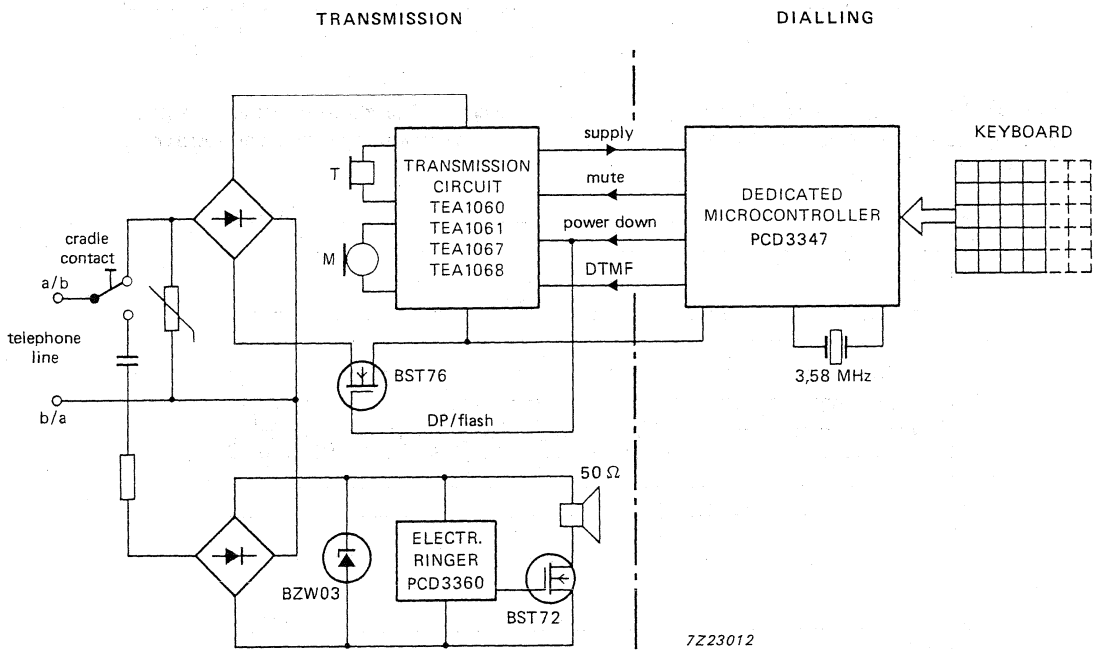


Fig. 33 Block diagram of electronic featurephone with common line interface.

Single-chip 8-bit Telecom Microcontroller

PCD3350A

FEATURES

- 8-bit CPU, ROM, EEPROM, RAM, I/O in a 44-lead quad flat pack
- 8k ROM bytes; 256 RAM bytes
- 256 EEPROM bytes
- 32 kHz crystal oscillator for real-time clock
- EEPROM programmable real-time clock
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 34 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 8-bit reloadable timer 2
- 3 single-level vectored interrupts: external, 8-bit programmable timer/event counter 1, derivative (triggered by reloadable timer 2)
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT CS203 compatible)
- Melody output for ringer application
- Programmable DTMF clock divider
- Power-on reset
- Stop and idle modes
- Logic supply V_{DD}: 1.8 V to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- CPU Clock frequency: 1 MHz to 16 MHz (3.58 MHz or 10.74 MHz for DTMF)
- Operating temperature range: –25 °C to 70 °C
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3350A. The shared characteristics of the PCD33xxA family of microcontrollers are described in the PCD33xxA family data sheet, which should be read in conjunction with this publication.

The PCD3350A is a microcontroller oriented towards telephony applications. It includes 8k ROM bytes, 256 RAM bytes, 34 I/O lines, and an on-chip dual tone multi-frequency (DTMF) generator. In addition to dialling, the generated frequencies can be made available as square waves on port line P1.7/MDY for melody generation, providing ringer operation. The PCD3350A also incorporates 256 bytes of electrically erasable programmable read-only memory (EEPROM), permitting data storage without battery back-up. The EEPROM can be used for storing telephone numbers. Finally, the PCD3350A includes a low power 32 kHz crystal oscillator with an EEPROM programable real time clock (RTC) working in standby mode. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3350AH	44	QFP	plastic	SOT205AG

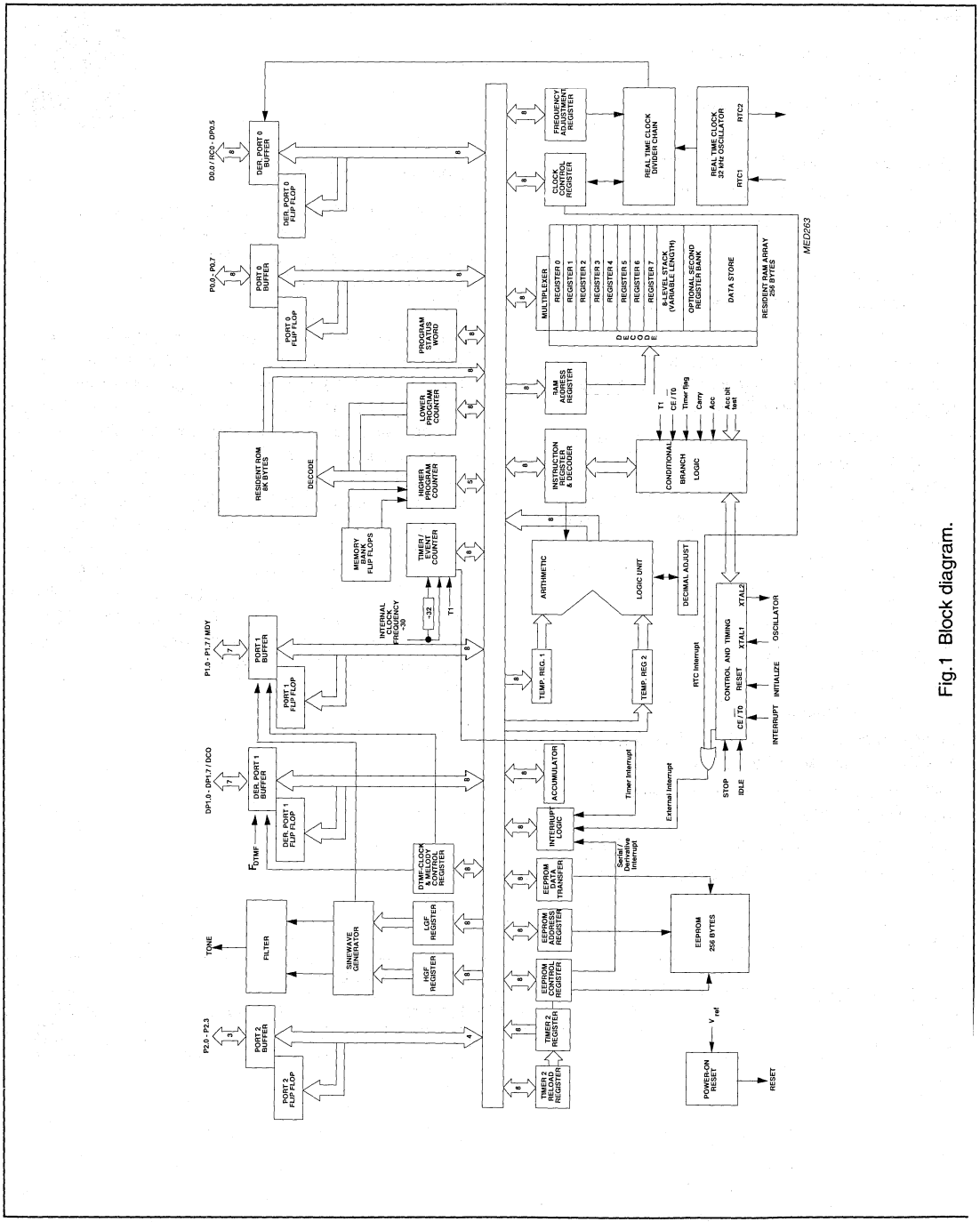


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
P2.1-P2.3	1-3	**Port 2:** quasi-bidirectional I/O lines
DP0.0 / RCO	4	**Derivative port 0:** quasi bidirectional I/O line / Real Time Clock (RTC)
DP0.1 - DP0.5	5-9	**Derivative port 0:** quasi bidirectional I/O lines
RTC1	10	**RTC:** 32 kHz oscillator input
RTC2	11	**RTC:** 32 kHz oscillator output
CE / T0N	12	**Enable:** Chip Enable / Test 0
T1	13	**Test 1**: count input of 8-bit timer / event counter 1
RESET	14	**Reset:** reset input
DP1.0 - DP1.6	15-21	**Derivative port 1:** quasi bidirectional I/O lines
DP1.7 / DCO	22	**Derivative port 1:** quasi bidirectional I/O lines / DTMF clock output
P0.0 - P0.3	23-26	**Port 0:** quasi bidirectional I/O lines
XTAL1	27	**Crystal oscillator:** external clock input
XTAL2	28	**Crystal oscillator:** output
P0.4 - P0.7	29-32	**Port 0:** quasi bidirectional I/O lines
P1.0 - P1.2	33-35	**Port 1:** quasi bidirectional I/O lines
V_{SS}	36	**Ground**
TONE	37	**DTMF:** output
V_{DD}	38	**Supply voltage**
P1.3 - P1.6	39-42	**Port 1:** quasi bidirectional I/O lines
P1.7 / MDY	43	**Port 1:** quasi bidirectional I/O lines / melody output
P2.0	44	**Port 2:** quasi bidirectional I/O line

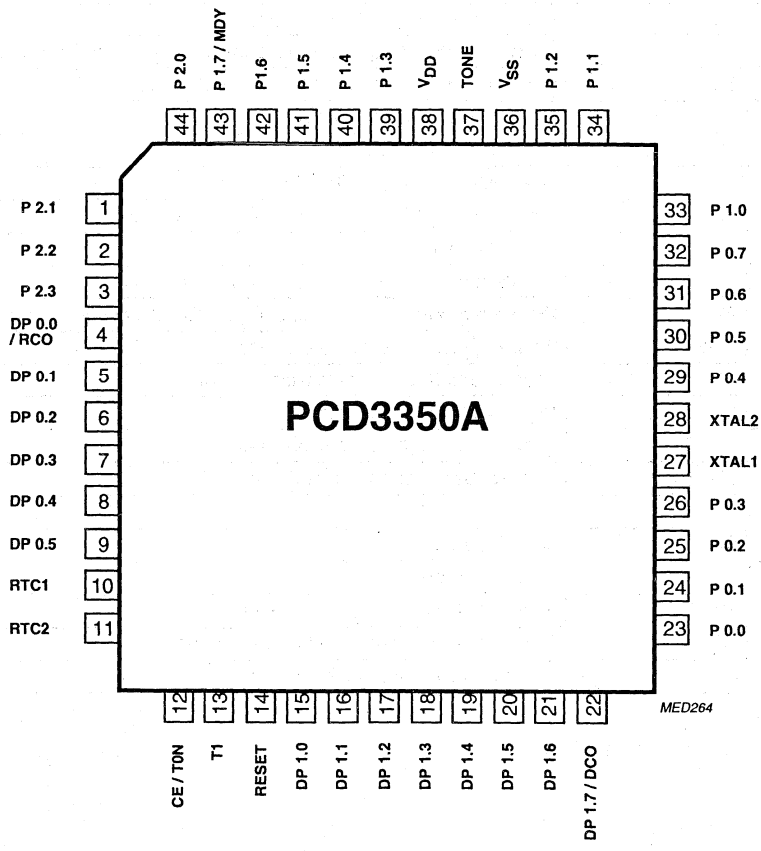


Fig.2 Pin configuration.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Single-chip 8-bit Telecom Microcontroller

PCD3351A/52A/53A

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 2 k ROM bytes; 64 RAM bytes (PCD3351A)
- 4 k ROM bytes; 128 RAM bytes (PCD3352A)
- 6 k ROM bytes; 128 RAM bytes (PCD3353A)
- 128 EEPROM bytes
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- One 8-bit programmable timer/event counter
- Two 8-bit reloadable timers
- 3 single-level vectored interrupts: external, 8-bit programmable timer/event counter 1, derivative (triggered by reloadable timer 2)
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT CS203 compatible)
- Melody output for ringer application
- Power-on reset
- Stop and idle modes
- Logic supply from 1.8 V to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency from 1 MHz to 16 MHz (3.58 MHz for DTMF suggested)
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3351A , PCD3352A and PCD3353A. The shared characteristics of the PCD33XXA family of microcontrollers are described in the PCD33XXA family data sheet, which should be read in conjunction with this publication.

The PCD3351A, PCD3352A and PCD3353A are microcontrollers orientated towards telephony applications which contain an on-chip dual tone multi-frequency (DTMF) generator. In addition to dialling, the generated frequencies can be made available as square waves on port line P1.7/MDY for melody generation thus providing ringer operation. The PCD3351A/52A/53A also incorporate 128 bytes of electrically erasable programmable read-only memory (EEPROM), permitting data storage without battery back-up. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD}+0.5	V
I_I,I_O	DC input or output current	−10	+10	mA
I_{SS}	ground supply current	−50	+50	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
T_{stg}	storage temperature range	−55	+150	°C
T_j	operating junction temperature	−	90	°C

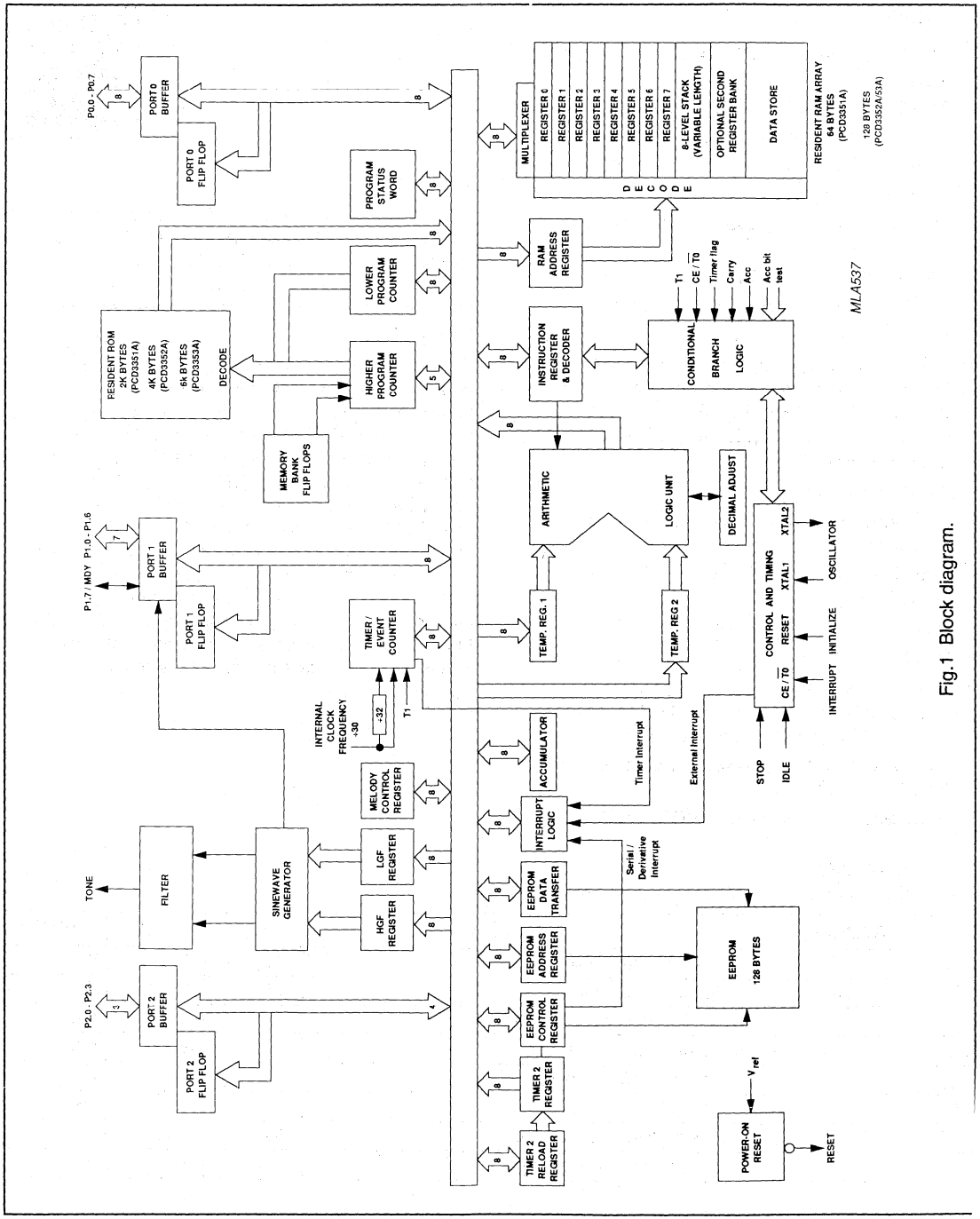


Fig.1 Block diagram.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3351AP/52AP/53AP	28	DIL	plastic	SOT117
PCD3351AT/52AT/53AT	28	mini-pack	plastic	SOT136A

Note to the Ordering Information

Full and up-to-date data for this device is available upon request via your Philips local sales office.

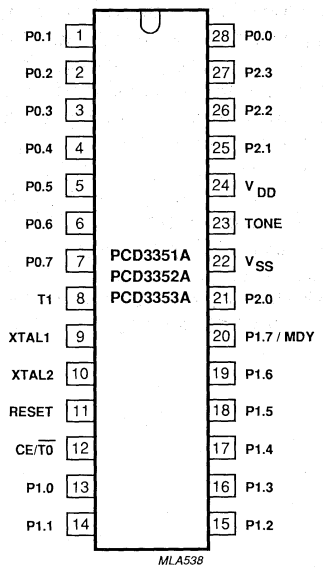


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
P0.1-P0.7	1-7	I/O	Port 0: quasi-bidirectional I/O lines
T1	8	I	Test 1/count input of 8-bit timer/event counter 1
XTAL1	9	I	crystal oscillator/ external clock input
XTAL2	10	O	crystal oscillator output
RESET	11	I	reset input
CE/$\overline{T0}$	12	I	chip enable/test 0
P1.0-P1.6	13-19	I/O	Port 1: quasi-bidirectional I/O line
P1.7/MDY	20	I/O	Port 1: quasi-bidirectional I/O line/melody output
P2.0	21	I/O	Port 2: quasi-bidirectional I/O line
V_{SS}	22	P	ground
TONE	23	O	DTMF output
V_{DD}	24	P	positive supply voltage
P2.1-P2.3	25-27	I/O	Port 2: quasi-bidirectional I/O lines
P0.0	28	I/O	Port 0: quasi-bidirectional I/O line

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Single-chip 8-bit Telecom Microcontroller with on-chip DTMF

PCD3354A

FEATURES

- 8-bit CPU, ROM, RAM, EEPROM, I/O in a 44-lead quad flat pack
- 8k ROM bytes; 256 RAM bytes
- 256 EEPROM bytes
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 36 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 8-bit reloadable timer 2
- 3 single-level vectored interrupts: external, 8-bit programmable timer/event counter 1, derivative (triggered by reloadable timer 2)
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT CS203 compatible)
- Melody output for ringer application
- Programmable DTMF clock divider
- Power-on reset
- Stop and idle modes
- Logic supply V_{DD}: 1.8 V to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- CPU Clock frequency: 1 MHz to 16 MHz (3.58 MHz, 10.74 MHz for DTMF)
- Operating temperature range: –25 °C to 70 °C
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3354A. The shared characteristics of the PCD33xxA family of microcontrollers are described in the PCD33xxA family data sheet, which should be read in conjunction with this publication.

The PCD3354A is a microcontroller oriented towards telephony applications. It includes 8k ROM bytes, 256 RAM bytes, 36 I/O lines, and an on-chip dual tone multi-frequency (DTMF) generator. In addition to dialling, the generated frequencies can be made available as square waves on port line P1.7/MDY for melody generation, providing ringer operation. The PCD3354A also incorporates 256 bytes of electrically erasable programmable read-only memory (EEPROM), permitting data storage without battery back-up. The EEPROM can be used for storing telephone numbers. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3354AH	44	QFP	plastic	SOT205AG

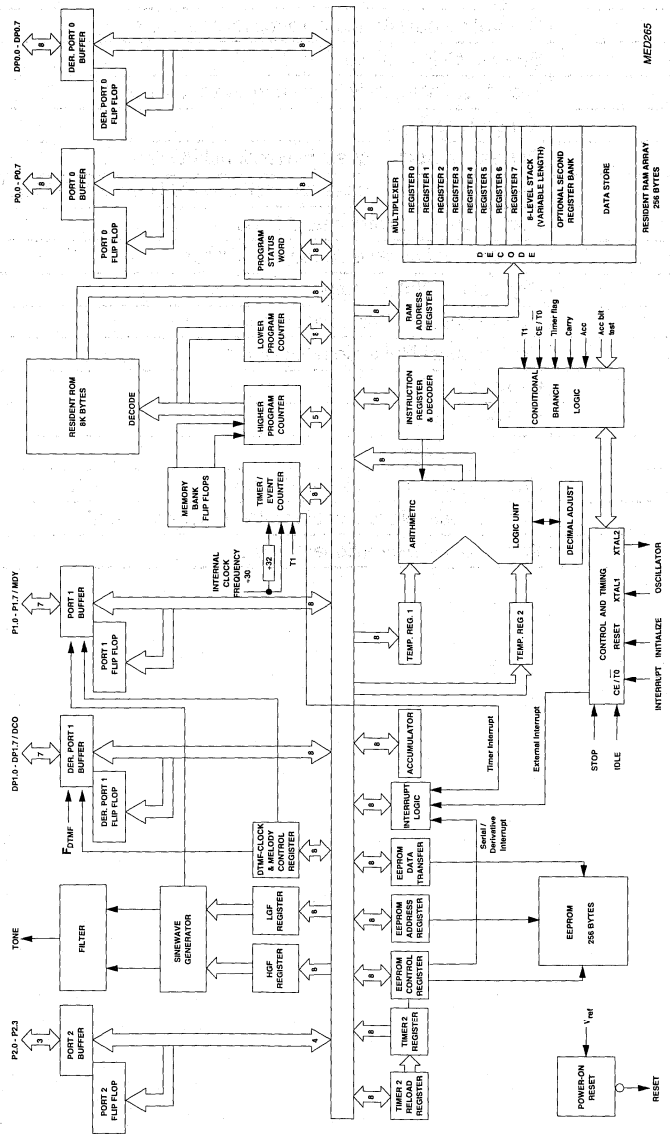


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
P2.1-P2.3	1-3	**Port 2:** quasi-bidirectional I/O lines
DP0.0 - DP0.7	4-11	**Derivative port 0:** quasi bidirectional I/O line
CE/T0N	12	**Enable:** Chip enable / Test 0
T1	13	**Test 1:** count input of 8-bit timer/event counter 1
RESET	14	**Reset:** reset input
DP1.0 - DP1.6	15-21	**Derivative port 1:** quasi bidirectional I/O line
DP1.7 / DCO	22	**Derivative port 1:** quasi bidirectional I/O line / DTMF clock input
P0.0 - P0.3	23-26	**Port 0:** quasi-bidirectional I/O line
XTAL1	27	**Crystal oscillator:** external clock input
XTAL2	28	**Crystal oscillator:** output
P0.4 - P0.7	29-32	**Port 0:** quasi bidirectional I/O lines
P1.0 - 1.2	33-35	**Port 1:** quasi-bidirectional I/O lines
V_{SS}	36	**Ground**
TONE	37	**DTMF:** output
V_{DD}	38	**Supply voltage**
P1.3 - P1.6	39-42	**Port 1:** quasi-bidirectional I/O lines
P1.7 / MDY	43	**Port 1:** quasi-bidirectional I/O line / melody output
P2.0	44	**Port 2:** quasi bidirectional I/O line

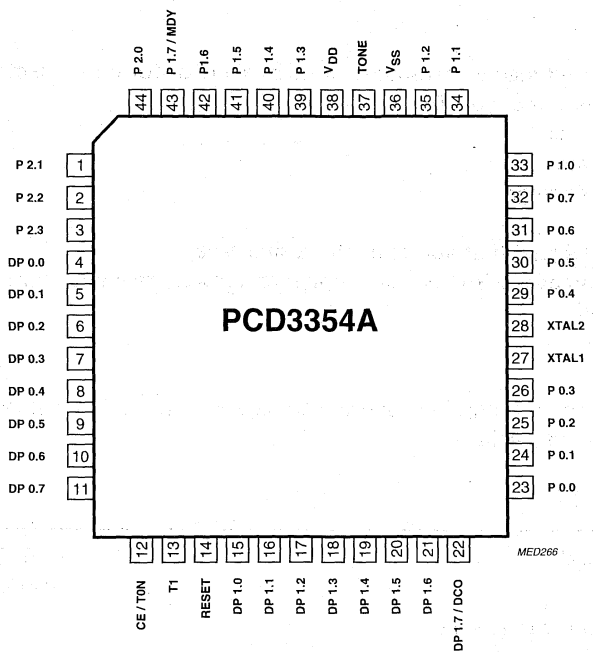


Fig.2 Pin configuration.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Programmable multi-tone telephone ringer

PCD3360

GENERAL DESCRIPTION

The PCD3360 is a CMOS integrated circuit, designed to replace the electro-mechanical bell in telephone sets. It meets most postal requirements, particularly with tone sequence possibilities and input frequency selectivity. Output signals for a loudspeaker or for a piezo-electric (PXE) transducer are provided. No audio transformer is required since the loudspeaker is driven in class D.

Features

- Output signals for electro-dynamic transducer (loudspeaker) or for piezo-electric transducer (PXE)
- 7 basic frequencies (tones) and a pause
- 4 selectable tone sequences
- 4 selectable repetition rates
- 3 selectable impedance settings
- 3-step automatic swell
- Delta-modulated output signal that approximates a sinewave
- Input frequency discriminator with selectable upper and lower frequency limits
- Output for optical signal

Note

Tone sequences (up to 16 tones long), impedance settings and automatic swell levels are mask programmable for customized versions.

QUICK REFERENCE DATA

Available frequencies (tones)		533/600/667/800/ 1000/1067 and 1333	Hz
Number of intervals per tone sequence		15 or 16	
Lower limits of frequency discriminator		13,33 or 20	Hz
Upper limits of frequency discriminator		30 or 60	Hz
Impedance settings (with 50 Ω loudspeaker)	approx.	7 or 10,5 or 17,5	kΩ
Switch-on delay at 25 Hz	max.	60	ms

PACKAGE OUTLINES

PCD3360P: 16-lead DIL; plastic (SOT38).
PCD3360T: 16-lead mini-pack; plastic (SO16L; SOT162A).

Programmable multi-tone telephone ringer

PCD3360

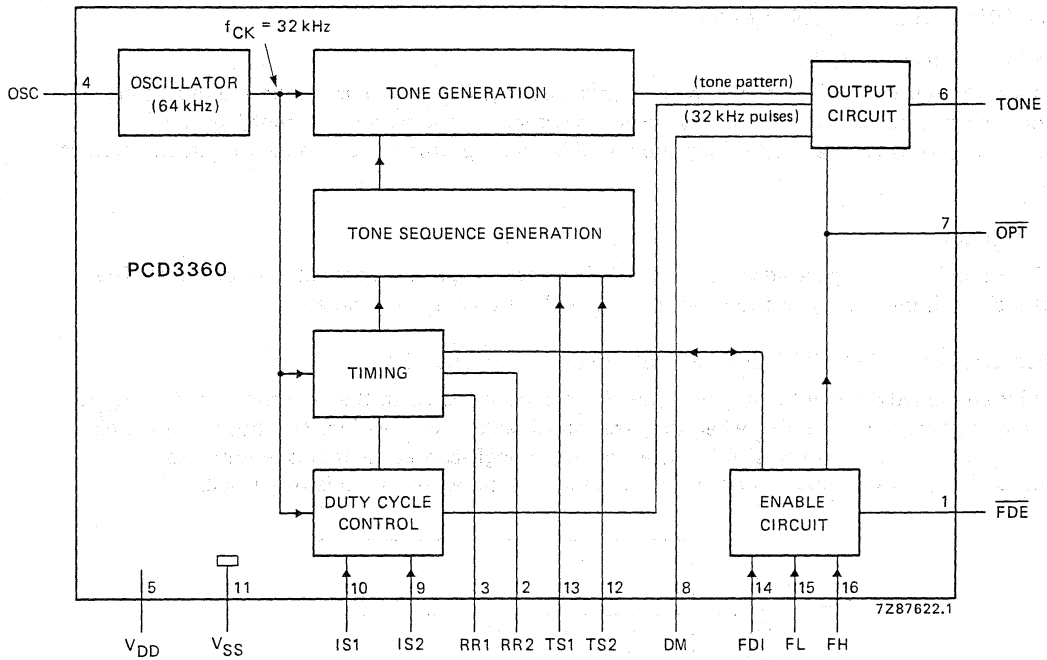


Fig. 1 Block diagram.

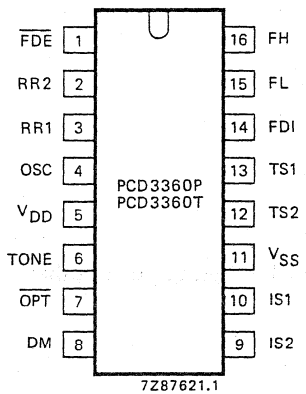


Fig. 2 Pinning diagram for PCD3360P and PCD3360T.

PINNING

1	$\overline{FDE}$	frequency discriminator enable
2	RR2	repetition rate selection
3	RR1	repetition rate selection
4	OSC	oscillator
5	V_{DD}	positive supply
6	TONE	tone output
7	$\overline{OPT}$	optical signal output
8	DM	drive mode selection
9	IS2	impedance setting and automatic swell
10	IS1	impedance setting and automatic swell
11	V_{SS}	negative supply
12	TS2	tone sequence selection
13	TS1	tone sequence selection
14	FDI	frequency discriminator input
15	FL	lower frequency limit selection
16	FH	upper frequency limit selection

FUNCTIONAL DESCRIPTION (see Fig. 1)

Supply pins (V_{DD} and V_{SS})

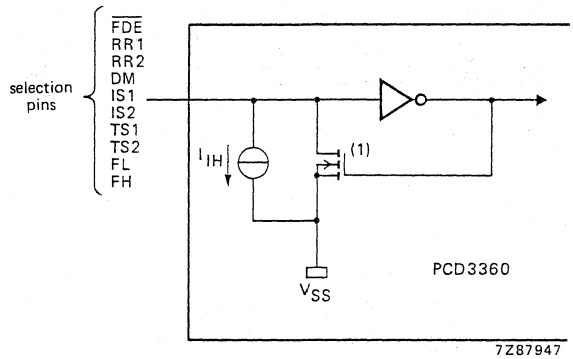
If the supply voltage (V_{DD}) drops below the standby voltage (V_{SB}), the oscillator and most other functions are switched off and the supply current is reduced to the standby current (I_{SB}). The automatic swell register retains its information until V_{DD} drops further to a value V_{AS} at which reset occurs.

Oscillator (OSC)

The 64 kHz oscillator is operated via an external resistor and capacitor connected to pin OSC. The oscillator signal is divided by two to provide the 32 kHz internal system clock.

Selection pins ($\overline{FDE}$, RR2, RR1, DM, IS2, IS1, TS2, TS1, FL and FH)

These pins are pulled down internally by a pull-down current I_{IH} when they are connected to V_{DD}, and by a pull-down resistance R_{IL} when they are connected to V_{SS} (see Fig. 3). Thus when the pins are open-circuit they are defined LOW. Therefore only a single-contact switch is required to connect the pins to V_{DD}; yet the supply current is only marginally increased as I_{IH} is very small.



(1) Transistor resistance = R_{IL} when switched on.

Fig. 3 Input circuit of selection pins.

Frequency discriminator circuit (pins $\overline{FDE}$ and FDI)

The frequency discriminator circuit prevents the ringer being activated by dial pulses, speech or other unqualified signals.

The circuit is enabled or disabled by input $\overline{FDE}$.

When $\overline{FDE}$ is HIGH, FDI acts as a logic enable input.
The circuit will produce tone sequences provided FDI is HIGH and V_{DD} exceeds V_{SB}.
When $\overline{FDE}$ is LOW, FDI acts as the frequency discriminator input.
The circuit will produce tone sequences provided V_{DD} exceeds V_{SB} and the signal at FDI fulfils the conditions set by FL and FH.

When the frequency discriminator is enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the circuit will start to produce tone sequences after two rising or two falling edges have occurred at FDI. The time between these edges must be within the limits set by FL and FH.

FUNCTIONAL DESCRIPTION (continued)

The circuit will continue to produce tone sequences provided the time between subsequent falling edges or between subsequent rising edges remains within the limits set by FL and FH, otherwise it will stop. Because two edges are required for detection, either positive or negative, the switch-on delay will vary between 1 and 1,5 cycles of the incoming ringing frequency.

FDI has a Schmitt-trigger action; the levels are set by an external resistor R2 (see Fig. 8) and an internal sink current that is switched from 20 μA (typ.) for FDI = LOW to $< 0{,}1$ μA for FDI = HIGH. Excess current entering FDI via R2 is absorbed by internal diodes clamped to V_{DD} and V_{SS}.

Selection of frequency discriminator limits (FL and FH)

With the frequency discriminator enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the lower and upper limits of the input frequency are set by inputs FL and FH as shown by Table 1 and Table 2 respectively.

Table 1 Selection of lower frequency discriminator limits (f_{osc} = 64 kHz)

FL input state	lower discriminator limit (Hz)
LOW	20
HIGH	13,33

Table 2 Selection of upper frequency discriminator limits (f_{osc} = 64 kHz)

FH input state	upper discriminator limit (Hz)
LOW	60
HIGH	30

Selection of tone sequences (TS1 and TS2)

A tone sequence is composed of 15 or 16 equal time intervals. Each time interval may be filled with one of seven available tones or with a pause; these are shown together with their corresponding internal ROM tone code in Fig. 4.

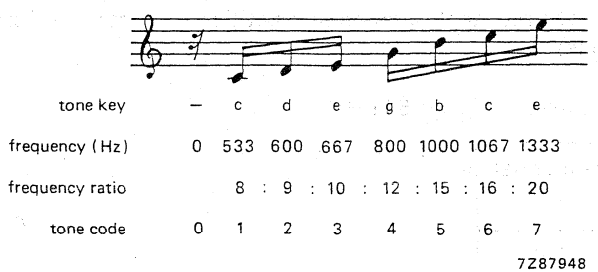


Fig. 4 Available tones and their corresponding internal ROM tone code.

Four tone sequences are programmed in the internal ROM (see Fig. 5). Inputs TS1 and TS2 determine which tone sequence is selected and output at pin TONE. The sequences are mask programmable with any length up to 16 time intervals.

The tone sequences are repeated continuously provided the enable conditions at inputs $\overline{FDE}$ and FDI are valid and $V_{DD} > V_{SB}$; the first sequence always starts with the first tone shown in Fig. 5.

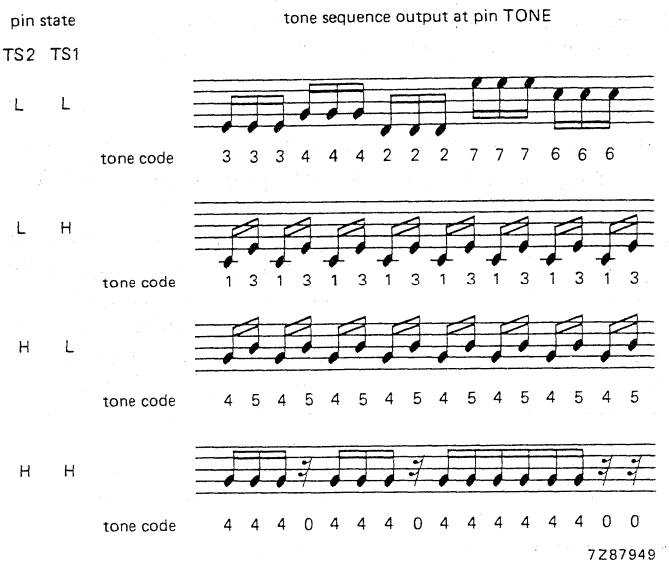


Fig. 5 Tone sequences mask-programmed in the PCD3360.

Selection of repetition rates (RR1 and RR2)

The duration of a time interval within a tone sequence is determined by the state of inputs RR1 and RR2 as shown in Table 3. The resultant variation of repetition rate acts as a distinguishing feature between adjacent telephones.

Table 3 Duration of time intervals (f_{osc} = 64 kHz)

input state		time interval ms
RR1	RR2	
L	L	15
L	H	30
H	L	45
H	H	60

The repetition rate variation can be extended by mask programming (for customer defined versions) the same tone combination for all 4 tone sequences, but with a different number of time intervals per tone. Thus the repetition rate can be selected from 16 values by inputs RR1, RR2, TS1 and TS2.

FUNCTIONAL DESCRIPTION (continued)

Drive mode selection (DM)

The output signal at pin TONE can be selected for application with electro-dynamic or piezo-electric transducers. An example of both signals, for a tone frequency of 667 Hz, is shown in Fig. 6.

Loudspeaker mode

In the loudspeaker mode (DM = LOW), pin TONE outputs a delta-modulated signal that approximates a sinewave sampled at a rate of 32 kHz. The output pulse duration is determined by pins IS1 and IS2. The resultant acoustic spectrum is aurally more acceptable and has greater penetration than a square wave spectrum because more power is concentrated at the fundamental frequency.

PXE mode

In the PXE mode (DM = HIGH), pin TONE outputs a square wave. In this mode the ringer impedance and sound pressure level are determined by the characteristics (e.g. the size) of the PXE transducer; inputs IS1 and IS2 are inactive.

Setting of impedance, sound pressure level and automatic swell (IS1 and IS2)

With DM = LOW (loudspeaker mode), inputs IS1 and IS2 determine the pulse duration of the output signal and thereby the d.c. resistance R_{xy} (seen at points x and y in Fig. 8), the input impedance Z_I and and also the Sound Pressure Level (SPL). The selection of 3 impedance settings and automatic swell is shown in Table 4.

Table 4 Setting of pulse duration and automatic swell (DM = LOW)

input state		function	ringing burst number (N)	pulse duration (μs)		R_{xy} (kΩ)	Z_I (kΩ)	SPL (dBr)
IS1	IS2			fund.	harm.			
L	L	automatic swell	1	1,9	–	40	tbf	tbf
			2	2,9	–	20	17,5	−4
			> 2	4,1	1,8	5	7	0
L	H	constant level	–	2,9	–	20	17,5	−4
H	L		–	3,8	–	10	10,5	tbf
H	H		–	5,4	–	5	7	0

Where:

1. Typical pulse duration values of the fundamental and harmonic frequencies are for f_{osc} = 64 kHz and f_{CK} = 32 kHz.
2. SPL is the relative Sound Pressure Level, and 0 dBr is defined as the SPL for IS1 = IS2 = HIGH.
3. Values of the d.c. resistance R_{xy}, bell impedance (Z_I) and SPL are valid for a value of input voltage V_I = 40 V_{rms} at 25 Hz in Fig. 8.

Setting of impedance, sound pressure level and automatic swell

When pins IS1 and IS2 are both LOW, the circuit operates in the automatic swell mode. The SPL then increases in three steps so that the maximum level is reached for the third ringing burst.
Each time V_{DD} drops below V_{AS} the automatic swell register is reset and the next ringing burst is considered as N = 1 (see Table 4).
A buffer capacitor C3 (see Fig. 8) must hold $V_{DD} > V_{AS}$ during the time between two consecutive ringing bursts of a series.

For each of the other three combinations of pins IS1 and IS2 the pulse duration has a constant value. Thus the ringer can be designed so that the impedance represented at the telephone line will comply with postal requirements that vary in relation to parallel or series connections of more than one ringer.

To satisfy some applications, a harmonic signal is added to the fundamental frequency in the last step of the automatic swell mode. The pulses representing this harmonic signal are interleaved with the pulses of the fundamental signal (see Fig. 7). The difference in pulse duration shown in Table 4, is chosen so that the harmonic level is 10 dB below the fundamental level.
The harmonic frequency range is from 2 kHz to 3,2 kHz. The individual harmonic frequencies for the seven tone codes and the relative fundamental frequencies are shown in Table 5.

Table 5 Harmonic frequency in relation to tone code and fundamental frequency

tone code	frequency (Hz)	
	fundamental	harmonic
1	533	3200
2	600	2400
3	667	2667
4	800	3200
5	1000	2000
6	1067	2133
7	1333	2667

Using a single mask it is possible to program the following:

- Addition of harmonics in all the other input states of IS1 and IS2
- All pulse duration values
- Other even harmonic frequencies.

Optical output ($\overline{OPT}$)

The $\overline{OPT}$ output is designed to drive an optical signal transducer or lamp. It is LOW when the ringer circuit is enabled and HIGH when the ringer circuit is disabled. This output can also be used to switch the transmitter ON and OFF in the base of a cordless telephone set.

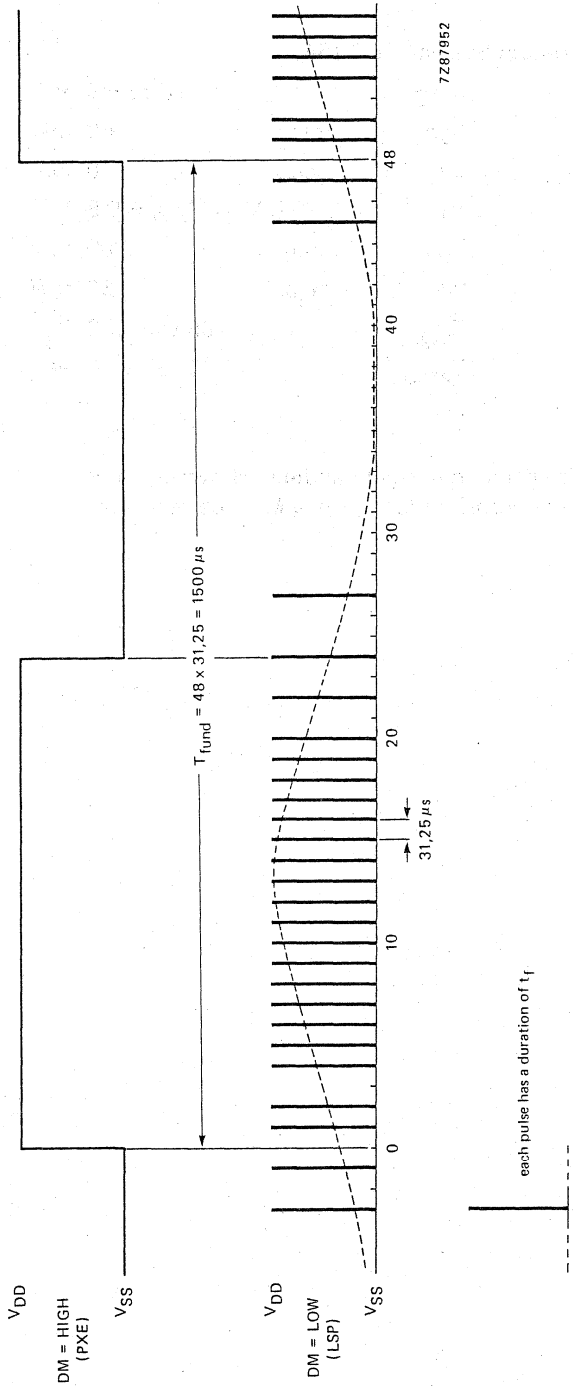


Fig. 6 Fundamental signal (667 Hz) at pin TONE (for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

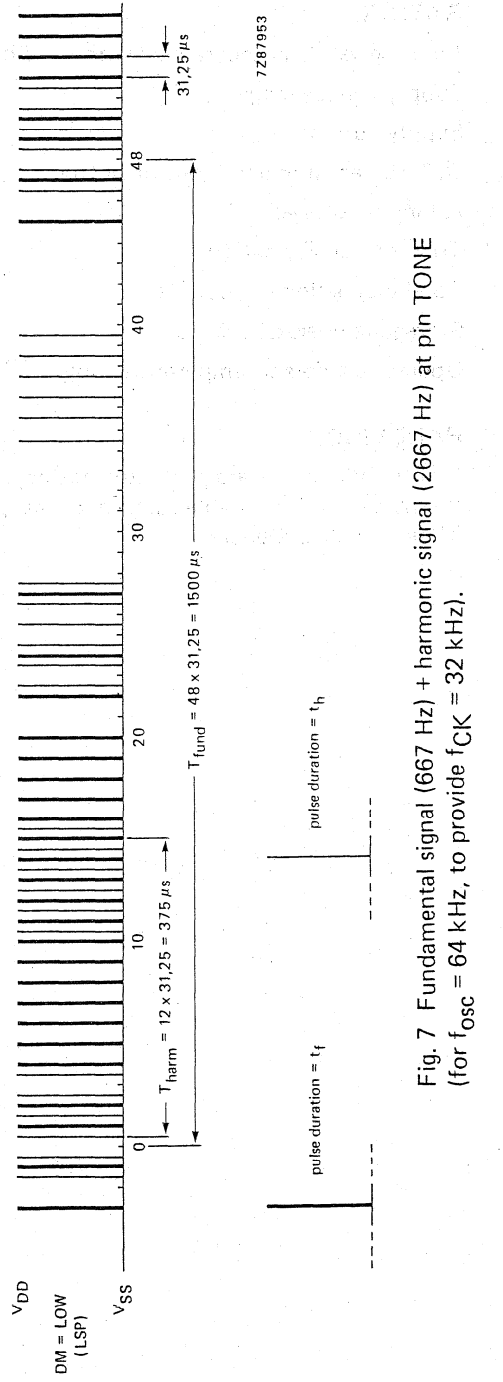


Fig. 7 Fundamental signal (667 Hz) + harmonic signal (2667 Hz) at pin TONE (for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to + 9	V
Supply current	I_{DD}	max.	50	mA
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Total dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	V_{SB}+0,1	–	8,0	V
Standby supply voltage (note 1)	V_{SB}	3,9	4,8	5,7	V
Supply voltage for automatic swell reset (note 2)	V_{AS}	–	0,5V_{SB}	–	V
Operating supply current (note 3)	I_{DD}	–	110	140	μA
Standby supply current at $V_{DD} < V_{SB}$ (note 4)	I_{SB}	–	3	8	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	0,3V_{DD}	V
Input voltage HIGH (any pin)	V_{IH}	0,7V_{DD}	–	V_{DD}	V
Pull-down circuits of inputs					
FDE, RR1, RR2, DM, IS1, IS2, TS1, TS2, FL, FH					
pull-down resistance with input at V_{SS}	R_{IL}	–	20	–	kΩ
pull-down current with input at V_{DD}	I_{IH}	–	0,1	–	μA
Pull-down circuit of FDI					
pull-down current with V_{FDI} = 0,3V_{DD}; T_{amb} = 25 °C	I_{SL}	14	23	32	μA
temperature coefficient of I_{SL}	$-\Delta I_{SL}$	–	0,5	–	%/°C
pull-down current with V_{FDI} = 0,8V_{DD}	I_{SH}	–	0,1	–	μA
pull-down current with $V_{DD} < V_{SB}$	I_{SX}	–	0,1	–	μA
Current into input FDI (note 5)	$\pm I_{IS}$	–	–	0,2	mA
Outputs					
TONE, $\overline{OPT}$					
Output sink current at V_{OL} = 0,5 V	I_{OL}	1	2	–	mA
Output source current at V_{OH} = V_{DD}−0,5 V	$-I_{OH}$	1	2	–	mA

A.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Switch-on delay (with $\overline{FDE}$ = LOW and ringing frequency within limits set by FL and FH)	$t_{d(on)}$	1	–	1,5	note 6
Switch-off delay (with $\overline{FDE}$ = LOW)					
at FL = LOW	$t_{d(off)}$	–	–	50	ms
at FL = HIGH	$t_{d(off)}$	–	–	75	ms
Oscillator frequency at R_{osc} = 365 kΩ; C_{osc} = 56 pF; T_{amb} = 25 °C (note 7)	f_{osc}	60	64	68	kHz
Frequency variation					
as a function of V_{DD}	$-\Delta f_{osc}$	–	1	–	%/V
as a function of T_{amb}	$-\Delta f_{osc}$	–	0,05	–	%/K

Notes to the characteristics

1. For $V_{DD} < V_{SB}$ the circuit is in standby.
2. At $V_{DD} = V_{AS}$ the automatic swell register is reset.
3. R_{osc} = 365 kΩ; C_{osc} = 56 pF; FDI = $\overline{FDE}$ = V_{DD}; all other inputs and outputs open circuit.
4. The standby supply current is measured with all inputs and outputs open-circuit with the exception of OSC.
5. The current I_{IS} is clamped to V_{DD} and to V_{SS} by two internal diodes. Correct operation is ensured with $V_{FDI} > V_{DD}$ or $V_{FDI} < V_{SS}$, provided the maximum value of I_{IS} is not exceeded. (The input FDI has an extended HIGH and LOW input voltage range.)
6. The switch-on delay is measured in cycles of incoming ringing frequency.
7. Lead lengths of R_{osc} and C_{osc} to be kept to a minimum.

APPLICATION INFORMATION

Application of the PCD3360 in a telephone ringer circuit together with a loudspeaker is shown in Fig. 8.

The threshold levels V_H and V_L of the frequency discriminator circuit are determined by:

- The logic threshold of input FDI ($0{,}5V_{DD}$ typ. 3,4 V for V_{DD} = 6,8 V)
- The pull-down current of input FDI (20 μA typ. for FDI $<$ 3,4 V)
- The value of R2 (680 kΩ in Fig. 8)

For a positive slope, the voltage at R2 must exceed the value V_H before FDI will become HIGH; V_H is the sum of the input threshold and the voltage drop across R2 thus:

$V_H = 3{,}4 + (680 \times 10^3) \times (20 \times 10^{-6}) = 17$ V.

For a negative slope, the voltage at R2 must decrease below the value V_L before FDI will become LOW. Because the current into FDI is negligible with FDI = HIGH the voltage drop across R2 can be discounted, thus $V_L = 3{,}4$ V.

The minimum operating voltage across C3 is 17,8 V which is determined by:

- The minimum operating voltage of the PCD3360 (5,8 V)
- The supply current of the PCD3360 (120 μA max.)
- The value of R3 (100 kΩ in Fig. 8)

The total switch-on delay equals approximately the time required to charge the supply capacitor C3 to the minimum operating value, plus the specified switch-on delay of the PCD3360.

The high operating voltage combined with the class D output stage ensures optimal energy conversion and thereby a high sound level. The design can easily be optimized for parallel or series connection of more than one ringer. The diode bridge, zener diode (D1) and resistor R1 protect the ringer against transients up to 5 kV. During these surges the voltage on the 68 V zener diode (BZW03) can rise to 100 V; the DMOS transistor BST72A (TR1) has a maximum drain-source voltage of 100 V. Up to 220 V, 50 Hz can be applied to the a/b terminals without damaging the ringer.
The choke (L1) in series with the 50 Ω loudspeaker increases the sound pressure level by approximately 3 dB by suppression of the 32 kHz carrier frequency and its sidebands.
The flyback diode BAX18A (D2) is a fast type with low forward voltage to obtain high efficiency.

Application of the PCD3360 together with a PXE transducer is shown in Fig. 9. The only significant difference between Fig. 8 and Fig. 9 is the output stage. Two BST72A transistors provide an output voltage swing almost equal to the voltage at C3. Pins IS1 and IS2 are inoperative because DM = HIGH. Volume control is possible using resistor R_V.

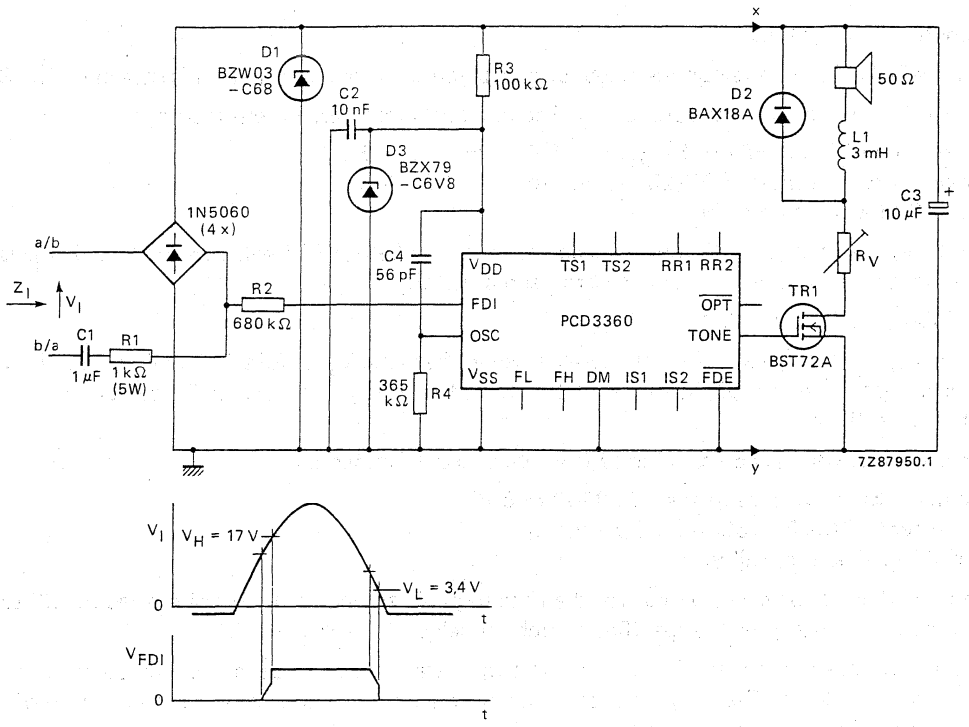


Fig. 8 Transformerless electronic ringer with PCD3360 and a loudspeaker.

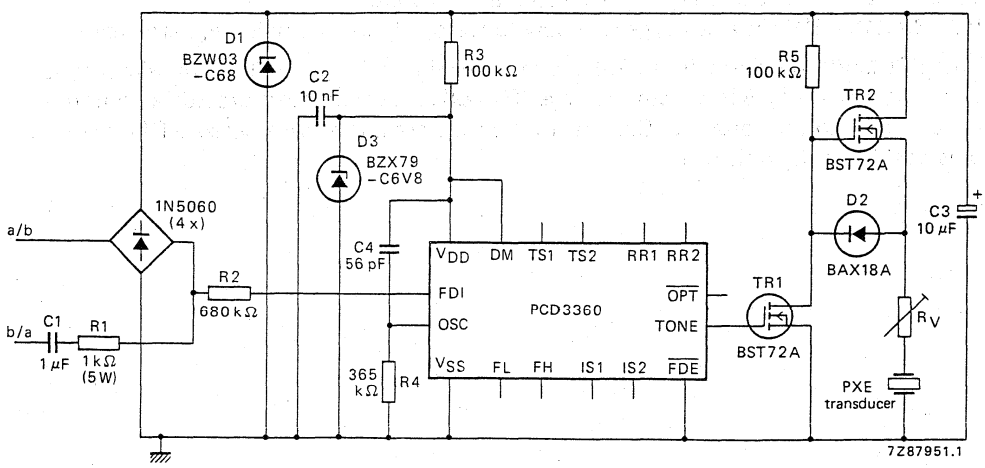


Fig. 9 PCD3360 ringer with PXE transducer.

CONTENTS

1 INTRODUCTION

This data sheet describes the shared properties of the PCD33XXA family of microcontrollers and its quickly growing number of derivative microcontrollers. For a particular microcontroller, this data sheet should be read in conjunction with the individual data sheet of the specific device.

2 FEATURES

- 8-bit CPU, ROM, RAM, I/O all in one package
- Up to 8 kbytes ROM
- Up to 256 bytes RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 8 or more quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts: external, timer/event counter, SIO/derivative
- Two test inputs, one of which also serves as the external interrupt input
- Serial I/O interface (some devices only)
- Power-on-reset, Stop and Idle modes
- Supply voltage range: 1.8 to 6 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: –25 to +70 °C
- Manufactured in silicon gate CMOS process.

3 GENERAL DESCRIPTION

The PCD33XXA family of microcontrollers provide up to 8 kbytes of program memory and up to 256 bytes of RAM. All devices include flexible I/O ports, an 8-bit programmable timer/event counter and a choice of single-level vectored interrupts. The instruction set is based on that of the well-known MAB8048. Being similar to the MAB8400 family of NMOS controllers, some devices can serve as CMOS replacements, especially where the lower power consumption and higher speed provide advantages.

A range of prototyping devices with external program memory and 'Piggy-backs', as well as emulation probes and prototyping systems are available.

4 BLOCK DIAGRAM

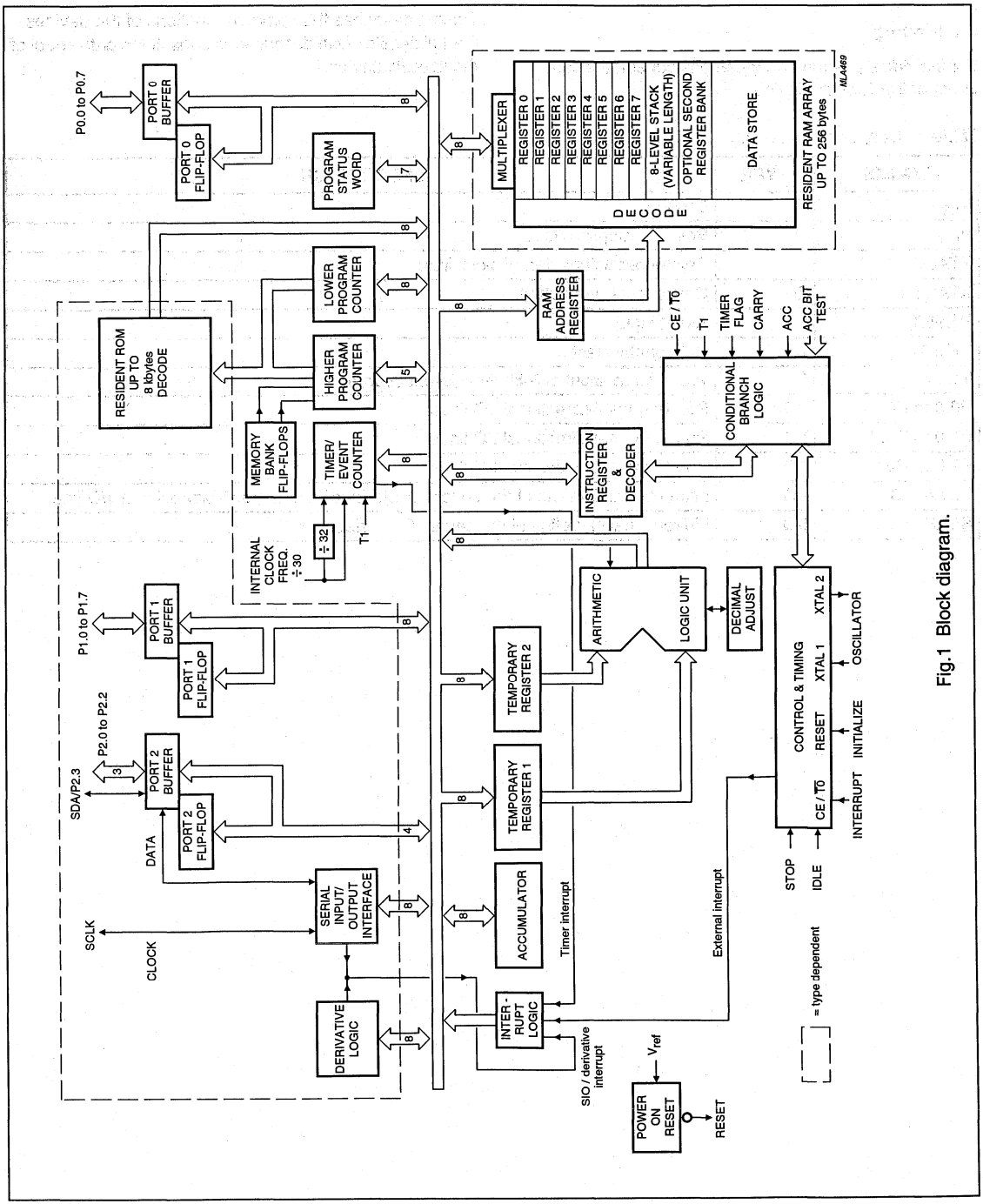


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

For individual pinning configurations consult the data sheet of the specific device.

5.2 Pin description

Table 1 describes the common functions of the devices. For full details of pin descriptions consult the data sheet of the specific device.

Table 1 Common functions.

SYMBOL	TYPE	DESCRIPTION
V_{SS}	P	Ground
V_{DD}	P	Positive supply voltage
XTAL1	I	Crystal oscillator/external clock input
XTAL2	O	Crystal oscillator output
RESET	I	Reset input
CE/$\overline{T0}$	I	Chip enable/Test 0
T1	I	Test 1/count input of 8-bit timer/event counter 1
P0.0 to P0.7	I/O	Port 0: quasi-bidirectional I/O lines
P1.0 to P1.7	I/O	Port 1: quasi-bidirectional I/O lines
P2.0 to P2.2	I/O	Port 2: quasi-bidirectional I/O lines
SDA/P2.3	I/O	bidirectional data line of the serial I/O interface/Port 2: quasi-bidirectional I/O line
SCLK	I/O	bidirectional clock line of the serial I/O interface

6 FUNCTIONAL DESCRIPTION

6.1 Central processing unit

The PCD33XXA family provides an adequate instruction set with arithmetic, logic, branching, input/output and control facilities. Special highlights are the instructions for BCD arithmetic, nibble handling, conditional branches, loop control (DJNZ) and table look-up (MOVP).

Code and execution efficiency is achieved by using a maximum of two bytes and two execution cycles per instruction (see Chapter 7).

6.2 Program memory

The program memory consists of up to 8 kbytes of read-only memory (ROM). Each location is directly addressable by the Program Counter. The program memory is mask-programmed at the factory. Figure 2 illustrates the program memory map.

Four program memory locations are of special importance:

- Location 0: first instruction to be executed after the processor is reset
- Location 3: first instruction of an external interrupt (CE/$\overline{T0}$) routine
- Location 5: first instruction of a SIO/derivative interrupt routine
- Location 7: first instruction of a timer/event counter interrupt routine.

Only 11 bits of the 13-bit Program Counter function as a counter. The two most significant bits can only be preset. The program memory is therefore, structured into banks of 2 kbytes. Transfer of control to other memory banks is performed by unconditional branches (JMP) or subroutine calls (CALL) when another memory bank has been pre-selected (by SEL MB instruction).

Each program memory bank is further divided into 8 pages of 256 bytes. Indirect (JMPP) and conditional branches cannot cross page boundaries.

6.3 Data memory

Data memory consists of up to 256 bytes of random access memory (RAM). All locations are indirectly addressable using RAM pointer registers. Up to 16 register locations are directly addressable. Data memory also includes an 8-level Program Counter stack addressed by a 3-bit Stack Pointer. All RAM locations make efficient program loop counters if used with the decrement register and test instruction (DJNZ). Figure 3 illustrates the data memory map.

6.3.1 Working registers

Locations 0 to 7 are working registers. They are accessible by efficient one byte/one cycle instructions, thus making these locations suitable for frequently accessed intermediate results.

As an alternative to locations 0 to 7, locations 24 to 31 may be used as working registers. Register Bank selection is made by SEL RB0/RB1 instructions. Register Bank 1 may be used as an extension of Register Bank 0, as an alternative register bank for interrupt service or as general purpose data memory.

The first two locations of each bank (R0, R1, R0' and R1') serve as RAM pointers that indirectly address all RAM locations.

6.3.2 Program Counter stack

Locations 8 to 23 may be used as an 8-level Program Counter stack reserving 2 locations per level, or as general purpose RAM. The stack (see Fig.5) saves return addresses and status during interrupt or subroutine servicing. Nesting of subroutines and/or interrupts is permitted up to 8-levels deep.

The 3-bit Stack Pointer always points to the next free stack level. Following device reset, the Stack Pointer points to level 0 (locations 8 and 9). On each subroutine call (CALL) or interrupt, the contents of the Program Counter and bits 4, 6 and 7 of the Program Status Word are transferred to the level indicated by the Stack Pointer. The Stack Pointer increments and points to the next free level. Overflow from level 7 to level 0 occurs after nesting eight levels deep. Further subroutine calls and/or interrupts must not occur at this stage since this would result in loss of program content; overriding level 0 content.

Return from interrupt must be performed by the RETR instruction, which decrements the Stack Pointer and restores the Program Counter and Program Status Word, valid before the interrupt occurred. Return from subroutine should be performed by the RET instruction. In contrast to RETR, RET does not restore the Program Status Word.

As a general rule, the use of RETR in conjunction with a subroutine call is not recommended. The use of RETR must also be avoided with subroutines called from interrupt routines because it prematurely terminates the interrupt state (see Section 6.6).

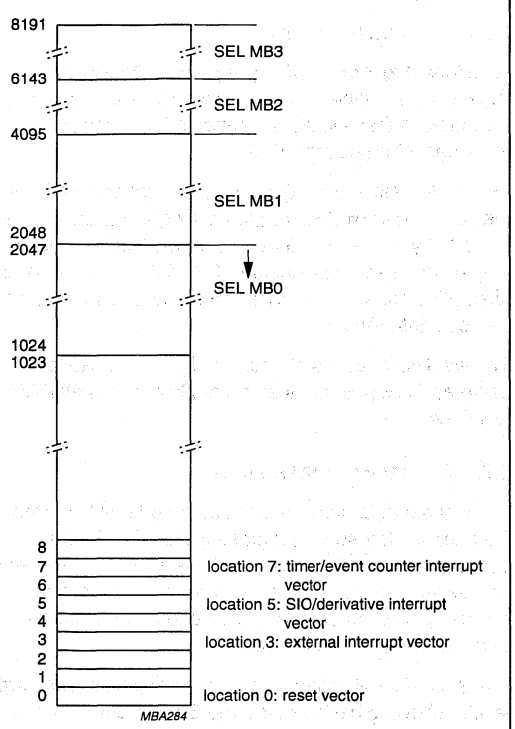


Fig.2 Program memory map,

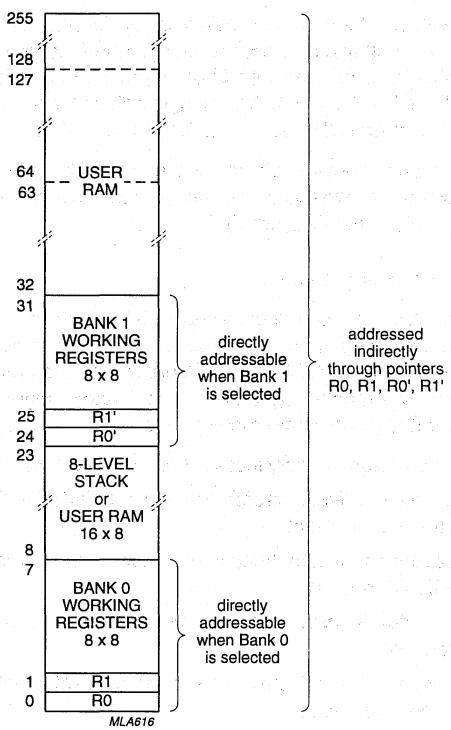


Fig.3 Data memory map.

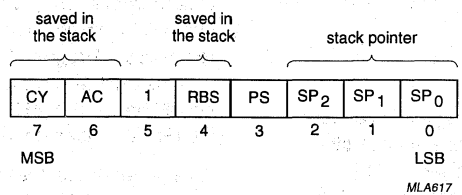


Fig.4 Program Status Word.

6.4 Program Counter

The 13-bit Program Counter is able to address up to 8 kbytes of ROM (see Fig.6). 11 bits (PC0 to PC10) are auto-incrementing. The two most significant bits (PC11 and PC12) must be changed under program control by SEL MB followed by a JMP or CALL instruction.

6.5 Program Status Word

The Program Status Word (PSW) is an 8-bit register in the CPU which stores information about the current status of the microcontroller (see Fig.4).

The PSW bits are:

- Bits 0 to 2: Stack Pointer bits (SP0, SP1, SP2)
- Bit 3: timer Prescaler Select (PS); 0 = modulo-32, 1 = modulo-1 (no prescaling)
- Bit 4: working Register Bank Select (RBS); 0 = register bank 0, 1 = register bank 1
- Bit 5: not used (fixed at 1)
- Bit 6: Auxiliary Carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7: Carry (CY); the carry flag indicates that the previous operation resulted in an overflow of the Accumulator.

All bits can be read using the MOV A, PSW instruction. Bits 0, 1 and 2 are affected by CALL, RET, RETR and interrupts. Bit 3 can be controlled by MOV PSW, A and bit 4 by SEL RB instructions. Bit 6 is set and cleared as a side-effect of ADD and ADDC instructions. Bit 7 is affected by ADD, ADDC, DA, RLC, RRC, CLR C and CPL C instructions.

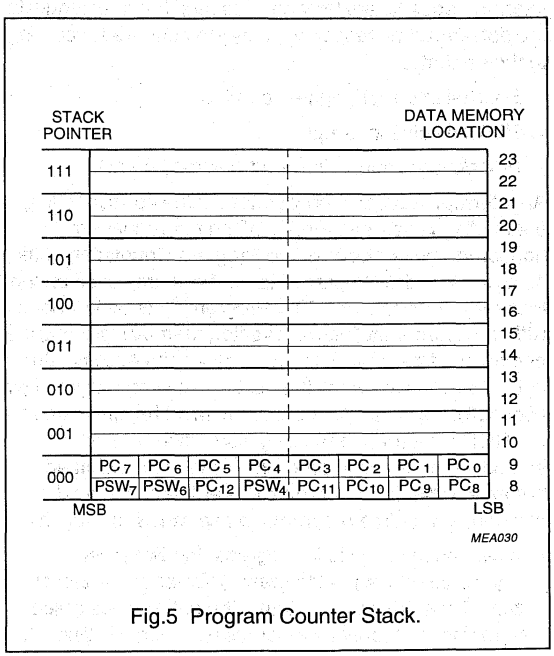


Fig.5 Program Counter Stack.

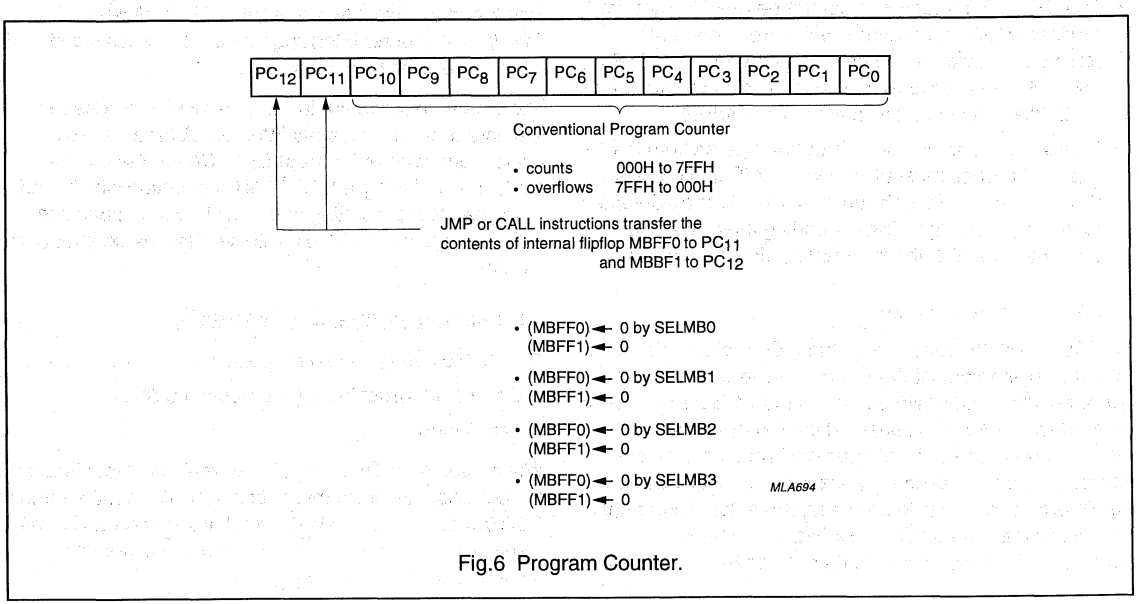


Fig.6 Program Counter.

6.6 Interrupts

External, SIO/derivative and timer/event counter interrupts are handled by the PCD33XXA family. The interrupt mechanism is single level, i.e. an executing interrupt routine cannot be pre-empted unless by reset. Further interrupt requests are latched. If several interrupt requests are detected simultaneously, they are honoured according to their priority:

- External interrupt (highest priority)
- SIO/derivative interrupt
- Timer/event counter interrupt (lowest priority).

An interrupt request is only sensed if the corresponding enable flag is set (see Fig.7). When the request is honoured, the contents of the Program Counter and bits 4, 6 and 7 of the Program Status Word are saved on the Program Counter stack. The Program Counter is loaded with the appropriate interrupt vector, thereby indicating the beginning of the interrupt routine. Since the Accumulator is not automatically saved, it must be saved and restored by user software. The interrupt routine must be terminated by the RETR (return and restore) instruction. At least one instruction of the main program will then be executed before another interrupt routine is entered. To avoid erroneous real-time programs, a few words of caution:

- While the interrupt is in progress, the two most significant bits of the Program Counter are frozen at zero. Thus, interrupt routines and subroutines called from interrupt routines must reside entirely in Bank 0.
- The SEL MB instruction must not be used in interrupt routines and in subroutines called from interrupt routines. Otherwise, the changed contents of MBFF0 and MBFF1 (see Fig.6) may lead to erroneous JMP and CALL destinations after return from interrupt.
- Subroutines and nested subroutines called from the interrupt routine must all end with RET since RETR clears the Interrupt In Progress flag (IIP), as a side-effect (see Figs 7 and 8). Further pending interrupts would then interfere with the interrupt routine in progress.

6.6.1 External interrupt

A LOW-to-HIGH transition on the CE/$\overline{T0}$ pin is latched in the digital filter/latch if the HIGH state exceeds 7 clock periods after a LOW state of more than 4 clock periods. If the external interrupt is enabled the External Interrupt Flag (EIF) is also asserted, thus constituting a valid external interrupt request. As soon as the IIP is clear, indicating that no interrupt routine is in progress, the external interrupt is invoked by a forced CALL to location 3. The EIF is simultaneously cleared (see Figs 7 and 8). The interrupt routine may acknowledge the interrupt via port lines. Execution of a DIS I (disable external interrupt) instruction cancels a stored interrupt request by clearing both the digital filter/latch and the EIF.

6.6.2 SIO/Derivative interrupt

The SIO/derivative interrupt is shared between the serial I/O interface (if available) and the derivative logic (if available). Software polling may be necessary to determine the origin of a request.

An interrupt condition in the serial I/O interface and/or the derivative logic will pull the PIN line LOW. If the SIO/derivative interrupt is enabled and no interrupt routine is in progress, the SIO/derivative interrupt routine will be invoked by a forced CALL to program memory location 5. The SIO/derivative interrupt routine must include instructions that will remove the cause of the SIO/derivative interrupt and thus reset PIN to its inactive HIGH state (for further details see Section 6.11). For derivative interrupts, consult the data sheet of the specific device.

6.6.3 Timer/event counter interrupt

If the timer/event counter interrupt is enabled, a timer/event counter 1 overflow sets the Timer Interrupt Flag (TIF). As soon as IIP is clear, meaning that no interrupt routine is in progress, the timer/event counter interrupt routine is invoked by a forced CALL to program memory location 7. The TIF is simultaneously cleared (see Figs 7 and 8). Execution of a DIS TCNTI (disable timer/event counter interrupt) instruction cancels a stored interrupt request by clearing TIF.

The timer/event counter interrupt may also be used to simulate a second external interrupt. After an enable timer/event counter interrupt (EN TCNTI), the counter mode is enabled by a STRT CNT instruction which loads FFH (the state preceding overflow) into the counter. A positive edge on the T1 pin will overflow the counter and set TIF.

6.7 Chip Enable/Test 0 Input (CE/$\overline{T0}$)

The CE/$\overline{T0}$ input has two purposes:

- External interrupt input (see Section 6.6)
- Test 0 input.

When used as a Test 0 input (external interrupt disabled) the conditional branch instruction JT0 will cause a jump if CE/$\overline{T0}$ = 1. The conditional branch instruction JNT0 will also cause a jump if CE/$\overline{T0}$ = 0. If CE/$\overline{T0}$ is not used, it must be tied to V_{DD} or V_{SS}.

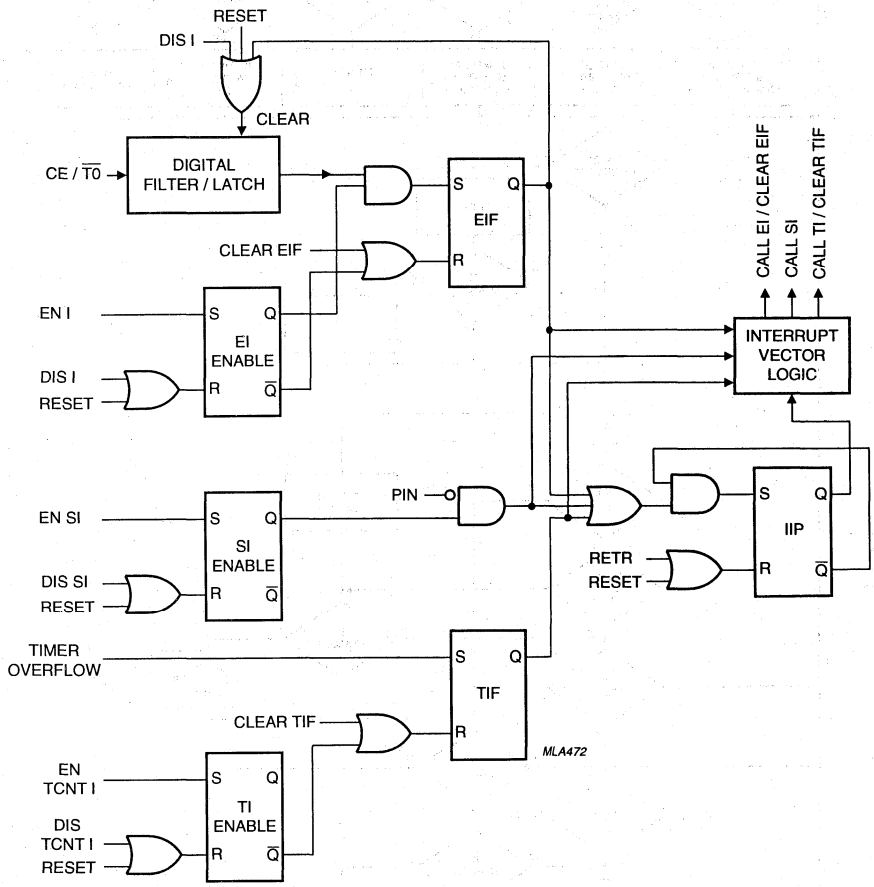


Fig.7 Simplified interrupt logic schematic (the R input overrules the S input for all flags).

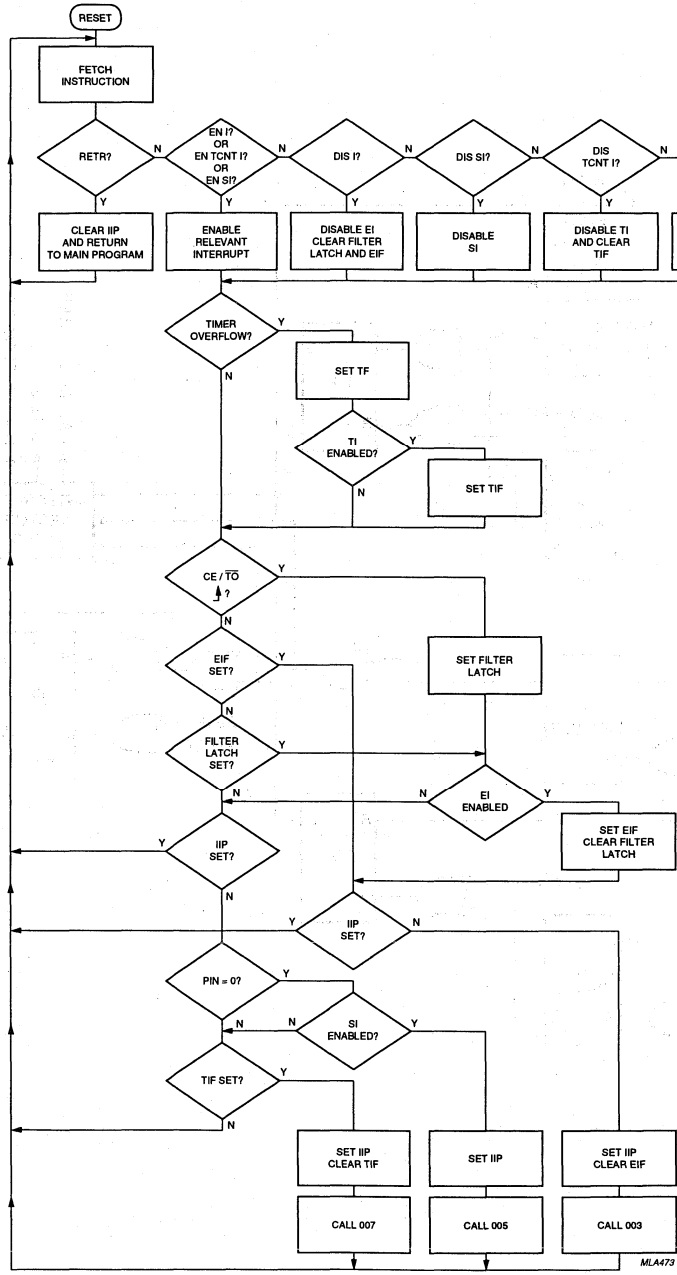


Fig.8 Flow chart illustrating CPU control in the presence of interrupts.

6.8 Timer/event counter 1

An internal 8-bit up counter is provided. The counter can be preset and read by the MOV T, A and MOV A, T instructions.

When the counter is to be used in the timer mode, a STRT T (start timer) instruction must be executed. Depending on the PS bit in the Program Status Word, the counter will increment every machine cycle (PS = 1, $\frac{1}{30}f_{xtal}$) or every 32 machine cycles (PS = 0, $\frac{1}{960}f_{xtal}$). STRT T clears the prescaler (see Fig.9) which is not otherwise accessible.

To count external events a STRT CNT (start event counter) instruction must be executed. A LOW-to-HIGH transition on pin T1 is counted if the HIGH state exceeds 4 clock periods after a LOW state of more than 4 clock periods. The maximum count rate is one increment per machine cycle ($\frac{1}{30}f_{xtal}$).

The timer mode and the event counter mode are both inhibited after reset or by executing a STOP TCNT (stop timer/event counter) instruction (see Fig.9).

In both the timer and in event counter modes, overflow has two effects:

- If the timer/event counter interrupt is enabled TIF is asserted thereby generating a timer/event counter interrupt request (see Section 6.6).
- The Timer Flag (TF) is set. TF can be tested by conditional branch instructions JTF (jump if TF = 1) or JNTF (jump if TF = 0). The JTF and JNTF instruction, as a side-effect, reset TF. The only other way to clear TF is to reset the microcontroller.

6.9 Test 1/count input (T1)

The T1 input has two purposes:

- Count input of 8-bit timer/event counter 1 (see Section 6.8)
- Test 1 input.

When used as a Test 1 input the conditional branch instruction JT1 will cause a jump if T1 = 1. The conditional branch instruction JNT1 will also cause a jump if T1 = 0. If T1 is not used, it must be tied to V_{DD} or V_{SS}.

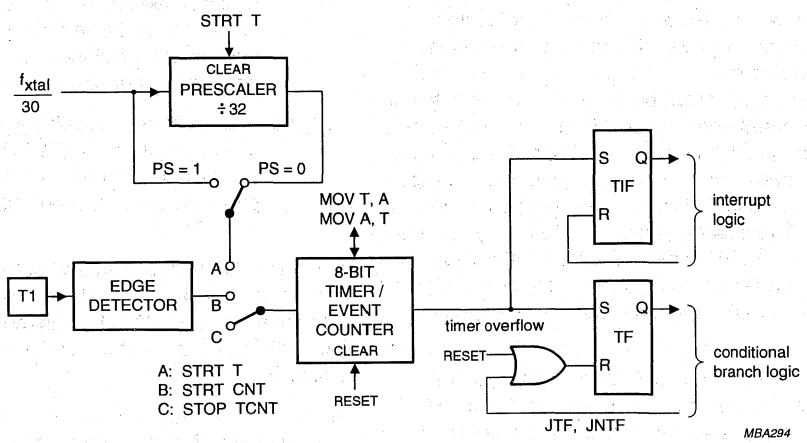


Fig.9 Timer/event counter 1.

6.10 Parallel ports

Three standard quasi-bidirectional I/O ports are defined:

- Port 0: parallel port of 8 lines (P0.0 to P0.7)
- Port 1: parallel port of 8 lines (P1.0 to P1.7)
- Port 2: parallel port of 4 lines (P2.0 to P2.2, SDA/P2.3).

Several members of the PCD33XXA family provide all 20 port lines. The eight Port 0 lines (P0.0 to P0.7) are available as a minimum. In addition to the standard ports, many PCD33XXA microcontrollers offer a variety of derivative ports. Please consult the data sheet of the specific device.

In general, all parallel ports can be used as either inputs or outputs. Output data written to a port is latched and remains unchanged until rewritten. If the port is used as an input, the external data is not latched and must remain stable until it is accessed by the CPU.

The standard port configuration is illustrated in Fig.11. When a logic 0 is written to the master/slave flip-flop, TR2 and TR3 are both in the OFF condition. TR1 turns ON and drives the output to V_{SS}.

When a logic 1 is written to the master/slave flip-flop, TR1 turns OFF. TR2 and TR3 both turn ON driving the output rapidly to V_{DD}. TR2 remains in the ON condition for the duration of the write pulse only. The constant current source is responsible for keeping the output line high. Sufficient source current is available for a TTL load HIGH level; the line can, however, be overridden by an external device. This is used when the port line serves as an input, but it may also be useful for wired-OR applications. In the latter case, unnecessary current through external devices is avoided since repeated logic 1 write operations will not activate TR2. The booster transistor TR2 is only asserted during a LOW-to-HIGH transition of the master/slave flip-flop. If the port line is to be used as an input, a logic 1 should first be stored in the master/slave flip-flop to turn TR1 OFF.

Access to Ports 0, 1 and 2 is provided by the parallel input/output instructions IN, OUTL, ANL and ORL. IN inputs port data to the Accumulator. OUTL outputs Accumulator data to the port. ANL and ORL are used for data manipulation in the port flip-flop. In contrast to Ports 0, 1 and 2, derivative ports are accessed by the derivative input/output instructions MOV, ANL and ORL. ANL and ORL are used for data manipulation in the port flip-flop. MOV is used for all data transfers between port and Accumulator. The source data for the Accumulator can be loaded from either the port line or the port flip-flop. Two derivative addresses are therefore provided per port (see Table 2).

All standard and derivative port accesses are performed by two-cycle instructions. Their instruction timing is shown in Fig.10. For input, data on port lines is sensed during timeslots 3 and 4 of machine cycle 2 (see Sections 6.12 and 6.13). For output, the data change occurs in timeslot 7. For OUTL, data changes during machine cycle 1. For ANL, ORL and MOV Dx, A, data changes during machine cycle 2.

Table 2 Derivative port address pair.

ADDRESS	TYPE	ACCESS
8-bit line address	R	derivative port line
8-bit flip-flop address	R/W	derivative port flip-flop

Three port output mask options are available:

Option 1 Standard Port; quasi-bidirectional I/O with switched pull-up current source of 100 µA (typ.) and p-channel booster transistor TR2. TR2 is only active for 1 clock cycle during LOW-to-HIGH transitions (see Fig.11).

Option 2 Open Drain; quasi-bidirectional I/O with only an n-channel open drain output. Application as an output requires connection of an external pull-up resistor (see Fig.12). If unused, an Option 2 output should be tied to V_{SS}. This keeps the input path from floating, thereby avoiding undesirable current flow through input stages.

Option 3 Push-pull; drive capability of the output will be 5 mA (typ.) at V_{DD} = 3 V in both polarities. Since short circuit currents would flow during input, push-pull lines must only be used as outputs (see Fig.13).

If available, SDA/P2.3 is shared between the parallel Port 2 and the serial I/O interface. Therefore, only option 2 is permitted for SDA/P2.3. For the remaining standard port lines (P0.0 to P2.2), all three options are generally available.

Besides port output mask options, the port flip-flop state, after reset, may be specified for each individual port line (except SDA/P2.3). Usually the 'set option' will be selected, which avoids short-circuits for ports intended as inputs. However, there may be cases in which the port should output a logic zero after reset. The user may then specify the 'reset option' for certain port lines.

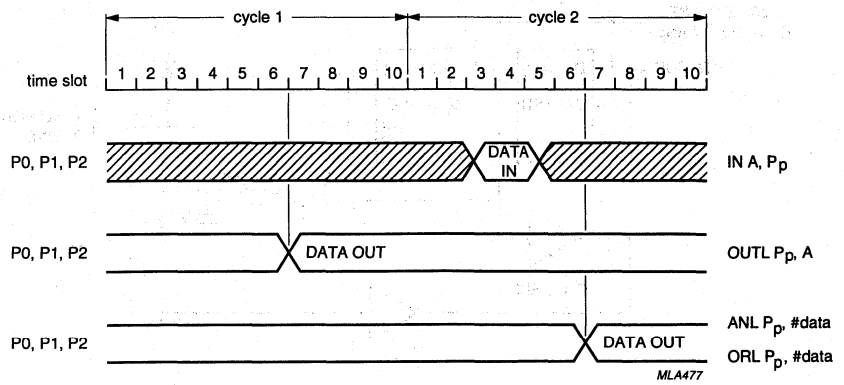


Fig.10 Input /output timing of standard and derivative ports.

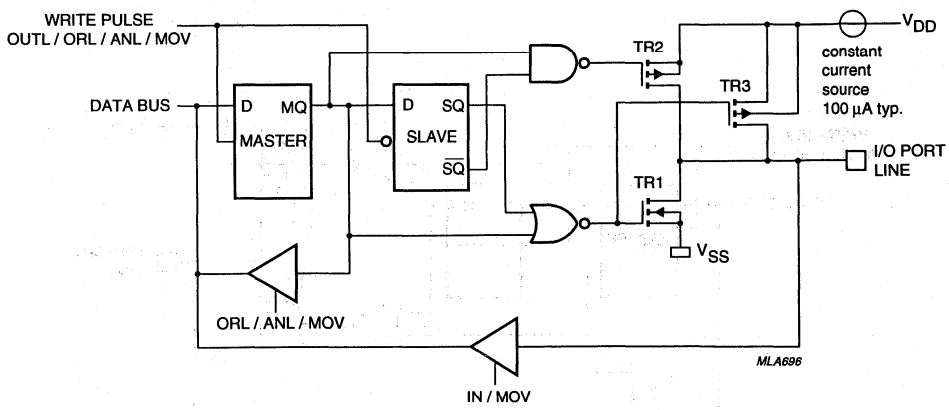


Fig.11 Standard output with switched current source.

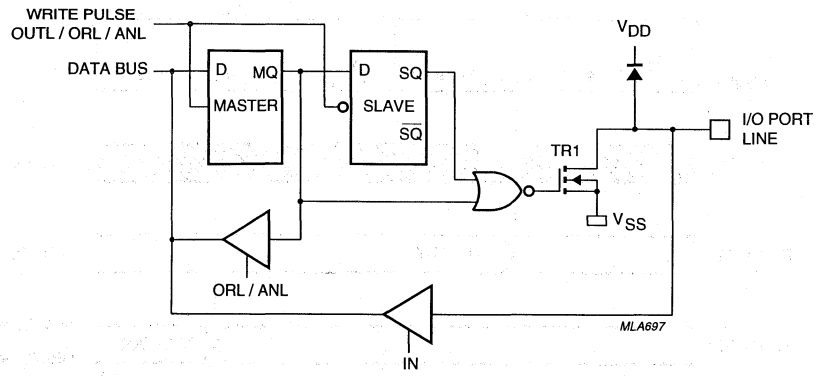


Fig.12 Open drain output.

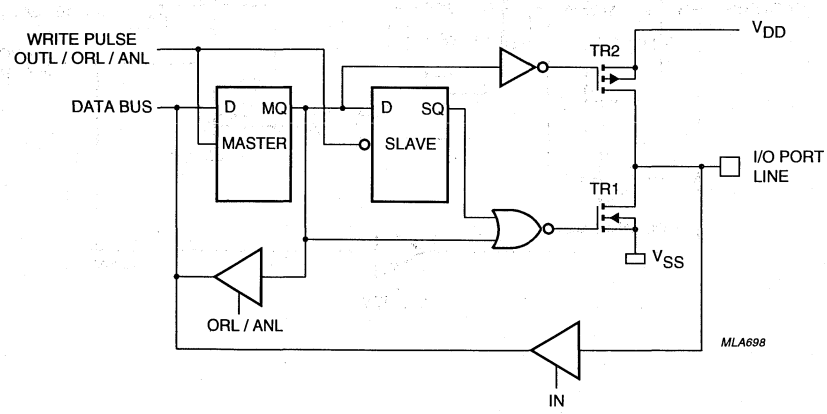


Fig.13 Push-pull output.

6.11 Serial I/O interface

Many members of the PCD33XXA family have a serial I/O interface (I^2C-bus or 'Inter-Integrated Circuit Bus'). This two-line serial bus extends the microcontroller capabilities when implemented with the powerful I^2C-bus devices of the PCF85XX, PCD33XX and 'Clips' peripheral families.

Microcontrollers that do not have a serial I/O interface can simulate it by software, by using port pins. However, such microcontrollers must continuously monitor the serial bus. As well as degrading the maximum data transfer rate, this approach may also consume significant processing and memory resources.

If available, however, the serial I/O interface detects the valid 7-bit I^2C-bus address of the device, transfers serial data and provides data conversion to and from parallel format, all without disrupting program execution. Only when a complete byte has been transferred, an interrupt is requested by which the next data byte can be written to or read out of the serial I/O interface. The serial I/O interface also facilitates the implementation of multimaster systems in which two or more microcontrollers communicate via the same I^2C-bus. An automatic arbitration procedure resolves bus conflicts.

The I^2C-bus consists of a bidirectional clock line (SCL) and a bidirectional data line (SDA). Whereas SCL uses the dedicated pin SCLK, SDA and Port line P2.3 share the pin, SDA/P2.3. When the serial I/O interface is enabled, SDA/P2.3 is disabled as a port line. Input signals on SCLK and SDA are filtered for enhanced noise immunity. When used as outputs, SCLK and SDA/P2.3 require an external pull-up resistor because they are open drain. If unused, SCLK and SDA/P2.3 should be tied to V_{SS} (see Section 6.10, Option 2).

Communication between CPU and serial I/O interface is handled through the four serial I/O interface registers S0, S0', S1 and S2 (see Fig.14).

A detailed description of the I^2C-bus specification, with applications, is given in the brochure *"The I^2C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

6.11.1 Data shift register (S0)

The Data Shift Register converts serial data to a parallel format and vice versa. The leading bit of a serial transfer corresponds to the most significant bit of the parallel word. An interrupt request is issued after transfer of a complete byte and after detection of the valid I^2C-bus address. Register S0 is read by MOV A, S0. It is written to by MOV S0, A or MOV S0, #data if the ESO (Enable Serial I/O) bit in the Status Register (S1) is set.

6.11.2 Address register (S0')

The Address Register contains the 7-bit I^2C-bus address of the device and the ALS (Always Selected) bit. When ALS is zero, which is the recommended mode of operation, bus transfers are ignored unless the valid device address immediately follows the start condition. Besides the stored 7-bit address, the 'general call address' (pre-defined as zero) is also acceptable as a valid address. If ALS is set, however, any transfer on the bus will be stored in the Data Shift Register.

The Address Register S0' is write-only. It can be written by MOV S0, A and MOV S0, #data if the ESO (Enable Serial I/O) bit in the Status Register (S1) is zero.

6.11.3 Clock control register (S2)

The Clock Control Register defines the frequency of f_{SCLK} as the microcontroller clock frequency divided by an integer (see Table 3). It also defines ASC (Asymmetrical Clock) and ACK (Acknowledge).

If ASC = 1, the generated SCLK has a duty cycle of approximately 75%. The asymmetrical clock limits the I^2C-bus transmission rate to below 55 kHz. Divisors 39, 45 and 51 are not allowed if ASC = 1. However, an SCLK duty cycle of approximately 50% results if ASC = 0. This permits I^2C-bus transmission rates of up to 100 kHz. All divisors of Table 3 are available. It is, therefore, recommended to select ASC = 0.

For the normal I^2C-bus protocol ACK must be set. After each byte transfer an extra SCLK pulse is generated during which the receiver may acknowledge reception. If ACK is zero, no acknowledge phase is available. This mode is temporarily used when a master/receiver refuses the acknowledgement in order to signal an end of transmission to the slave transmitter (see Section 6.11.4.9).

The Clock Control Register (S2) is write-only. It can be written to by MOV S2, A and MOV S2, #data.

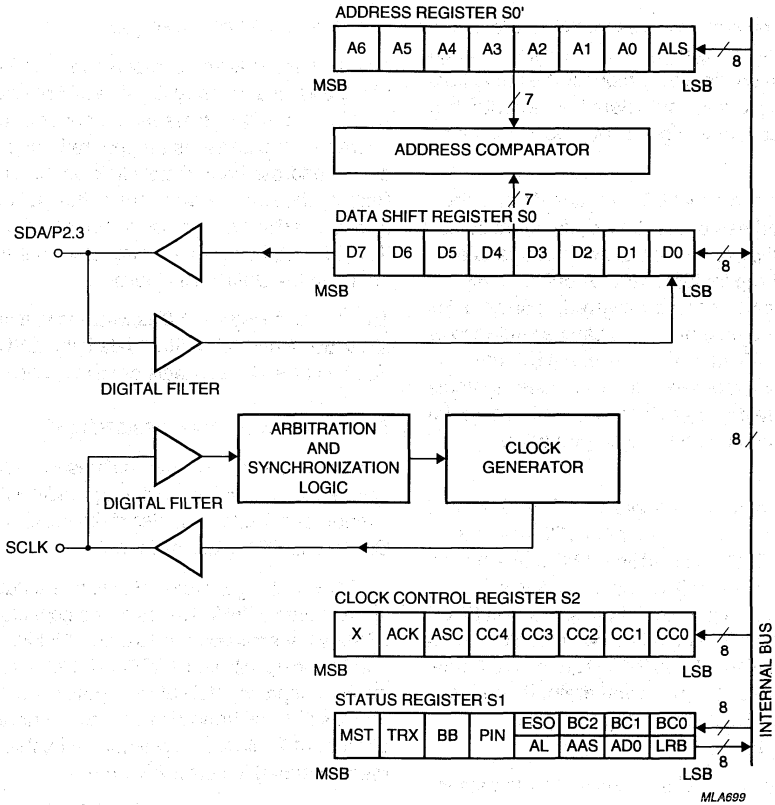


Fig.14 Block diagram of the serial I/O interface.

Table 3 f_{SCLK} as defined by Clock Control Register (S2).

CC4 TO CC0 (HEX)	f_{xtal} DIVISOR (DF)	f_{SCLK} (kHz) at		
		f_{xtal} = 3.58 MHz	f_{xtal} = 10 MHz	f_{xtal} = 16 MHz
00	forbidden	–	–	–
01	39	91.8	256.4[1]	410.3[1]
02	45	79.5	222.2[1]	355.6[1]
03	51	70.2	196.1[1]	313.7[1]
04	63	56.8	158.7[1]	254.0[1]
05	75	47.7	133.3[1]	213.3[1]
06	87	41.1	114.9[1]	183.9[1]
07	99	36.2	101.0[1]	161.6[1]
08	123	29.1	81.3	130.1[1]
09	147	4.4	68.0	108.8[1]
0A	171	20.9	58.5	93.6
0B	195	18.4	51.3	82.1
0C	243	14.7	41.2	65.8
0D	291	12.3	34.4	55.0
0E	339	10.6	29.5	47.2
0F	387	9.2	25.8	41.3
10	483	7.4	20.7	33.1
11	579	6.2	17.3	27.6
12	675	5.3	14.8	23.7
13	771	4.6	13.0	20.8
14	963	3.7	10.4	16.6
15	1155	3.1	8.7	13.9
16	1347	2.7	7.4	11.9
17	1539	2.3	6.5	10.4
18	1923	1.9	5.2	8.3
19	2307	1.6	4.3	6.9
1A	2691	1.3	3.7	5.9
1B	3075	1.2	3.3	5.2
1C	3843	0.9	2.6	4.2
1D	4611	0.8	2.2	3.5
1E	5379	0.7	1.9	3.0
1F	6147	0.6	1.6	2.6

Note

1. Not permitted; maximum f_{SCLK} = 100 kHz in I^2C-bus systems.

6.11.4 Status Register (S1)

The Status Register controls the serial I/O interface and provides feedback concerning on-going bus transfers. Register S1 can be accessed by MOV A, S1, MOV S1, A and MOV S1, #data. The lower nibble of the Status Register is twofold: control bits BC0 to BC2 and ESO can only be written, whereas feedback bits LRB, AD0, AAS and AL can only be read. Table 4 describes the status bits.

The status bits interact in intricate ways with each other. This must be kept in mind when an I^2C-bus application is programmed.

6.11.4.1 Master bit (MST) and Transmitter bit (TRX)

MST and TRX together define the state of the serial I/O interface. When not engaged in a bus transfer MST and TRX should always be at zero, the slave/receiver state (see Fig.15). A return to this state is always performed by software. If the previous state was the master state, the transition (to slave/receiver by MOV1,#D8H) involves a stop condition which, as a consequence, clears both MST and TRX.

The transition to the master/transmitter state is also a programmed event. However, transitions to the master/receiver and the slave/transmitter states occur automatically if ALS = 0 (standard I^2C-bus protocol). A slave/receiver becomes a slave/transmitter if $R/\overline{W} = 1$, in its valid address (following the start condition). A master/transmitter becomes a master/receiver if $R/\overline{W} = 1$, in the transmitted address.

6.11.4.2 Pending Interrupt Not bit (PIN)

If MST = 1 or, if ALS = 1, PIN is set to zero after every byte transfer. Conversely, PIN becomes zero when a valid address is detected and after each byte of the following transfer. In addition, the serial interrupt request, PIN = 0 initiates 'clock synchronization', i.e. the SCLK line is pulled to V_{SS} as long as PIN = 0. With this feature a slave may slow down a master, thus providing time to read the Data Register (in the case of a slave/receiver) or to write to the Data Register (in the case of a slave/transmitter). PIN is cancelled by an access to register S0 or by explicitly setting PIN to one.

If the SIO/derivative interrupt is disabled, the serial I/O interface may be serviced by testing PIN directly in user software.

6.11.4.3 Bus Busy bit (BB)

The Bus Busy bit (BB) is controlled by the serial I/O interface or by software in the bus master to generate the start and stop conditions. When a master clears BB (by MOV S1, #D8H), the serial I/O interface automatically clears MST and TRX, thereby returning to the slave/receiver state (see Fig.15). If BB = 1, write access to S1 is inhibited, except for the master or an addressed slave. Should BB be inadvertently set by excessive noise on the bus, the deadlock can be resolved by two consecutive MOV S1, #18H, the first of which just clears BB.

When a slave/transmitter detects an end of transmission (signalled by the lack of an acknowledgment from the master receiver), it has to access S1 in order to cancel PIN and to become slave/receiver. However, BB should remain set. This is reflected by MOV S1, #38H as illustrated in Fig.15. With PIN = 1, 'clock synchronization' terminates, enabling the master to generate the stop condition.

A start condition must only be generated when BB = 0; otherwise the serial I/O interface will respond as if bus arbitration has been lost (see Section 6.11.4.4).

6.11.4.4 Arbitration Lost bit (AL)

The AL bit is set by the serial I/O interface when it loses a bus arbitration in the master/transmitter mode. MST and TRX are cleared simultaneously to enable the interface, now in slave/receiver mode, to determine if it is validly addressed by the device that won the arbitration. PIN is activated when the byte transfer is complete. AL will be cleared when the serial interrupt is cancelled.

6.11.4.5 Addressed As Slave bit (AAS)

AAS is set by the serial I/O interface following a start condition when the valid address is detected (ALS = 0 in register S0') or when the first byte is received (ALS = 1 in register S0'). AAS is cleared when the serial interrupt is cancelled.

6.11.4.6 Address Zero bit (AD0)

AD0 is set, independently of ALS, by the serial I/O interface when byte 00H, the 'general call' address, is detected following a start condition. AD0 is cleared after a repeated start or a stop condition.

6.11.4.7 Last Received Bit (LRB)

LRB corresponds to the last bit transferred. If ACK = 1, LRB contains the acknowledgement bit. It remains valid as long as PIN = 0.

6.11.4.8 Enable Serial I/O bit (ESO)

When ESO = 0 access to register S0' is enabled. SCLK is in the high-impedance state and SDA/P2.3 is available as a normal port line.

When ESO = 1 the serial I/O interface and access to register S0 are enabled. Only when ESO = 1 may the other bits of register S1 be changed. SCLK and SDA/P2.3 are enabled as serial clock and data lines, respectively.

To avoid bus deadlock, ESO must be set to zero prior to the execution of the STOP instruction.

6.11.4.9 Bit Counter bits (BC0, BC1 and BC2)

The bit counter bits BC0, BC1 and BC2 should all be at zero for normal I^2C-bus operation. The bit counter is always cleared by a start condition. Therefore, all eight bits of the first byte are transferred.

If a non-zero bit counter value is chosen, it is only valid for one register S0 transfer since the counter decrements to zero. An important use of the bit counter arises when a master/receiver signals an end of transmission by sending a negative acknowledge after the last byte received. To do this, the last byte is received with bit ACK = 0 in register S2. The negative acknowledge is then issued by setting the bit counter to one and 'receiving' one bit from the HIGH level available on the SDA line. The slave/transmitter interprets the same signals as a negative acknowledgement.

Table 4 Overview of Status Register bits.

BIT	NAME	TYPE	DESCRIPTION
MST	Master	R/W	MST = 0: slave (SCLK input). MST = 1: master (SCLK output).
TRX	Transmitter		TRX = 0: receiver (SDA/P2.3 input. TRX = 1: transmitter (SDA/P2.3 output).
BB	Bus Busy	R/W	BB = 0: bus inactive (R)/generates stop condition (W). BB = 1: bus busy (R)/generates start condition (W).
PIN	Pending Interrupt Not	R/W	PIN = 0: serial interrupt pending (after byte transfer, valid address or lost arbitration). SCLK line forced to V_{SS}. PIN = 1: no serial interrupt pending.
ESO	Enable Serial Output	W	ESO = 0: serial I/O interface disabled/write access to S0' possible. ESO = 1: serial I/O interface enabled write access to S0 possible.
BC0 to BC2	Bit Counter 0 to 2	W	3-bit binary value of 0 to 7, counting down the number of bits transferred (0 used for complete byte).
AL	Arbitration Lost	R	Set: when a bus conflict is lost. Reset: when corresponding serial interrupt (PIN) is cancelled.
AAS	Addressed As Slave	R	Set: following a start condition if valid address is detected (ALS = 0) or if first byte is received (ALS = 1). Reset: when corresponding serial interrupt (PIN) is cancelled.
AD0	Address zero	R	Set: following a start condition if byte 00H ('general call' address) is detected. Reset: after a repeated start or a stop condition.
LRB	Last Received Bit	R	Set or Reset depending on the value of the last bit transferred, acknowledgement bit if ACK = 1.

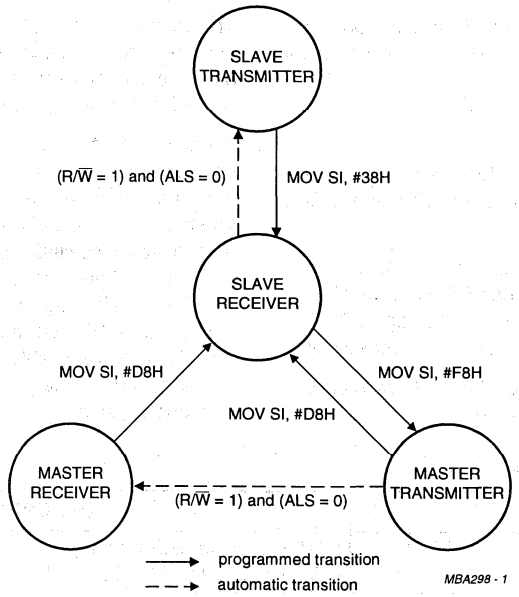


Fig.15 State diagram of the serial I/O interface.

6.12 Timing

Every machine cycle consists of 10 time slots which are again subdivided into 3 clock periods each (see Fig.16).

Permitted clock frequencies range from 1 MHz to a maximum, which is a function of the supply voltage. At $V_{DD} \geq 4.5$ V, a 16 MHz maximum clock frequency is guaranteed.

The clock signal may be internally generated by an on-chip oscillator. Alternatively, an external clock may be applied to pin XTAL1. In this configuration, a short circuit with an internal pull-up transistor on XTAL1 may occur while the oscillator is inhibited (see Section 6.13). Care should be taken to avoid excessive current flow.

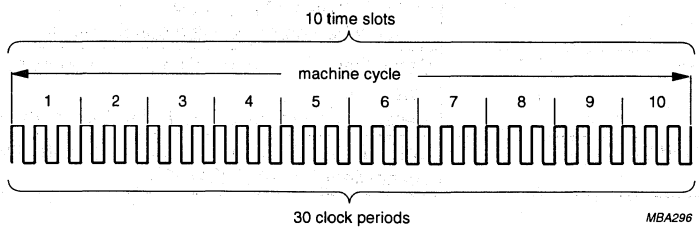


Fig.16 Timing of a machine cycle.

6.13 Oscillator

The on-chip oscillator basically consists of an inverter stage which includes a feedback resistor and load capacitors (see Fig.17). In most applications, a quartz crystal will be connected between XTAL1 and XTAL2. Alternatively, a ceramic resonator or an inductor may be used as a timing element.

When the supply voltage drops below the power-on reference level, the oscillator is inhibited. The internal oscillator can also be inhibited by the STOP instruction under software control (see Section 6.16).

The transconductance (g_m) of the inverter stage can be mask-programmed, thereby optimizing the oscillator for a specific frequency and resonator. Three standard transconductance options, referred to as LOW, MEDIUM and HIGH, can be specified by the user. Table 6 is intended as a rough selection guide for typical quartz and PXE resonators.

With $C_1 = C_2 = 10$ pF on-chip, external capacitors are not required for quartz oscillators. However, for adequate frequency stability, PXE resonators need external capacitors in the order of the static resonator capacitance C_0, such as external $C_1 = C_2 = 30$ to 100 pF.

Oscillator start-up time depends mainly on the external timing element. The start-up time of a quartz crystal is several milliseconds because of the narrow crystal bandwidth. For proper oscillator start-up, the transconductance (g_m) of the inverter stage must fulfil relationship (1); shown below.

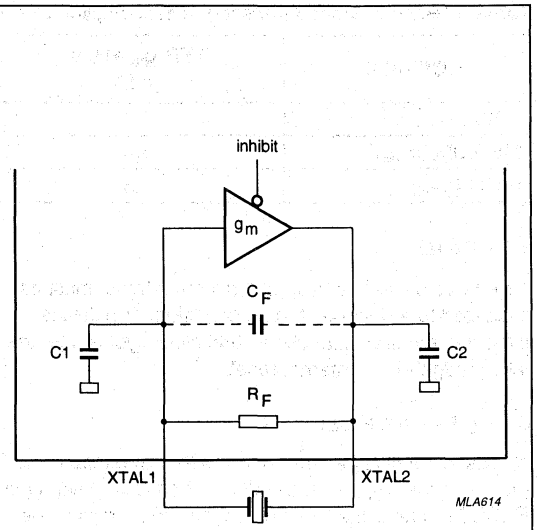


Fig.17 Oscillator with integrated elements.

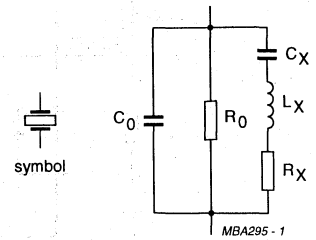


Fig.18 Crystal unit equivalent circuit.

Table 5 Notation to relationship (see Figs 17 and 18).

SYMBOL	DEFINITION
R_X	resonator series resistance
C_0	static resonator capacitance
R_0	resonator loss resistance
R_P	R_0 // R_F
R_F	feedback resistor
C_L	C1 x C2/(C1 + C2) (load capacitance)
C_F	parasitic feedback capacitance (typically 2 pF on-chip, external value depends on printed-circuit board wiring)
ω	$2\pi f_{osc}$

$$4.2\left[R_X\omega^2(C_L+C_0+C_F)^2+\frac{1}{R_P}\right] < g_m < \frac{C1\times C2}{\left[R_X(C_0+C_F)^2+\frac{1}{\omega^2 R_P}\right]} \quad (1)$$

Table 6 Recommended transconductance options for popular quartz and PXE resonators.

OPTION	TYP. g_m at 5 V (mS)	f_{osc} FOR QUARTZ (MHz)	f_{osc} FOR PXE (MHz)
LOW (g_{mL})	0.4	1 to 6	1 to 2.4
MEDIUM (g_{mM})	1.6	4 to 12	1 to 6
HIGH (g_{mH})	4.5	10 to 16	3 to 16

6.14 Reset

To ensure proper start-up, the microcontroller must be initialized to a defined starting condition. The device executes the first instruction 1866 clock cycles after the falling edge of the internal reset.

6.14.1 PASSIVE RESET

A passive reset is generated by the RC circuit illustrated in Fig.19. While V_{DD} rises, the discharged C_{reset} keeps the RESET pin near the V_{DD} level. When V_{DD} crosses the power-on reference level (V_{ref}) the power-on reset circuit generates a reset pulse of approximately 50 µs. This pulse is without effect since it feeds into the reset signal forced by the pulse on the RESET pin. The f_{xtal} dependent minimum V_{DD} must be reached before the voltage on RESET drops below $V_{IH} = 0.7V_{DD}$. This translates into a lower bound for $C_{reset}R_{reset}$ equal to twice the rise time of V_{DD} (for linearly rising V_{DD}) or eight times the time constant of V_{DD} (for exponentially rising V_{DD}). The internal diode rapidly discharges C_{reset} when V_{DD} falls off, ensuring reliable reset even after short interruptions of supply voltage. To avoid overload of the internal diode, an external diode should be added in parallel if $C_{reset} > 2.2$ µF.

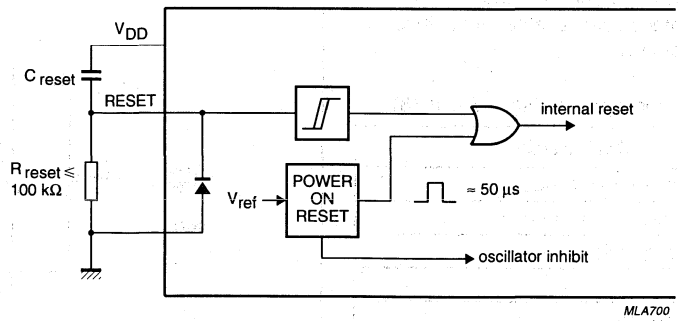


Fig.19 Passive power-on reset.

6.14.2 Internal reset

In systems where V_{DD} reaches its f_{xtal} dependent minimum operating value before the clock f_{xtal} is applied, reset can be performed without external components. This condition is generally fulfilled with quartz and PXE resonators since oscillator start-up takes several milliseconds. Besides, rapid power-up is usually available in battery-powered systems.

If the internal power-on reset is used the RESET pin should be connected to V_{SS}. When V_{DD} increases above the power-on reference level V_{ref}, the power-on reset circuit generates a reset pulse of approximately 50 µs. This pulse guarantees proper initialization under the conditions defined above.

The power-on reference level V_{ref} is a mask option. The user can select a reference voltage between 1.2 V and 3.6 V in discrete steps of 100 mV. The accuracy of the reference voltage is ±500 mV for the V_{ref} range 1.2 V to 3.0 V and ±800 mV for the V_{ref} range 3.1 V to 3.6 V. The chosen V_{ref} should have sufficient margin regarding the minimum intended V_{DD}.

A mask option without an internal power-on reset circuit is also available. It is recommended if the user does not intend to use the internal power-on-reset circuit. In this case, the supply current requirements in Stop mode (see Section 6.16) will reduce to the level of leakage currents, i.e. virtually zero at ambient temperature.

6.14.3 Active reset

An active reset can be generated by driving the RESET pin HIGH from an external logic device. Such an active reset pulse should not fall off before V_{DD} has reached its f_{xtal} dependent minimum operating value.

6.14.4 Reset state

After a reset, the device state is characterized as follows:

- Program Counter 0
- Memory bank 0
- Register Bank 0 - Stack Pointer 0 (location pair 8 and 9)
- All interrupts disabled
- Timer/event counter 1 stopped and cleared
- Timer prescaler modulo-32 (PS = 0)
- Timer flag cleared
- All port flip-flops (except SDA/P2.3) set to 1 (set option) or 0 (reset option) as selected by the user
- SDA/P2.3 is high-impedance with the port flip-flop set to 1
- SCLK is high-impedance
- Serial I/O interface disabled (ESO = 0) and in slave/receiver mode (S0, S0', S1 and S2 cleared except for PIN = 1)
- Idle and Stop modes cancelled.

6.15 Idle mode

The Idle mode is very useful in low-power applications. When all computational tasks are completed, the device can be put into standby instead of into a busy waiting loop. Nevertheless, the device is on the alert and ready to respond rapidly to any interrupt.

The microcontroller enters the Idle mode via the IDLE instruction. In the Idle mode, all activity is halted except for the oscillator, the timer/event counter 1 and the serial I/O interface (if available).

The microcontroller leaves the Idle mode when an enabled interrupt occurs. The interrupt routine is executed before operation resumes with the instruction following the IDLE opcode.

For timer/event counter interrupts and SIO/derivative interrupts, termination of the Idle mode is straightforward. However, care must be taken when the Idle mode is left by the external interrupt since CE/$\overline{T0}$ is triggered on the rising edge. If CE/$\overline{T0}$ was HIGH prior to entering the Idle mode, it must be taken LOW before the positive edge can be generated. Figure 20 specifies the exact timing for leaving the Idle mode via the external interrupt CE/$\overline{T0}$.

If no interrupt is enabled, the Idle mode can only be terminated by an active signal on the RESET pin. A normal reset sequence is executed (see Fig.20).

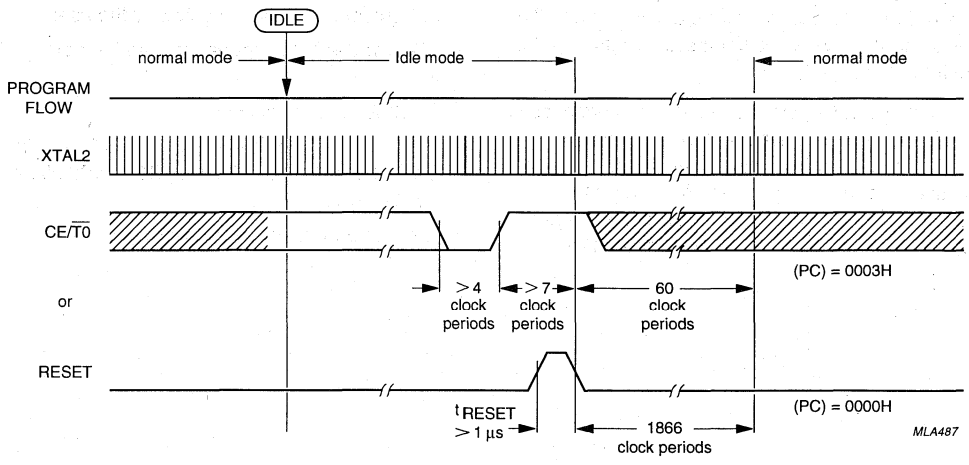


Fig.20 Entering and leaving the Idle mode.

6.16 Stop mode

The Stop mode allows very low-power applications. When all computational tasks are completed, the device can be almost completely shut off by stopping its oscillator. In contrast to the Idle mode, the device is not ready to respond rapidly to any interrupt.

When the microcontroller enters the Stop mode via the STOP instruction; the oscillator is switched off. All internal states and I/O levels are maintained.

The microcontroller leaves the Stop mode by a HIGH level on CE/$\overline{T0}$ or a reset. In the latter case, a normal reset sequence is executed (see Fig.21).

In contrast to the Idle mode and the external interrupt mechanism, the microcontroller responds to a HIGH level on CE/$\overline{T0}$ rather than to a positive edge. If CE/$\overline{T0}$ is HIGH when the STOP instruction is executed, the Stop mode will not be entered.

A positive edge on CE/$\overline{T0}$ continues program execution after a 1866 clock cycle delay, which ensures proper oscillator start-up. If the external interrupt is enabled, the device executes the instruction following the STOP opcode before diverting to the interrupt routine. If the external interrupt is disabled, program execution continues with the instructions following the STOP opcode (see Fig.21).

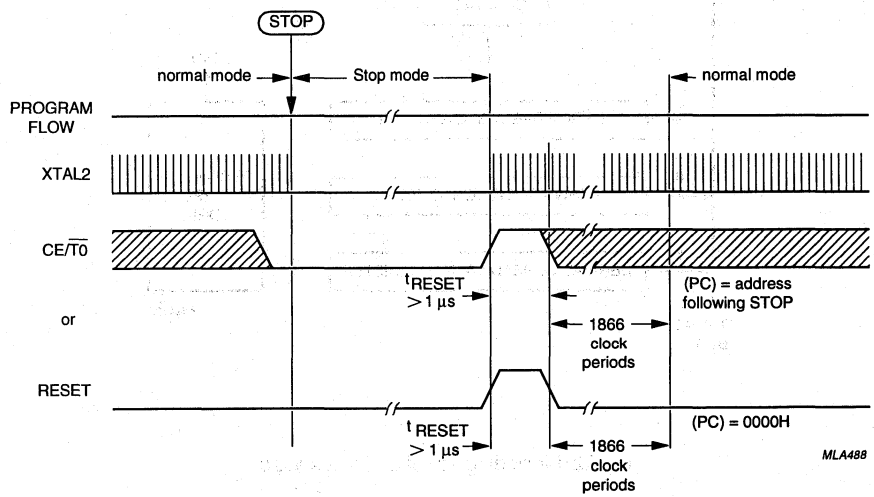


Fig.21 Entering and leaving the Stop mode.

6.17 Derivative logic

Derivative logic is provided with many members of the PCD33XXA family. The detailed description of the derivative circuitry is given in the data sheet of the specific device. In this section, the shared principles of derivative logic are briefly reviewed.

Derivative registers are accessed over the internal bus. The derivative registers are write-only, read-only or read/write (see Fig.22). They are addressed through the derivative Address Register when the derivative input/output instructions (MOV A, Dx; MOV Dx, A; ANL Dx, A and ORL Dx, A) are executed.

Derivative interrupts share the line PIN with the SIO interrupt (if available). When the derivative interrupt routine is executed, the PIN line must be de-activated by software.

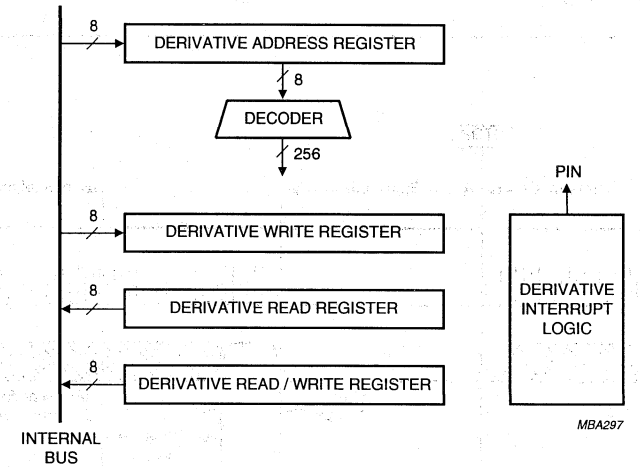


Fig.22 Block diagram of derivative logic.

Table 7 Summary of mask options.

FEATURE	OPTION	DESCRIPTION
ROM	any mix of instructions	program; size restricted by ROM size (see Tables 8 and 9)
Ports	option 1	standard output (see Fig.11)
	option 2	open drain output (see Fig.12)
	option 3	push-pull output (see Fig.13)
	set	flip-flop at logic 1 after reset
	reset	flip-flop at logic 0 after reset
Power-on reference	V_{ref}	1.2 to 3.6 V in increments of 100 mV; with ±500 mV accuracy
Oscillator	g_{mL}	LOW transconductance (see Table 6)
	g_{mM}	MEDIUM transconductance (see Table 6)
	g_{mH}	HIGH transconductance (see Table 6)

7 INSTRUCTION SET

The PCD33XXA instruction set consists of over 100 one and two-byte instructions. Program code efficiency is high because all RAM locations and all ROM locations on a 256-byte page require only a single-byte address. Table 9 lists the symbols that are used in Table 8 and the Instruction map is shown in Section 7.1.

Table 8 PCD33XXA family instruction set.

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
ACCUMULATOR					
ADD A, Rr[1]	6<8 + r>	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0 to 7
ADD A, @Rr[1]	6r	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((Rr))	r = 0, 1
ADD A, #data[1]	03 data	2/2	Add immediate data to A	(A)←(A) + data	
ADDC A, Rr[1]	7<8 + r>	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0 to 7
ADDC A, @Rr[1]	7r	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((Rr)) + (C)	r = 0, 1
ADDC A, #data[1]	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)	
ANL A, Rr	5<8 + r>	1/1	AND Rr with A	(A)←(A) AND (Rr)	r = 0 to 7
ANL A, @Rr	5r	1/1	AND RAM data addressed by Rr, with A	(A)←(A) AND ((Rr))	r = 0, 1
ANL A, #data	53 data	2/2	AND immediate data with A	(A)←(A) AND data	
ORL A, Rr	4<8 + r>	1/1	OR Rr with A	(A)←(A) OR (Rr)	r = 0 to 7
ORL A, @Rr	4r	1/1	OR RAM data, addressed by Rr, with A	(A)←(A) OR ((Rr))	r = 0, 1
ORL A, #data	43 data	2/2	OR immediate data with A	(A)←(A) OR data)	
XRL A, Rr	D<8 +r>	1/1	XOR Rr with A	(A)←(A) XOR (Rr)	r = 0 to 7
XRL A, @Rr	Dr	1/1	XOR RAM data, addressed by Rr, with A	(A)←(A) XOR ((Rr))	r = 0, 1
XRL A, #data	D3 data	2/2	XOR immediate data with A	(A)←(A) XOR data)	
INC A	17	1/1	Increment A by 1	(A)←(A) + 1	
DEC A	07	1/1	Decrement A by 1	(A)←(A) – 1	
CLR A	27	1/1	Clear A to zero	(A)←0	
CPL A	37	1/1	One's complement A	(A)←NOT(A)	
RL A	E7	1/1	Rotate A left	$(A_{n+1})\leftarrow(A_n)$, $(A_0)\leftarrow(A_7)$	n = 0 to 6
RLC A[2]	F7	1/1	Rotate A left through carry	$(A_{n+1})\leftarrow(A_n)$, $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0 to 6
RR A	77	1/1	Rotate A right	$(A_n)\leftarrow(A_{n+1})$, $(A_7)\leftarrow(A_0)$	n = 0 to 6
RRC A[2]	67	1/1	Rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$, $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0 to 6
DA A[2]	57	1/1	Decimal adjust A	(A)←(A) + 06H if AC = 1 or $(A_{0-3})>9$; (A)←(A) + 60H if $(A_{4-7})>9$	
SWAP A[2]	47	1/1	Swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
DATA MOVES					
MOV A, Rr	F<8 + r>	1/1	Move register contents to A	(A)←(Rr)	r = 0 to 7
MOV A, @Rr	Fr	1/1	Move RAM data addressed by Rr, to A	(A)←((Rr))	r = 0, 1
MOV A, #data	23 data	2/2	Move immediate data to A	(A)←data	
MOV Rr, A	A<8 + r>	1/1	Move Accumulator contents to register	(Rr)←(A)	r = 0 to 7
MOV@Rr, A	Ar	1/1	Move Accumulator contents to RAM location addressed by Rr	((Rr))←(A)	r = 0, 1
MOV Rr, #data	B<8 + r> data	2/2	Move immediate data to Rr	(Rr)←data	r = 0 to 7
MOV @Rr, #data	Br data	2/2	Move immediate data to RAM location addressed by Rr	((R0))←data	r = 0, 1
XCH A, Rr	2<8 + r>	1/1	Exchange A contents with Rr	(A)↔(Rr)	r = 0 to 7
XCH A, @Rr	2r	1/1	Exchange Accumulator contents with RAM data addressed by Rr	(A)↔((Rr))	r = 0, 1
XCHD A, @Rr	3r	1/1	Exchange lower nibbles of A and RAM data addressed by Rr	(A_{0-3})↔((Rr_{0-3}))	r = 0, 1
MOV A, PSW	C7	1/1	Move PSW contents to Accumulator	(A)←(PSW)	
MOV PSW, A(3)	D7	1/1	Move Accumulator bit 3 to PSW_3 (PS)	(PS)←(A_3)	
MOV P A, @A	A3	1/2	Move indirectly addressed data in current page to A	(PC_{0-7})←(A), (A)←((PC))	
CARRY FLAG					
CLR C(2)	97	1/1	Clear carry bit	(C)←0	
CPL C(2)	A7	1/1	Complement carry bit	(C)←NOT(C)	
REGISTER					
INC Rr	1<8 + r>	1/1	Increment register by 1	(Rr)←(Rr) + 1	r = 0 to 7
INC @Rr	1r	1/1	Increment RAM data, addressed by Rr, by 1	((Rr))←((Rr)) + 1	r = 0,1
DEC Rr	C<8 + r>	1/1	Decrement register by 1	(Rr)←(Rr) – 1	r = 0 to 7
DEC @Rr	Cr	1/1	Decrement RAM data addressed by Rr, by 1	((Rr))←((Rr)) – 1	r = 0, 1

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
BRANCH					
JMP addr	<2n>4 addr	2/2	Unconditional jump within a 2 kbyte bank	$(PC_{8-10})\leftarrow n$ $(PC_{0-7})\leftarrow addr$ $(PC_{11-12})\leftarrow$ (MBFF0-1)	n = 0 to 7
JMPP @A	B3	1/2	Indirect jump within a page	$(PC_{0-7})\leftarrow((A))$	
DJZN Rr, addr	E<8 + r> addr	2/2	Decrement Rr by 1 and jump if not zero to addr	$(Rr)\leftarrow(Rr)-1$; if (Rr) not zero, then $(PC_{0-7})\leftarrow addr$	r = 0 to 7
DJNZ @Rr, addr	Er	2/2	Decrement RAM data, addressed by Rr, by 1 and jump if not zero to addr	$((Rr))\leftarrow((Rr))-1$; if ((Rr)) not zero, then $(PC_{0-7})\leftarrow addr$	r = 0 to 1
JBb addr	<2b + 1> 2 addr	2/2	Jump to addr if Accumulator bit b = 1	If $(A_b) = 1$, then $(PC_{0-7})\leftarrow addr$	b = 0 to 7
JC addr	F6 addr	2/2	Jump to addr if C = 1	If (C) = 1, then $(PC_{0-7})\leftarrow addr$	
JNC addr	E6 addr	2/2	Jump to addr if C = 0	If (C) = 0, then $(PC_{0-7})\leftarrow addr$	
JZ addr	C6 addr	2/2	Jump to addr if A = 0	If (A) = 0, $(PC_{0-7})\leftarrow addr$	
JNZ addr	96 addr	2/2	Jump to addr if A is NOT zero	If $(A) \neq 0$, then $(PC_{0-7})\leftarrow addr$	
JT0 addr	36 addr	2/2	Jump to addr if T0 = 1	If T0 = 1, then $(PC_{0-7})\leftarrow addr$	
JNT0 addr	26 addr	2/2	Jump to addr if T0 = 0	If T0 = 0, then $(PC_{0-7})\leftarrow addr$	
JT1 addr	56 addr	2/2	Jump to addr if T1 = 1	If T1 = 1, then $(PC_{0-7})\leftarrow addr$	
JNT1 addr	46 addr	2/2	Jump to addr if T1 = 0	If T0 = 0, then $(PC_{0-7})\leftarrow addr$	
JTF addr[4]	16 addr	2/2	Jump to addr if Timer Flag = 1	If TF = 1, then $(PC_{0-7})\leftarrow addr$	
JNTF addr[4]	06 addr	2/2	Jump to addr if Timer Flag = 0	If T0 = 0, then $(PC_{0-7})\leftarrow addr$	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
TIMER/EVENT COUNTER					
MOV A,T	42	1/1	Move timer/event counter contents to A	(A)←(T)	
MOV T, A	62	1/1	Move A contents to timer/event counter	(T)←(A)	
STRT CNT	45	1/1	Start event counter		
STRT T	55	1/1	Start timer		
STOP TCNT	65	1/1	Stop timer/event counter		
EN TCNTI	25	1/1	Enable timer/event counter interrupt		
DIS TCNTI	35	1/1	Disable timer/event counter interrupt		
CONTROL					
EN I	05	1/1	Enable external (chip enable) interrupt		
DIS I	15	1/1	Disable external (chip enable) interrupt		
SEL RB0[5]	C5	1/1	Select Register Bank 0	(RBS)←0	
SEL RB1[5]	D5	1/1	Select Register Bank 1	(RBS)←1	
SEL MB0[10]	E5	1/1	Select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
SEL MB1[10]	F5	1/1	Select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
SEL MB2[10]	A5	1/1	Select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
SEL MB3[10]	B5	1/1	Select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
STOP	22	1/1	Enter Stop mode		
IDLE	01	1/1	Enter Idle mode		
SUBROUTINE					
CALL addr[6]	<2n + 1> 4addr	2/2	Jump to subroutine	((SP))←(PC) ($PSW_{4,6,7}$), (SP)←(SP) + 1, (PC_{8-10})←n, (PC_{0-7})←addr, (PC_{11-12}) ←(MBFF0-1)	n = 0 to 7
RET[6]	83	1/2	Return from subroutine	(SP)←(SP) – 1, (PC)←((SP))	
RETR[6]	93	1/2	Return from interrupt and restore bits 4, 6 and 7 of PSW	(SP)←(SP) – 1, ($PSW_{4,6,7}$) + (PC)←((SP))	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
PARALLEL INPUT/OUTPUT					
IN A, P0	08	1/2	Input Port 0 data to Accumulator	(A)←(P0)	
IN A, P1	09	1/2	Input Port 1 data to Accumulator	(A)←(P1)	
IN A, P2[7]	0A	1/2	Input Port 2 data to Accumulator	(A)←(P2)	
OUTL P0, A	38	1/2	Output A data to Port 0	(P0)←(A)	
OUTL P1, A	39	1/2	Output A data to Port 1	(P1)←(A)	
OUTL P2, A	3A	1/2	Output A data to Port 2	(P2)←(A)	
ANL P0, #data	98 data	2/2	AND Port 0 data with immediate data	(P0)←(P0) AND data	
ANL P1, #data	99 data	2/2	AND Port 1 data with immediate data	(P1)←(P1) AND data	
ANL P2, #data	9A data	2/2	AND Port 2 data with immediate data	(P2)←(P2) AND data	
ORL P0, #data	88 data	2/2	OR Port 0 data with immediate data	(P0)←(P0) OR data	
ORL P1, #data	89 data	2/2	OR Port 1 data with immediate data	(P1)←(P1) OR data	
ORL P2, #data	8A data	2/2	OR Port 2 data with immediate data	(P2)←(P2) OR data	
DERIVATIVE INPUT/OUTPUT					
MOV A, Dx[8]	8C direct	2/2	Move derivative register contents to A	(A)←(Dx)	x = 0 to 255
MOV Dx, A[8]	8D direct	2/2	Move A contents to derivative register	(Dx)←(A)	x = 0 to 255
ANL Dx, A[8]	8E direct	2/2	AND derivative register with A	(Dx)←(Dx) AND (A)	x = 0 to 255
ORL Dx, A[8]	8F direct	2/2	OR derivative register with A	(Dx)←(Dx) OR (A)	x = 0 to 255
SERIAL INPUT/OUTPUT					
MOV A, S0	0C	1/2	Move serial I/O register 0 contents to A	(A)←(S0)	
MOV A, S1[9]	0D	1/2	Move serial I/O register 1 contents to A	(A)←(S1)	
MOV S0, A	3C	1/2	Move A contents to serial I/O register 0	(S0)←(A)	
MOV S1, A[9]	3D	1/2	Move A contents to serial I/O register 1	(S1)←(A)	
MOV S2, A	3E	1/2	Move A contents to serial I/O register 2	(S2)←(A)	
MOV S0, #data	9C data	2/2	Move immediate data to serial I/O register 0	(S0)←data	
MOV S1, #data[9]	9D data	2/2	Move immediate data to serial I/O register 1	(S1)←data	
MOV S2, #data	9E data	2/2	Move immediate data to serial I/O register 2	(S2)←data	
EN SI	85	1/1	Enable serial I/O interrupt		
DIS SI	95	1/1	Disable serial I/O interrupt		
NOP	00	1/1	No operation	$(PC_{0\text{-}10})\leftarrow (PC_{0\text{-}10}) + 1$	

Notes to Table 8.

1. PSW CY, AC affected.
2. PSW CY affected.
3. PSW PS affected.
4. Execution of a JTF or JNTF instruction resets the Timer Flag (TF).
5. PSW RBS affected.
6. PSW SP_0, SP_1 and SP_2, affected.
7. (A) = 0000, P2.3, P2.2, P2.1 and P2.0.
8. For more information on the derivative I/O instructions of a particular microcontroller, consult the specific microcontroller data sheet.
9. (S1) has a different meaning for read and write operations. See Section 6.11.4.
10. SEL MB instructions may not be used within interrupt routines.

Table 9 Definitions of symbols used in Table 8.

SYMBOL	DESCRIPTION
A	Accumulator
AC	auxiliary (half) carry
addr	program memory address
Bb	bit designation (b = 0 to 7)
CE/T0	CE/T0 input
CY	carry bit
Dx	mnemonic derivative register
data	8-bit number or expression
MB0	program memory bank 0
MB1	program memory bank 1
MB2	program memory bank 2
MB3	program memory bank 3
MBFF0	memory bank flip-flop 0
MBFF1	memory bank flip-flop 1
PC	Program Counter
PS	timer prescaler select
PSW	Program Status Word
RB0	Register Bank 0
RB1	Register Bank 1
RBS	Register Bank Select
Rr	register designation (r = 0 to 7)
SPn	Stack Pointer (n = 0, 1 or 2)
T	Timer 1
T1	T1 input
TF	Timer Flag
x	derivative register address (x = 0 to 255)
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with
#	immediate data prefix
@	indirect address prefix
*	hexadecimal; 8...F selects R0...R7
&	hexadecimal; 0, 2, 4, 6, 8, A, C, E selects page 0...7 in JMP, i.e. $(PC_{8\text{-}10}) \leftarrow \&_{1\text{-}3}$
%	hexadecimal; 1, 3, 5, 7, 9, B, D, F selects page 0...7 in CALL, i.e. $(PC_{8\text{-}10}) \leftarrow \&_{1\text{-}3}$ selects bit b = 0...7 in JBb, i.e. $b = \&_{1\text{-}3}$

7.1 Instruction map

first hexadecimal character of opcode — second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, #data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	IN A,Pp 1	IN A,Pp 2		MOV A,Sn 0	MOV A,Sn 1		
1	INC @ Rr 0	INC @ Rr 1	JB0 addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	INC Rr 1	INC Rr 2	INC Rr 3	INC Rr 4	INC Rr 5	INC Rr 6	INC Rr 7
2	XCH A, @Rr 0	XCH A, @Rr 1	STOP	MOV A, #data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr 0	XCH A,Rr 1	XCH A,Rr 2	XCH A,Rr 3	XCH A,Rr 4	XCH A,Rr 5	XCH A,Rr 6	XCH A,Rr 7
3	XCHD A, @Rr 0	XCHD A, @Rr 1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	OUTL Pp,A 1	OUTL Pp,A 2		MOV Sn,A 0	MOV Sn,A 1	MOV Sn,A 2	
4	ORL A, @Rr 0	ORL A, @Rr 1	MOV A, T	ORL A, #data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	ORL A,Rr 1	ORL A,Rr 2	ORL A,Rr 3	ORL A,Rr 4	ORL A,Rr 5	ORL A,Rr 6	ORL A,Rr 7
5	ANL A, @Rr 0	ANL A, @Rr 1	JB2 addr	ANL A, #data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0	ANL A,Rr 1	ANL A,Rr 2	ANL A,Rr 3	ANL A,Rr 4	ANL A,Rr 5	ANL A,Rr 6	ANL A,Rr 7
6	ADD A, @Rr 0	ADD A, @Rr 1	MOV T, A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	ADD A,Rr 1	ADD A,Rr 2	ADD A,Rr 3	ADD A,Rr 4	ADD A,Rr 5	ADD A,Rr 6	ADD A,Rr 7
7	ADDC A, @Rr 0	ADDC A, @Rr 1	JB3 addr		CALL page 3			RR A	ADDC A,Rr 0	ADDC A,Rr 1	ADDC A,Rr 2	ADDC A,Rr 3	ADDC A,Rr 4	ADDC A,Rr 5	ADDC A,Rr 6	ADDC A,Rr 7
8				RET	JMP page 4	EN SI			ORL Pp,#data 0	ORL Pp,#data 1	ORL Pp,#data 2		MOV A,Dx	MOV Dx,A	ANL Dx,A	ORL Dx,A
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data 0	ANL Pp,#data 1	ANL Pp,#data 2		MOV Sn,#data 0	MOV Sn,#data 1	MOV Sn,#data 2	
A	MOV @ Rr,A 0	MOV @ Rr,A 1		MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0	MOV Rr,A 1	MOV Rr,A 2	MOV Rr,A 3	MOV Rr,A 4	MOV Rr,A 5	MOV Rr,A 6	MOV Rr,A 7
B	MOV @Rr, #data 0	MOV @Rr, #data 1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data 0	MOV Rr,#data 1	MOV Rr,#data 2	MOV Rr,#data 3	MOV Rr,#data 4	MOV Rr,#data 5	MOV Rr,#data 6	MOV Rr,#data 7
C	DEC @Rr 0	DEC @Rr 1			JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr 0	DEC Rr 1	DEC Rr 2	DEC Rr 3	DEC Rr 4	DEC Rr 5	DEC Rr 6	DEC Rr 7
D	XRL A, @Rr 0	XRL A, @Rr 1	JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr 0	XRL A,Rr 1	XRL A,Rr 2	XRL A,Rr 3	XRL A,Rr 4	XRL A,Rr 5	XRL A,Rr 6	XRL A,Rr 7
E	DJNZ @ Rr,addr 0	DJNZ @ Rr,addr 1			JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr,addr 0	DJNZ Rr,addr 1	DJNZ Rr,addr 2	DJNZ Rr,addr 3	DJNZ Rr,addr 4	DJNZ Rr,addr 5	DJNZ Rr,addr 6	DJNZ Rr,addr 7
F	MOV A, @Rr 0	MOV A, @Rr 1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	MOV A,Rr 1	MOV A,Rr 2	MOV A,Rr 3	MOV A,Rr 4	MOV A,Rr 5	MOV A,Rr 6	MOV A,Rr 7

MBA281

8-bit microcontroller with on-chip DTMF generator

PCD3755A

CONTENTS

8-bit microcontroller with on-chip DTMF generator

PCD3755A

1 INTRODUCTION

This data sheet details the specific properties of the PCD3755A. The shared characteristics of the PCD3755A are described in the PCD33XXA family data sheet, which should be read in conjunction with this publication.

2 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM, I/O in a 28-lead package
- 8 kbyte user-programmable ROM (one-time programmable)
- 128 bytes RAM
- 128 bytes EEPROM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines (for the implemented port options, see Section 8.2)
- 8-bit programmable timer/event counter 1
- 8-bit reloadable timer 2
- 3 single-level vectored interrupts:
  - external
  - 8-bit programmable timer/event counter 1
  - derivative (triggered by reloadable timer 2)
- Two test inputs, one of which also serves as the external interrupt input
- Dual Tone Multi-Frequency (DTMF) tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (*"CEPT T/CS46"* compatible)
- Melody output for ringer application
- Power-on reset
- Stop and Idle modes
- Logic supply voltage: V_{DD} = 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency 1 to 16 MHz (3.58 MHz for DTMF advised)
- Operating temperature range: −25 to +70 °C
- Manufactured in silicon gate CMOS process.

3 GENERAL DESCRIPTION

The PCD3755A is a microcontroller oriented towards telephony applications. It includes an on-chip Dual Tone Multi-Frequency (DTMF) generator. In addition to dialling, the generated frequencies can be made available as square-waves on Port line P1.7/MDY for melody generation, providing ringer operation. The PCD3755A also incorporates 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM), permitting data storage without battery backup. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3755AP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3755AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

5 BLOCK DIAGRAM

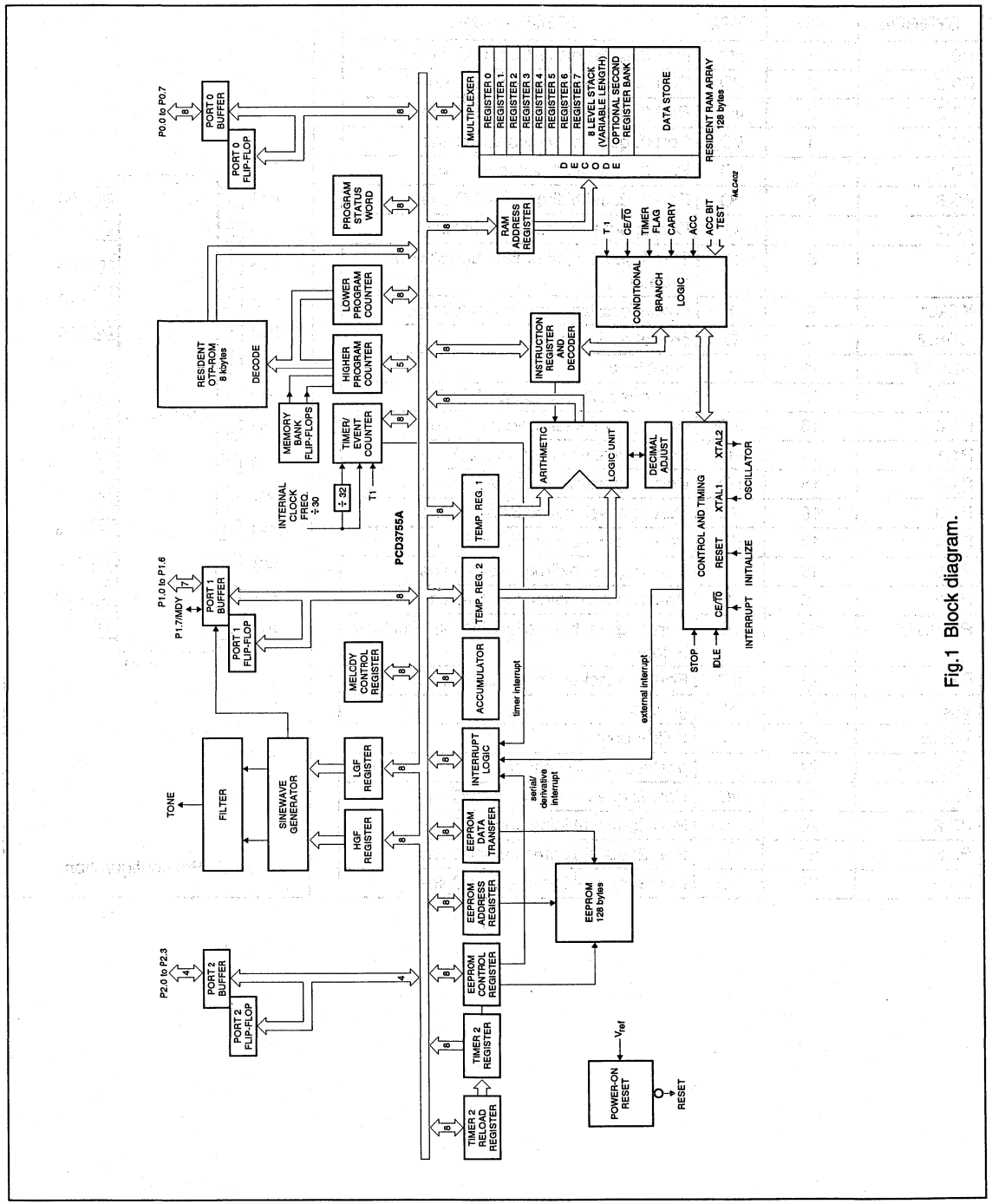


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
P0.1	1	I/O	Port 0; quasi-bidirectional I/O line
P0.2	2	I/O	Port 0; quasi-bidirectional I/O line
P0.3	3	I/O	Port 0; quasi-bidirectional I/O line
P0.4	4	I/O	Port 0; quasi-bidirectional I/O line
P0.5	5	I/O	Port 0; quasi-bidirectional I/O line
P0.6	6	I/O	Port 0; quasi-bidirectional I/O line
P0.7	7	O	Port 0; quasi-bidirectional I/O line
T1	8	T1	Test 1/count input of 8-bit timer/event counter 1
XTAL1	9	I	crystal oscillator/external clock input
XTAL2	10	O	crystal oscillator output
RESET	11	I	reset input
CE/$\overline{T0}$	12	I	chip enable/test 0 (active LOW)
P1.0	13	I/O	Port 1; quasi-bidirectional I/O line
P1.1	14	I/O	Port 1; quasi-bidirectional I/O line
P1.2	15	I/O	Port 1; quasi-bidirectional I/O line
P1.3	16	I/O	Port 1; quasi-bidirectional I/O line
P1.4	17	I/O	Port 1; quasi-bidirectional I/O line
P1.5	18	I/O	Port 1; quasi-bidirectional I/O line
P1.6	19	I/O	Port 1; quasi-bidirectional I/O line
P1.7/MDY	20	I/O	Port 1; quasi-bidirectional I/O line/melody output
P2.0	21	I/O	Port 2; quasi-bidirectional I/O line
V_{SS}	22	P	ground
TONE	23	O	DTMF output
V_{DD}	24	P	positive supply voltage
P2.1	25	I/O	Port 2; quasi-bidirectional I/O line
P2.2	26	I/O	Port 2; quasi-bidirectional I/O line
P2.3	27	I/O	Port 2; quasi-bidirectional I/O line
P0.0	28	I/O	Port 2; quasi-bidirectional I/O line

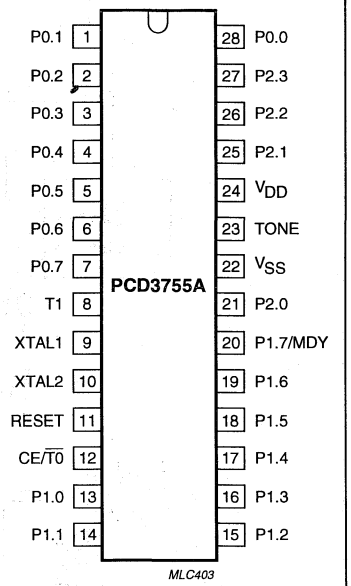


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Parallel ports

All standard quasi-bidirectional I/O ports are available.

- Port 0; parallel port of 8 lines (P0.0 to P0.7)
- Port 1; parallel port of 8 lines (P1.0 to P1.7)
- Port 2; parallel port of 4 lines (P2.0 to P2.3).

One line of Port 1 is shared with the square-wave melody (MDY) output derived from the DTMF generator (P1.7/MDY). If this alternative function is not employed, P1.7/MDY may serve as a general purpose port line. This occurs if the following condition is fulfilled; see melody control register (Table 7) for symbols.

P1.7/MDY is a general purpose port line if EMO = 0, i.e. if the melody output is not used.

Port configuration PCD3755A: see Section 8.2.

7.2 Frequency generator section

A versatile frequency generator section is provided (Fig.3). If used as intended, a 3.58 MHz quartz crystal or PXE resonator will be chosen in the application. The frequency generator includes precision circuitry for Dual Tone Multi-Frequency (DTMF) signals, which is typically used for tone dialling in telephone sets.

The tone output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits per second.

Besides DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available. Their frequencies are provided either in purely sinusoidal form on the tone output (TONE) or as a square-wave on line P1.7/MDY. The latter is typically used for ringer applications in telephone sets.

If no tones are generated, the tone output (TONE) is in a three-state mode.

7.2.1 Frequency generator derivative registers

Table 1 summarizes the derivative addresses, the register mnemonics and the access types of the frequency generator section.

Table 1 Derivative addresses of the frequency generator section

Dx ADDRESS (HEX)	TYPE	MNEMONIC	DESCRIPTION
11	W	HGF	high group frequency register
12	W	LGF	low group frequency register
13	R/W	MDYCON	melody control register

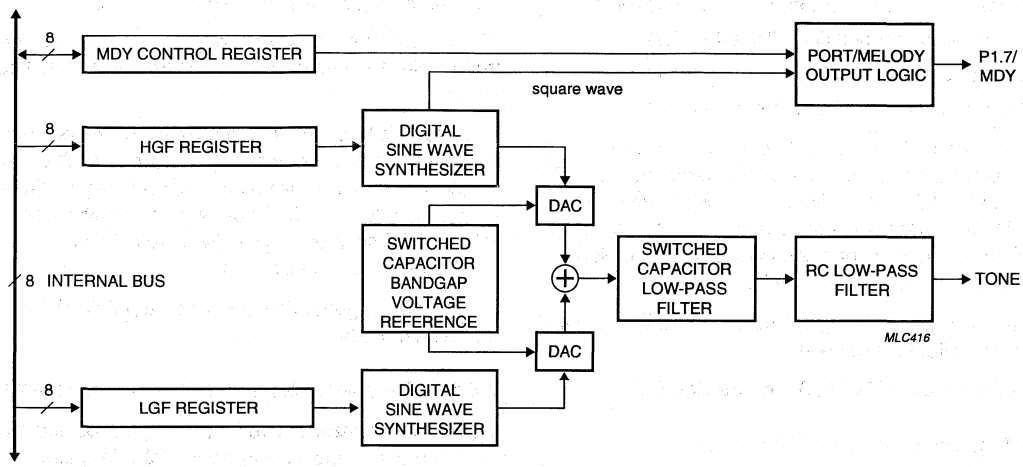


Fig.3 Block diagram of the frequency generator section.

7.2.2 Frequency registers

The two frequency registers define two frequencies. From these, the digital sine wave synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature. The amplitude of the low group frequency sine wave is attenuated by 2 dB compared to the amplitude of the high group frequency sine wave.

The two sine waves are summed and then filtered by on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the *"CEPT CS203"* recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00 H, the whole frequency generator is shut off, resulting in lower power consumption. A value of x ($60 \leq x \leq 255$) in a frequency register yields a digital sine wave signal with a frequency: $f = \frac{f_{xtal}}{23\,(x+2)}$.

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

7.2.3 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.579545 MHz, the DTMF standard frequencies can be implemented (Table 2). The relationship between the telephone keyboard symbols and the frequency register contents are given in Table 3.

Table 2 DTMF standard frequencies and their implementation

STANDARD FREQUENCY (Hz)	x-value (HEX)	GENERATED FREQUENCY (Hz)	FREQUENCY DEVIATION	
			(%)	(Hz)
697	DD	697.90	0.13	0.90
770	C8	770.46	0.06	0.46
852	B5	850.45	−0.18	−1.55
941	A3	943.23	0.24	2.23
1209	7F	1206.45	−0.21	−2.55
1336	72	1341.66	0.42	5.66
1477	67	1482.21	0.35	5.21
1633	5D	1638.24	0.32	5.24

Table 3 Dialling symbols, corresponding DTMF frequency pairs and frequency register contents

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQUENCY PAIRS (Hz)	LGF CONTENTS (HEX)	HGF CONTENTS (HEX)
0	941/1336	A3	72
1	697/1209	DD	7F
2	697/1336	DD	72
3	697/1447	DD	67
4	770/1209	C8	7F
5	770/1336	C8	72
6	770/1447	C8	67
7	852/1209	B5	7F
8	852/1336	B5	72
9	852/1477	B5	67
A	697/1633	DD	5D
B	770/1633	C8	5D
C	852/1633	B5	5D
D	941/1633	A3	5D
*	941/1209	A3	7F
#	941/1477	A3	67

7.2.4 MODEM FREQUENCIES

Again assuming an oscillator frequency f_{xtal} = 3.579545 MHz, the standard modem frequency pairs summarized in Table 4 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling low-group frequency generation.

Table 4 Standard modem frequency pairs and their implementation

MODEM FREQUENCY (Hz)	STANDARD	HGF CONTENT (HEX)	GENERATED FREQUENCY (Hz)	FREQUENCY DEVIATION	
				(%)	(Hz)
980	V.21	9D	978.82	–0.12	–1.18
1180	V.21	82	1179.03	–0.08	–0.97
1070	Bell 103	8F	1073.33	0.31	3.33
1270	Bell 103	79	1265.30	–0.37	–4.70
1200	Bell 202	80	1197.17	–0.24	–2.83
2200	Bell 202	45	2192.01	0.36	–7.99
1300	V.23	67	1296.94	–0.24	–3.06
2100	V.23	48	2103.14	0.15	3.14
1650	V.21	5C	1655.66	0.34	5.66
1850	V.21	52	1852.77	0.15	2.77
2025	Bell 103	4B	2021.20	–0.19	–3.80
2225	Bell 103	44	2223.32	–0.08	–1.68

7.2.5 MUSICAL SCALE FREQUENCIES

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.579545 MHz (Table 5). It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling low group frequency generation.

Table 5 Musical scale frequencies and their implementation

STANDARD SCALE[1]	STANDARD FREQUENCY (Hz)	HGF (HEX)	GENERATED FREQUENCY (Hz)
D # 5	622.3	F8	622.5
E5	659.3	EA	659.5
F5	698.5	DD	697.9
F # 5	740.0	D0	741.1
G5	784.0	C5	782.1
G # 5	830.6	B9	832.3
A5	880.0	AF	879.3
A # 5	923.3	A5	931.9
B5	987.8	9C	985.0
C6	1046.5	93	1044.5
C # 6	1108.7	8A	1111.7
D6	1174.7	82	1179.0
D # 6	1244.5	7B	1245.1
E6	1318.5	74	1318.9
F6	1396.9	6D	1402.1
F # 6	1480.0	67	1482.2
G6	1568.0	61	1572.0
G # 6	1661.2	5C	1655.7
A6	1760.0	56	1768.5
A # 6	1864.7	51	1875.1
B6	1975.5	4D	1970.0
C7	2093.0	48	2103.1
C # 7	2217.5	44	2223.3
D7	2349.3	40	2358.1
D # 7	2489.0	3D	2470.4

Note

1. Standard scale based on A4 at 440 Hz.

7.3 Melody organization

7.3.1 MELODY OUTPUT

If bit EMO = 1 in the melody control register, a square-wave with the frequency defined by the HGF contents is output on line P1.7/MDY. The square-wave has a duty cycle of $^{12}/_{23}$ = 52%. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the logic HIGH state.

The melody output is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications. Being a square-wave, the signal will include the attenuated harmonics of the base frequency.

The HGF contents may be determined from Table 5. However, even higher frequency standards may be produced since the limitation $60 \leq x \leq 255$ is relaxed to $2 \leq x \leq 255$ in this application. Due to the low-pass filters, the simultaneous signal on the tone output is not useful for $x < 60$.

EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs!

7.3.2 MELODY CONTROL REGISTER

The 8-bit melody control register defines the behaviour of the melody output. It can be read or written. Note that bits 1 to 7 are fixed at zero (see Table 6).

Table 7 summarizes the significance of the EMO control bit.

Table 6 The 8-bit melody control register

BIT POSITION							
7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
0	0	0	0	0	0	0	EMO[3]

Table 7 Significance of the EMO control register bit

BIT	NAME	DESCRIPTION
EMO	enable melody output	EMO = 0: P1.7/MDY is port line with standard output drive (1 R) EMO = 1: P1.7/MDY is melody output with push-pull output drive

7.4 EEPROM organization

7.4.1 EEPROM MEMORY AND 8-BIT TIMER 2

The PCD3755A includes 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). Such non-volatile storage provides data retention without battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequent numbers. More generally, EEPROM may be used for customizing microcomputers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM relies on the fact that a bit in EEPROM, once written to a one, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase access complements the read and write accesses in an EEPROM.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses take 5 ms each. To make these operations more efficient, several provisions are available in the PCD3755A. First, the EEPROM array is structured into 32 four-byte pages (Fig.4) permitting access to four bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes. Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (timer 2) with reload register is provided. Besides for EEPROM timing, timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

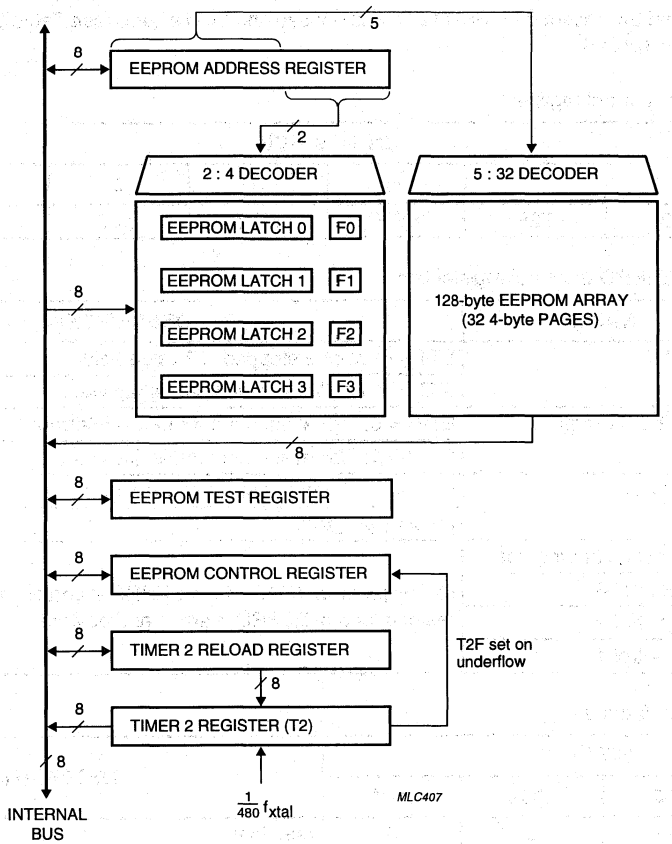


Fig.4 Block diagram of the EEPROM and timer 2 section.

7.4.2 EEPROM CONTROL REGISTER

The behaviour of the EEPROM and timer 2 section is defined by the 8-bit EEPROM Control Register (EPCR). It can be read or written. The Least Significant Bit (LSB) of EPCR is unused and fixed at zero (see Table 8). The EEPROM control register bits are given in Table 9.

Table 8 The EEPROM control register

BIT POSITION							
7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 9 Overview of EEPROM control register bits

BIT	NAME	DESCRIPTION
STT2	start T2	STT = 0; timer 2 stopped, T2 value held
		STT = 1; T2 decrements from reload value
ET2I	enable T2 interrupt	ET21 = 0; T2F event cannot request interrupt
		ET21 = 1; T2F event can request interrupt
T2F	timer 2 flag	set: when T2 underflow (or by program)
		reset by program
EWP	erase or write in progress	set: by program (EPW starts EEPROM and/or write and timer 2) reset: at end of EEPROM erase and/or write
MC3	mode control 3	
MC2	mode control 2	
MC1	mode control 1	

Table 10 Truth table for Table 9

BIT [1]				DESCRIPTION
EWP	**MC3**	**MC2**	**MC1**	
0	0	0	0	read byte
X	0	0	1	not allowed
0	0	1	0	incremental mode
1	0	1	X	write page
1	1	0	0	erase/write page
X	1	0	1	not allowed
X	1	1	0	not allowed
1	1	1	1	erase page

Note

1. X = don't care.

7.4.3 EEPROM ACCESS

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms. As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of ADDR, defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (Fig.4) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM latches 0 to 3 (Fig.4) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches. ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called page setup, before the actual erase and/or write cycle can be executed. Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.4.4, 7.4.5, 7.4.6 and 7.4.7.

7.4.4 EEPROM ADDRESS REGISTER

The EEPROM Address Register (ADDR) determines the EEPROM location to which an EEPROM access is directed (Table 11). AD2 to AD6 select one of 32 pages.

The two least significant ADDR bits are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM latches 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 10) is active during page set-up, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM latch 3 is reached, i.e. when AD0 and AD1 are both one.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the eight-bit counter wraps around to zero.

7.4.5 EEPROM DATA REGISTER

The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, i.e. from derivative address 03H, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, i.e. to derivative address 03H, loads data into the EEPROM latch (Fig.4) defined by bits AD0 and AD1 of ADDR.

Table 11 EEPROM address register

BIT POSITION							
7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

7.4.6 EEPROM LATCHES

The four EEPROM latches 0 to 3 cannot be read by user software (Fig.4). Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.4.7 EEPROM FLAGS

The four EEPROM flags F0 to F3 cannot be directly accessed by user software (Fig.4). An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4.8 EEPROM TEST REGISTER

The EEPROM Test register (TST), finally, is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.4.9 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles. As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM latches 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect. Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR.

Table 12 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 10) must be selected. Auto-incrementing stops at EEPROM latch 3. It is not mandatory to start at EEPROM latch 0 as in Table 13.

Table 13 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send it to ADDR
MOV A, R0	load 1st byte from register 0
MOV DATR, A	send 1st byte to EEPROM latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM latch 1
MOV A, R2	load 3rd byte from register 2
MOV DATR, A	send 3rd byte to EEPROM latch 2
MOV A, R3	load 4th byte from register 3
MOV DATR, A	send 4th byte to EEPROM latch 3

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle. In the following, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

7.4.10 EEPROM MACROS

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. Particularly, a new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading EWP in the EPCR.

For write, erase and erase/write cycles, it is assumed that the timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 18). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a timer 2 interrupt provided that ET2I = 1 and that the SIO/derivative interrupt is enabled.

7.4.11 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 14 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.4.12 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.4.9. The actual transfer to the EEPROM is then performed as shown in Table 15.

Table 15 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

The last instruction also starts timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM latch 0 (by AD0 and AD1). This allows efficient coding of multi-page write operations.

7.4.13 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.4.9. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

Table 16 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

The last instruction also starts timer 2. Erasure takes 5 ms upon which timer register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of erase/write page.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

7.4.14 ERASE PAGE

The EEPROM flags are set as described in Section 7.4.9. The corresponding page bytes are erased.

Table 17 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

The last instruction also starts timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'. Note that ADDR does not auto-increment after an erase cycle.

7.4.15 8-BIT TIMER

The 8-bit timer 2 is a down-counter decremented at a rate of $1/480 f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.4.16 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $1/480 f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 18 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

Table 18 Required reload values for EEPROM erase and write cycles at various oscillator frequencies

f_{xtal} (MHz)	RELOAD VALUE[1] (HEX)
1	0A
2	14
3.58	25
6	3E
10	68
16	A6

Note

1. The reload value is: $(5 \text{ ms} \times 1/480 f_{xtal}) - 1$.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

7.4.17 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, timer 2 is started by setting STT2. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while timer 2 is operating.

7.4.18 DERIVATIVE INTERRUPTS

Since the PCD3755A includes no serial I/O interface, the SIO/derivative interrupt (see *"PCD33XXA family data sheet"*) reduces to a derivative interrupt. One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 11 and 18).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The SIO/derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

7.4.19 TIMING

Although the PCD3755A operates over a clock frequency range from 1 MHz to 16 MHz, $f_{xtal} = 3.579545$ MHz will usually be chosen to take full advantage of the frequency generator section.

7.4.20 RESET

In addition to the conditions given in the *"PCD33XXA family data sheet"*, all derivative registers are cleared in the reset state.

7.4.21 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

7.4.22 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

It is absolutely **not permitted** to enter stop mode while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero! The timer 2 section is frozen during stop mode. After exit from stop mode by a HIGH level on CE/$\overline{T0}$, timer 2 proceeds from the held state.

8 INSTRUCTION SET RESTRICTIONS

Since no serial I/O interface is provided, the serial input/output instructions are not available except EN SI and DIS SI, which enable, respectively, disable the derivative interrupt.

As RAM space is restricted to 128 bytes, care should be taken to avoid accesses to non-existing RAM locations.

Table 19 Summary of derivative addresses and control registers

Dx ADDRESS (HEX)	TYPE	MNEMONIC (see Fig.5)	DESCRIPTION
00	–	–	not used
01	R/W	ADDR	EEPROM address register
02	–	–	not used
03	R/W	DATR	EEPROM data register
04	R/W	EPCR	EEPROM control register
05	R/W	RELR	timer 2 reload register
06	R	T2	timer 2 register
07	R/W	TST	test register
08	–	–	not used
10	–	–	not used
11	W	HGF	high group frequency register
12	W	LGF	low group frequency register
13	R/W	MDYCON	melody control register
14	–	–	not used
FF	–	–	not used

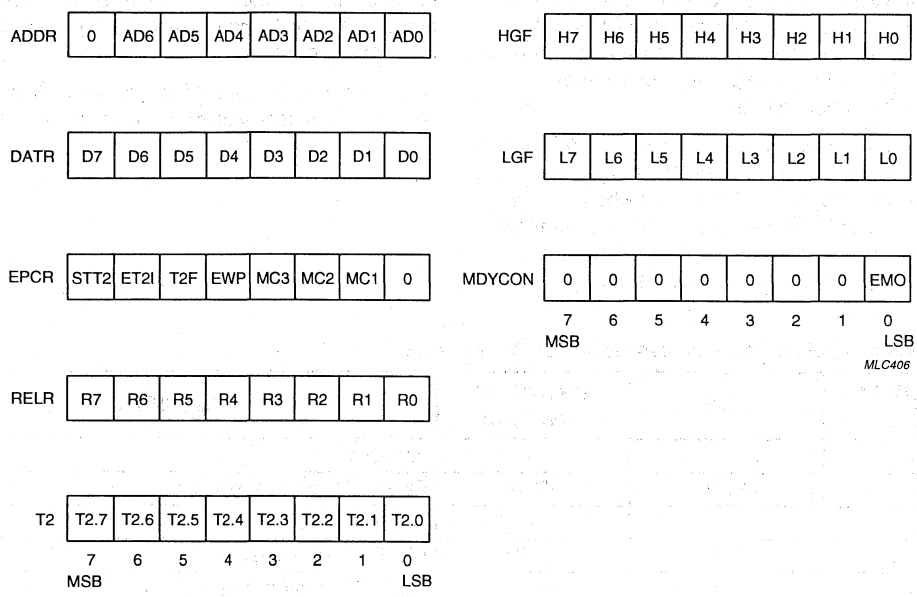


Fig.5 Control registers.

8.1 User-programmable ROM (OTP)

8.1.1 PROGRAM/DATA

Any mix of instructions and data up to ROM size of 8 kbytes. The user-programmable ROM can be programmed with the OM5007 OTP adapter board and a conventional EPROM programmer (please refer to separate *"PCD33XXA family development tools data sheet"*).

8.2 Configuration

Table 20 Port output drive and state after reset

Power-on reset reference: 1.3 V; oscillator: g_{mL}.

PORT	STATE	PORT	STATE	PORT	STATE	PORT	STATE	PORT	STATE
P0.0	1S	P0.4	1S	P1.0	1S	P1.4	1S	P2.0	2S
P0.1	1S	P0.5	1S	P1.1	1S	P1.5	1S	P2.1	2S
P0.2	1S	P0.6	1S	P1.2	1S	P1.6	1R	P2.2	2S
P0.3	1S	P0.7	1S	P1.3	1S	P1.7	1R	P2.3'	2S

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−1.0	+10	mA
I_O	DC output current	−1.0	+10	mA
I_{SS}	ground supply current	−5.0	+50	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	−	90	°C

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

11 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V (note 1); V_{SS} = 0 V; T_{amb} = −25 °C to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.579545 MHz (g_{mL}); $R_X \leq 100\ \Omega$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	operating supply voltage	see note 1; Fig.6	1.8	−	6.0	V
		RAM data retention in stop mode	1.0	−	6.0	V
I_{DD}	operating supply current	see note 2; Figs 8 and 9				
		V_{DD} = 3 V; HGF ≠ 0 and/or LGF ≠ 0	−	0.8	1.6	mA
		V_{DD} = 3 V; HGF = LGF = 0	−	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL}); HGF = LGF = 0	−	1.5	4.0	mA
$I_{DD(ID)}$	idle mode supply current	see note 2; Figs 10 and 11				
		V_{DD} = 3 V; HGF ≠ 0 and/or LGF ≠ 0	−	0.7	1.4	mA
		V_{DD} = 3 V; HGF = LGF = 0	−	0.25	0.5	mA
		V_{DD} 5 V; f_{xtal} = 10 MHz (g_{mL}); HGF = LGF = 0	−	1.1	3.4	mA
$I_{DD(ST)}$	stop mode supply current	see notes 2 and 3; Fig.7				
		V_{DD} 1.8 V; T_{amb} = 25 °C	−	2.8	5.5	µA
		V_{DD} 1.8 V; T_{amb} = 70 °C	−	−	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	µA
Port outputs						
I_{OL}	LOW level port output sink current	V_{DD} = 3 V; V_O = 0.4 V; see Fig.12	0.7	3.5	–	mA
I_{OH}	HIGH level port output pull-up source current	V_{DD} = 3 V; V_O = 2.7 V; see Fig.13	–10	–30	–	µA
		V_{DD} = 3 V; V_O = 0 V; see Fig.13	–	–140	–300	µA
I_{OH}	HIGH level port output push-pull source current	V_{DD} = 3 V; V_O = 2.6 V; see Fig.14	–0.7	–3.5	–	mA
Tone output; see notes 1 and 4; Fig.16						
$V_{HG(rms)}$	HGF voltage (RMS value)		158	181	205	mV
$V_{LG(rms)}$	LGF voltage (RMS value)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; see note 5	–	–2.5	–	dB
EEPROM; see notes 1, 6 and 7						
$CY_{t/w}$	endurance (erase/write cycles)		100000	–	–	
t_{ret}	data retention time		10	–	–	years
Power-on reset level						
V_{POR}	output voltage		0.8	1.3	1.8	V
Oscillator						
g_{mL}	LOW transconductance	V_{DD} = 5 V; see Fig.15	0.2	0.4	1.0	S
R_F	feedback resistance		0.3	1.0	3.0	MΩ

Notes

1. Tone output, EEPROM erase and EEPROM write require $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, open-drain outputs connected to V_{SS}, all other outputs open-circuit. Maximum values: external clock at XTAL1 and XTAL2 open-circuit. Typical values: 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$; RESET, T1 and CE/$\overline{T0}$ at V_{SS}; crystal connected between XTAL1 and XTAL2; open-drain outputs connected to V_{SS}; all other outputs open-circuit.
4. Values are specified for DTMF frequencies only (CEPT CS203).
5. Related to the Low Group Frequency (LGF) component (CEPT CS203).
6. Verified on sampling basis.
7. After final testing the value of each EEPROM bit is logic HIGH, but this cannot be guaranteed after board assembly.

12 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to 70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	see note 1	–	30	–	ns
t_f	fall time all outputs	see note 1	–	30	–	ns
f_{xtal}	clock frequency	see Fig.6	1	–	16	MHz

Note

1. V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF.

13 PROGRAMMING CHARACTERISTICS (see note 1 and Fig.17)

SYMBOL	TIMING PARAMETER	FIGURE	MIN.	MAX.	UNIT
Timing					
t_{AL}	address low byte strobe	18, 20	0.5	–	µs
t_{AH}	address high byte strobe	18, 20	0.5	–	µs
t_{WR}	write prom strobe	18	0.5	–	µs
t_{RDY}	write in progress	18	tbf	tbf	
t_{PC}	precharge strobe	18, 20	0.5	–	µs
t_d	precharge delay	18, 20	0.5	–	µs
t_{PP}	program pulse width	18	tbf	tbf	
$t_{PP(nom)}$	nominal program pulse width	18	tbf	tbf	
t_{ACL}	read access time low voltage	18	tbf	tbf	
Voltages					
V_{prg}	programming voltage	18	tbf	tbf	V
V_{test1}	program mode test 1 voltage	18, 20	tbf	tbf	V
V_{test2}	program mode test 2 voltage	–	tbf	tbf	V
$V_{prg(ext)}$	external program voltage	–	tbf	tbf	V
V_{DD}	supply voltage	–	tbf	tbf	V
$V_{DD(V)}$	supply voltage during verify	–	tbf	tbf	V
$V_{DD(prg)}$	supply voltage during program	–	tbf	tbf	V

Note

1. Available programmers:
   a) CEIBO MP-51 (OM4260).
   b) Adaptor for PCD3755A (OM5026).

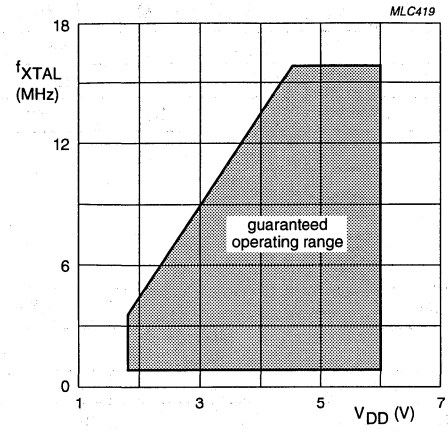


Fig.6 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

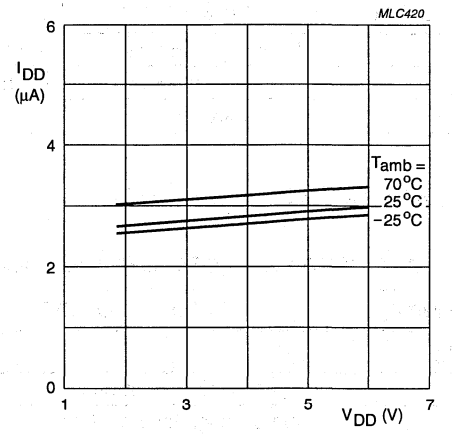
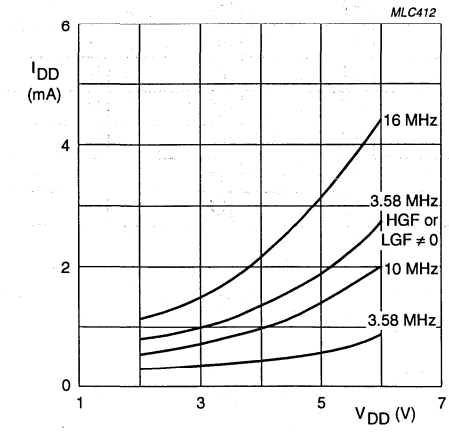
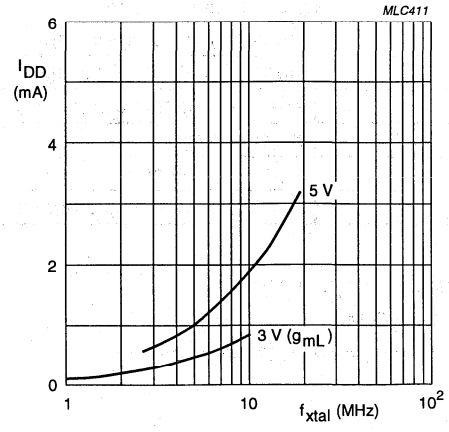


Fig.7 Typical supply current (I_{DD}) in stop mode as a function of supply voltage (V_{DD}).



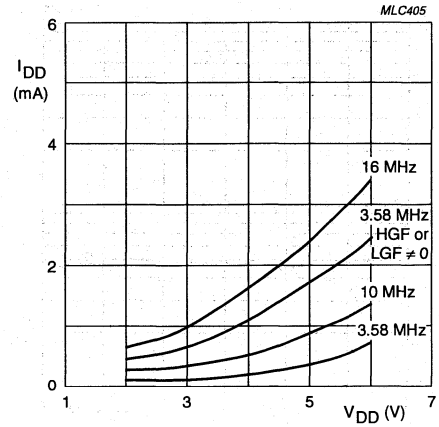
Measured with crystal between XTAL1 and XTAL2.

Fig.8 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



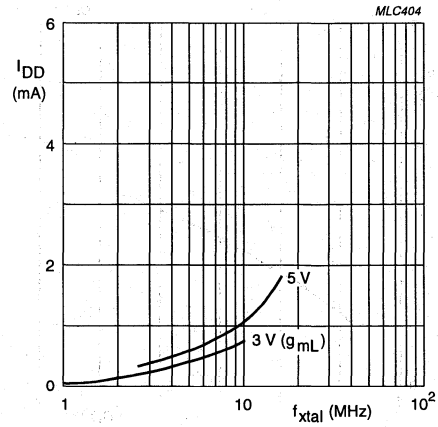
Measured with function generator on XTAL1.

Fig.9 Typical operating supply current (I_{DD}) as a function of crystal frequency (f_{xtal}).



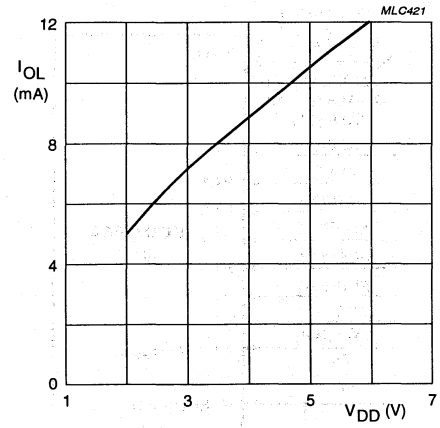
Measured with crystal between XTAL1 and XTAL2.

Fig.10 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.11 Typical supply current (I_{DD}) during Idle mode as a function of crystal frequency (f_{xtal}).



V_O = 0.4 V.

Fig.12 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

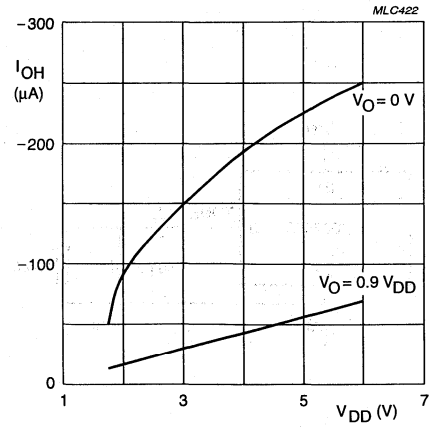
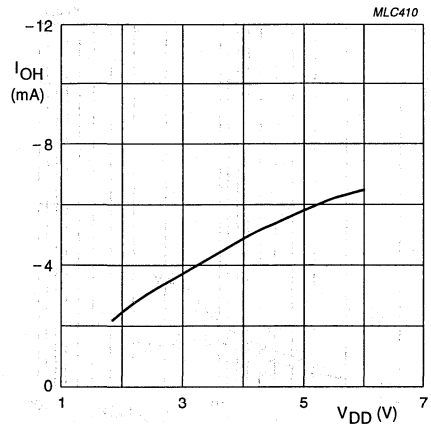
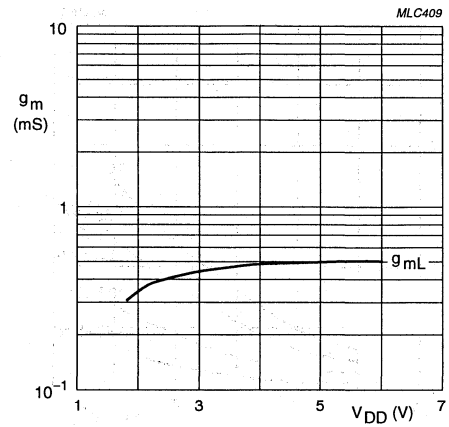


Fig.13 Typical HIGH level port output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = -0.4$ V.

Fig.14 Typical HIGH level port output push-pull source current (I_{OH}) as a function of supply voltage (V_{DD}).



For the options: g_{mL}, g_{mM} and g_{mH}.

Fig.15 Typical transconductance values as a function of supply voltage (V_{DD}).

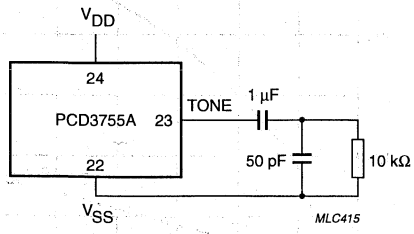


Fig.16 Tone output test circuit.

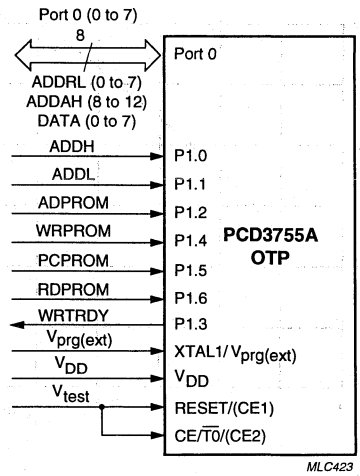
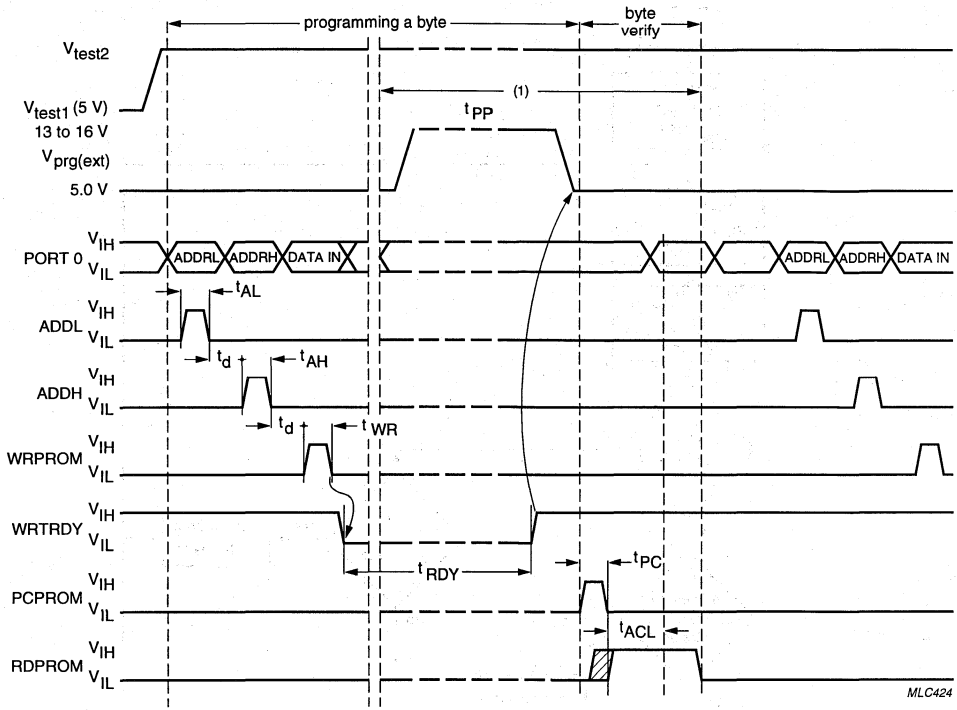


Fig.17 Programming interface.



(1) See flowchart Fig.19.

Fig.18 OTP programming timing.

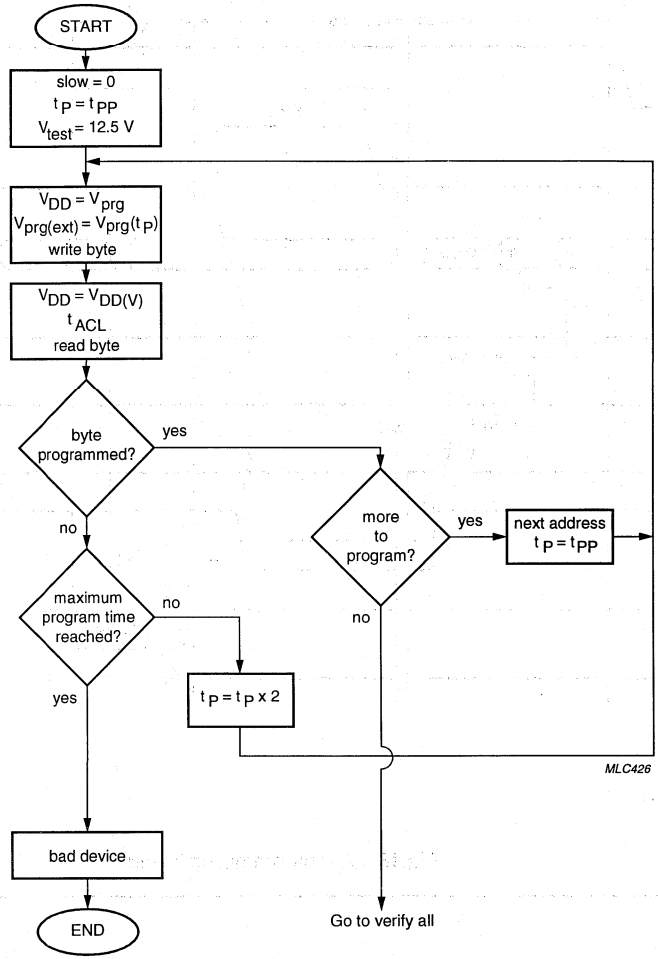


Fig.19 Programming flowchart.

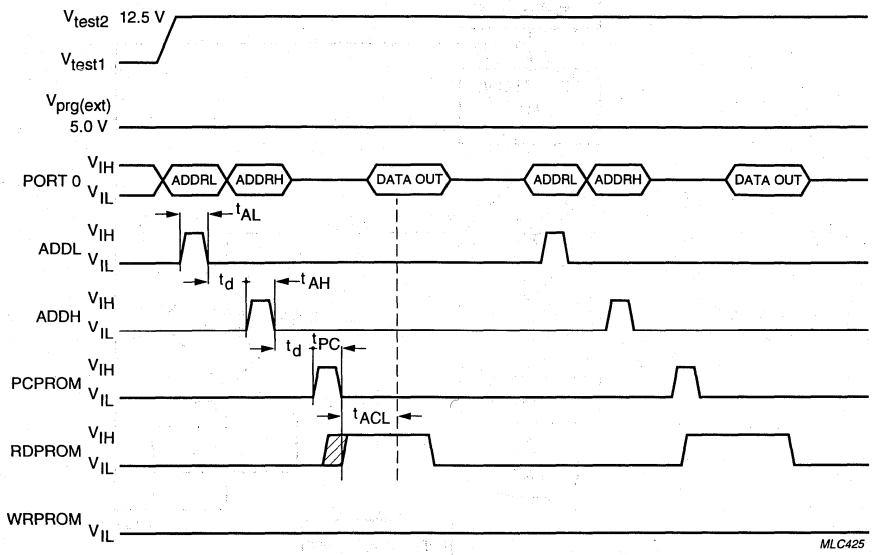


Fig.20 OTP verification timing.

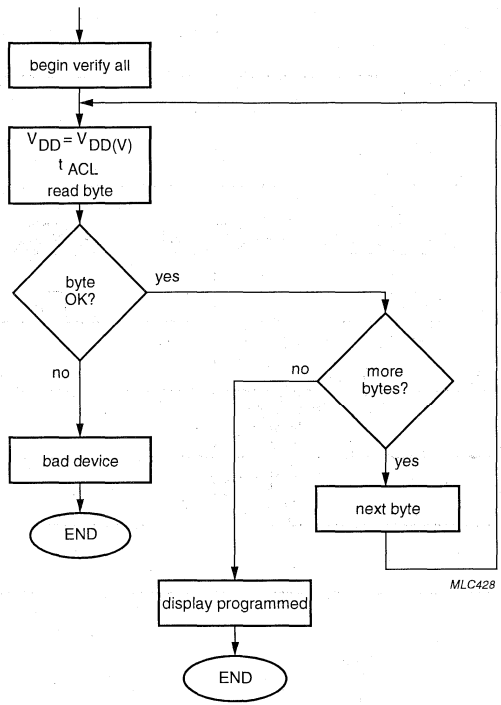


Fig.21 Verify flowchart.

Analog Voice Scrambler/Descrambler

PCD4440T

FEATURES

- Scrambler or descrambler function
- Scrambling in frequency domain
- Selectable split frequency (up to 10 selections per second)
- Telephony-band filtering included
- No increase in bandwidth
- No external components required
- Small signal delay
- Insensitive to distortion and group delay of transmission channel
- Control via serial (I^2C) bus
- Low transfer loss of speech
- Mute option
- Transparent mode
- High signal input impedance
- Low signal output impedance
- Low power consumption

APPLICATIONS

- Cordless telephones
- Security telephones
- Portable phones
- PMR

GENERAL DESCRIPTION

The PCD4440 is a silicon gate CMOS integrated circuit intended to be used in radio, mobile- and line powered telecommunications products utilizing a microcontroller for the control functions. Analog scrambling/descrambling is based on the split frequency method realized in a sophisticated switched-capacitor technology. The PCD4440 is compatible with most microcontrollers and communicates via a two line bidirectional bus (I^2C).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD4440T	8	mini-pack	plastic	SOT176C

BLOCK DIAGRAM

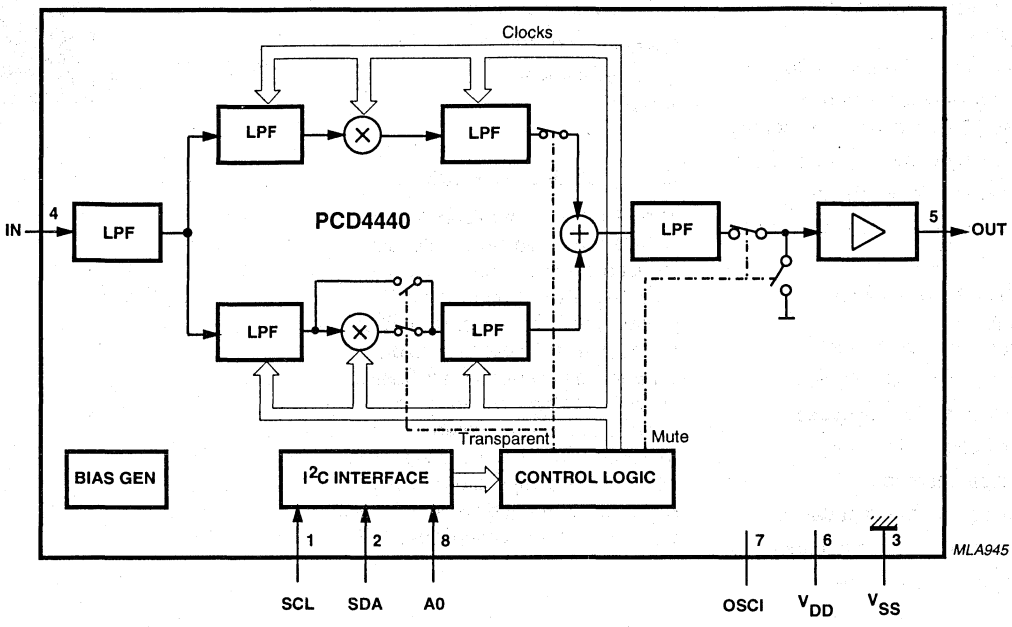


Fig.1 Block diagram.

Analog Voice Scrambler/Descrambler

PCD4440T

PINNING

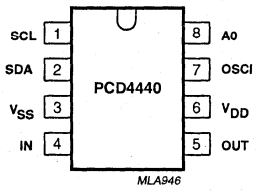


Fig.2 Pin configuration.

Pin Description

SYMBOL	PIN	FUNCTION
SCL	1	serial clock line (I^2C)
SDA	2	serial data line (I^2C)
V_{SS}	3	negative Supply
IN	4	signal input
OUT	5	signal output
V_{DD}	6	positive supply
OSCI	7	oscillator input
A0	8	slave address input (I^2C)

FUNCTIONAL DESCRIPTION

To provide privacy for the end user of a cordless telephone set, the radio-link audio signal must be scrambled. In the microphone and the incoming telephone line audio path a scrambler circuit has to be implemented. Consequently the audio signal to the telephone line and to the earpiece must be descrambled. Both functions can be fulfilled by the PCD4440 by simply inserting it in the audio path.

The PCD4440 accomplishes this task by first filtering the incoming signal, limiting the bandwidth to 3500 Hz. Then the signal is split into a high ($> f_S$) and a low ($< f_S$) frequency band. Both frequency bands are inverted and added again to provide a single output signal.

Values for 9 split frequencies f_S can be controlled by a scramble code table in the microcontroller. Control of these split frequencies is accomplished via the serial two wire I^2C-bus. In addition to the split frequencies (fs), a transparent mode and mute instruction can be selected.

In Fig.3, the signal path for both bands is drawn. The lower band path (on the left side of the diagram) operates on frequencies $f \leq f_S$ (Split Frequency), the upper band path (on the right side) on frequencies $f \geq f_S$.

The input signal contains frequencies from f_1 up to f_2. The output signal is band limited (only in scrambling mode) from f_l (300 Hz) to f_h (3500 Hz). In the left path, the input signal is first limited to f_S. The following modulator inverts the lower band. f_l is folded up to f_S, f_S down to f_l. In general, an input frequency f_{in} is folded to $f_{out} = f_S + f_l - f_{in}$. Finally the folded signal is band limited to f_S again.

In the right path, the input signal is first limited to f_h. The following modulator inverts the upper band. f_S is folded up to f_h, f_h down to f_S. In general, an input frequency f_{in} is folded to $f_{out} = f_S + f_h - f_{in}$. Finally, the folded signal is band limited to f_h again. In the last step, the bands are added and buffered.

In the transparent mode, the input signal is band limited to 3500 Hz. Frequencies form 0 - 300 Hz are not filtered out.

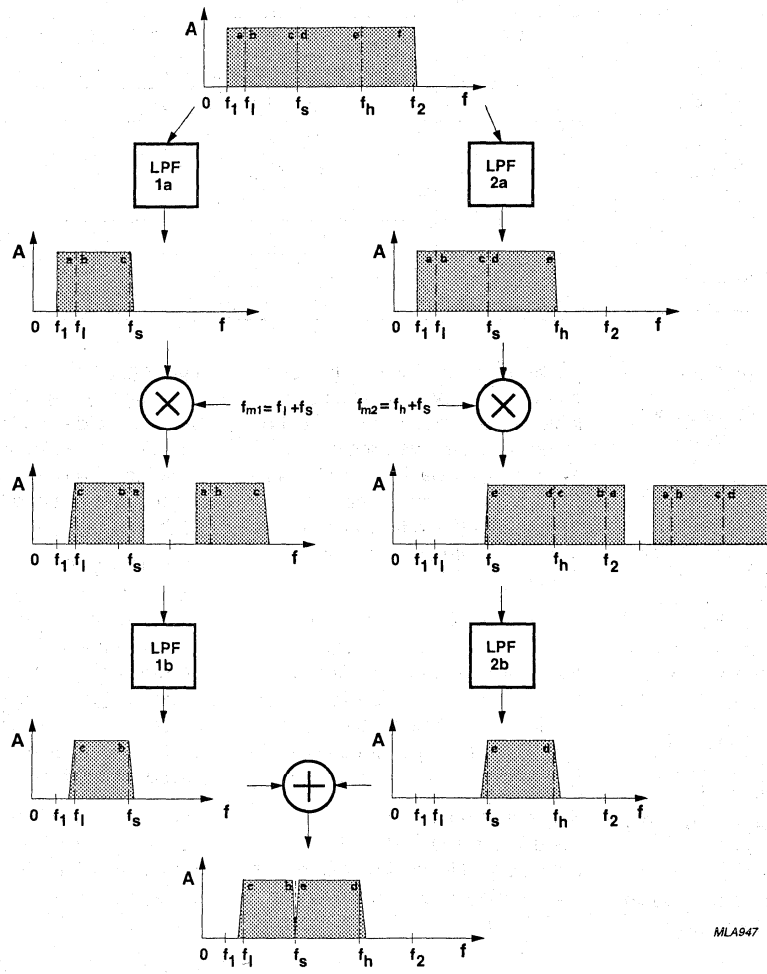


Fig.3 Scrambler signal path.

APPLICATIONS

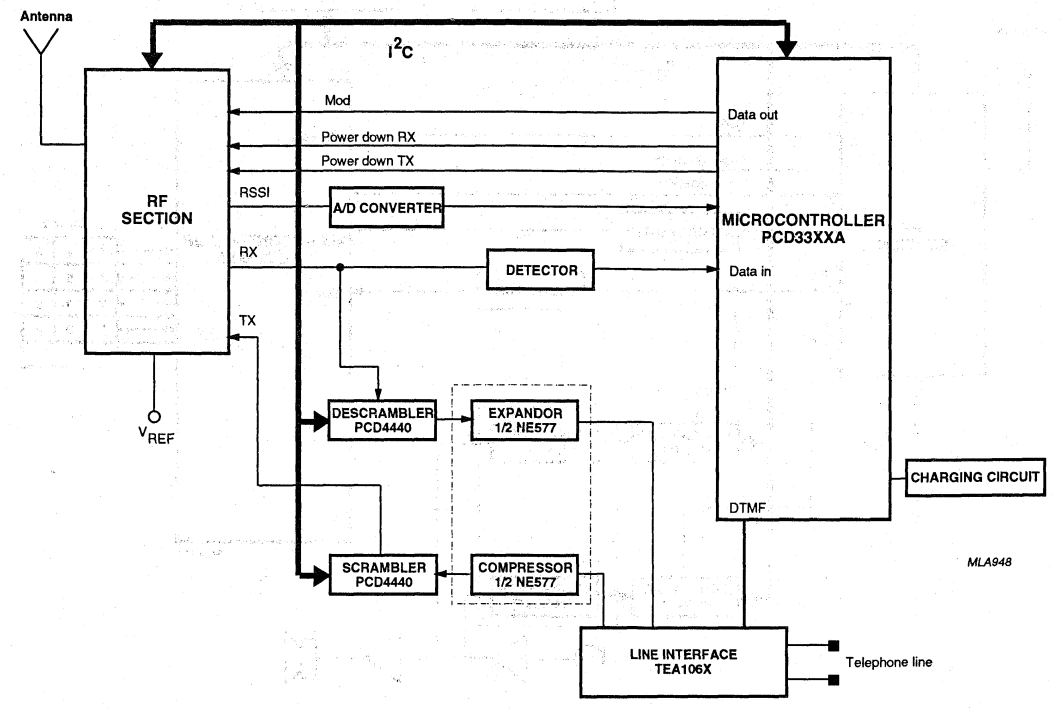


Fig.4 CT0 handset with direct (Manchester code) data system.

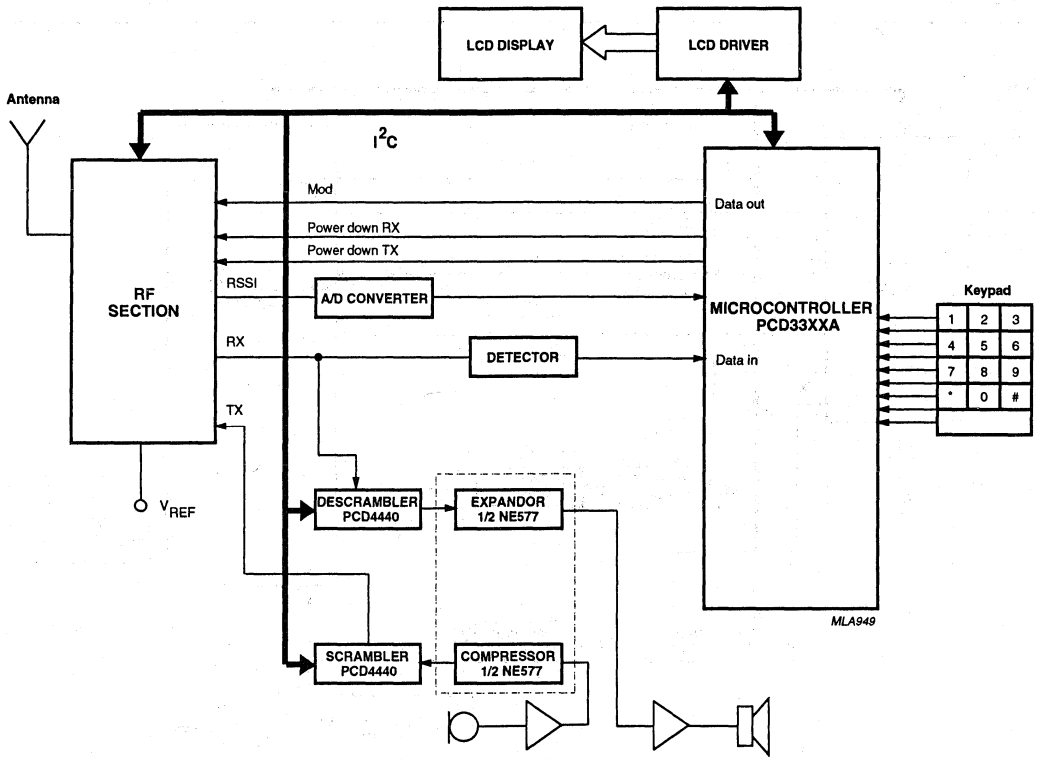


Fig.5 CT0 Base unit with direct (Manchester code) data system.

HANDLING

Handling MOS devices
Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Advanced POCSAG Paging Decoder PCD5003

FEATURES

- Wide operating supply voltage range: 1.5 to 6.0 V
- Low operating current: 50 μA typ. (ON), 25 μA typ. (OFF)
- Temperature range: −25 to +70 °C
- *"CCIR Radio paging Code No. 1"* (POCSAG) compatible
- 512, 1200 and 2400 bits/s data rates using 76.8 kHz crystal
- Built-in data filter (16-times oversampling) and bit clock recovery
- Advanced ACCESS synchronization algorithm
- 2-bit random and (optional) 4-bit burst address error correction
- Up to 6 user addresses (RICs), each with 4 functions/alert cadences
- Up to 6 user address frames, independently programmable
- Standard POCSAG sync word, plus up to 4 user programmable sync words
- Received data inversion (optional)
- Call alert via beeper, vibrator or LED
- 2-level acoustic alert using single external transistor
- Alert control: automatic (POCSAG), via cadence register or alert input pin
- Separate power control of receiver and RF-oscillator for battery economy
- Synthesizer set-up and control interface (3-line serial)
- On-chip EEPROM for storage of user addresses (RICs), pager configuration and synthesizer data
- On-chip SRAM buffer for message data
- Slave I²C-bus interface to microcontroller for transfer of message data, status/control and EEPROM programming
- Wake-up interrupt for microcontroller, programmable polarity
- Direct and I²C-bus control of operating status (ON/OFF)
- Battery-low indication (external detector)
- Out-of-range condition indication
- Real time clock reference output
- On-chip voltage doubler.

APPLICATIONS

- Display pagers, basic alert-only pagers
- Information services
- Personal organizers
- Telepoint
- Telemetry/data transmission.

GENERAL DESCRIPTION

The PCD5003 is a very low power POCSAG decoder and pager controller. It supports data rates of 512, 1200 and 2400 bits/s using a single 76.8 kHz crystal. On-chip EEPROM is programmable at 2.5 V minimum supply. The PCD5003 is Fast I²C-bus compatible (maximum 400 kbits/s).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5003H	TQFP32	plastic thin quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
PCD5003U/10	–	film-frame carrier (naked die) 32 pads	

BLOCK DIAGRAM

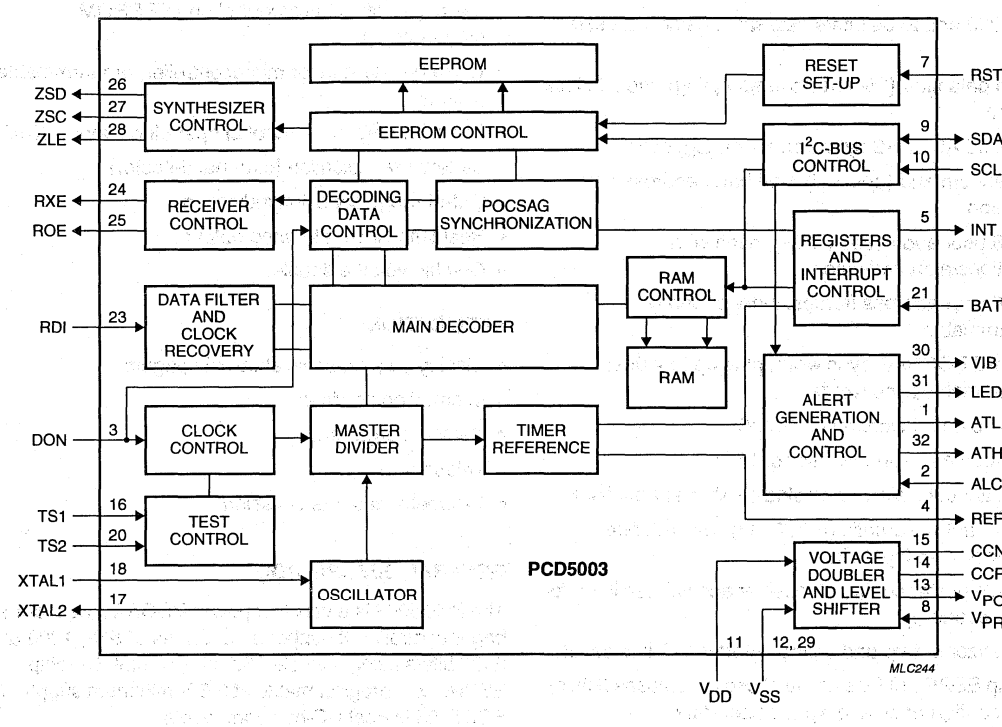


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ATL	1	alert LOW-Level output
ALC	2	alert control input (normally LOW by internal pull-down)
DON	3	direct ON/OFF input (normally LOW by internal pull-down)
REF	4	real time clock frequency reference output
INT	5	interrupt output
n.c.	6	not connected
RST	7	reset input (normally LOW by internal pull-down)
V_{PR}	8	external positive voltage reference input
SDA	9	I^2C-bus serial data input/output
SCL	10	I^2C-bus serial clock input
V_{DD}	11	main positive supply voltage
V_{SS}	12	main negative supply voltage
V_{PO}	13	voltage converter positive output
CCP	14	voltage converter shunt capacitor (positive side)
CCN	15	voltage converter shunt capacitor (negative side)
TS1	16	test input 1 (normally LOW by internal pull-down)
XTAL2	17	decoder crystal oscillator output
XTAL1	18	decoder crystal oscillator input
n.c.	19	not connected
TS2	20	test input 2 (normally LOW by internal pull-down)
BAT	21	battery sense input
n.c.	22	not connected
RDI	23	received POCSAG data input
RXE	24	receiver circuit enable output
ROE	25	receiver oscillator enable output
ZSD	26	synthesizer serial data output
ZSC	27	synthesizer serial clock output
ZLE	28	synthesizer latch enable output
V_{SS}	29	main negative supply voltage
VIB	30	vibrator motor drive output
LED	31	LED drive output
ATH	32	alert HIGH-level output

The PCD5003 is available in a TQFP32 package and as naked die. The pinning for TQFP32 package is shown in Fig.2.

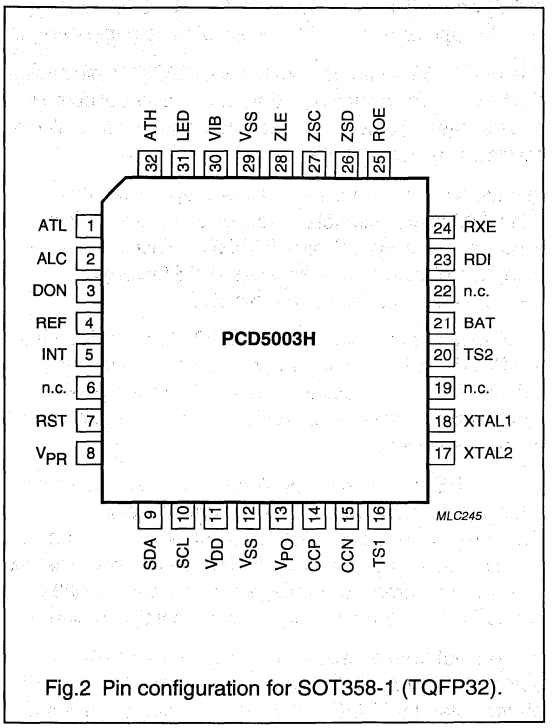


Fig.2 Pin configuration for SOT358-1 (TQFP32).

FUNCTIONAL DESCRIPTION

Introduction

The PCD5003 is a very low power decoder and pager controller specifically designed for use in new generation radio pagers. The architecture of the PCD5003 allows for flexible application in a wide variety of radio pager designs.

The PCD5003 is fully compatible with *"CCIR Radio paging Code No. 1"* (also known as the POCSAG code) operating at data rates of 512, 1200 and 2400 bits/s using a single oscillator crystal of 76.8 kHz.

In addition to the standard POCSAG sync word the PCD5003 is also capable of recognizing up to 4 User Programmable Sync Words (UPSWs). This permits the reception of both private services and POCSAG transmissions via the same radio channel.

Used together with the Philips UAA2080 Paging Receiver, the PCD5003 offers a highly sophisticated, miniature solution for the radiopaging market. Control of an RF synthesizer circuit is also provided to ease alignment and channel selection.

On-chip EEPROM provides storage for user addresses (Receiver Identity Codes or RICs) and Special Programmed Functions (SPFs), which eliminates the need for external storage devices and interconnection. The low EEPROM programming voltage makes the PCD5003 well-suited for 'over-the-air' programming/reprogramming.

On request from an external controlling device or automatically (by SPF programming), the PCD5003 will provide standard POCSAG alert cadences by driving a standard acoustic 'beeper'. Non-standard alert cadences may be generated via a cadence register or a dedicated control input.

Via external bipolar transistors the PCD5003 can also produce a HIGH-level acoustic alert as well as drive an LED indicator and a vibrator motor.

The PCD5003 contains a low-power, high-efficiency voltage converter (doubler) designed to provide a higher voltage supply to LCD drivers or microcontrollers. In addition, an independent level shifted interface is provided allowing communication to a microcontroller operating at a higher voltage than the PCD5003.

Interface to such an external device is provided by an I^2C-bus which allows received call identity and message data, data for the programming of the internal EEPROM, alert control and pager status information to be transferred between the devices. Pager status includes features provided by the PCD5003 such as battery-low and out-of-range indications.

A selectable low frequency timing reference is provided for use in real time clock functions.

Data synchronization is achieved by the Philips patented ACCESS® algorithm ensuring that maximum advantage is made of the POCSAG code structure particularly in fading radio signal conditions. The algorithm allows for data synchronization without preamble detection whilst minimizing battery power consumption.

Random and (optional) burst error correction techniques are applied to the received data to optimize on call success rate without deteriorating falsing rate beyond specified POCSAG levels.

When the PCD5003 is used in combination with a microcontroller, communication takes place via an I^2C-bus interface. A dedicated interrupt line minimizes the required microcontroller activity.

The POCSAG paging code

A transmission using the *"CCIR Radio paging Code No. 1"* (POCSAG code) is constructed in accordance with the following rules (see Fig.3).

The transmission is started by sending a **preamble**, consisting of at least 576 continuously alternating bits (10101010...). The preamble is followed by an arbitrary number of batch blocks. Only complete batches are transmitted.

Each **batch** comprises 17 codewords of 32 bits each. The first codeword is a synchronization codeword with a fixed pattern. The **sync** word is followed by 8 frames (0 to 7) of 2 codewords each, containing message information. A codeword in a frame can either be an address, message or idle codeword.

Idle codewords also have a fixed pattern and are used to fill empty frames or separate messages.

Address codewords are identified by an MSB of logic 0 and are coded as shown in Fig.3. A user address or RIC consists of 21 bits. Only the upper 18 bits are encoded in the address codeword (bits 2 to 19).

The lower 3 bits designate the frame number in which the address is transmitted.

Four different **call types** can be distinguished on each user address. The call type is determined by two function bits in the address codeword (bits 20 and 21), as shown in Table 1.

Alert-only calls only consist of a single address codeword. Numeric and alphanumeric calls have message codewords following the address.

Message codewords are identified by an MSB of logic 1 and are coded as shown in Fig.3. The message information is stored in a 20-bit field (bits 2 to 21). The data format is determined by the call type: 4 bits per digit for numeric messages and 7 bits per (ASCII) character for alphanumeric messages.

Each codeword is protected against transmission errors by 10 CRC check bits (bits 22 to 31) and an even-parity bit (bit 32). This permits correction of maximum 2 random errors or up to 3 errors in a burst of 4 bits (a 4-bit burst error) per codeword.

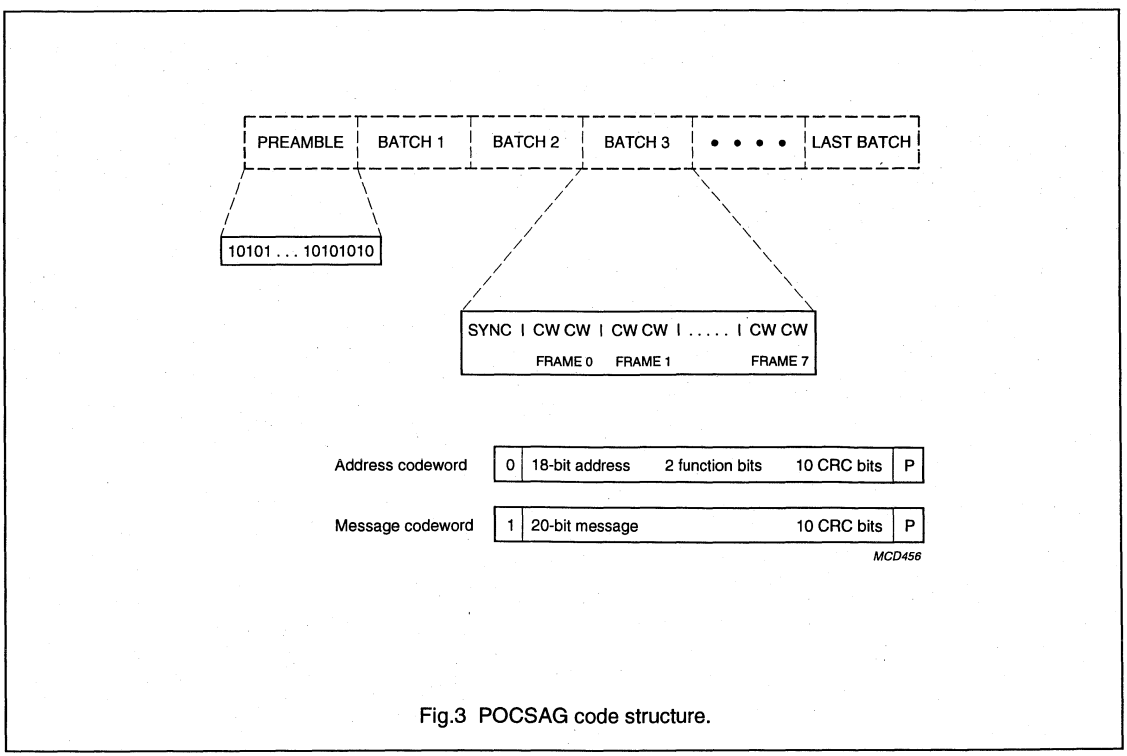


Fig.3 POCSAG code structure.

Table 1 POCSAG call types

BIT 20 (MSB)	BIT 21 (LSB)	CALL TYPE	DATA FORMAT
0	0	numeric	4-bits per digit
0	1	alert-only	–
1	0	alert-only	–
1	1	alphanumeric	7-bits per ASCII character

Error correction

In the PCD5003 error correction methods have been implemented as shown in Table 2.

Random error correction is default for both address and message codewords. In addition, burst error correction can be enabled by SPF programming. Up to 3 erroneous bits in a 4-bit burst can be corrected.

The error correction method used is identified in the message data output to the microcontroller, allowing rejection of calls with too many errors.

Table 2 Error correction

ITEM	DESCRIPTION
Preamble	4 random errors in 31 bits
Synchronization codeword	2 random errors in 32 bits
Address codeword	2 random errors, plus: 4-bit burst errors (optional)
Message codeword	2-bit-random errors, plus: 4-bit burst errors (optional)

Operating states

The PCD5003 has 2 operating states:

- ON status
- OFF status.

The operating state is determined by a Direct Control input (DON) and bit D4 in the control register (see Table 3).

Table 3 Truth table for decoder operating status

DON INPUT	CONTROL BIT D4	OPERATING STATUS
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

ON STATUS

In ON status the decoder pulses the receiver and oscillator enable outputs (respectively RXE and ROE) according to the code structure and the synchronization algorithm. Data received serially at the data input (RDI) is processed for call receipt. Reception of a valid paging call is signalled to the microcontroller by means of an interrupt signal. The received address and message data can then be read via the I^2C-bus interface.

OFF STATUS

In OFF status the decoder will neither activate the receiver or oscillator enable outputs, nor process any data at the data input. The crystal oscillator remains active to permit communication with the microcontroller.

In both operating states an accurate timing reference is available via the REF output. By SPF programming the signal periodicity may be selected as: 32.768 kHz, 50 Hz, 2 Hz or $1/60$ Hz.

Current consumption is reduced by switching off internal decoder sections whenever the receiver is not enabled.

Reset

The decoder can be reset by applying a positive pulse on input pin RST. A power-on reset circuit consisting of an RC network can be connected to this input as well. Conditions during and after a reset are described in Chapter "Operating instructions".

Bit rates

The PCD5003 can be configured for data rates of 512, 1200 or 2400 bit/s by SPF programming. These data rates are derived from a single 76.8 kHz oscillator frequency.

Oscillator

The oscillator circuit is designed to operate at 76.8 kHz. Typically, a tuning fork crystal will be used as a frequency source. Alternatively, an external clock source can be connected to pin XTAL1 only, but a slightly higher oscillator current is consumed.

To allow easy oscillator adjustment (e.g. by means of a variable capacitor) a 32.768 kHz reference frequency can be selected at output REF by SPF programming.

Input data processing

Data input is binary and fully asynchronous. Input bit rates of 512, 1200 and 2400 bits/s are supported. As a programmable option, the polarity of the received data can be inverted before further processing.

The input data is noise filtered by means of a digital filter. Data is sampled at 16 times the data rate and averaged by majority decision.

The filtered data is used to synchronize an internal clock generator by monitoring transitions. The recovered clock phase can be adjusted in steps of $1/8$ or $1/32$ bit period per received bit.

The larger step size is used when bit synchronization has not been achieved, the smaller when a valid data sequence has been detected (e.g. preamble or sync word).

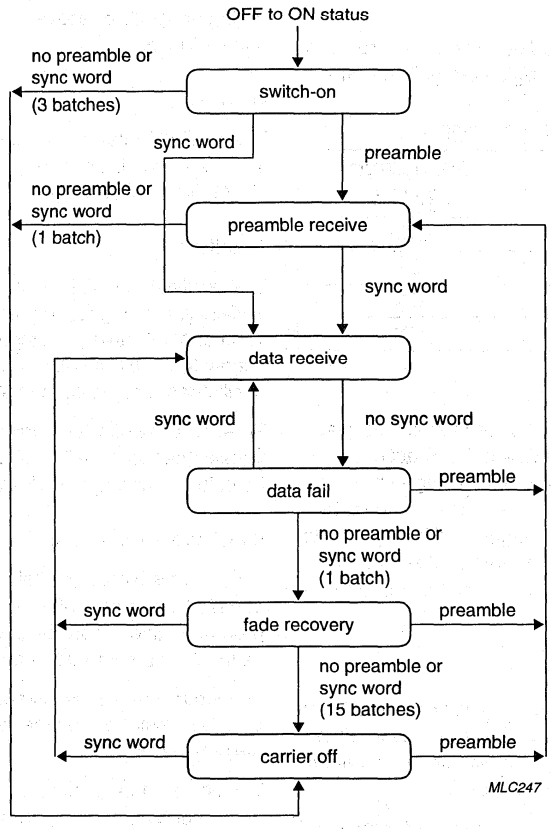


Fig.4 ACCESS® synchronization algorithm.

Synchronization strategy

In ON status the PCD5003 synchronizes to the POCSAG data stream by means of the Philips ACCESS® algorithm. A flow diagram is shown in Fig.4. Where 'sync word' is used, this implies both the standard POCSAG sync word and any enabled User Programmable Sync Word (UPSW).

Several modes of operation can be distinguished depending on the synchronization state. Each mode uses a different method to obtain data synchronization. The Receiver and Oscillator Enable outputs (respectively RXE and ROE) are switched accordingly, with the appropriate establishment times (respectively t_{RXON} and t_{ROON}).

Before comparing received data with preamble, an enabled sync word or programmed user addresses, the appropriate error correction is applied.

Initially, after switching to ON status, the decoder is in **Switch-on** mode. Here the receiver will be enabled for a period up to 3 batches, testing for preamble and sync word. Failure to detect preamble or sync word will cause switching to Carrier Off mode.

Detection of preamble switches to **Preamble Receive** mode, in which sync word is looked for. The receiver will remain enabled while preamble is detected. When neither sync word nor preamble is found within 1 batch duration Carrier Off mode is entered.

Upon detection of a sync word **Data Receive** mode is entered. The receiver is activated only during enabled user address frames and sync word periods. When an enabled user address has been detected, the receiver will be kept enabled for message codeword reception until the call termination criteria are met.

During call reception data bytes are stored in an internal SRAM buffer, capable of storing 2 batches of message data.

Messages are transmitted contiguously, only interrupted by sync words at the beginning of each batch. When a message extends beyond the end of a batch, no testing for sync takes place. Instead, a message data transfer will be initiated by an interrupt to the external controller. Data reception continues normally after a period corresponding to the sync word duration.

If any message codeword is found to be uncorrectable, Data Fail mode is entered and no data transfer will be attempted at the next sync word position. Instead, a test for sync word will be carried out.

In **Data Fail** mode message reception continues normally for 1 batch duration. Upon detection of sync word at the expected position the decoder returns to Data Receive mode. If sync word again fails to appear, batch synchronization is deemed lost. Call reception is then terminated and Fade Recovery mode is entered.

Fade Recovery mode is intended to scan for sync word and preamble over an extended window (nominal position ±8 bits). This is done for a period of up to 15 batches, allowing recovery of synchronization from long fades in the radio signal. Detection of preamble switches to Preamble Receive mode, while sync word detection switches to Data Receive mode. When neither is found within a period of 15 batches, the radio signal is considered lost and Carrier Off mode is entered.

The purpose of **Carrier Off** mode is to detect a valid radio transmission and synchronize to it quickly and efficiently. Because transmissions may start at random, the decoder enables the receiver for 1 codeword in every 18 codewords looking for preamble and sync word. By using a buffer containing 32 bits (n bits from the current scan, 32 – n from the previous scan) effectively every batch bit position can be tested within a continuous transmission of at least 18 batches. Detection of preamble switches to Preamble Receive mode, while sync word detection switches to Data Receive mode.

Call termination

Call reception is terminated:

- Upon reception of any address codeword (including Idle codeword) requiring no more than single bit error correction
- In Data Fail mode, when a sync word is not found at the expected batch position
- When a forced call termination command is received from an external controller.

The latter method permits an external controller to stop call reception depending on the number and type of errors which occurred in a codeword. After a forced call termination the decoder will enter Data Fail mode.

The type of error correction as well as the call termination conditions are indicated by status bits in the message data output.

Following call termination, transfer of the data received since the previous sync word period is initiated by means of an interrupt to the external controller.

Call data output format

POCSAG call information is stored in the decoder SRAM in blocks of 3 bytes per codeword. Each stored call consists of a Call Header, followed by Message Data blocks and concluded by a Call Terminator. In the event of concatenated messages the Call Terminator is replaced with the Call Header of the next message. An alert-only call only has a Call Header and a Call Terminator.

The formats of a Call Header, a Message Data block and a Call Terminator are shown in Tables 4, 6 and 8.

A **Call Header** contains information on the last sync word received, the RIC which began call reception and the type of error correction performed on the address codeword.

A **Message Data** block contains the data bits from a message codeword plus the type of error correction performed. No deformatting is done on the data bits: numeric data appear as 4-bit groups per digit, alphanumeric data have a 7-bit ASCII representation.

The **Call Terminator** contains information on the last sync word received, information on the way the call was terminated (Forced Call Termination command, loss of sync word in Data Fail mode) and the type of error correction performed on the terminating codeword.

Sync word indication

The sync word recognized by the PCD5003 is shown in the Call Header (bits S3 to S1). The decimal value represents the identifier number in the EEPROM of the UPSW in question. A value of 7 indicates the standard POCSAG sync word.

Error type indication

Table 10 shows how the different types of detected errors are encoded in the call data output format.

A message codeword containing more than a single bit error (bit E3 = 1) may appear as an address codeword (bit M1 = 0) after error correction. In this event the codeword is processed as message data and does not cause call termination.

Data transfer

Data transfer is initiated either during sync word periods or as soon as the receiver is disabled after call termination. If the SRAM buffer is full, data transfer is initiated immediately during the next codeword.

When the PCD5003 is ready to transfer received call data an external interrupt will be generated via output INT. Any message data can be read by accessing the RAM output register via the I^2C-bus interface. Bytes will be output starting from the position indicated by the RAM read pointer.

Table 4 Call Header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	S3	S2	S1	R3	R2	R1	DF
2	0	S3	S2	S1	R3	R2	R1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 5 Call Header bit identification

BITS (MSB to LSB)	IDENTIFICATION
S3 to S1	identifier number of sync word for current batch (7 = standard POCSAG)
R3 to R1	identifier number of user address (RIC)
DF	Data Fail mode indication (1 = Data Fail Mode); note 1
F0, F1	function bits of received address codeword (bits 20, 21)
E3 to E1	detected error type; see Table 10; E3 = 0 in a concatenated call header

Note

1. The DF bit in the Call Header is set:
   a) When the sync word of the batch in which the (beginning of the) call was received, did not match the standard POCSAG or a user-programmed sync word. The sync word identifier (bits S3 to S1) will then be made 0.
   b) When any codeword of a previous call received in the same batch was uncorrectable.

Table 6 Message Data format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	M2	M3	M4	M5	M6	M7	M8	M9
2	M10	M11	M12	M13	M14	M15	M16	M17
3	M18	M19	M20	M21	E3	E2	E1	M1

Table 7 Message Data bit identification

BITS (MSB to LSB)	IDENTIFICATION
M2 to M21	Message codeword data bits
E3 to E1	Detected error type; see Table 10
M1	Message codeword flag

Table 8 Call Terminator format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	FT	S3	S2	S1	0	0	0	DF
2	FT	S3	S2	S1	0	0	0	X
3	X	X	F0	F1	E3	E2	E1	0

Table 9 Call Terminator bit identification

BITS (MSB to LSB)	IDENTIFICATION
FT	Forced Call Termination (1 = yes)
S3 to S1	identifier number of last sync word
R3 to R1	identifier number of user address (RIC)
DF	Data Fail mode indication (1 = Data Fail mode); note 1
F0, F1	function bits of received address codeword (bits 20, 21)
E3 to E1	detected error type; see Table 10; E3 = 0 in a call terminator

Note

1. The DF bit in the Call Terminator is set:
   a) When any call data codeword in the terminating batch was uncorrectable, while in Data Receive mode.
   b) When the sync word at the start of the terminating batch did not match the standard POCSAG or a user-programmed sync word, while in Data Fail mode.

Successful call termination occurs by reception of a valid address codeword with less than 2 bit errors.
Unsuccessful termination occurs when sync word is not detected while in Data Fail mode.

It is generally possible to distinguish these two conditions using the sync word identifier number (bits S3 to S1); the identifier number will be non-zero for correct termination, and zero for sync word failure.

Only when a call is received in Data Fail mode and the call is terminated before the end of the batch, is it not possible to distinguish unsuccessful from correct termination.

Reception of message data can be terminated at any time by transmitting a Forced Call Termination command to the Control register via the I^2C-bus. Any call received will then be terminated immediately and Data Fail mode will be entered.

Table 10 Error type identification

E3	E2	E1	ERROR TYPE	NUMBER OF ERRORS
0	0	0	no errors - correct codeword	0
0	0	1	parity bit in error	1
0	1	0	single bit error	1 + parity
0	1	1	single bit error and parity error	1
1	0	0	not used	
1	0	1	4-bit burst error and parity error	3 (e.g.1101)
1	1	0	2-bit random error	2
1	1	1	uncorrectable codeword	3 or more

Receiver and oscillator control

A paging receiver and an RF oscillator circuit can be controlled independently via enable outputs RXE and ROE respectively. Their operating periods are optimized according to the synchronization mode of the decoder. Each enable signal has its own programmable establishment time (see Table 11).

External receiver control and monitoring

An external controller may enable the receiver control outputs continuously via an I²C-bus command, overruling the normal enable pattern. Data reception continues normally. This mode can be left by means of a Reset or an I²C-bus command.

External monitoring of the receiver control output RXE is possible via bit D6 in the Status register, when enabled via the Control register (D2 = 1). Each change of state of output RXE will generate an external interrupt at output INT.

Battery condition input

A logic signal from an external sense circuit signalling battery condition can be applied to the BAT input. This input is sampled each time the receiver is disabled (RXE ↓ 0).

When enabled via the Control register (D2 = 0), the condition of input BAT is reflected in bit D6 of the Status register. Each change of state of bit D6 causes an external interrupt at output INT.

When using the UAA2080 pager receiver a Battery-Low condition corresponds to a logic HIGH-level. With a different sense circuit the reverse polarity can be used as well, because every change of state is signalled to an external controller.

After a reset the initial condition of the Battery-Low indicator in the Status register is zero.

Table 11 Receiver and oscillator establishment times (note 1)

CONTROL OUTPUT	ESTABLISHMENT TIME				UNIT
RXE	5	10	15	30	ms
ROE	20	30	40	50	ms

Note

1. The exact values may differ slightly from the above values, depending on the bit rate (see Table 22).

Synthesizer control

Control of an external frequency synthesizer is possible via a dedicated 3-line serial interface (outputs ZSD, ZSC and ZLE). This interface is common to a number of available synthesizers. The synthesizer is enabled using the oscillator enable output ROE.

The frequency parameters must be programmed in EEPROM. Two blocks of maximum 24 bits each can be stored. Any unused bits must be programmed at the beginning of a block: only the last bits are used by the synthesizer.

Data is transferred to the synthesizer each time the PCD5003 is switched from OFF to ON status. Transfer takes place serially in two blocks, starting with bit 0 (MSB) of block 1 (see Table 25).

Data bits on ZSD change on the falling flanks of ZSC. After clocking all bits into the synthesizer, a latch enable pulse copies the data to the internal divider registers. A timing diagram is given in Fig.5.

The data output timing is synchronous, but has a pause in the bit stream of each block. This pause occurs in the 13th bit while ZSC is LOW. The nominal pause duration t_p depends on the bit rate and is shown in Table 12. The total duration of the 13th bit is given by $t_{ZCL} + t_p$.

A similar pause occurs between the first and the second data block. The delay between the first latch enable pulse and the second data block is given by $t_{ZDL2} + t_p$. The complete start-up timing of the synthesizer interface is given in Fig.12.

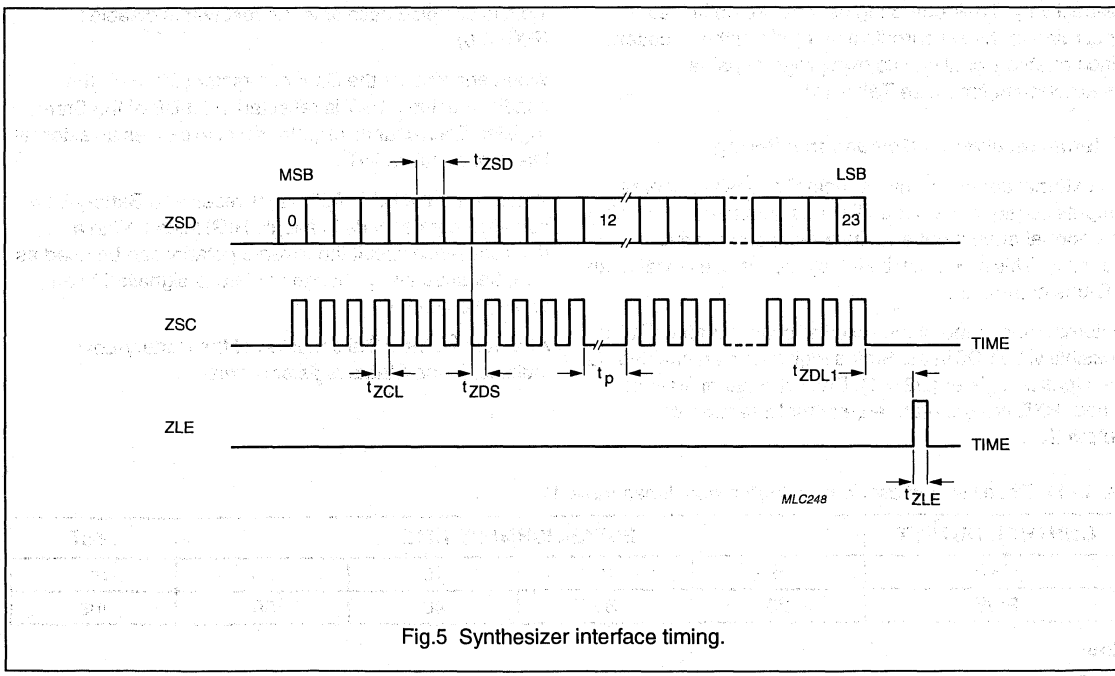


Fig.5 Synthesizer interface timing.

Table 12 Synthesizer programming pause

BIT RATE (bit/s)	t_p (clocks)	t_p (µs)
512	119	1549
1200	33	430
2400	1	13

Serial microcontroller interface

The PCD5003 has an I²C-bus serial microcontroller interface capable of operating at 400 kbits/s. The PCD5003 is a slave transceiver with I²C-bus address 39 Dec (bits A6 to A0 = 0100111).

Data transmission requires 2 lines: SDA (data) and SCL (clock), each with an external pull-up resistor. The clock signal (SCL) for any data transmission must be generated by the external controlling device.

A transmission is initiated by a start condition (S: SCL = 1, SDA = ↓) and terminated by a stop condition (P: SCL = 1, SDA = ↑).

Data bits must be stable when SCL is HIGH. If there are multiple transmissions, the stop condition can be replaced with a new start condition.

Data is transferred on a byte basis, starting with a device address and a read/write indicator. Each transmitted byte must be followed by an Acknowledge bit (ACK: active LOW). If a receiving device is not ready to accept the next complete byte, it can force a bus wait state by holding SCL LOW.

The general I²C-bus transmission format is shown in Fig.6. Formats for master/slave communication are shown in Fig.7.

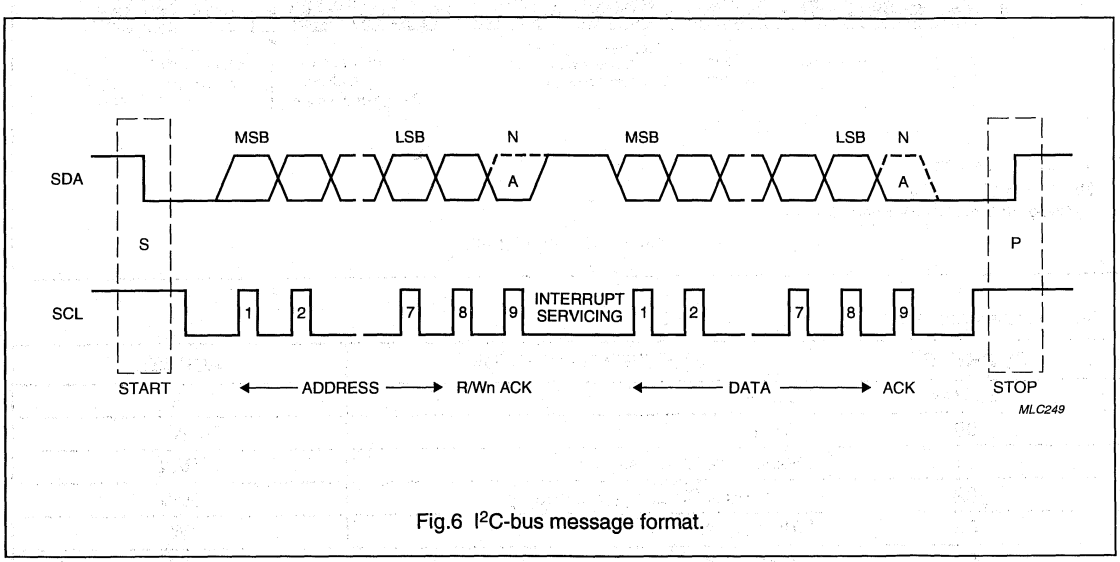


Fig.6 I²C-bus message format.

Decoder I²C-bus access

All internal access to the PCD5003 takes place via I²C-bus interface. For this purpose the internal registers, SRAM and EEPROM have been memory mapped and are accessed via an **index register**. Table 13 shows the index addresses of all internal blocks.

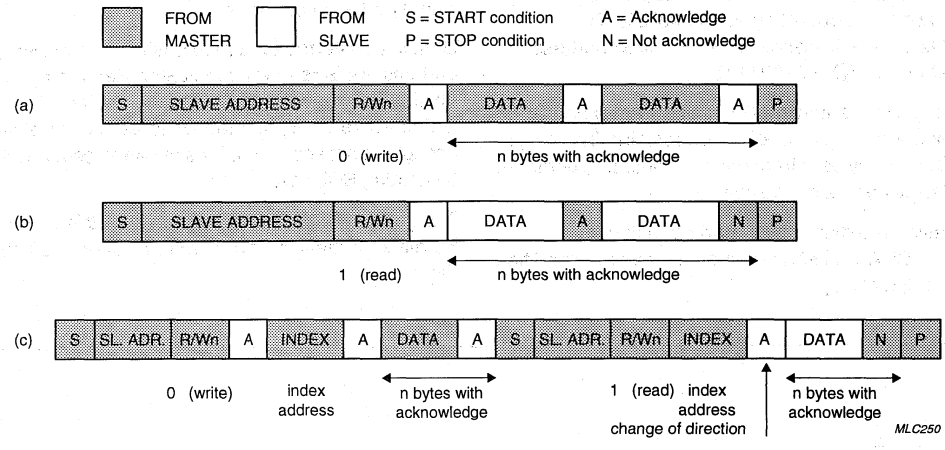
Registers are addressed directly, while RAM and EEPROM are addressed indirectly via address pointers and I/O registers.

Remark: The EEPROM memory map is non-contiguous and organized as a matrix. The EEPROM address pointer contains both row and column indicators.

Data written to read-only bits will be ignored. Values read from write-only bits are undefined and must be ignored.

Each I²C-bus message to the PCD5003 must start with its slave address, followed by the index address of the memory element to be accessed. The different I²C-bus message types are shown in Fig.7.

As a slave the PCD5003 cannot initiate bus transfers by itself. To prevent an external controller from having to monitor the operating status of the decoder, all important events generate an external interrupt on output INT.



(a) Master writes to slave.
(b) Master reads from slave.
(c) Combined format (shown: write plus read).

Fig.7 Message types.

Table 13 Index register

ADDRESS(1)	REGISTER FUNCTION	ACCESS
00 Hex	Status	R
00	Control	W
01	Real Time Clock: seconds	R/W
02	Real Time Clock: $^1/_{100}$ second	R/W
03	Alert Cadence	W
04	Alert Setup	W
05	Periodic Interrupt Modulus	W
05	Periodic Interrupt Counter	R
06	RAM Write Address pointer	R
07	EEPROM Address pointer	R/W
08	RAM Read Address pointer	R/W
09	RAM Data Output	R
0A	EEPROM Data Input/Output	R/W
0B to 0F	unused	note 2

Notes

1. The index register only uses the least significant nibble, the upper 4 bits are ignored.
2. Writing to registers 0B to 0F has no effect, reading produces meaningless data.

External interrupt

The PCD5003 can signal events to an external controller via an interrupt signal on output INT. The interrupt polarity is programmable via SPF programming. The interrupt source is shown in the status register.

Interrupts are generated by the following events (more than one event possible):

- Call data available for output (bit D2)
- SRAM pointers becoming equal (bit D3)
- Expiry of periodic time-out (bit D7)
- Expiry of alert time-out (bit D4)
- Change of state in Out-of-Range indicator (bit D5)
- Change of state in Battery-Low indicator or in receiver control output RXE (bit D6).

Immediate interrupts are generated by status bits D3, D4, D6 (RXE monitoring) and D7. Bits D2, D5 and D6 (BAT monitoring) generate interrupts as soon as the receiver is disabled (RXE = 0).

When call data is available (D2 = 1) but the receiver remains switched on, an interrupt is generated at the next sync word position.

The interrupt output INT is reset after completion of a status read operation.

Status/Control register

The Status/Control register consists of two independent registers, one for reading (Status) and one for writing (Control).

The Status register shows the current operating condition of the decoder and the cause(s) of an external interrupt. The Control register activates/deactivates certain functions. Tables 14 and 15 show the bit allocations of both registers.

All status bits will be reset after a status read operation except for the Out-of-Range, Battery-Low and Receiver Enable indicator bits (see note 1 to Table 14).

Table 14 Status register (00 Hex, read)

BIT (1)	VALUE	DESCRIPTION
D1, D0	0 0	no new call data
	0 1	call data available
	1 0	reserved for future use
	1 1	reserved for future use
D3, D2	0 0	no data to be read (default after reset)
	0 1	RAM read/write pointers different: data to be read
	1 0	RAM read/write pointers equal: no more data to read
	1 1	RAM buffer full or overflow
D4	1	alert time-out expired
D5	1	Out-of-Range
D6	1	BAT input HIGH or RXE output active (selected by Control bit D2)
D7	1	periodic timer interrupt

Note

1. After a status read operation bits D3, D4 and D7 are always reset, bits D1 and D0 only when no second call is pending. D2 is reset when the RAM is empty (read and write pointers equal).

Table 15 Control register (00 Hex, write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	1	forced call termination (automatically reset after termination)
D1	1	EEPROM programming enable
D2	0	BAT input selected for monitoring (Status bit D6)
	1	RXE output selected for monitoring (Status bit D6)
D3	1	receiver continuously enabled (RXE = 1, ROE = 1)
D4	0	decoder in OFF status (while DON = 0)
	1	decoder in ON status
D5 to D7	X	not used: ignored when written

Pending interrupts

A secondary Status register is used for storing status bits of pending interrupts. This occurs:

- When a new call is received while the previous one was not yet acknowledged by reading the Status register
- When an interrupt occurs during a status read operation.

After completion of the status read the primary register is loaded with the contents of the secondary register, which is then reset. Next, an immediate interrupt is generated, output INT becoming active 1 decoder clock cycle after it was reset following the status read.

Remark: In the event of multiple pending calls only the status bits of the last call are retained.

Out-of-Range Indication

The Out-of-Range condition occurs when entering Fade Recovery or Carrier Off mode. This condition is reflected in bit D5 of the Status register. The Out-of-Range condition is left when entering Data Receive mode.

The Out-of-Range bit (D5) in the Status register is updated each time the receiver is disabled (RXE $\downarrow$ 0). Every change of state in bit D5 generates an interrupt.

Real time clock

The PCD5003 provides a periodic reference pulse at output REF. The frequency of this signal can be selected by SPF programming:

- 32768 Hz
- 50 Hz (square-wave)
- 2 Hz
- $1/60$ Hz.

The 32768 Hz signal does not have a fixed period: it consists of 32 pulses evenly distributed over 75 main oscillator cycles at 76.8 kHz. The timing is shown in Fig.13.

When programmed for $1/60$ Hz (1 pulse per minute) the pulse at output REF is held off while the receiver is enabled.

Except for the 50 Hz frequency the pulse width t_{RFP} is equal to one decoder clock period.

The real time clock counter runs continuously irrespective of the operating condition of the PCD5003. It contains a **seconds register** (maximum 59) and a **$1/100$ second register** (maximum 99), which can be read or written via the I²C-bus. The bit allocation of both registers is shown in Tables 16 and 17.

Table 16 Real time clock: seconds register (01 Hex, read/write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	–	1 second
D1	–	2 seconds
D2	–	4 seconds
D3	–	8 seconds
D4	–	16 seconds
D5	–	32 seconds
D6	X	not used: ignored when written, undetermined when read
D7	X	not used: ignored when written, undetermined when read

Table 17 Real time clock: $1/100$ second register (02 Hex, read/write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	–	0 01 second
D1	–	0.02 second
D2	–	0.04 second
D3	–	0.08 second
D4	–	0.16 second
D5	–	0.32 second
D6	–	0.64 second
D7	X	not used: ignored when written, undetermined when read

Periodic interrupt

A periodic interrupt can be realised with the Periodic Interrupt Counter. This 8-bit counter is incremented every $1/100$ second and produces an interrupt when it reaches the value stored in the Periodic Interrupt Modulus register. The Counter register is then reset and counting continues.

Operation is started by writing a non-zero value to the Modulus register. Writing a zero will stop interrupt generation immediately and will halt the Periodic Interrupt Counter after 2.55 seconds.

The Modulus register is write-only, the Counter register can only be read. Both registers have the same index address (05 Hex).

Received call delay

Call reception causes both the Periodic Interrupt Modulus and the Counter register to be reset.

Since the Periodic Interrupt Counter runs for another 2.55 seconds after a reset, the received call delay (in $1/100$ second units) can be determined by reading the Counter register.

Alert generation

The PCD5003 is capable of controlling 3 different alert transducers: acoustic beeper (HIGH- and LOW-level), LED and vibrator motor. The associated outputs are ATH/ATL, LED and VIB respectively. ATL is an open drain output capable of directly driving an acoustic alerter via a resistor. The other outputs require external transistors.

Each alert output can be individually enabled via the Alert Setup register. Alert level and warble can be separately selected. The alert pattern can either be standard POCSAG or determined via the Alert Cadence register. Direct alert control is possible via input ALC.

The Alert Setup register is shown in Table 18.

Standard POCSAG alerts can be selected by setting bit D0 in the Alert Setup register, bits D6 and D7 determining the alert pattern used.

Automatic generation via all alert outputs of the POCSAG alert pattern matching the received call type can be enabled by SPF programming (SPF byte 03, bit D2).

Table 18 Alert setup register (04 Hex, write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	0	call alert via Cadence Register
	1	POCSAG call alert (pattern selected by D7, D6)
D1	0	LOW-level acoustic alert (ATL), pulsed vibrator alert (25 Hz)
	1	HIGH-level acoustic alert (ATL + ATH), continuous vibrator alert
D2	0	normal alerts (acoustic and LED)
	1	warbled alerts: 16 Hz (LED: on/off, ATL/ATH: alternate f_{AWH}, f_{AWL})
D3	1	acoustic alerts enable (ATL, ATH)
D4	1	vibrator alert enabled (VIB)
D5	1	LED alert enabled (LED)
D7, D6[1]	0 0	POCSAG alert pattern FC = 00, see Fig.8(a)
	0 1	POCSAG alert pattern FC = 01, see Fig.8(b)
	1 0	POCSAG alert pattern FC = 10, see Fig.8(c)
	1 1	POCSAG alert pattern FC = 11, see Fig.8(d)

Note

1. Bits D7 and D6 correspond to function bits 20 and 21 respectively in the address codeword, which designate the POCSAG call type as shown in Table 1.

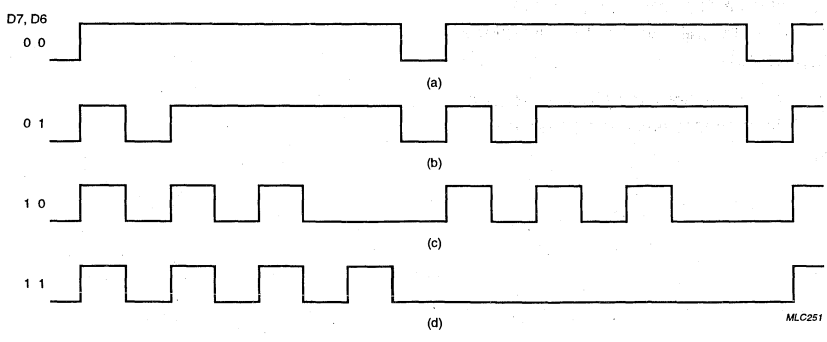


Fig.8 POCSAG alert patterns.

ALERT CADENCE REGISTER (03 HEX, WRITE)

When not programmed for POCSAG alerts (Alert Setup register bit D0 = 0), the 8-bit Alert Cadence register determines the alert pattern. Each bit represents a 62.5 ms time slot, a logic 1 activating the enabled alert transducers. The bit pattern is rotated with the MSB (bit D7) being output first and the LSB (bit D0) last.

When the last time slot (bit D0) is started an interrupt is generated to allow loading of a new pattern. When the pattern is not changed it will be repeated. Writing a zero to the Alert Cadence register will halt alert generation.

ACOUSTIC ALERT

Acoustic alerts are generated via outputs ATL and ATH. For LOW-level alerts only ATL is active, while for HIGH-level alerts ATH is also active. ATL is driven in counter phase with ATH.

The alert level is controlled by bit D1 of the Alert Setup register.

When D1 is reset for standard POCSAG alerts (D0 = 1), a LOW-level acoustic alert is generated during the first 4 seconds (ATL), followed by 12 seconds at HIGH-level (ATL + ATH). When D1 is set, the full 16 seconds are at HIGH-level. An interrupt is generated upon expiry of the full alert time.

When using the Alert Cadence register, D1 would normally be updated by external control when the alert time-out interrupt occurs at the start of the 8th cadence time slot. Since D1 acts immediately on the alert level, it is advised to reset the last bit of the previous pattern to prevent unwanted audible level changes.

LED ALERT

The LED output pattern corresponds either to the selected POCSAG alert or to the contents of the Alert Cadence register. No equivalent exists for high/low-level alerts.

VIBRATOR ALERT

The vibrator output (VIB) is activated continuously during a standard POCSAG alert or whenever the Alert Cadence register is non-zero.

Two alert levels are supported: low-level (25 Hz square-wave) and high-level (continuous). The vibrator level is controlled by bit D1 in the Alert Setup register.

WARBLED ALERT

When enabled by setting bit D2 in the Alert Setup register, the signals on outputs ATL, ATH and LED are warbled with a 16 Hz modulation frequency. Output LED is switched on and off at the modulation rate, while outputs ATL and ATH switch between f_{AWH} and f_{AWL} alerter frequencies.

DIRECT ALERT CONTROL

A direct Alert Control input (ALC) is available for generating user alarm signals (e.g. Battery-Low warning). A HIGH-level on input ALC activates all enabled alert outputs, overruling any ongoing alert patterns.

ALERT PRIORITY

Generation of a standard POCSAG alert (D0 = 1) overrides any alert pattern in the Alert Cadence register. After completion of the standard alert, the original cadence is restarted from the position it was left at. The Alert Setup register will now contain the settings for the standard alert.

The highest priority has been assigned to the Alert Control input (ALC). All enabled alert outputs will be activated while ALC is set. Outputs are activated/deactivated synchronous with the decoder clock. Activation requires an extra delay of 1 clock when no alerts are being generated.

When input ALC is reset, acoustic alerting does not cease until the current output frequency cycle has been completed.

AUTOMATIC POCSAG ALERTS

Standard alert patterns have been defined for each POCSAG call type, as indicated by the function bits in the address codeword (see Table 1). The timing of these alert patterns is shown in Fig.9.

When enabled by SPF programming (SPF byte 03, bit D2) standard POCSAG alerts will automatically be generated on outputs ATL, ATH, LED and VIB upon call reception. The alert pattern matches the call type as indicated by the function bits in the received address codeword.

The original settings of the Alert Setup register will be lost. Bit D0 is reset after completion of the alert.

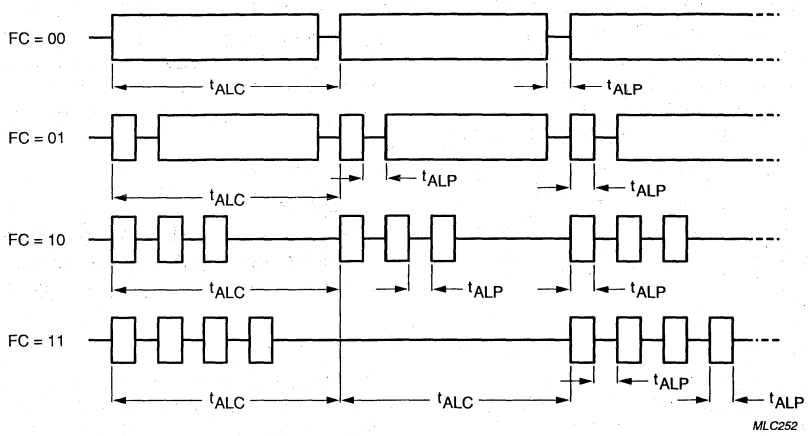


Fig.9 POCSAG alert timing.

RAM organization

SRAM ACCESS

The on-chip SRAM can hold up to 96 bytes of call data. Each call consists of a Call Header (3 bytes), Message Data blocks (3 bytes per codeword) and a Call Terminator (3 bytes).

The RAM is filled by the decoder and can be read via the I²C-bus interface. The RAM is accessed indirectly by means of a read address pointer and a data output register. A write address pointer indicates the position of the last message byte stored.

Status register bit D2 is set when the read and write pointers are different. It is reset only when the SRAM pointers become equal during reading, i.e. when the RAM becomes empty.

Status bit D3 is set when the read and write pointers become equal. This can be due to a RAM empty or a RAM full condition. It is reset after a status read operation.

Interrupts are generated as follows:

- When Status bit D2 is set and the receiver is disabled (RXE = 0): data is available for reading
- Immediately when Status bit D3 is set: RAM is either empty (Status bit D2 = 0) or full (Status bit D2 = 1).

To avoid loss of data due to RAM overflow at least 3 bytes of data must be read during reception of the codeword following the 'RAM full' interrupt.

RAM WRITE ADDRESS POINTER (06 HEX, READ)

The RAM write address pointer is automatically incremented during call reception, as the decoder writes each data byte to RAM. The RAM write address pointer can only be read. Values range from 0 to 5F Hex.
Bit D7 (MSB) is not used and its value is undefined when read.

RAM READ ADDRESS POINTER (08 HEX, READ/WRITE)

The RAM read address pointer is automatically incremented after reading a data byte via the RAM output register.

It can be accessed for writing as well as reading.

The values range from 0 to 5F Hex. When at 5F Hex a read operation will cause wrapping around to 00 Hex.
Bit D7 (MSB) is not used; it is ignored when written and undefined when read.

RAM DATA OUTPUT REGISTER (09 HEX, READ)

The RAM data output register contains the byte addressed by the RAM read address pointer. It can only be read, each read operation causing an increment of the RAM read address pointer.

EEPROM organization

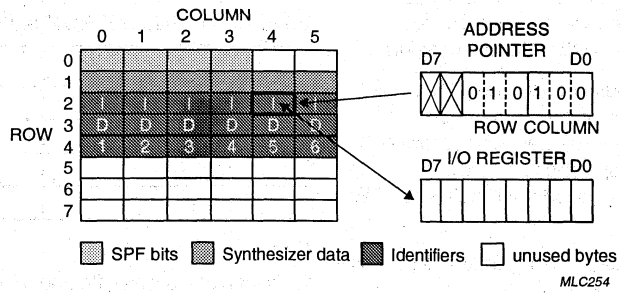


Fig.10 EEPROM organization and access.

EEPROM ACCESS

The EEPROM is intended for storage of user addresses (RICs), sync words and Special Programmed Function (SPF) bits representing the decoder configuration.

The EEPROM can store 48 bytes of information and is organized as a matrix of 8 rows by 6 columns. The EEPROM is accessed indirectly via an address pointer and a data I/O register.

The EEPROM is protected against inadvertent writing by means of the Programming Enable bit in the Control register (bit D1).

The EEPROM memory map is non-contiguous as can be seen in Fig.10, which shows both the EEPROM organization and the access method.

Identifier locations contain RICs or sync words. A total of 20 unassigned bytes is available for general purpose storage.

EEPROM ADDRESS POINTER (07 HEX, READ/WRITE)

An EEPROM location is addressed via the EEPROM address pointer. It is incremented automatically each time a byte is read or written via the EEPROM data I/O register.

The EEPROM address pointer contains two counters, for the row and the column number. Bits D2 to D0 contain the column number (0 to 5) and bits D5 to D3 the row number (0 to 7). Bits D7 and D6 of the address pointer are not used. Data written to these bits will be ignored, while their values are undefined when read.

The column and row counters are connected in series. Upon overflow of the column counter (column = 5) the row counter is automatically incremented and the column counter wraps to 0. On overflow the row counter wraps from 7 to 0.

EEPROM DATA I/O REGISTER (0A HEX, READ/WRITE)

The byte addressed by the EEPROM address pointer can be written or read via the EEPROM Data I/O register. Each access automatically increments the EEPROM address pointer.

EEPROM ACCESS LIMITATIONS

Since the EEPROM address pointer is used during data decoding, the EEPROM may not be accessed while the receiver is active (RXE = 1). It is advised to switch to OFF state before accessing the EEPROM.

The EEPROM cannot be written unless the EEPROM Programming Enable bit (bit D1) in the Control register is set.

For writing a minimum supply voltage V_{PG} is required (2.5 V typ.). The supply current needed during writing (I_{PG}) will be ≈500 μA.

EEPROM READ OPERATION

EEPROM read operations must start at a valid address in the non-contiguous memory map. Single-byte or block reads are permitted.

EEPROM WRITE OPERATION

EEPROM write operations must always take place in blocks of 6 bytes, starting at the beginning of a row. Programming a single byte will reset the other bytes in the same row. Modifying a single byte in a row requires re-writing the unchanged bytes with their old contents.

After writing each block a pause of maximum 7.5 ms is required to complete the programming operation internally. During this time the external microcontroller may generate an I²C-bus Stop condition. If another I²C-bus transfer is started the decoder will pull SCL LOW during this pause.

After writing the EEPROM Programming Enable bit (D1) in the Control register must be reset.

INVALID WRITE ADDRESS

When an invalid write address is used, the column counter bits (D2 to D0) are forced to zero before being loaded into the address pointer. The row counter bits are used normally.

INCOMPLETE PROGRAMMING SEQUENCE

A programming sequence may be aborted by an I²C-bus Stop condition. Next, the EEPROM Programming Enable bit (D1) in the Control register must be reset.

Any bytes received of the last 6-byte block will be ignored and the contents of this (incomplete) EEPROM block will remain unchanged.

UNUSED EEPROM LOCATIONS

A total of 20 EEPROM bytes is available for general purpose storage (see Table 19).

Table 19 Unused EEPROM addresses

ROW	HEX
0	04, 05[1]
5	28 to 2D
6	30 to 35
7	38 to 3D

Note

1. When using bytes 04 and 05 Hex, care must be taken to preserve the SPF information stored in bytes 00 to 03 Hex.

SPECIAL PROGRAMMED FUNCTION ALLOCATION

The SPF bit allocation in the EEPROM is shown in Tables 20 to 24. The SPF bits are located in row 0 of the EEPROM and occupy 4 bytes.

Bytes 04 and 05 Hex are not used and are available for general purpose storage.

Table 20 Special Programmed Functions (00 Hex)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	reserved for future use; logic 0 when read
D1	X	reserved for future use
D2	X	reserved for future use
D3	X	reserved for future use
D4	X	reserved for future use
D5	X	reserved for future use
D6	X	reserved for future use; logic 0 when read
D7	1	received data inversion enabled

Table 21 Special Programmed Functions (01 Hex)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1, D0	0 0	5 ms receiver establishment time (nominal); note 1
	0 1	10 ms
	1 0	15 ms
	1 1	30 ms
D3, D2	0 0	20 ms oscillator establishment time (nominal); note 1
	0 1	30 ms
	1 0	40 ms
	1 1	50 ms
D5, D4	0 0	512 bits/s received bit rate
	0 1	1024 bits/s (not used in POCSAG)
	1 0	1200 bits/s
	1 1	2400 bits/s
D6	1	synthesizer interface enabled (programming at switch-on)
D7	1	voltage converter enabled

Note

1. Since the exact establishment time is related to the programmed bit rate, Table 22 shows the values for the various bit rates.

Table 22 Establishment time as a function of bit rate

NOMINAL ESTABLISHMENT TIME	ACTUAL ESTABLISHMENT TIME (bits)			
	512 bits/s	1024 bits/s	1200 bits/s	2400 bits/s
5 ms	5.9 ms (3)	5.9 ms (6)	5.0 ms (6)	5.0 ms (12)
10 ms	11.7 ms (6)	11.7 ms (12)	10.0 ms (12)	10.0 ms (24)
15 ms	15.6 ms (8)	15.6 ms (16)	16.7 ms (20)	16.7 ms (40)
20 ms	23.4 ms (12)	23.4 ms (24)	20.0 ms (24)	20.0 ms (48)
30 ms	31.2 ms (16)	31.2 ms (32)	26.7 ms (32)	26.7 ms (64)
40 ms	39.1 ms (20)	39.1 ms (40)	40.0 ms (48)	40.0 ms (96)
50 ms	46.9 ms (24)	46.9 ms (48)	53.3 ms (64)	53.3 ms (128)

Table 23 Special Programmed Functions (02 Hex)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	not used
D1	X	not used
D3, D2	0 0	32768 Hz Real Time Clock reference
	0 1	50 Hz square-wave
	1 0	2 Hz
	1 1	$\frac{1}{60}$ Hz
D4	1	Signal test mode enabled (REF and INT outputs)
D5	0	Burst error correction enabled
D7, D6	X X	reserved for future use

Table 24 Special Programmed Functions (03 Hex)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1, D0	0 0	2048 Hz Acoustic alerter frequency
	0 1	2731 Hz
	1 0	4096 Hz
	1 1	3200 Hz
D2	1	Automatic POCSAG alert generation enabled
D3	X	not used
D4	X	not used
D5	X	not used
D6	0	INT output polarity: active LOW
	1	INT output polarity: active HIGH
D7	X	not used

SYNTHESIZER PROGRAMMING DATA

Data for programming a PLL synthesizer via pins ZSD, ZSC and ZLE can be stored in row 1 of the EEPROM. Six bytes are available starting from address 08 Hex.

Data is transferred in two serial blocks of 24 bits each, starting with bit 0 (MSB) of block 1. Any unused bits must be programmed at the beginning of a block.

Table 25 Synthesizer programming data (08 to 0D Hex)

ADDRESS (HEX)	BIT (MSB: D7)	DESCRIPTION
08	D7 to D0	bits 0 to 7 of data block 1 (bit 0 is MSB)
09	D7 to D0	bits 8 to 15
0A	D7 to D0	bits 16 to 23
0B	D7 to D0	bits 0 to 7 of data block 2 (bit 0 is MSB)
0C	D7 to D0	bits 8 to 15
0D	D7 to D0	bits 16 to 23

IDENTIFIER STORAGE ALLOCATION

Up to 6 different identifiers can be stored in EEPROM for matching with incoming data. The PCD5003 can distinguish two types of identifiers:

- User addresses (RIC)
- User Programmable Sync Words (UPSW).

Identifiers are stored in EEPROM rows 2, 3 and 4. Each identifier location consists of 3 bytes in the same column. The identifier number is equal to the column number + 1.

Only the last 4 identifiers (numbers 3 to 6) can be programmed as a UPSW. Identifiers 1 and 2 always represent RICs. A UPSW represents an unused address and must differ by more than 6 bits from preamble to guarantee detection.

The standard POCSAG sync word is always enabled and has identifier number 7.

Table 26 shows the memory locations of the 6 identifiers. The bit allocation per identifier is given in Table 27.

Table 26 Identifier storage allocation (10 to 25 Hex)

ADDRESS (HEX)	BYTE	DESCRIPTION
10 to 15	1	identifier number 1 to 6
18 to 1D	2	identifier number 1 to 6
20 to 25	3	identifier number 1 to 6

Table 27 Identifier bit allocation

BYTE	BIT (MSB: D7)	DESCRIPTION
1	D7 to D0	bits 2 to 9 of POCSAG codeword (RIC or UPSW); notes 1 and 2
2	D7 to D0	bits 10 to 17
3	D7, D6	bits 18, 19
	D5	frame number bit FR3 (RIC); note 3
	D4	frame number bit FR2 (RIC)
	D3	frame number bit FR1 (RIC)
	D2	identifier type selection (0 = UPSW, 1 = RIC); note 4
	D1	identifier enable (1 = enabled)
	D0	reserved for future use, logic 0 when read

Notes

1. The bit numbering corresponds with the numbering in a POCSAG codeword: bit 1 is the flag bit (0 = address, 1 = message).
2. A UPSW needs 18 bits to be matched for successful identification. Bit 1 (MSB) must be logic 0; bits 2 to 19 contain the identifier bit pattern; they are followed by 2 predetermined random (function) bits and the UPSW is completed by 10 CRC error correction bits and an even-parity bit.
3. Bits FR3 to FR1 (MSB: FR3) contain the 3 least significant bits of the 21-bit RIC.
4. Identifiers 1 and 2 (RIC only) will be disabled by programming bit D2 as logic 0.

Voltage doubler

An on-chip voltage doubler provides an unregulated DC output for supplying an LCD or a low power microcontroller on output V_{PO}. An external ceramic capacitor of typical 100 nF is required between pins CCN and CCP. The voltage doubler is enabled via SPF programming.

Level-shifted interface

All interface lines are suited for communication with a microcontroller operating from a higher supply voltage. The external device must have a common reference at V_{SS} of the PCD5003.

The reference voltage for the level-shifted interface must be applied to input V_{PR}. This could be the on-chip voltage doubler output V_{PO} if required. When the microcontroller has a separate (regulated) supply this separate supply voltage should be connected to V_{PR}.

The level-shifted interface lines are: RST, DON, ALC, REF, INT.

The I^2C-bus interface lines SDA and SCL can be level-shifted independently of V_{PR} by means of the standard external pull-up resistors.

Signal test mode

A special Signal test mode is available for monitoring the performance of a receiver circuit together with the front-end of the PCD5003.

For this purpose the output of the digital noise filter and the recovered bit clock are made available at outputs REF and INT respectively. All synchronization and decoding functions are normally active.

Signal test mode is activated/deactivated by SPF programming.

OPERATING INSTRUCTIONS

Reset conditions

When the PCD5003 is reset by applying a HIGH-level on input RST, the condition of the decoder is as follows:

- OFF status (irrespective of DON input level)
- REF output frequency 32768 Hz
- All internal counters reset
- Status/Control register reset
- INT output at LOW-level
- No alert transducers selected
- LED, VIB and ATH outputs at LOW-level
- ATL output high-impedance
- SDA, SCL inputs high-impedance
- Voltage converter disabled.

Within t_{RSU} after release of the reset condition (RST LOW) the programmed functions are activated. The settings affecting the external operation of the PCD5003 are as follows:

- REF output frequency
- Voltage converter
- INT output polarity
- Signal test mode.

When input DON is HIGH, the decoder starts operating in ON status immediately following t_{RSU}.

Power-on reset circuit

Input RST has an internal high-ohmic pull-down resistor (nom. 2 MΩ at 2.5 V supply). This can be used together with an external capacitor to V_{PR} to make a power-on reset signal.

Since this pull-down varies considerably with processing and supply voltage, a more accurate reset duration can be realised with an additional external resistor to V_{SS}.

Reset timing

The start-up time for the crystal oscillator may exceed 1 second (typ. 800 ms). It is advised to apply a reset condition at least during the first part of this period. The minimum reset pulse duration t_{RST} is 50 µs.

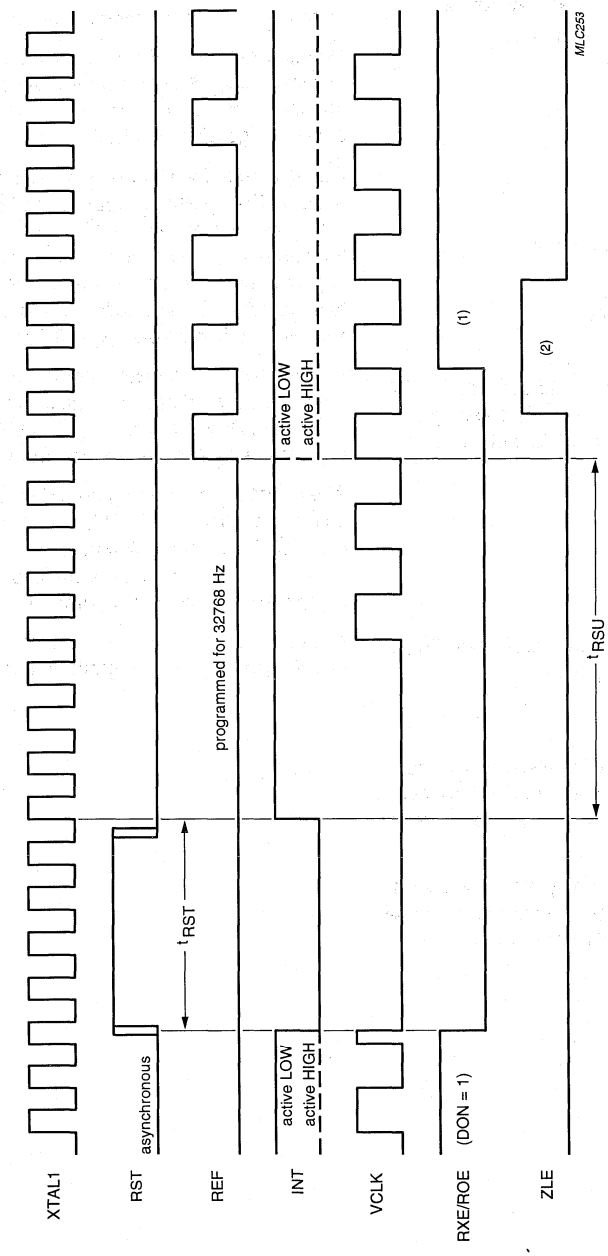
During reset the oscillator is active, but clock signals are inhibited internally. Once the reset condition is released the end of the oscillator start-up period can be detected by a rising edge on output INT.

During a reset the voltage converter clock (VCLK) is held at zero. The resulting output voltage drop may cause problems when the external resetting device is powered by the internal voltage doubler. A sufficiently large buffer capacitor between output V_{PO} and V_{SS} must be provided to supply the microcontroller during reset. The voltage at V_{PO} will not drop below $V_{DD} - 0.7$ V.

Immediately after a reset all programmable internal functions will start operating according to a programmed value of 0. During the first 8 full clock cycles (t_{RSU}) all programmed values are loaded from EEPROM.

After reset the receiver outputs RXE and ROE become active immediately, if DON is HIGH and the synthesizer is disabled. When the synthesizer is enabled, RXE and ROE will only become active after the second pulse on ZLE completes the loading of synthesizer data.

The full reset timing is shown in Fig.11. The start-up timing including synthesizer programming is given in Fig.12.



(1) The RXE/ROE output signals are shown for disabled synthesizer. When the synthesizer is enabled RXE/ROE are held off until after the second pulse on ZLE (programming complete).
(2) The ZLE output signal is shown for enabled synthesizer and DON = 1. When DON = 0 output ZLE remains HIGH until ON state is entered (DON = 1 or control register bit D4 = 1).

Fig.11 Reset timing.

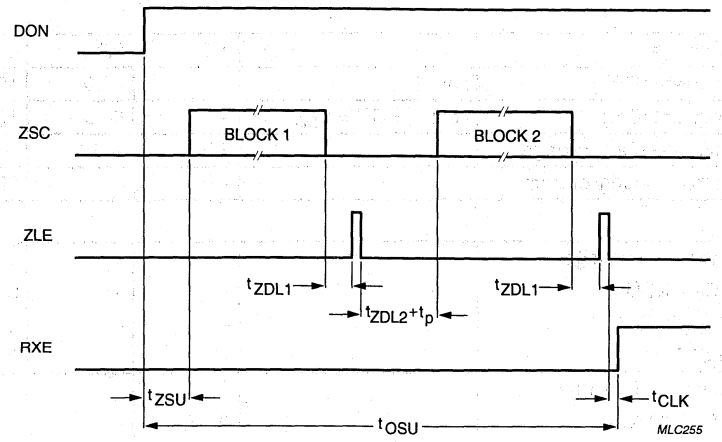


Fig.12 Start-up timing including synthesizer programming.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_n	input voltage any pin	V_{SS} − 0.8	V_{DD} + 0.8	V
P_{tot}	total power dissipation	−	250	mW
P_O	power dissipation per output	−	100	mW
T_{amb}	operating ambient temperature	−25	+70	°C
T_{stg}	storage temperature	−55	+125	°C

DC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		1.5	2.7	6.0	V
I_{DD0}	supply current (OFF)	note 1	–	25.0	40.0	µA
I_{DD1}	supply current (ON)	note 1; DON = V_{DD}	–	50.0	80.0	µA
V_{PG}	programming supply voltage		2.5	–	–	V
I_{PG}	programming supply current		–	–	800	µA
Inputs						
V_{IL}	LOW level input voltage					
	RDI, BAT XTAL1		–	–	$0.3V_{DD}$	V
	DON, ALC, RST		–	–	$0.3V_{PR}$	V
	SDA, SCL		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage					
	RDI, BAT XTAL1		$0.7V_{DD}$	–	–	V
	DON, ALC, RST		$0.7V_{PR}$	–	–	V
	SDA, SCL		$0.7V_{DD}$	–	–	V
I_{IL}	LOW level input current	T_{amb} = 25 °C				
	RDI, BAT,TS1, TS2	$V_I = V_{SS}$	0	–	−0.5	µA
	DON, ALC, RST	$V_I = V_{SS}$	0	–	−0.5	µA
I_{IH}	HIGH level input current	T_{amb} = 25 °C				
	TS1, TS2	$V_I = V_{DD}$	6	–	20	µA
	RDI, BAT	$V_I = V_{DD}$; RXE = 0	6	–	20	µA
	RDI, BAT	$V_I = V_{DD}$; RXE = 1	0	–	0.5	µA
	DON, ALC, RST	$V_I = V_{DD}$	250	500	850	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
I_{OL}	LOW level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OL} = 0.3 V	80	–	–	µA
	ATH	V_{OL} = 0.3 V	250	–	–	µA
	INT, REF	V_{OL} = 0.3 V	80	–	–	µA
	ZSD, ZSC, ZLE	V_{OL} = 0.3 V	70	–	–	µA
	ATL	V_{OL} = 1.2 V; note 2	13	27	55	mA
	ROE, RXE	V_{OL} = 0.3 V	80	–	–	µA
I_{OH}	HIGH level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OH} = 0.7 V	–0.6	–	–2.4	mA
	ATH	V_{OH} = 0.7 V	–3.0	–	–11.0	mA
	INT, REF	V_{OH} = 2.4 V	–80	–	–	µA
	ZSD, ZSC, ZLE	V_{OH} = 2.4 V	–60	–	–	µA
	ATL	ATL high-impedance	–	–	–0.5	µA
	ROE, RXE	V_{OH} = 2.4 V	–600	–	–	µA

Notes

1. All inputs = V_{SS}; all outputs open-circuit; SDA, SCL pulled up to V_{DD}; clock signal at XTAL1: f_{OSC} = 76800 Hz, amplitude: V_{SS} to V_{DD}; outputs RXE and ROE logic 0; REF output: $f_{ref} = 1/60$ Hz.
2. Maximum output current is subject to absolute maximum ratings per output (see Chapter "Limiting values").

DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 2.7 V; V_{SS} = 0 V; $V_{PR} = V_{PO}$; T_{amb} = –25 to +70 °C; C_s = 100 nF; voltage converter enabled.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.5	–	3.0	V
$V_{PO(0)}$	output voltage; no load	V_{DD} = 2.7; I_{PO} = 0	–	5.4	–	V
V_{PO}	output voltage	V_{DD} = 2.0 V; I_{PO} = –250 µA	3.0	3.5	–	V
I_{PO}	output current	V_{DD} = 2.0 V; V_{PO} = 2.7 V	–400	–650	–	µA
		V_{DD} = 3.0 V; V_{PO} = 4.5 V	–650	–900	–	µA

OSCILLATOR CHARACTERISTICS

Quartz crystal type: MX-1V or equivalent.

Quartz crystal parameters: f = 76 800 Hz; $R_{S(max)}$ = 35 kΩ; C_L = 8 pF; C_0 = 1.4 pF; C_1 = 1.5 fF; TC = -35×10^{-6}/K.

Maximum overall tolerance: $\pm 200 \times 10^{-6}$ (includes: cutting, temperature, aging).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{XO}	output capacitance XTAL2		–	10	–	pF
g_m	oscillator transconductance	V_{DD} = 1.5 V	6	12	–	µS

AC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; T_{amb} = 25 °C;. f_{OSC} = 76800 Hz.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock						
T_{CLK}	system clock period	f_{OSC} = 76800 Hz	–	13.02	–	µs
Call alert frequencies						
f_{AL}	alert frequency	SPF byte 03 Hex; bits:				
		D1, D0 = 0 0	–	2048	–	Hz
		D1, D0 = 0 1	–	2731	–	Hz
		D1, D0 = 1 0	–	3200	–	Hz
		D1, D0 = 1 1	–	4096	–	Hz
f_{AW}	warbled alert; modulation frequency	alert setup bit D2 = 1; outputs ATL, ATH, LED	–	16	–	Hz
f_{AWH}	warbled alert; high acoustic alert frequency	alert setup bit D2 = 1; outputs ATL, ATH	–	f_{AL}	–	Hz
f_{AWL}	warbled alert; low acoustic alert frequency	alert setup bit D2 = 1; outputs ATL, ATH	–	$\frac{1}{2}f_{AL}$	–	Hz
f_{VBP}	pulsed vibrator frequency (square-wave)	low-level alert	–	25	–	Hz
Call alert duration						
t_{ALT}	alert time-out period		–	16	–	s
t_{ALL}	ATL output time-out period	low level alert	–	4	–	s
t_{ALH}	ATH output time-out period	high level alert	–	12	–	s
t_{VBL}	VIB output time-out period	low level alert	–	4	–	s
t_{VBH}	VIB output time-out period	high level alert	–	12	–	s
t_{ALC}	alert cycle period		–	1	–	s
t_{ALP}	alert pulse duration		–	125	–	ms
Real time clock reference						
f_{ref}	real time clock reference frequency	SPF byte 02 Hex; bits:				
		D3, D2 = 0 0; note 1	–	32768	–	Hz
		D3, D2 = 0 1; note 2	–	50	–	Hz
		D3, D2 = 1 0	–	2	–	Hz
		D3, D2 = 1 1	–	$\frac{1}{60}$	–	Hz
t_{RFP}	real time clock reference pulse duration	all reference frequencies except 50 Hz (square-wave)	–	13.02	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver control						
t_{RXT}	RXE, ROE transition time	C_L = 5 pF	–	100	–	ns
t_{RXON}	RXE establishment time (nominal values: actual duration is bit rate dependent, see Table 22)	SPF byte 01 Hex; bits:				
		D1, D0 = 0 0	–	5	–	ms
		D1, D0 = 0 1	–	10	–	ms
		D1, D0 = 1 0	–	15	–	ms
		D1, D0 = 1 1	–	30	–	ms
t_{ROON}	ROE establishment time (nominal values: actual duration is bit rate dependent, see Table 22)	SPF byte 01 Hex; bits:				
		D3, D2 = 0 0	–	20	–	ms
		D3, D2 = 0 1	–	30	–	ms
		D3, D2 = 1 0	–	40	–	ms
		D3, D2 = 1 1	–	50	–	ms
I²C-bus interface						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	µs
t_{HIGH}	SCL clock HIGH period		0.6	–	–	µs
t_{SUDAT}	data set-up time		100	–	–	ns
t_{HDDAT}	data hold time		0	–	–	ns
t_r	SDA, SCL rise time		–	–	300	ns
t_f	SDA, SCL fall time		–[3]	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
t_{SUSTA}	start condition set-up time		0.6	–	–	µs
t_{HDSTA}	start condition hold time		0.6	–	–	µs
t_{SUSTO}	stop condition set-up time		0.6	–	–	µs
Reset						
t_{RST}	external reset duration		50	–	–	µs
t_{RSU}	set-up time after reset	oscillator running	–	–	105	µs
t_{OSU}	set-up time after switch-on	oscillator running	–	–	4	ms
Data input						
t_{TDI}	data input transition time		–	–	100	µs
t_{DI1}	data input logic 1 duration		infinite			
t_{DI0}	data input logic 0 duration		infinite			
POCSAG data timing (512 bits/s)						
f_{DI}	data input rate	SPF byte 01 Hex; bits D5, D4 = 0 0	–	512	–	bits/s
t_{BIT}	bit duration		–	1.9531	–	ms
t_{CW}	codeword duration		–	62.5	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms
POCSAG data timing (1200 bits/s)						
f_{DI}	data input rate	SPF byte 01 Hex; bits D5, D4 = 1 0	–	1200	–	bits/s
t_{BIT}	bit duration		–	833.3	–	µs
t_{CW}	codeword duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
POCSAG data timing (2400 bits/s)						
f_{DI}	data input rate	SPF byte 01 Hex; bits D5, D4 = 1 1	–	2400	–	bits/s
t_{BIT}	bit duration		–	416.6	–	µs
t_{CW}	codeword duration		–	13.3	–	ms
t_{PA}	preamble duration		240	–	–	ms
t_{BAT}	batch duration		–	226.6	–	ms
Synthesizer control						
t_{ZSU}	synthesizer set-up duration	oscillator running; note 4	1	–	2	bits
f_{ZSC}	output clock frequency	note 5	–	38400	–	Hz
t_{ZCL}	clock pulse duration		–	13.02	–	µs
t_{ZSD}	data bit duration	note 5	–	26.04	–	µs
t_{ZDS}	data bit set-up time		–	13.02	–	µs
t_{ZDL1}	data load enable delay		–	91.15	–	µs
t_{ZLE}	load enable pulse duration		–	13.02	–	µs
t_{ZDL2}	inter block delay		–	117.19	–	µs

Notes

1. 32768 Hz reference signal: 32 pulses per 75 clock cycles, alternately separated by 1 or 2 pulse periods (pulse duration: t_{RFP}). The timing is shown in Fig.13.
2. 50 Hz reference signal: square-wave.
3. Fall time may be faster than prescribed in the I²C-bus specification. This does not influence the functionality but may cause more interference.
4. Duration depends on programmed bit rate; after reset t_{ZSU} = 1.5 bits.
5. Nominal values; pause in 12th data bit (see Table 12).

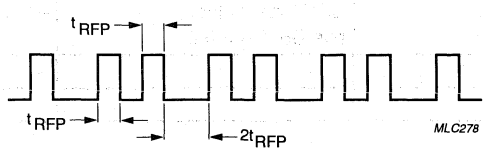


Fig.13 Timing of the 32768 Hz reference signal.

APPLICATION INFORMATION

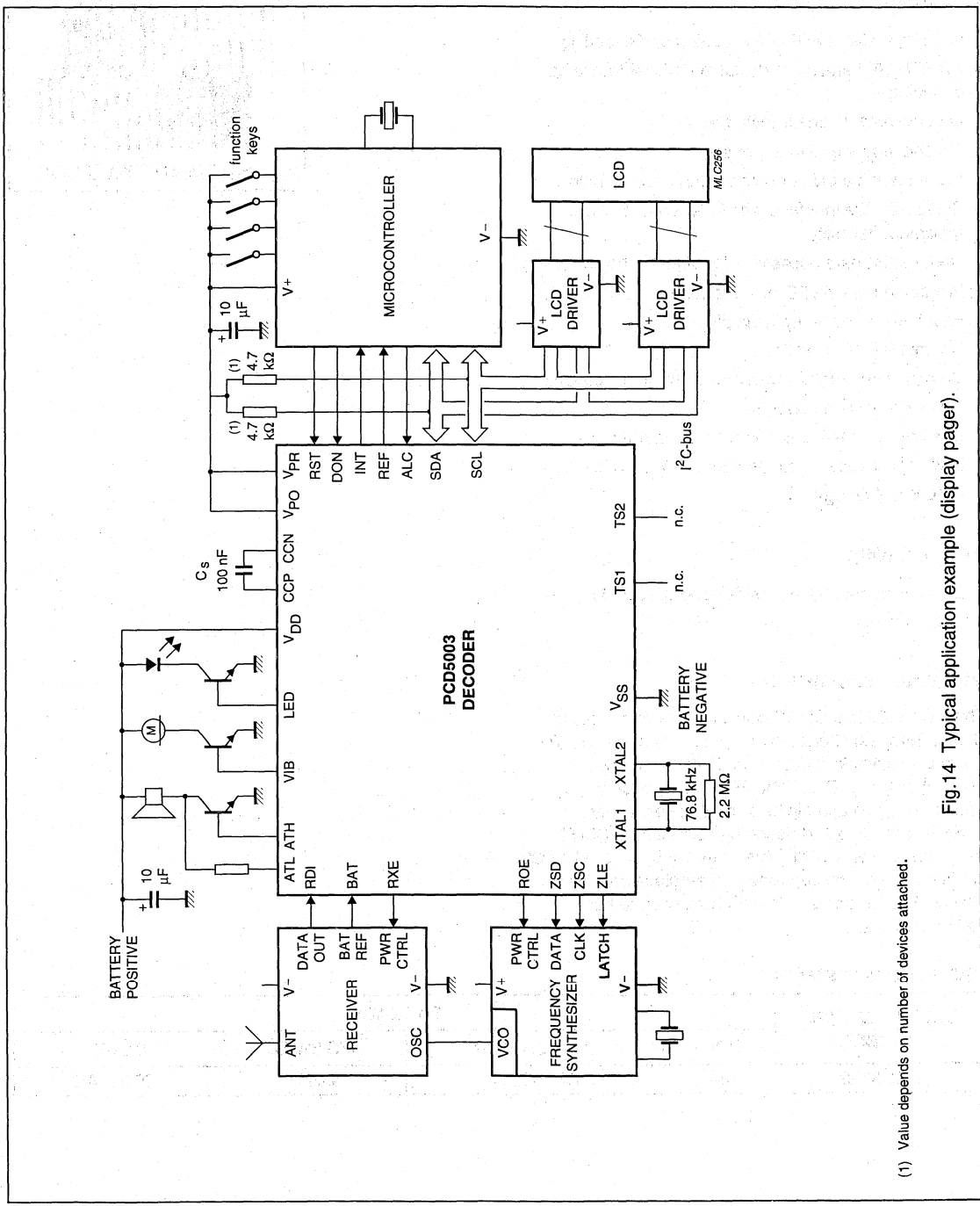
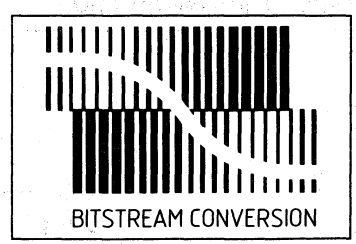


Fig.14 Typical application example (display pager).

(1) Value depends on number of devices attached.

ADPCM CODEC for digital cordless telephone

PCD5032



FEATURES

- G.721 compliant ADPCM encoding and decoding
- BITSTREAM analog-to-digital and digital-to-analog decoding
- On-chip receive and transmit filter
- On-chip ringer and tone generator
- Programmable gain of receive and transmit path
- Serial ADPCM interface with independent timing for maximum flexibility
- Linear PCM data accessible for digital echo cancelling
- Programmable via I²C-bus interface
- Fast receiver mute input via pin
- On-chip reference voltage
- On-chip symmetrical supply for electret microphone
- Few external components
- Low power consumption in standby mode
- Low supply voltage (single supply 2.7 V up to 6 V)
- CMOS technology

APPLICATIONS

- Digital European Cordless Telephony (DECT)
- CT2 cordless

GENERAL DESCRIPTION

The PCD5032 is a CMOS device designed for use in Digital European Cordless Telephone systems (DECT) but is also suitable for other cordless telephony applications (e.g. CT2). The PCD5032 performs analog-to-digital and digital-to-analog conversion, ADPCM encoding and decoding compliant to CCITT recommendation G.721 (blue book 1988). The PCD5032 contains on-chip microphone and earpiece amplifiers. The device can be used in both handset and base station designs.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD5032	44	QFP44S14	plastic	SOT205AG

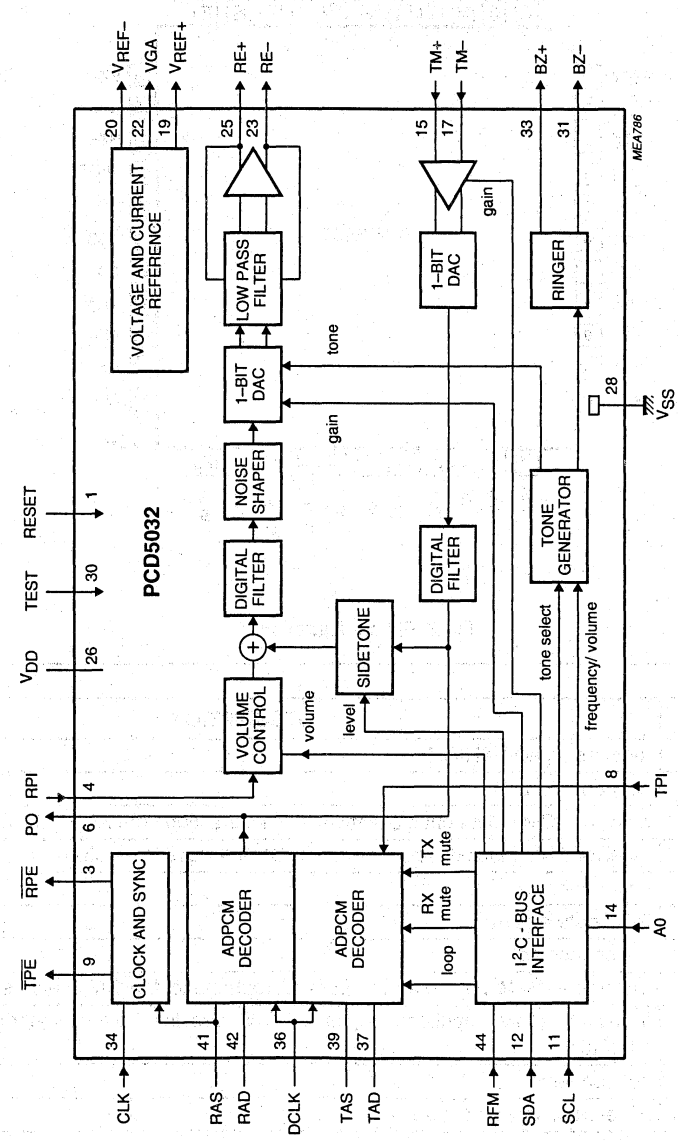


Fig.1 Block diagram.

PINNING

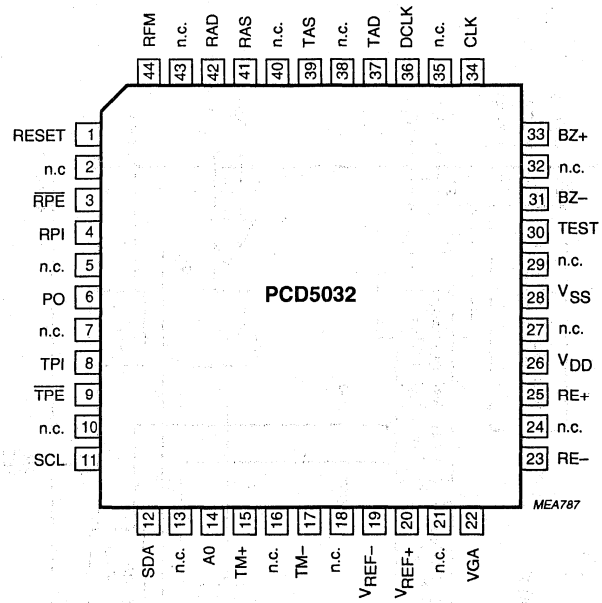


Fig.2 Pin configuration.

SYMBOL	PIN	DESCRIPTION
RESET	1	reset input; active HIGH
n.c.	2	not connected
$\overline{\text{RPE}}$	3	receiver PCM output enable (active LOW) ; direction from ADPCM interface to earpiece
RPI	4	receiver PCM input; direction from ADPCM interface to earpiece
n.c.	5	not connected
PO	6	PCM data output
n.c.	7	not connected
TPI	8	transmitter PCM input; direction from microphone to ADPCM interface
$\overline{\text{TPE}}$	9	transmitter PCM output enable (active LOW); direction from microphone to ADPCM interface
n.c.	10	not connected
SCL	11	serial clock input; I²C-bus
SDA	12	serial data input; I²C-bus
n.c.	13	not connected
A0	14	address select input; I²C-bus

SYMBOL	PIN	DESCRIPTION
TM+	15	transmitter audio positive input (microphone)
n.c.	16	not connected
TM–	17	transmitter audio negative input (microphone)
n.c.	18	not connected
V_{REF-}	19	negative reference voltage output; internally generated, intended for electret microphone supply
V_{REF+}	20	positive reference voltage output; internally generated, intended for electret microphone supply
n.c.	21	not connected
VGA	22	analog signal ground output
RE–	23	receiver audio negative output (earpiece)
n.c.	24	not connected
RE+	25	receiver audio positive output (earpiece)
V_{DD}	26	positive supply voltage (2.9 V to 6 V)
n.c.	27	not connected
V_{SS}	28	negative supply voltage (0 V)
n.c.	29	not connected
TEST	30	test mode input; to be connected to V_{SS} in normal application
BZ–	31	ringer negative output
n.c.	32	not connected
BZ+	33	ringer positive output
CLK	34	clock input
n.c.	35	not connected
DCLK	36	data clock input (ADPCM)
TAD	37	transmitter ADPCM data output; direction from microphone to ADPCM interface
n.c.	38	not connected
TAS	39	transmitter ADPCM sync input; direction from microphone to ADPCM interface
n.c.	40	not connected
RAS	41	receiver ADPCM sync input; direction from ADPCM interface to earpiece
RAD	42	receiver ADPCM data input; direction from ADPCM interface to earpiece
n.c.	43	not connected
RFM	44	receiver fast mute input; direction from ADPCM interface to earpiece

Note to the pin description

1. Pins 19, 20, 22, 26 and 28 are general pins.
   Pins 15, 17, 23, 25, 31 and 33 are analog pins.
   Pins 1, 3, 4, 6, 8, 9, 11, 12, 14, 30, 34, 36, 37, 39, 41, 42 and 44 are digital pins.

APPLICATION INFORMATION

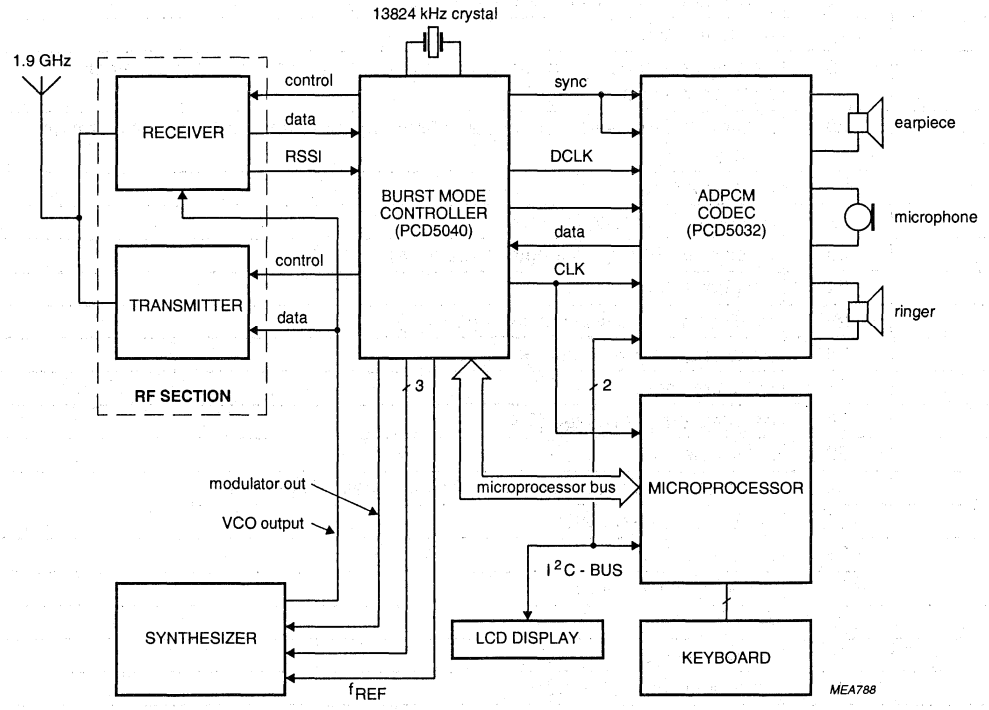


Fig.3 Typical block diagram for a DECT handset.

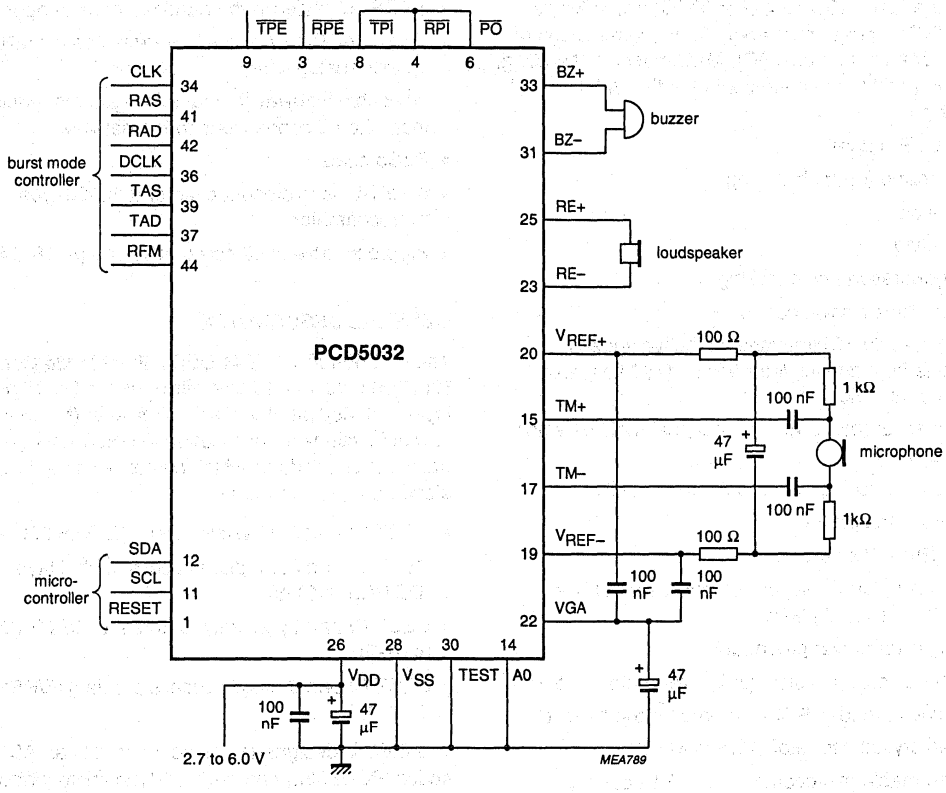


Fig.4 Typical handset application diagram for the PCD5032.

DECT burst mode controller PCD5040/PCD5041

FEATURES

- An embedded RISC controller (PCC) with 4 k byte (RAM/ROM) program memory for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning and the general control of the BMC hardware
- PP and FP modes
- TDMA frame (de)multiplexing
- Encryption
- Scrambling
- CRC generation and checking
- Beacon transmission control
- Switches up to 12 simultaneous active speech channels from speech interface to 1152 kbs radio interface, and vice versa
- RSSI measurement with on-chip peak/hold detector and 4-bit ADC
- Local call switching for up to 6 internal calls
- Quality control report
- Digital Phase-Locked Loop
- Synchronization (handset to active bearer, base station to cluster of RFPs)
- Seamless handover procedure
- Fast (hardware) and slow (software) mute function
- 1.5 k byte extended RAM memory for the handset
- On-chip crystal oscillator (13.824 MHz)
- Programmable microcontroller clock frequency
- Programmable interrupts
- Low power consumption in standby mode
- Low supply voltage (2.7 V to 6 V)
- SACMOS technology

Interfaces to:

- 1 ADPCM codec in the handset mode of operation
- Up to 2 ADPCM codecs in a simple base station (with up to 2 analog lines)
- 2048 kb/s highway interface for systems requiring more than 2 connections to the network
- Radio head
- 80C51-type microcontroller, or a 68000-type microcontroller
- Programmable synthesizer interface (8, 16, 24 bits)

GENERAL DESCRIPTION

The PCD5040/PCD5041 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT physical layer and Medium Access Control layer (MAC) time critical functions for application in DECT handset and base station products which comply with the following standards (plus updates):

- DECT CI part 2; physical layer (DE/RES 3001-2)
- DECT CI part 3; medium access control layer (DE/RES 3001-3)
- DECT CI part 7; security features for DECT (DE/RES 3001-7)
- DECT CI part 9; public access profile (DE/RES 3001-9)

The BMC is designed to be connected to an ADPCM codec (PCD5032) and an 8051-type microcontroller without glue logic. Other codecs and microcontrollers (e.g. 68000-family) are also supported. Two versions of the BMC will become available. The PCD5040 will have a RAM supported memory containing the BMC firmware, while the PCD5041 has a ROM instead. Both versions have the same pinning.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD5040/PCD5041	64	QFP64REC	plastic	SOT208A

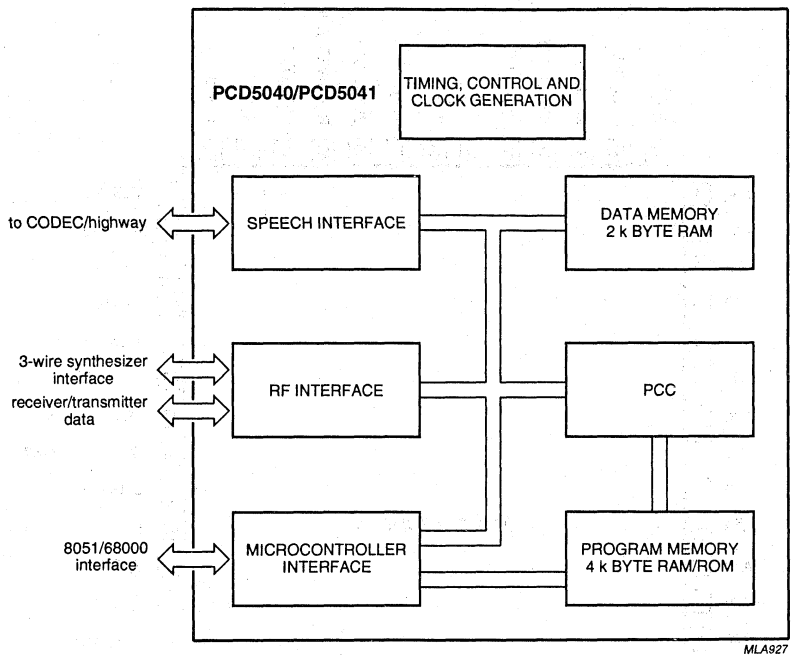


Fig.1 Block diagram.

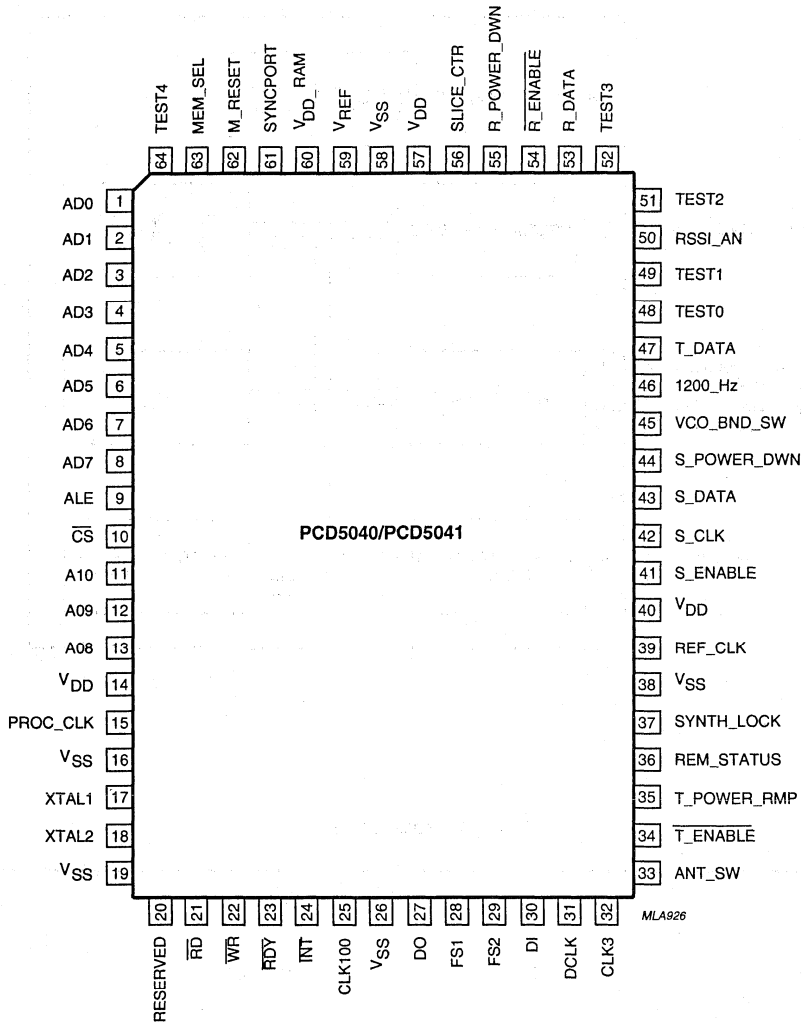


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
AD0 to AD7	1 to 8	address/data bus input/output lines
ALE	9	address latch enable input
$\overline{CS}$	10	chip select input; active LOW
A10 to A8	11 to 13	address bus input lines
V_{DD}	14	positive supply voltage
PROC_CLK	15	microcontroller clock output; programmable from $f_{CLK/96}$ to f_{CLK}, where f_{CLK} is the crystal oscillator frequency
V_{SS}	16	negative supply voltage
XTAL1	17	crystal oscillator input
XTAL2	18	crystal oscillator output
V_{SS}	19	negative supply voltage
RESERVED	20	reserved
$\overline{RD}$	21	read input; active LOW
$\overline{WR}$	22	write input; active LOW
$\overline{RDY}$	23	ready signal output; active LOW, to initiate wait states in the microcontroller
$\overline{INT}$	24	interrupt output; active LOW
CLK100	25	100 Hz frame timer output
V_{SS}	26	negative supply voltage
DO	27	3-state data output on the speech interface
FS1	28	8 kHz framing signal output to ADPCM codec 1 for simple base plus handset, otherwise 8 kHz framing input
FS2	29	8 kHz framing signal output to ADPCM codec 2 in the base station mode
DI	30	data input on the speech interface
DCLK	31	1152 kHz data clock output for simple base plus handset, otherwise 2048 kHz data clock input signal
CLK3	32	3.456 MHz clock output; nominal value, used to adjust system timing
ANT_SW	33	switch output; selects one of two antennas
$\overline{T\_ENABLE}$	34	transmitter enable input; active LOW
T_POWER_RMP	35	transmitter power ramp control output
REM_STATUS	36	8-bit serial data input; can be read in for each s-lot
SYNTH_LOCK	37	lock indication input from synthesizer
V_{SS}	38	negative supply voltage
REF_CLK	39	reference frequency output for the synthesizer; i.e. the crystal oscillator clock f_{CLK}
V_{DD}	40	positive supply voltage
S_ENABLE	41	synthesizer enable output
S_CLK	42	clock signal output; to be used with S_DATA
S_DATA	43	serial data output to the synthesizer
S_POWER_DWN	44	synthesizer power down control output

SYMBOL	PIN	DESCRIPTION
VCO_BND_SW	45	VCO bandswitch control signal output
1200_Hz	46	control signal output for dual synthesizer schemes
T_DATA	47	serial data output to transmitter
TEST0	48	input to select test mode 0; normal operation set to logic 0
TEST1	49	input to select test mode 1; normal operation set to logic 0
RSSI_AN	50	analog input signal for basic DECT systems; peak signal strength measured after a low-pass filter
TEST2	51	input to select test mode 2; normal operation set to logic 0
TEST3	52	input to select test mode 3; normal operation set to logic 0
R_DATA	53	receive data input
$\overline{\text{R\_ENABLE}}$	54	receiver enable output; active LOW
R_POWER_DWN	55	receiver power down output
SLICE_CTR	56	slice time constant control output
V_{DD}	57	positive supply voltage
V_{SS}	58	negative supply voltage
V_{REF}	59	reference input fot the ADC
V_{DD}_RAM	60	positive supply voltage for data RAM
SYNCPORT	61	this signal is the SYNCPORT input/output in the base station; it is an output in a master base station, input in a slave base station, in accordance with Annex C, DECT CI specification part 2. SYNCPORT is not active in the handset
M_RESET	62	BMC master reset input signal
MEM_SEL	63	input to select PCC program memory at the microcontroller interfcae
TEST4	64	input to select test mode 4; normal operation set to logic 0

Power failure detector and reset generator

PCF1252-X family

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

GENERAL DESCRIPTION

The PCF1252-X family are CMOS voltage detectors designed especially for power-ON/OFF detection in microcontroller/microprocessor systems (for initialization and data storage purposes). The output $\overline{POWF}$ is activated at a precise, temperature stable, trip-point. The RESET output has a built-in delay with duration determined by an external capacitor (C_{CT}). A second comparator (comparator 2) has been included to allow for the possibility of a second monitoring point in the system.

Features

- Low current consumption, typically 6 μA
- 10 versions available, trip-points vary from 2.55 V to 4.75 V
- Temperature stable trip-point
- Variable RESET delay
- Reset polarity selection
- Comparator for second level detection (e.g. overvoltage detection)
- Advance warning of power failure

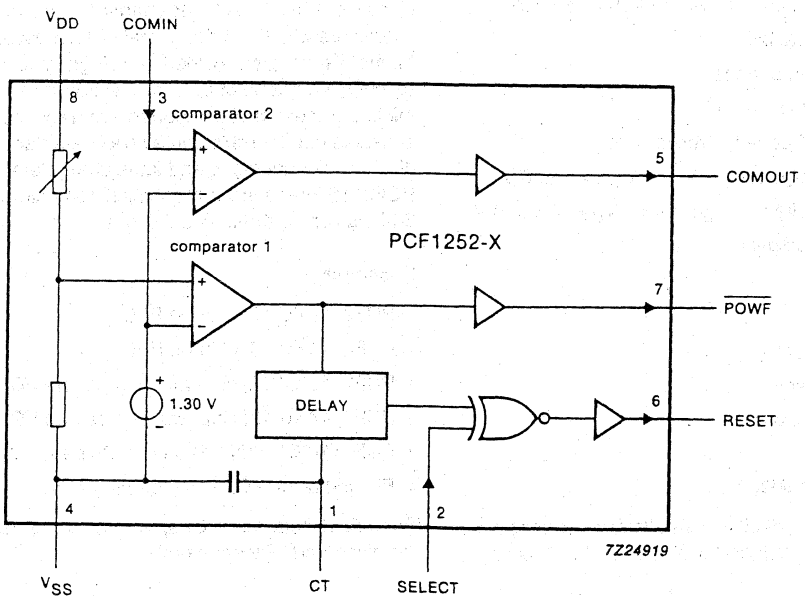


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF1252-XP: 8-lead DIL; plastic (SOT97).
PCF1252-XT: 8-lead mini-pack; plastic (SO8; SOT96A).

LCD controller/drivers

PCF2116 family (PCF2114X; PCF2116X)

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

FEATURES

- Single chip LCD controller / driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF2116 family of LCD controller/drivers consists of 2 similar members: PCF2116X and PCF2114X, later referred to as PCF2116. The specific differences are expressed in separate paragraphs for PCF2116X and PCF2114X respectively. The letter X in PCF2116X or PCF2114X specifies the character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, G and J (see Figs 7 to 10). Set 'A' in PCF2116A characterises the built-in standard character set. Other character sets are available on request.

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana characters. The PCF2116 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus.

Packages

- PCF2116XU/10; chip on FFC
- PCF2114XU/10; chip on FFC
- PCF2116XU/12; chip with bumps on FFC
- PCF2114XU/12; chip with bumps on FFC
- PCF2116XH; SQFP128 (14 × 20 mm)
- Pin grid array PGA144 (samples only).

For further details see Chapters "Bonding pad locations"and "Package outline".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF2114XH	128	SQFP128	plastic	SOT387-1
PCF2116XH	128	SQFP128	plastic	SOT387-1
PCF2114XU	116	FFC116	–	–
PCF2116XU	116	FFC116	–	–

BLOCK DIAGRAM

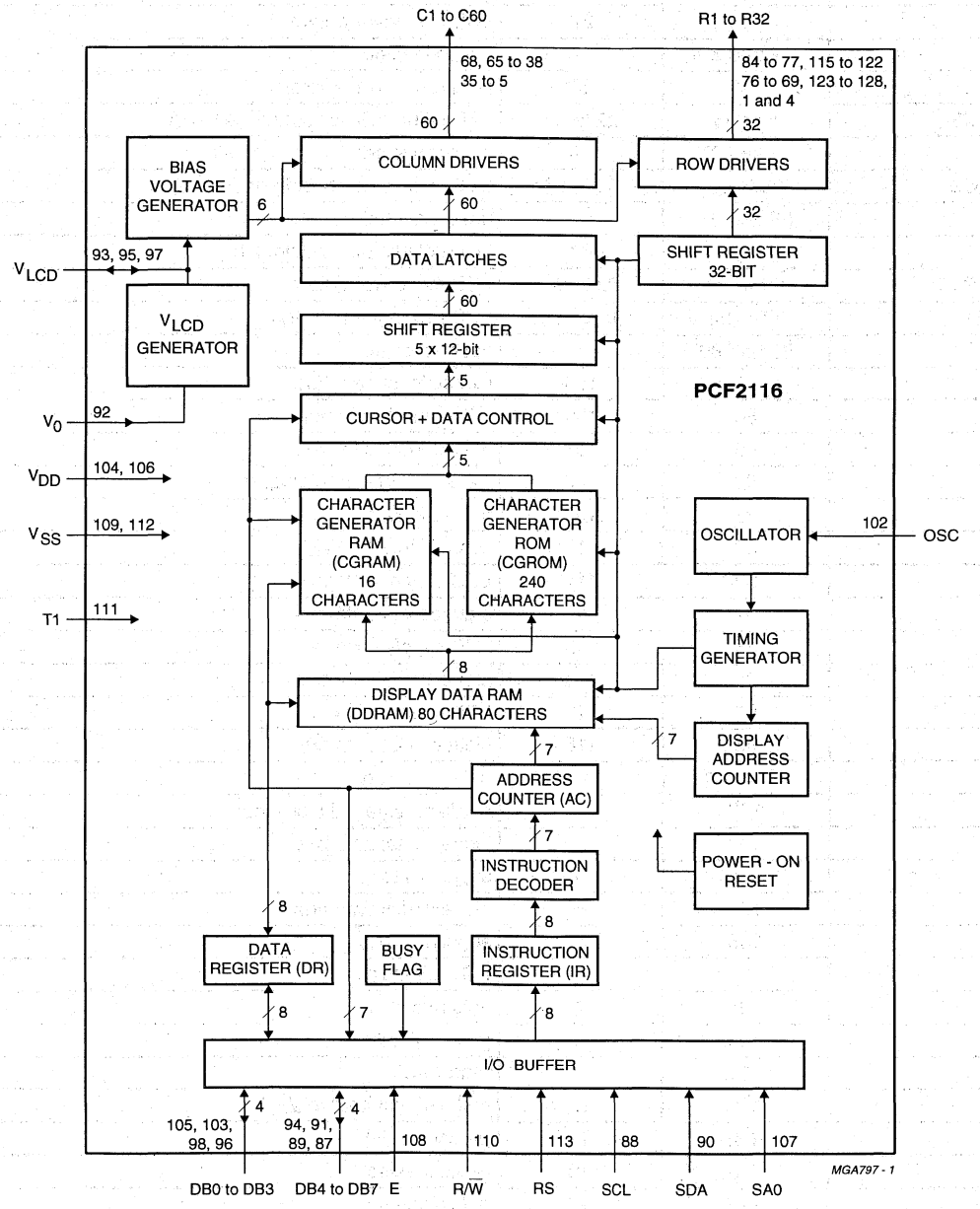


Fig.1 Block diagram (SQFP128).

PINNING

SYMBOL	SQFP128 PIN	FFC PAD	DESCRIPTION
R31	1	27	LCD row driver output
n.c.	2 and 3	–	not connected
R32	4	28	LCD row driver output
C60 to C30	5 to 35	29 to 59	LCD column driver outputs 60 to 30
n.c.	36 and 37	–	not connected
C29 to C2	38 to 65	60 to 87	LCD column driver outputs 29 to 2
n.c.	66 and 67	–	not connected
C1	68	88	LCD column driver output 1
R24 to R17	69 to 76	89 to 96	LCD row driver outputs
R8 to R1	77 to 84	97 to 104	LCD row driver outputs
n.c.	85 and 86	–	not connected
DB7	87	105	bidirectional data bus
SCL	88	106	I^2C serial clock input
DB6	89	107	bidirectional data bus
SDA	90	108	I^2C serial data input/output
DB5	91	109	bidirectional data bus
V_0	92	110	control input for V_{LCD}
V_{LCD1}	93	111	LCD supply voltage
DB4	94	112	bidirectional data bus
V_{LCD2}	95	113	LCD supply voltage
DB3	96	114	bidirectional data bus
V_{LCD3}	97	115	LCD supply voltage
DB2	98	116	bidirectional data bus
n.c.	99 to 101	–	not connected
OSC	102	1	oscillator/external clock input
DB1	103	2	bidirectional data bus
V_{DD2}	104	3	supply voltage
DB0	105	4	bidirectional data bus
V_{DD1}	106	5	supply voltage
SA0	107	6	I^2C address pin
E	108	7	data bus clock
V_{SS1}	109	8	ground (logic)
$R/\overline{W}$	110	9	read/write
T1	111	10	test pad (connect to V_{SS})
V_{SS2}	112	11	ground (logic)
RS	113	12	register select
n.c.	114	–	not connected
R9 to R16	115 to 122	13 to 20	LCD row driver outputs
R25 to R30	123 to 128	21 to 26	LCD row driver outputs

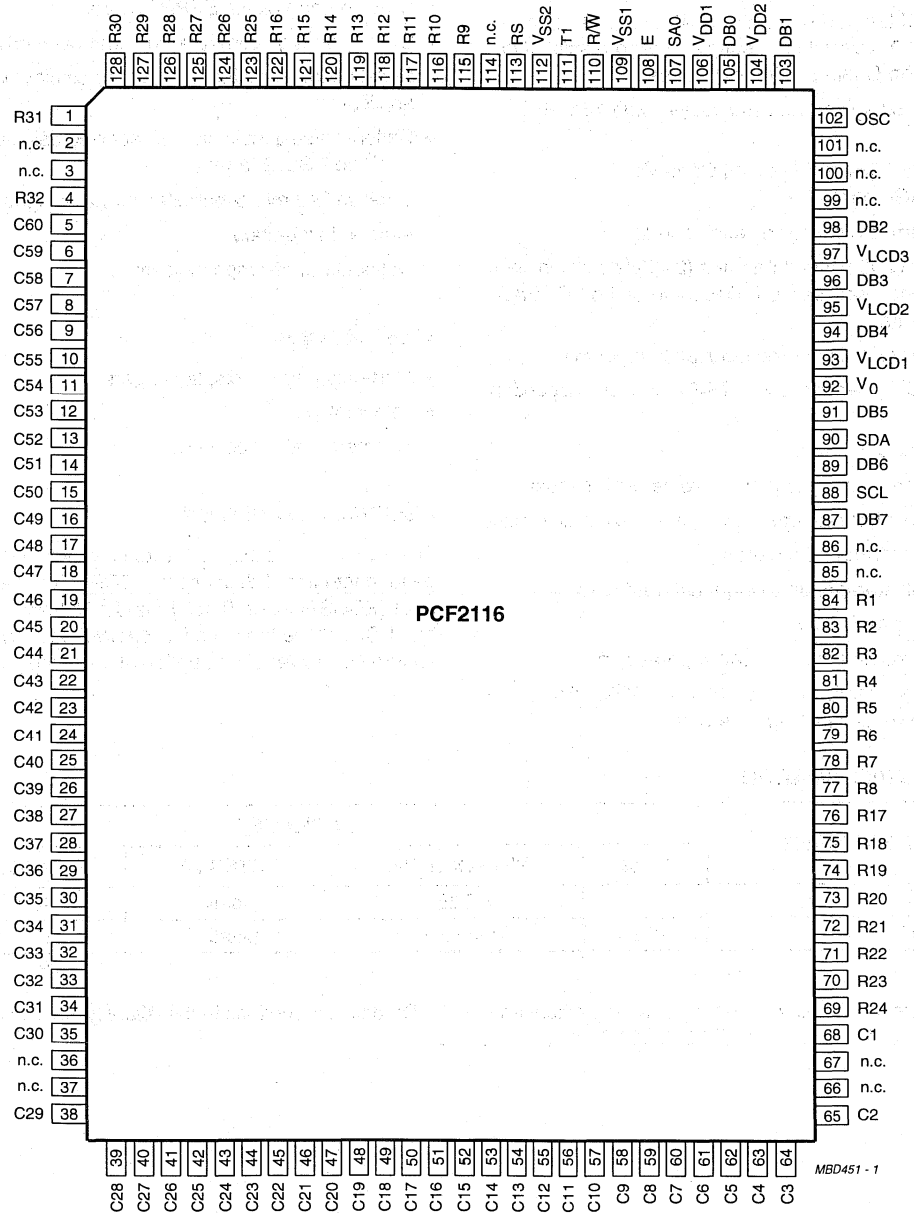


Fig.2 Pin configuration (SQFP128).

POCSAG Paging Decoder PCF5001

FEATURES

- Wide operating supply voltage range (1.5 to 6.0 V)
- Extended temperature range: –40 to +85 °C (between –40 to –10 °C, minimum supply voltage restricted to 1.8 V), see Chapter "Limiting values"
- Very low supply current (60 µA typ. with 76.8 kHz crystal)
- Decodes CCIR radio paging Code No. 1 (POCSAG-code)
- Programmable call termination conditions
- 512 and 1200 bits/s data rates (2400 bits/s with some restrictions), see Section "Decoding of the POCSAG data stream"
- Improved ACCESS synchronization algorithm
- Supports 4 user addresses (RICs) in two independent frames
- Eight different alert cadences
- Directly drives magnetic or piezo ceramic beeper
- High level alert requires only a single external transistor
- Optional vibrator type alerting
- Silent call storage, up to eight different calls
- Repeat alarm facility
- Programmable duplicate call suppression
- Interfaces directly to UAA2033T, UAA2050T and UAA2080 digital paging receivers
- Programmable receiver power control for battery economy
- On-chip non-volatile EEPROM storage
- On-chip voltage converter with improved drive capability
- Serial microcontroller interface for display pager applications
- Optional visual indication of received call data using a modified RS232 format
- Level shifted microcontroller interface signals
- Alert on low battery
- Optional out-of-range indication.

APPLICATIONS

- Alert-only pagers, display pagers
- Telepoint
- Telemetry/data receivers.

GENERAL DESCRIPTION

The PCF5001 is a fully integrated low-power decoder and pager controller. It decodes the CCIR radio paging Code No.1 (POCSAG-Code) at 512 and 1200 bits/s data rates. The PCF5001 is fabricated in SACMOS technology to ensure low power consumption at low supply voltages.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF5001T	28	SO28L	plastic	SOT136-1
PCF5001H	32	TQFP32[1]	plastic	SOT358-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

BLOCK DIAGRAMS

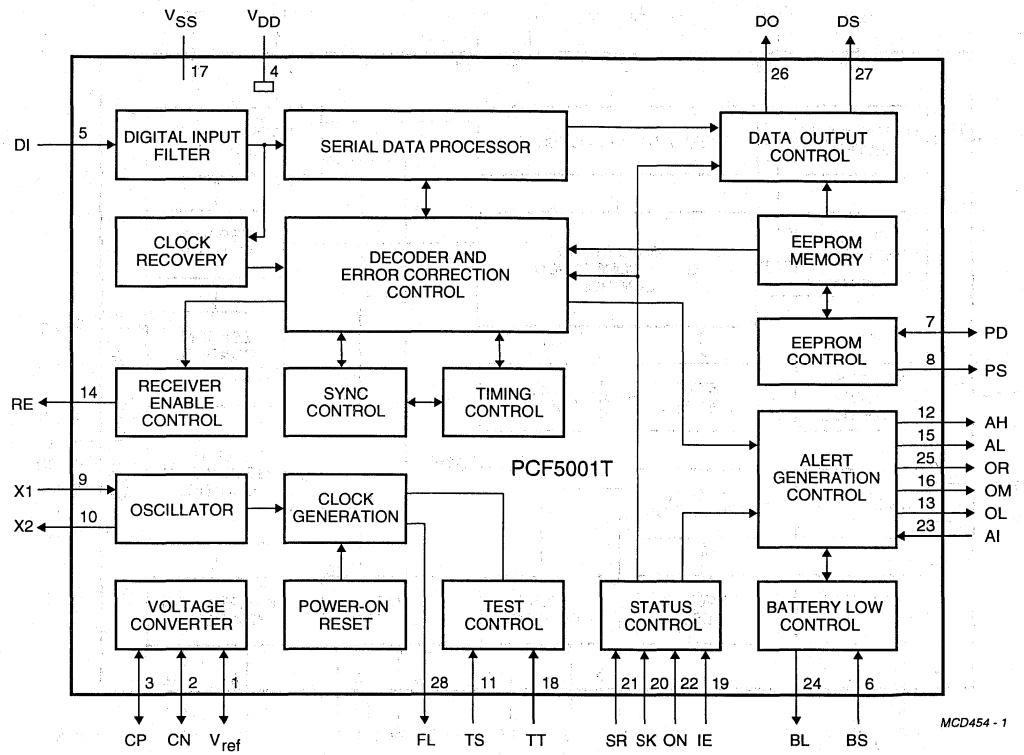


Fig.1 Block diagram (SO28L; SOT136-1).

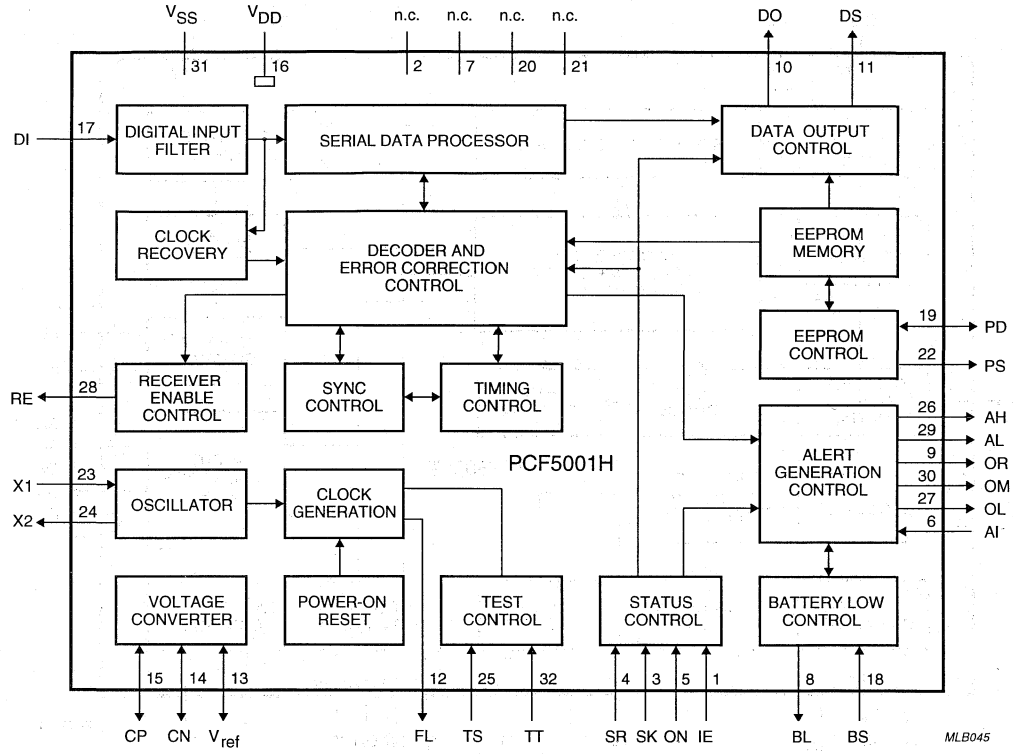


Fig.2 Block diagram (TQFP32; SOT358-1).

PINNING

SYMBOL	PIN		DESCRIPTION
	SO28L SOT136-1	TQFP32 SOT358-1	
V_{ref}	1	13	Microcontroller interface reference voltage output. The LOW level of pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE is related to the voltage on V_{ref}. May be driven from an external negative voltage source or must be connected to V_{SS}, if pins CN and CP are left open-circuit. When the on-chip voltage converter is used, this pin provides a negative output voltage.
CN	2	14	Voltage converter external shunt capacitance, negative side. Connect the negative side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
CP	3	15	Voltage converter external shunt capacitor, positive side. Connect the positive side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
V_{DD}	4	16	Main positive power supply. This pin is common to all supply voltages and is referred to as 0 V (common).
DI	5	17	Serial data input (POCSAG code). The serial data signal train applied to this pin is processed by the decoder. Pulled LOW by an on-chip pull-down when the receiver is disabled (RE = LOW).
BS	6	18	Battery-low indication input. The decoder samples this input during synchronization scan, when it is in ON or SILENT status and the receiver is enabled (RE = HIGH). A battery-low condition is assumed, if the decoder detects four consecutive samples HIGH. An audible battery-low indication is made by the decoder, when operating in ON status. Normally LOW by the operation of an on-chip pull-down.
PD	7	19	EEPROM programming data input and output. Normally HIGH by the operation of an on-chip pull-up. During programming of the on-chip EEPROM, PD is a bidirectional data and control signal.
PS	8	22	EEPROM programming strobe input. Normally LOW by the operation of an on-chip pull-down. During programming of the on-chip EEPROM, PS is a unidirectional control input.
X1	9	23	Crystal oscillator input. Connect a 32768 Hz or 76800 Hz crystal and a biasing resistor between this pin and X2. In addition, provide a load capacitance to V_{DD}, which may also be used for frequency tuning.
X2	10	24	Crystal oscillator output. Return connection for the external crystal and resistor at X1.
TS	11	25	Scan test mode enable input. Always LOW by operation of an on-chip pull-down.
AH	12	26	Alert HIGH-level output. This output can directly drive an external bipolar transistor to control HIGH-level alerting in conjunction with AL, by means of an alerter or beeper.
OL	13	27	LED indication output. This output can directly drive an external bipolar transistor to control the visual alert function by means of an LED. It may also be used for visual indication of received call data during call reception.

SYMBOL	PIN		DESCRIPTION
	SO28L SOT136-1	TQFP32 SOT358-1	
RE	14	28	Receiver enable output. May be used to control the paging receiver power control input, to minimize power consumption. The decoder provides a HIGH-level at this pin, when receiver operation is requested. Each time the decoder does not require any input data at DI the receiver enable output is LOW.
AL	15	29	Alert LOW-level output. Open drain alert output in anti-phase to AH, to provide LOW-level alerting. HIGH-level alerting is generated in conjunction with AH.
OM	16	30	Vibrator output. This output can directly drive an external bipolar transistor to control a vibrator type alerter.
V_{SS}	17	31	Main negative supply voltage.
TT	18	32	Test mode enable input. Always LOW by operation of an on-chip pull-down.
IE	19	1	Interface enable input. While the interface enable input is active HIGH, operation of the ON, SK, SR, AI, BL and OR inputs and outputs is possible. When IE is LOW the inputs do not respond to applied signals and the outputs are made high-impedance. In alert only pager mode the interface enable input does not have any effect on the operation of inputs ON, SK and SR, but IE must be referenced to LOW or HIGH.
SK	20	3	Silent state control input. The silent control input selects the decoder ON status (LOW-level) or SILENT status (HIGH-level), if the ON input is active HIGH. An on-chip pull-up is provided, if the decoder has been programmed for alert-only pager mode, whereby the pull-up is disabled for display pager mode. In display pager mode status change is possible provided the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
SR	21	4	Status request and reset input. A HIGH-going pulse on this input causes (a) status indication cadence to be generated, if the decoder is not alerting or (b) resetting of a call alert, repeated call alert or battery-low alert, if active or (c) triggers the call store re-alert facility, if repeat mode is active. In display pager mode operation of SR is possible only, if the interface control input is active. Normally LOW by the operation of an on-chip pull-down.
ON	22	5	On/off control input. The on/off control input selects the decoder ON status (HIGH-level) or OFF status (LOW-level). An on-chip pull-up resistor is provided, if the decoder has been programmed for alert-only pager mode, but the pull-up resistor is disabled for display pager mode. In display pager mode status change is possible provided the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
AI	23	6	Alarm input. A HIGH-level on this input causes generation of a continuous HIGH-level alert via AH and AL outputs, if the decoder operates in ON status or OFF status. In addition, the LED output is active independent from the decoder status, but in accordance with AI. Pulsing the input may be used to modulate the alert and LED indication. Normally LOW in alert-only pager mode by operation of an on-chip pull-down.

SYMBOL	PIN		DESCRIPTION
	SO28L SOT136-1	TQFP32 SOT358-1	
BL	24	8	Battery-low indication output. If the decoder encounters a battery-low condition a battery-low output latch is set HIGH. The battery-low output latch may be tested for a battery-low condition, whenever the interface enable input (IE) is active (HIGH), otherwise the battery-low output is made high-impedance. The battery-low output latch is reset only, by switching the decoder to OFF status.
OR	25	9	Out-of-range indication output. Whenever the decoder detects an out-of-range condition an out-of-range output latch is set HIGH after expiry of the programmed out-of-range hold-off time selected by means of special programming (SPF06 and SPF07) of the EEPROM. The out-of-range latch may be tested for an out-of-range condition, whenever the interface enable input (IE) is active (HIGH), otherwise the out-of-range output is made high-impedance. The out-of- range output is reset by detection of a valid data transmission or by switching the decoder to OFF status.
DO	26	10	Serial interface data output. During normal decoder operation, accepted calls and possibly subsequent message data are serially output via this pin in conjunction with the data strobe output (DS). This pin is also used to output the EEPROM contents upon special command, if the decoder is programmed for display pager.
DS	27	11	Serial interface data strobe output. Provides a clock signal for the received call data and EEPROM data appearing at the data output (DO). Each time this output is LOW the data at DO is valid. Additional start and stop conditions allow easy identification of data sequence start and end.
FL	28	12	Frequency reference output. When programmed for display pager mode, this output provides a clock reference with 16384 or 32768 Hz per second, selected by SPF32. See Chapter "Functional description" .
n.c.	–	2, 7, 20, 21	Not connected.

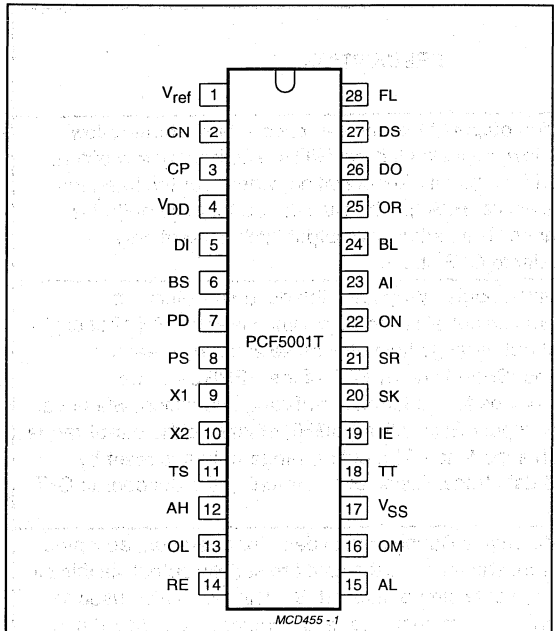


Fig.3 Pin configuration (SO28L; SOT136-1).

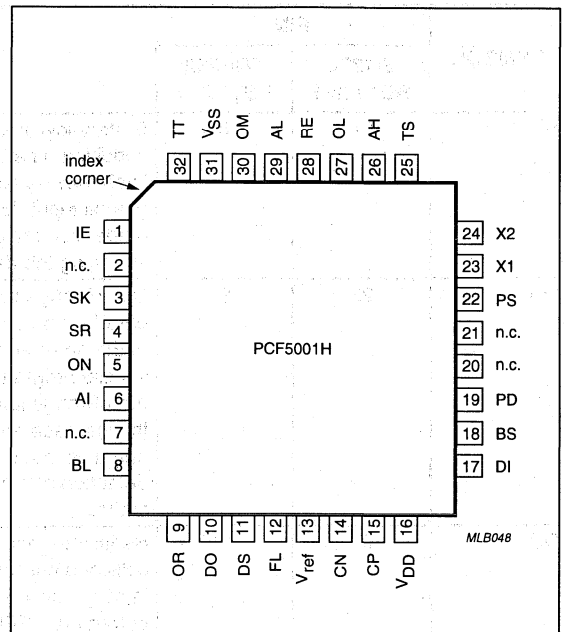


Fig.4 Pin configuration (TQFP32; SOT358-1).

FUNCTIONAL DESCRIPTION

The PCF5001 is a very low power Decoder and Pager Controller specifically designed for use in new generation radio pagers. The architecture of the PCF5001 allows for flexible application in a wide variety of radio pager designs.

The PCF5001 is fully compatible with *"CCIR radio paging Code Number 1"* (also known as the POCSAG code) operating at the originally specified 512 bits/s data rate, and also at the newly specified 1200 bits/s data rate (2400 bits/s operation is also possible). The PCF5001 also offers features which extend the basic flexibility and efficiency of this code standard.

The PCF5001 supports two basic modes of operation

In Alert-Only-Pager mode only a minimum number of external components are required to build a complete tone-only pager. Selection of operating states ON, OFF or SILENT is achieved using a slider switch interface.

In Display-Pager mode the state input logic is switched to a bus interface structure. Received calls and messages are transferred to an external microcontroller via the serial microcontroller interface. A built-in voltage converter with increased drive capabilities can supply doubled supply voltage output, and appropriate logic level shifting on microcontroller interface signals is provided.

Upon reception of valid calls one of eight different call cadences is generated; upon status interrogation status indication tones make the current status of the decoder available to the user.

On-chip non-volatile 114-bit EEPROM storage is provided to hold up to four user addresses, two frame numbers and the programmed decoder configuration.

Synchronization to the input data stream is achieved using the improved ACCESS algorithm, which allows for data synchronization and re-synchronization without preamble detection while minimizing battery power consumption by receiver power control. One of four error correction algorithms is applied to the received data to optimize the call success rate.

The POCSAG paging code

A transmission using the CCIR radio paging Code No.1 (POCSAG code) is constructed in accordance with the following rules (see Fig.5).

The transmission is started by sending a preamble, which is a sequence of at least 576 continually alternating bits (10101010...). The preamble precedes a number of batch blocks. The transmission is terminated after the last batch.

Each batch comprises a synchronization codeword with a fixed 32-bit pattern followed by eight frames (numbered 0 to 7). Only complete batches are transmitted.

A frame consists of two codewords, each 32-bits long. A codeword is either an address or a message or an idle codeword. Idle codewords are transmitted to fill empty batches or to separate messages.

An address codeword is coded as shown in Fig.5. The upper 18-bits of the 21-bit digital user address (or RIC = Receiver Identification Code) are coded in the codeword itself (bits 2 to 19), which is protected against transmission errors by a number of CRC check bits (bits 22 to 31). Bit 32 is a simple overall even-parity bit. The lower three bits of the digital user address are coded in the number of the frame, in which the address codeword is transmitted. Two function bits (bits 20 and 21) allow distinguishing of four different calls to one user address.

In a message codeword 20-bits of any display information can be put into the message bits, which are protected again by additional check bits.

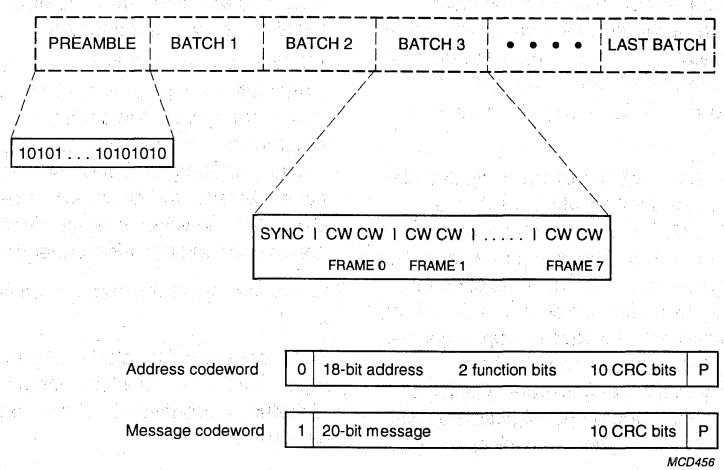


Fig.5 POCSAG code structure.

Modes and states of the decoder

The PCF5001 supports two basic operating modes:

- Alert-only pager
- Display pager mode.

Two further modes, the Programming mode and the Test mode, are implemented to program and verify the EEPROM contents and to support pager production and approval tests, respectively.

In Alert-only pager mode no external microcontroller is required, see Fig.21. A three position slider switch interface is provided to select the internal state of the decoder. The decoder performs regular scanning of the switch inputs to detect a status change. A push-button interface is provided on the SR input, which is used as input for user acknowledgment actions and status interrogation. Upon reception of valid calls, tone alert cadences are generated. A call storage is provided to store calls received while operating in Silent status and to recall cadences upon repeat mode operation. The voltage doubler and the frequency reference output are disabled in this mode.

In Display pager mode the PCF5001 operates as decoder and pager controller in combination with an external microcontroller, see Fig.22. The internal states of the decoder are determined by appropriate logic levels on the status inputs. A bus type interface structure is used to interface the decoder to the microcontroller. The decoder's on-chip voltage converter provides doubled supply voltage output to provide a higher supply voltage to the microcontroller and any additional hardware. The logic levels of the interface's input and output signals are level shifted to allow for direct coupling between microcontroller and the decoder. Upon detection of a valid call, address and message information are transferred to the external microcontroller using the serial microcontroller interface. In addition, appropriate call alert cadences are generated.

If the decoder is in one of the two operating modes, it is always in one of the following three internal states:

- OFF status. This is the power saving, inactive status of the PCF5001. The paging receiver is disabled, no decoding of input data takes place. However, the crystal oscillator is kept running to ensure that scanning of the status inputs/status switch is maintained to allow changing into one of the following two active states.
- ON status. This is the normal active status of the decoder. Incoming calls are compared with the user addresses stored in the internal EEPROM. Upon detection of valid calls, alert cadences and LED indication are generated and data is shifted out at the serial microcontroller interface.
- SILENT status. The Silent status is the same as the On status with the exception that valid calls no longer cause generation of call alert cadences. Instead, if programmed as alert-only pager, the decoder stores up to eight different calls and generates appropriate alert cadences after the decoder has been put back into the On status. However, special silent override calls will cause generation of alert cadences, if enabled.

The decoder operating status is selected as indicated in Table 1.

When programmed for alert-only pager a switch debounce period is applied to the status inputs. For status change and status interrogation in display pager mode, see Figs 6 and 7.

Table 1 Truth table for decoder operating status.

ON INPUT	SK INPUT	OPERATING STATUS
0	0	OFF
0	1	OFF (EEPROM transfer mode; note 1)
1	0	ON
1	1	SILENT

Note

1. The EEPROM transfer mode applies to display pager mode only.

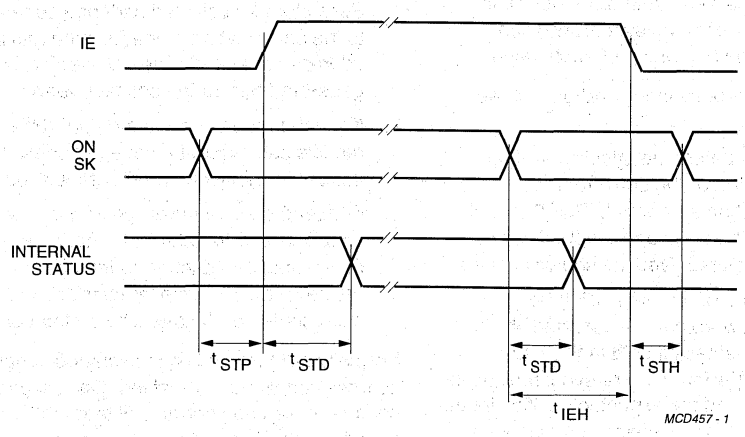


Fig.6 Status change in display pager mode.

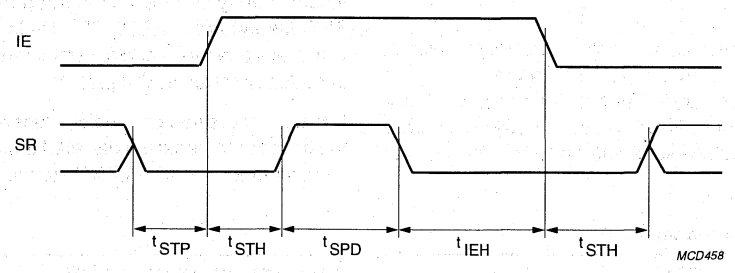


Fig.7 Status interrogation in display pager mode.

Decoding of the POCSAG data stream

The POCSAG coded input data stream is first noise filtered by a digital filter. From the filtered data a sampling clock synchronous to the data rate is derived. The PCF5001 supports 512 bits/s and 1200 bits/s data rates. This results in a 512 Hz or 1200 Hz sampling clock frequency, respectively. Synchronization on the POCSAG code structure is performed using the improved Philips ACCESS algorithm, which employs a state machine with six internal states.

A data rate of 2400 bits/s is possible if an external clock generator of 153.6 kHz is connected to X1. The minimum supply voltage is then −1.8 V.

The receiver enable output is activated a period equal to t_{RXON} before the input data is actually needed. The decoder has first to achieve bit and word synchronization before it can receive calls. The algorithm searches first for the preamble and then for synchronization codeword patterns. This is carried out for the duration of 3 batches in Power-on mode or 1 batch (=preamble duration) in Preamble Receive mode. Error correction algorithms are

applied to the data before it is compared with preamble and synchronization codeword patterns. The synchronization process is terminated and thus Data Receive mode entered as soon as synchronization codewords are seen at the beginning of each batch.

The decoder handles loss of synchronization in three steps:

1. If the decoder fails to detect the synchronization pattern at the beginning of the current batch it continues data reception as normal. This Data Fail mode is signalled in the message output when an address codeword was received, as shown in Table 4.
2. If also at the beginning of the next batch no synchronization codeword can be detected, the algorithm assumes a small bit shift in the Fade Recovery mode and performs more synchronization codeword checks around the expected position for the following 15 batches. Call reception is suspended.
3. If it fails to re-synchronize in the Fade Recovery mode, the Carrier Off mode is selected, in which the decoder attempts to regain synchronization by bit-wise shifting its synchronization scan window. Using this technique re-synchronization is obtained within a continuous data stream of at least 18 batches without preamble detection.

In Data Receive mode, the input data stream is sampled at the synchronization codeword position and the programmed frame positions. The received codewords are error corrected and then, if address codewords, compared with the stored user addresses related to that frame. On detection of a valid call, the decoder performs the following three operations:

1. Set a store for call alert cadence generation according to the combination of the function bits in the accepted address codeword. The call alert cadence will not be generated before the call has been terminated.
2. Keep the receiver enable output (RE) active and receive subsequent message codewords, until any of the call termination criteria are fulfilled.
3. Trigger the serial message transfer by sending a start condition and transfer deformatted message codewords as attached to the address codeword via the serial microcontroller interface to an external microcontroller, followed by a stop condition.

Normally call termination is assumed, when a valid idle or address codeword is received. On reception of uncorrectable codewords, call termination takes place in accordance with conditions shown in Table 2.

Generation of output signals

The PCF5001 provides output indications for call alert, repeat mode alert, out of range alert, battery-low alert, status indication alert and start-up alert. Some of the alert functions may be freely configured by programming of SPF bits within the EEPROM. Table 3shows the outputs which are used for special output indications, if the decoder operates in ON status.

Remark: reception of special silent override calls causes the decoder to generate call alert indication via AL and AH even if it operates in SILENT status.

Table 2 Call termination on error.

SPF12	SPF13	CALL TERMINATION EVENT
0	X[1]	Any two consecutive codewords or the codeword directly following the address codeword uncorrectable.
1	0	Any single codeword uncorrectable.
1	1	Any two consecutive codewords uncorrectable.

Note

1. X = don't care.

Table 3 Output signals.

ALERT FUNCTION	OUTPUT ACTIVE(1)					
	AL	AH	OL	OM	OR	BL
Start-up	(yes)	–	yes	yes	–	–
Status indication	yes	–	–	–	–	–
Call reception	(yes)	(yes)	yes	SPF11	–	–
Repeat mode	(SPF16)	(SPF16)	SPF16	–	–	–
Out-of-range	–	–	SPF15	–	yes	–
Battery-low	(yes)	(yes)	–	–	–	yes
Alarm input	(yes)	(yes)	yes	–	–	–

Note

1. Entries in parenthesis are not valid, if the decoder operates in SILENT status.

Alerter

The PCF5001 provides the AL and AH outputs for acoustical LOW-level and HIGH-level signalling. LOW-level alerting is provided by the AL output only. For HIGH-level alerting both, AL and AH are active in anti-phase. The square-wave output signals produce tone alert cadences by means of a magnetic or piezo ceramic beeper. The alert frequency, 2048 Hz or 2731 Hz square-wave, is selected by programming of SPF31.

When valid calls are received while operating in ON status, the PCF5001 generates call alert cadences. The first four seconds are generated at LOW-level, a further twelve seconds are generated at HIGH-level. Alert tone generation and LED indication automatically terminate after sixteen seconds unless terminated by pulsing the status request and reset input (SR). Call alert generation is inhibited until completion of message codeword reception and the termination word is sent by the decoder. Call alert generation commences after an alert delay period, t_{ALD}, at the earliest, see Fig.8. Call alert deletion is possible during the alert delay period.

The call alert cadence is modulated according to the two function bits (FC) in the received address codeword, see Fig.9.

Valid calls received on RIC B or RIC D cause the alerter frequency to be warbled by means of an additional 16 Hz and 1024 Hz signal (respective 1365 Hz for SPF31 = 1) as opposed to RIC A and RIC C where no alert frequency warble takes place. Thus, eight different call cadences are distinguishable.

On status interrogation by the status request and reset input (SR) the PCF5001 generates a status cadence at LOW-level, in accordance with the present internal decoder status (see Fig.10).

When detecting a battery-low condition the PCF5001 provides a battery-low indication. Operating in ON status causes generation of a battery-low alert at HIGH-level for sixteen seconds or until terminated by pulsing SR. Operating in SILENT status or repeat mode the battery-low alert is stored and inhibited until switching to ON status.

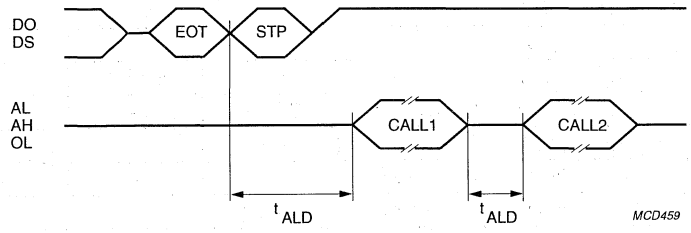


Fig.8 Call alert delay.

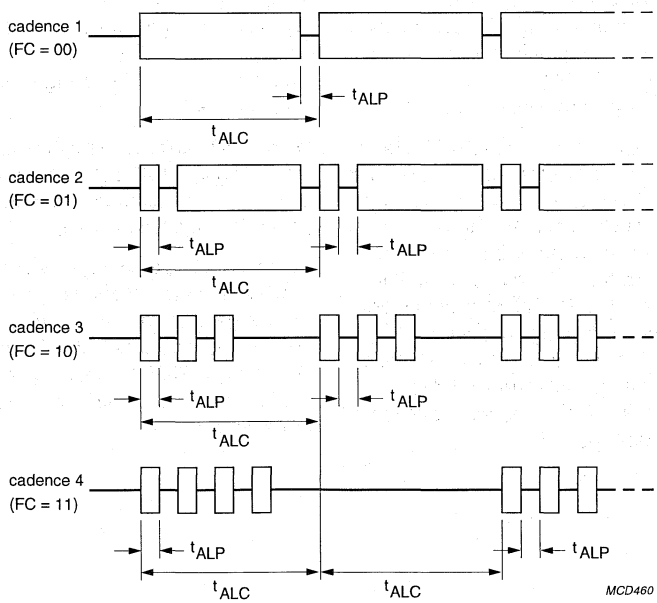


Fig.9 Call alert cadences.

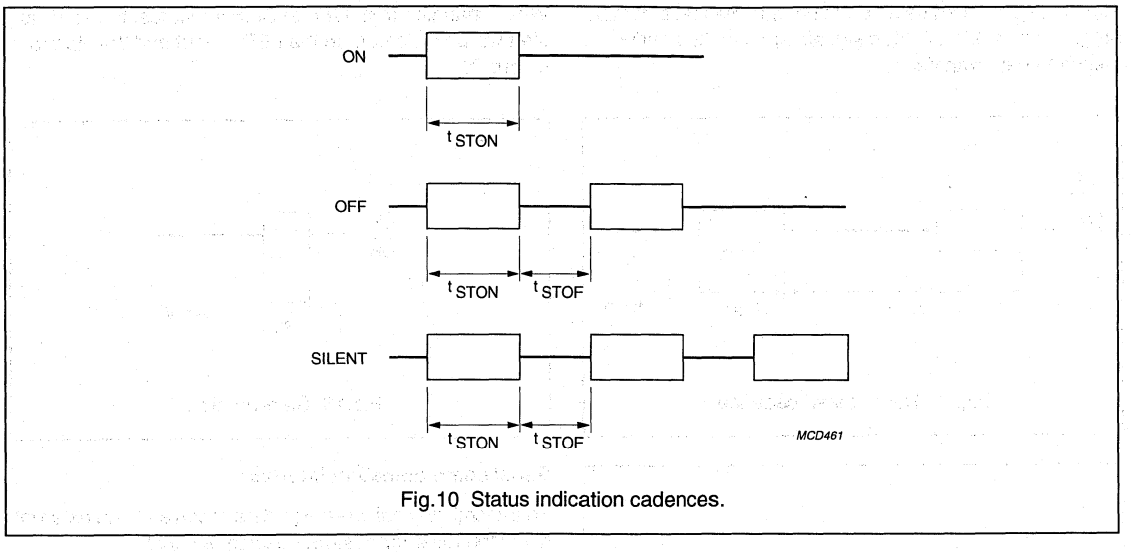


Fig.10 Status indication cadences.

Silent call storage and Repeat mode

When programmed for alert only pager the PCF5001 provides a call alert storage for storing of call alerts received during SILENT status or for call alerts which caused the decoder to enter Repeat mode. Call alert is not stored, when call indication is terminated by action of the status request and reset input (SR).

Allowing the call indication to time-out by expiration of a sixteen second alert operation causes the Repeat mode to be entered, while operating in ON status or SILENT status. Such call alerts are stored for later repeated call alert on interrogation by the user. When Repeat mode has been entered and the decoder operates in ON status, the repeat call store is interrogated by pulsing the status request and reset input (SR) or on switching to ON status if the decoder operates in SILENT status. When silent override calls are received, which entered the Repeat mode, interrogation of repeat call store operates as in decoder ON status. After interrogation of repeat call store and subsequent generation of all stored call alerts the call store is cleared and the Repeat mode is terminated.

When programmed by means of SPF16, a repeat alert cadence is generated periodically, whenever Repeat mode has been entered. Operating in ON status causes the repeat alert cadence to be generated at HIGH-level and warbled by means of an additional 16 Hz and 1024 Hz signal (respective 1365 Hz for SPF31 = 1) as shown in Fig.11. The LED output indicates the same alert cadence and alert warble. In SILENT status only the LED output is active.

No call alert storage occurs when the decoder is programmed for display pager mode.

Duplicate Call Suppression

The PCF5001 provides a Duplicate Call Suppression with time-out facility, to identify duplicate call reception. When selected by programming of SPF14, the PCF5001 inhibits any duplicate call alert in alert-only pager mode. In display pager mode, duplicate call indication is achieved only via the serial microcontroller interface. A call is assumed to be duplicate if its address and function bit setting is equal to the latest received call, which initialized the call address and function bit reference. The Duplicate Call Suppression time-out is selectable by programming of SPF06 and SPF07.

LED indicator

The PCF5001 provides for visual signalling using a LED via output OL.

Call alert indication is provided by the LED with the same cadence and warble modulation as for the alerter outputs AL and AH. Call alert indication occurs in ON and SILENT status and automatically terminates after sixteen seconds time-out unless terminated by pulsing the status request and reset input (SR).

When detecting an out-of-range condition and enabled by programming of SPF15, the LED output provides an out-of-range indication as shown in Fig.12.

The LED output can be made to provide message data by programming SPF17. Alert signals are inhibited during message data transfer.

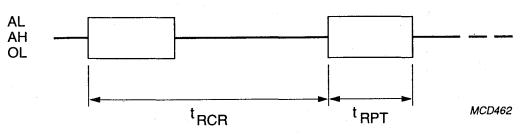


Fig.11 Repeat alert cadence.

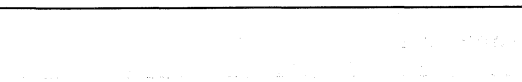


Fig.12 Out-of-range indication.

Vibrator output

The PCF5001 provides the OM output for activating a vibrator-type alerter for call alert indication. The vibrator output is enabled by programming of SPF11.

Calls received while operating in SILENT status cause activation of the vibrator output for the normal call alert cadence or until terminated by operation of the status request and reset input (SR). Silent override calls, calls received in decoder ON status and repeated call alerts are alerted normally by the AL and AH outputs.

Start-up alert

To indicate the establishment of operational condition whenever the decoder status has been changed from OFF to ON or SILENT status, the PCF5001 provides a start-up alert indication. Switching from OFF to ON status causes generation of a start-up alert cadence at LOW-level and on the LED output OL (see Fig.13).

When changing from OFF to SILENT status, the start-up alert will be indicated on the LED output and the vibrator output OM.

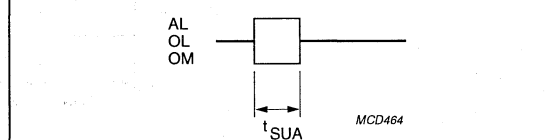


Fig.13 Start-up alert.

Serial communication interface

To transmit any call message data received to an external microcontroller for post-processing, a serial communication interface has been provided by a serial data output signal DO and a data strobe signal DS as shown in Fig.14.

Upon interrogation the PCF5001 is also able to transfer EEPROM contents via the serial communication interface, see Section "Read-back operation via Microcontroller Interface" .

Message data transfer

The transfer of message data via DO and DS is organized in 8-bit words providing additional start and stop conditions as shown in Fig.15.

On reception of a valid call address the PCF5001 generates a start condition and outputs an address word as shown in Fig.15 a.

The address word indicates call address, function bit setting and decoder flags as shown in Table 4.

Message codewords received and concatenated to a valid call address are transferred after completion of the address word. The message bits received in the message codewords are split into blocks and are converted to obtain the message words. The message words comprise an error flag to indicate message words, which are derived from uncorrectable message codewords as shown in Table 5.

Message data is output at a rate of 2048 bits/s with a minimum delay of 2 bits between consecutive message words.

Termination of call reception causes a termination word to be transferred, which indicates successful or unsuccessful call termination as shown in Table 6.

Serial data transfer for a received call ends with a stop condition as shown in Fig.15 c.

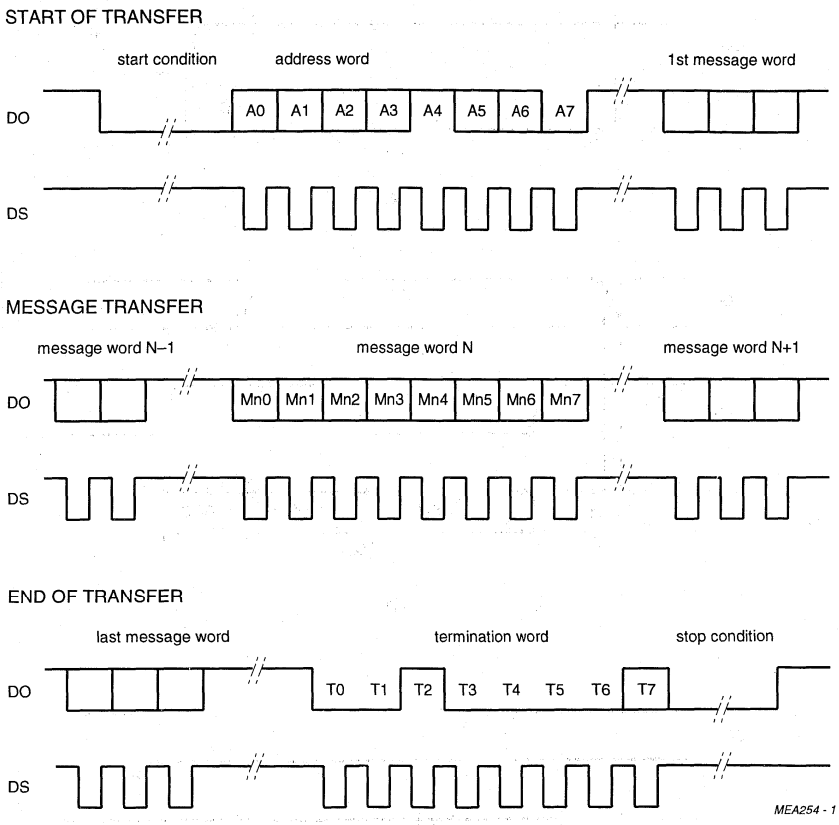
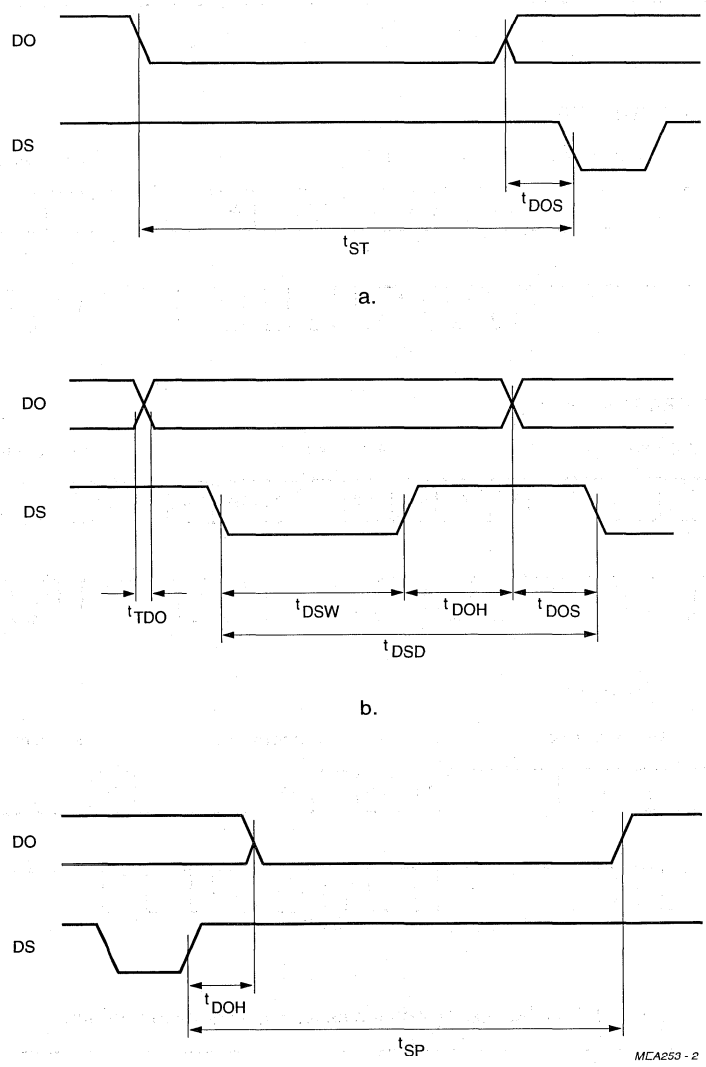


Fig.14 Call data transfer on the serial communication interface.



a. Start condition.
b. Data bit.
c. Stop condition.

Fig.15 Serial communication interface timing.

Call Data output on LED

When enabled by programming of SPF17 = 1, message data will appear on the LED output OL. The data format and timing are equal to the signal on DO, except that the start/stop conditions are replaced with start/stop bits (respectively 1 and 0). The data format is shown in Fig.16. No alert signals will appear on OL during message data transfer. Consecutive message words have a minimum separation of 1 start bit and 1 stop bit.

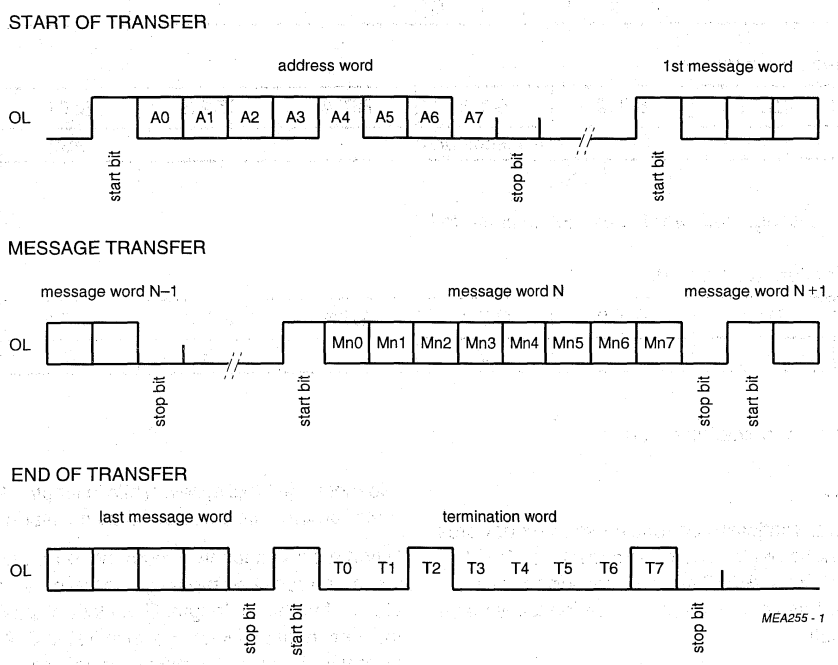


Fig.16 Call data transfer on the LED output.

Serial communication call data format

Table 4 Address word format.

FUNCTION CODE		CALL ADDRESS			BIT 4	SYNC STATUS	DUPLEX CALL	BIT 7
BIT 0 (LSB)	BIT 1 (MSB)	BIT 2	BIT 3	RIC		BIT 5	BIT 6	
Bit 21 of address codeword	bit 20 of address codeword	0	0	A	1	0 = Data Receive; 1 = Data fail	1 = Duplex Call time-out active	0
		0	1	B				
		1	0	C				
		1	1	D				

Table 5 Message word format.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7[1]
LSB			message bits			MSB	error flag

Note

1. Bit 7 = 1, if message codeword could not be corrected.

Table 6 Termination word format.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7[1]
0	0	1	0	0	0	0	error flag

Note

1. Bit 7 = 1, if call termination on error.

Data conversion

The PCF5001 automatically converts message codewords received in numeric or alphanumeric format into ASCII format. Depending on SPF13 and the function bit setting in the received address codeword a conversion takes place as shown in Table 7.

When a conversion from alphanumeric format to ASCII takes place, the received message codewords are split into message blocks, seven bits in length. After adding the error flag they are transferred as message words.

When a conversion from numeric format to ASCII takes place, the received message codewords are split into blocks, four bits in length. Each four bit block is converted to a seven bit block as shown in Table 8. After adding the error flag they are transferred as message words.

Table 7 Message data conversion.

SPF13	FUNCTION BITS		MESSAGE FORMAT
	BIT 20 (MSB)	BIT 21 (LSB)	
0	X[1]	X[1]	numeric
1	0	0	numeric
1	X[1]	1	alphanumeric
1	1	X[1]	alphanumeric

Note

1. X = don't care.

Table 8 Numeric format to ASCII conversion.

4-BIT BLOCK				CHARACTER	7-BIT BLOCK						
LSB			MSB		LSB						MSB
0	0	0	0	'0'	0	0	0	0	1	1	0
1	0	0	0	'1'	1	0	0	0	1	1	0
0	1	0	0	'2'	0	1	0	0	1	1	0
1	1	0	0	'3'	1	1	0	0	1	1	0
0	0	1	0	'4'	0	0	1	0	1	1	0
1	0	1	0	'5'	1	0	1	0	1	1	0
0	1	1	0	'6'	0	1	1	0	1	1	0
1	1	1	0	'7'	1	1	1	0	1	1	0
0	0	0	1	'8'	0	0	0	1	1	1	0
1	0	0	1	'9'	1	0	0	1	1	1	0
0	1	0	1	'*'	0	1	0	1	0	1	0
1	1	0	1	'U'	1	0	1	0	1	0	1
0	0	1	1	' '	0	0	0	0	0	1	0
1	0	1	1	'–'	1	0	1	1	0	1	0
0	1	1	1	']'	1	0	1	1	1	0	1
1	1	1	1	'['	1	1	0	1	1	0	0

Memory Organization

The PCF5001 POCSAG decoder contains non-volatile EEPROM memory to store four user addresses, two frame numbers and specially programmed function bits (SPF01 to SPF32) for decoder application configuration. The EEPROM is organized as three arrays of 38 bits each as shown in Fig.17.

A user address (or RIC) in POCSAG code comprises of 21 bits, but the three least significant bits are coded in the frame number and therefore not explicitly transmitted. In the PCF5001, addresses A/B and C/D must share the same frame number: addresses A and B reside in frame FR1 (FR10, FR11 and FR12), addresses C and D reside in frame FR2 (FR20, FR21 and FR22). Figure 18 shows an example of decimal address to EEPROM content conversion. Each address must be explicitly enabled by resetting of the associated enable bit.

EEPROM ARRAY 1

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	$\overline{ENA}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
B17	B16	B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00	$\overline{ENB}$

EEPROM ARRAY 2

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
C17	C16	C15	C14	C13	C12	C11	C10	C09	C08	C07	C06	C05	C04	C03	C02	C01	C00	$\overline{ENC}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
D17	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	$\overline{END}$

EEPROM ARRAY 3

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SPF13	SPF12	SPF11	SPF10	SPF09	SPF08	SPF07	SPF06	SPF05	SPF04	SPF03	SPF02	SPF01	FR20	FR21	FR22	FR10	FR11	FR12

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
SPF32	SPF31	SPF30	SPF29	SPF28	SPF27	SPF26	SPF25	SPF24	SPF23	SPF22	SPF21	SPF20	SPF19	SPF18	SPF17	SPF16	SPF15	SPF14

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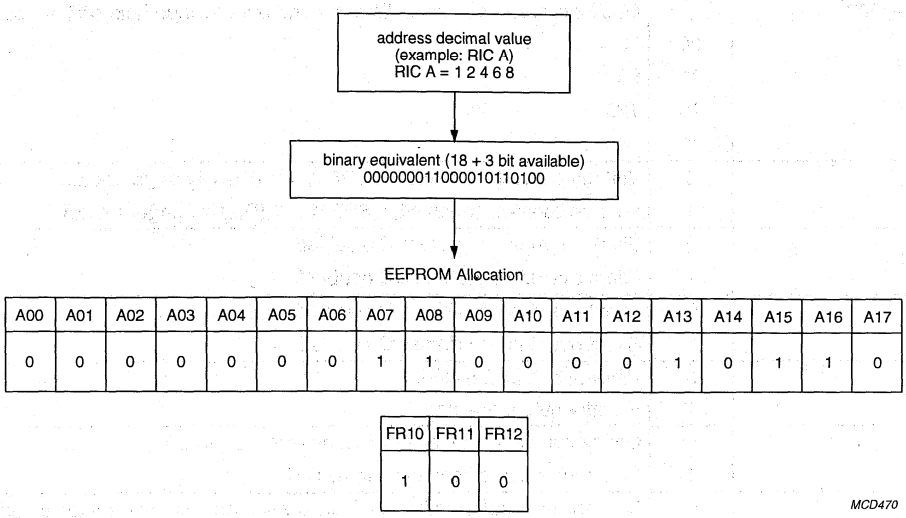
A00 represents the MSB of RIC A, B00 is the MSB of RIC C, etc.
FR10 represents the MSB of Frame 1 (valid for RICs A and B), FR20 is the MSB of Frame 2 (RICs C and D).

Fig.17 EEPROM memory organization.



A00 is the MSB of RIC A, FR10 is the MSB of Frame 1.

Fig.18 Decimal address to memory contents conversion example.

Description of the Special Programmed Function (SPF) bits

The following features can be selected by appropriate programming of the special programmed function bits as shown in Table 9.

Table 9 Special Programmed Function (SPF) bits.

SPF	BIT	FUNCTION
SPF01	0	Alert-only mode.
	1	Display pager mode.
SPF02	0	512 bits/s data rate.
	1	1200 bits/s data rate, possible with 76.8 kHz crystal only.
SPF03	0	32768 Hz crystal configuration.
	1	76800 Hz crystal configuration.
SPF04, SPF05		Receiver establishment time (depending on data rate).
	00	7.8 ms/512 bits/s; 53.3 ms/1200 bits/s.
	01	15.6 ms/512 bits/s; 6.7 ms/1200 bits/s.
	10	31.3 ms/512 bits/s; 13.3 ms/1200 bits/s.
	11	62.5 ms/512 bits/s; 26.7 ms/1200 bits/s.

SPF	BIT	FUNCTION
SPF06, SPF07		Duplicate call suppression time-out and out-of-range hold-off time-out.
	00	30 s.
	01	60 s.
	10	120 s.
	11	240 s.
SPF08	0	Voltage converter disabled, if SPF01 = 1 (Display pager mode).
	1	Voltage converter enabled, if SPF01 = 1 (Display pager mode).
SPF09	0	Silent override on address C disabled.
	1	Silent override on address C enabled.
SPF10	0	Silent override on address D disabled.
	1	Silent override on address D enabled.
SPF11	0	Vibrator output disabled.
	1	Vibrator output enabled.
SPF12	0	Call termination criteria combination method (note 1).
	1	Call termination criteria defined by SPF13.
SPF13	0	Numeric data deformatting, call termination on first uncorrectable codeword.
	1	Numeric data deformatting on function code 00 only, call termination on two uncorrectable codewords.
SPF14	0	Duplicate call suppression disabled.
	1	Duplicate call suppression enabled.
SPF15	0	Out of range indication at OL output disabled, hold-off period is zero regardless of SPF06 and SPF07 setting.
	1	Out of range indication at OL output enabled, hold-off period is according to SPF06 and SPF07 setting.
SPF16	0	Repeat alert disabled.
	1	Repeat alert enabled.
SPF17	0	Call data output on OL disabled.
	1	Call data output on OL enabled.
SPF18	–	Spare.
SPF19	–	Program always 0.
SPF20 to SPF30	–	Spares.
SPF31	0	Alerter frequency 2048 Hz.
	1	Alerter frequency 2731 Hz.
SPF32	0	Frequency reference output 16384 Hz if SPF01 = 1 (Display pager mode).
	1	Frequency reference output 32768 Hz if SPF01 = 1 (Display pager mode).

Note

1. Call termination on:

   First codeword immediately following address codeword uncorrectable.

   Two consecutive codewords uncorrectable.

EEPROM Write operation

The program mode is entered in OFF status by setting the PD input LOW and the PS input HIGH at any time. The program mode is left and normal operation resumed by either removing the power supply or setting the PD input HIGH after the 38th data bit while continuing to clock the PS input. The three EEPROM arrays can be programmed in any order. Selection of array is made during the second and third pulse on the PS input. The program mode has to be left after programming of each array.

After entering the program mode, keeping input PD LOW during the first pulse on PS selects Memory Write operation. After selection of the current array an erase cycle of duration t_{PEW} has to be carried out, during which the supply voltage at V_{SS} input must be at least V_{PG}. Program data for the selected array is entered bit by bit using PD as data input and the rising edge on PS as data strobe pulse. See Fig.19 for timing during an EEPROM write operation.

After the last bit a special write cycle of duration t_{PEW} has to be carried out again, during which the supply voltage at V_{SS} input must be V_{PG}. During conditions when the supply voltage is increased to V_{PG} the maximum DC ratings at V_{ref} must not be exceeded. When the on-chip voltage converter is enabled a voltage regulator diode or a damping resistor of sufficiently low impedance has to be connected between V_{ref} and V_{SS} to limit the voltage level at V_{ref} during program operation.

EEPROM Read operation

After entrance to the program mode, keeping input PD HIGH during the first pulse on PS selects Memory Read operation. After selection of the current array the programmed data is output bit-by-bit using PD as data output. A positive edge on PS input switches to the next bit. See Fig.19 for timing during an EEPROM read operation.

Read-back operation via Microcontroller Interface

In display pager mode, the PCF5001 is capable of delivering the EEPROM contents to an external microcontroller using the serial interface outputs DO and DS. The EEPROM data transfer mode is selected by applying a LOW to input ON and a HIGH to input SK while pulsing the SR input, and the interface is enabled (IE is HIGH). The data transfer is triggered by the falling edge on input SR. The transfer is organized as 15-byte transfers. The contents of each array are extended to 40 bits by trailing zeros. The EEPROM data transfer starts with array 1, bit 0. A valid data bit at DO is indicated by a LOW-level on DS as shown in Fig.20.

During EEPROM Read-back operation, the PCF5001 configuration and the outputs FL, OL are undefined. After completion of the Read-Back operation, the PCF5001 will re-enter the programmed configuration.

Voltage converter

The PCF5001 contains a switched capacitor-type on-chip voltage converter, which can provide doubled supply voltage to the external microcontroller and display control devices. The microcontroller interface signals are level shifted accordingly.

A capacitor of 100 nF (C_S) must be connected between pins CP and CN while a load capacitor of 10 µF is connected to V_{ref} as shown in Fig.22. The voltage converter operates in display pager mode only, when enabled by programming SPF08 (see Table 9).

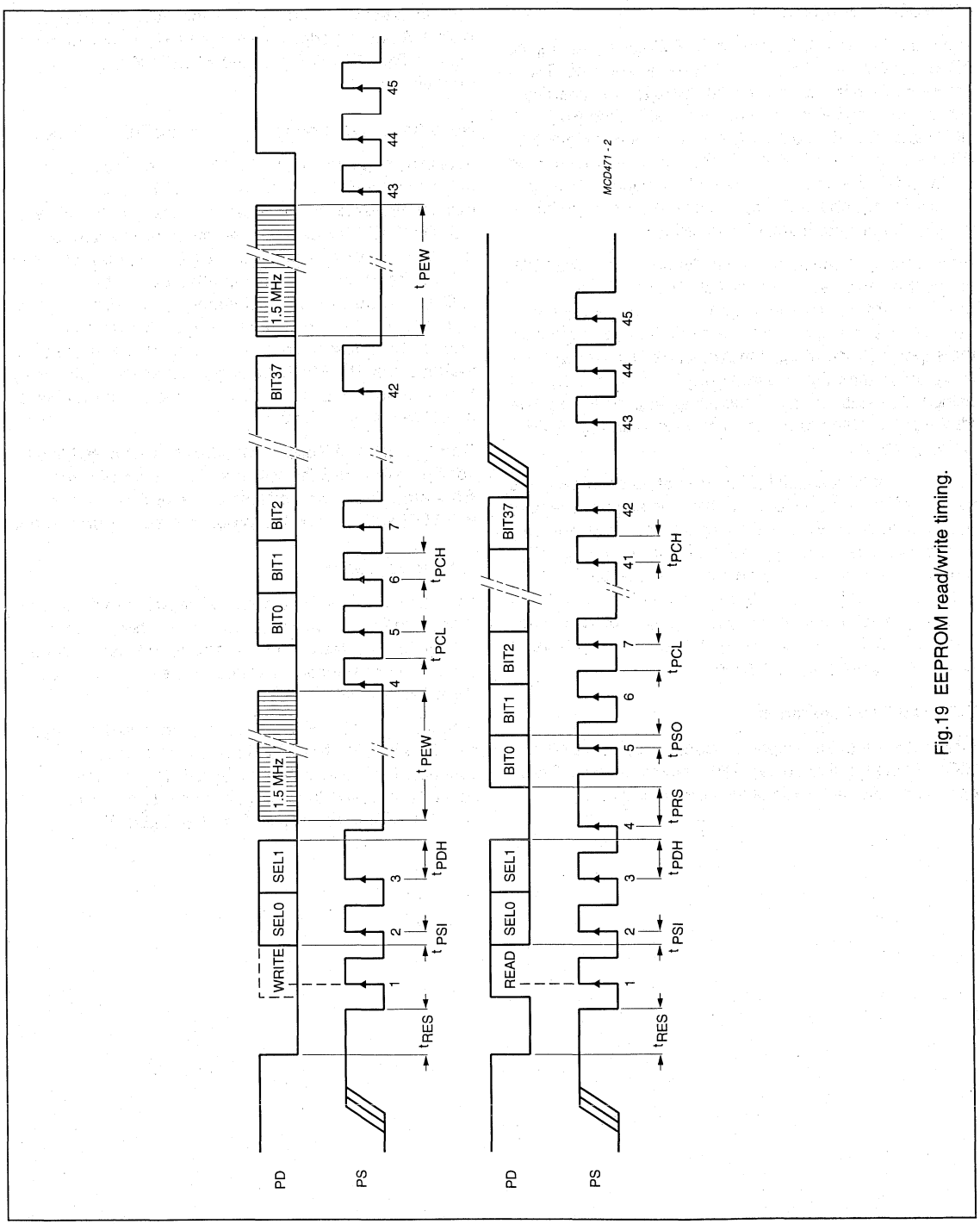


Fig.19 EEPROM read/write timing.

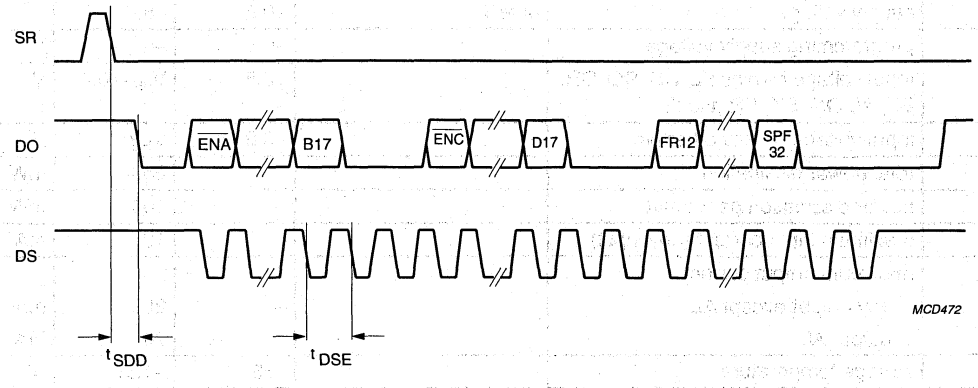


Fig.20 EEPROM data transfer to microcontroller timing.

Test modes of the decoder

The decoder supports two test modes, which are intended for use during pager production and type approval tests.

BOARD TEST MODE

Board test mode is selected by setting the PD input LOW at any time. In this test mode the following features are provided:

1. Receiver enable output is set constantly HIGH.
2. Output AL is activated by a LOW-level on ON input.
3. Output AH is activated by a HIGH-level on SR input.
4. Outputs OL and OM are activated by a HIGH-level on SK input.

Exit from board test mode is achieved by setting input PD HIGH.

PAGER TEST MODE (TYPE APPROVAL MODE)

Pager test mode is entered by reception of a valid call while board test mode is active, see above. In pager test mode:

1. Call alert cadences are terminated after 2 seconds.
2. Duplicate call suppression is disabled.

Exit from pager test mode is achieved by disconnecting the power supply from the decoder.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SS}	supply voltage	note 1	+0.5	−8.0	V
V_{PG}	programming supply voltage		−5.5	−	V
V_I	input voltage on pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE		+0.8	V_{ref} − 0.8	V
V_I	input voltage on any other pin		+0.8	V_{SS} − 0.8	V
P_{tot}	total power dissipation		−	250	mW
P_O	power dissipation per output		−	100	mW
I_I	maximum input current (any input)		−	10	mA
$I_{O(max)}$	maximum output current				
	any output except AL		−	20	mA
	output AL		−	70	mA
T_{stg}	storage temperature		−55	+125	°C
T_{amb}	operating ambient temperature		−40	+85	°C

Note

1. Input V_{DD} is referred to as common, 0 V.

DC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; V_{ref} = 2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Alert-only (SPF01 = 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	supply voltage		−1.5	−2.7	−6.0	V
I_{SS}	supply current	note 1	−	−60	−100	µA
V_{PG}	programming supply voltage	note 2	−4.5	−5.0	−5.5	V
I_{PG}	programming supply current		−	−500	−	µA
Inputs						
V_{IL1}	LOW level input voltage PD, PS, DI, BS, TS, TT and X1		0.7 V_{SS}	−	−	V
V_{IL2}	LOW level input voltage AI, ON, SR, SK and IE		0.7V_{ref}	−	−	V
V_{IH1}	HIGH level input voltage PD, PS, DI, BS, TS, TT and X1		−	−	0.3V_{SS}	V
V_{IH2}	HIGH level input voltage AI, ON, SR, SK and IE		−	−	0.3V_{ref}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	input current					
	BS, PS, TS and TT	$V_I = V_{DD}$	7.0	–	20.0	µA
	PD	$V_I = V_{SS}$	–9.0	–	–24.0	µA
	DI	$V_I = V_{DD}$; RE = 0	7.0	–	20.0	µA
	DI	$V_I = V_{DD}$; RE = 1	0	–	0.5	µA
	ON and SK	$V_I = V_{SS}$	–0.5	–0.8	–1.1	µA
	AI and SR	$V_I = V_{DD}$	7.0	–	20.0	µA
C_I	input capacitance BS, DI, PD, PS, TS, TT, AI, ON, SR, SK, IE and X1		2	–	–	pF
Outputs						
I_{OL}	LOW level output current					
	OL, OM and AH	$V_{OL} = -1.35$ V	100	–	–	µA
	DO, DS, BL, FL and OR	$V_{OL} = -1.35$ V	100	–	–	µA
	AL	$V_{OL} = -1.5$ V	17.5	–	–	mA
	RE	$V_{OL} = 2.2$ V	200	–	–	µA
I_{OH}	HIGH level output current					
	OL, OM and AH	$V_{OH} = -1.35$ V	–0.8	–	–1.8	mA
	DO, DS, BL, FL and OR	$V_{OH} = -1.35$ V	–100	–	–	µA
	AL	AL high-impedance	–	–	–0.2	µA
	RE	$V_{OH} = -0.5$ V	–1.0	–	–	mA
Oscillator						
C_{XO}	output capacitance X2		–	40	–	pF
g_m	oscillator transconductance	$V_{SS} = -1.5$ V	15	29	43	µS
		$V_{SS} = -6.0$ V	25	39	55	µS
V_{PU}	power-up reset threshold voltage		–	–1.2	–	V

Notes

1. All inputs = V_{SS}; voltage converter off; all outputs open-circuit.
2. See Section "EEPROM Write operation" and Chapter "Limiting values" for limitations of V_{ref} when programming while the voltage converter is enabled.

DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 0 V; V_{SS} = –3.0 V; V_{ref} = –6.0 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display Pager (SPF01 = 1).
Voltage converter enabled (SPF08 = 1); C_s = 100 nF.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	supply voltage		–1.5	–	–3.0	V
Voltage converter						
V_{ref0}	output voltage; no load	V_{SS} = –3.0 V	–5.8	–	–6.0	V
V_{ref}	output voltage	V_{SS} = –2.0 V; I_{ref} = 250 µA	–3.0	–3.5	–	V
I_{ref}	output current	V_{SS} = –2.0 V; V_{ref} = –2.7 V	400	600	–	µA
		V_{SS} = –3.0 V; V_{ref} = –4.5 V	600	900	–	µA
Inputs						
I_I	input current					
	AI, ON, SR and SK	$V_I = V_{ref}$	–	0	–0.5	µA
	ON and SK	$V_I = V_{DD}$	–	0	±0.5	µA
	SR	$V_I = V_{DD}$; V_{ref} = –6.0 V	–	17	–	µA

AC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = –2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only Pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Alert frequency						
f_{AL}	alert frequency	SPF31 = 0	–	2048	–	Hz
f_{AWH}	high alert warble frequency		–	1024	–	Hz
f_{AWL}	low alert warble frequency		–	16	–	Hz
f_{AL}	alert frequency	SPF31 = 1	–	2731	–	Hz
f_{AWH}	high alert warble frequency		–	1365	–	Hz
f_{AWL}	low alert warble frequency		–	16	–	Hz
f_{FL}	frequency reference FL	SPF32 = 0	–	16384	–	Hz
		SPF32 = 1	–	32768	–	Hz
Call alert duration						
t_{ALT}	time-out period		–	16	–	s
t_{ALL}	alert time LOW (AL output only)		–	4	–	s
t_{ALH}	alert time HIGH (AH and AL outputs)		–	12	–	s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{ALC}	call alert cycle time	see Fig.9	–	1	–	s
t_{ALP}	call alert pulse duration	see Fig.9	–	125	–	ms
t_{ALD}	call alert hold off period	see Fig.8	52	–	–	ms
t_{RPT}	repeat alert duration	see Fig.11	–	–	4	s
t_{RCR}	repeat alert recurrence time	see Fig.11	–	–	15	s
t_{RCP}	repeat alert cycle time		–	–	500	ms
t_{RPD}	repeat alert pulse duration		–	–	250	ms
t_{STON}	status alert time	see Fig.10	–	–	62.5	ms
t_{STOF}	status alert delay	see Fig.10	–	–	62.5	ms
t_{SUA}	start-up alert time	SPF02 = 0; see Fig.13	–	–	500	ms
		SPF02 = 1; see Fig.13	–	–	453	ms
t_{ORA}	out-of-range alert pulse width	see Fig.12	–	–	62.5	ms
t_{ORD}	out-of-range alert time	see Fig.12	–	–	2	s
t_{BLAL}	battery LOW-level alert time		–	–	16	s
Receiver control						
t_{RXT}	RE transition time	C_L = 5 pF	–	–	100	ns
t_{RXON}	RE establishment time	SPF04 = 0; SPF05 = 1	–	7.8	62.5	ms
Data output						
f_{DO}	data output rate		–	2048	–	bits/s
t_{DSD}	strobe period call data	see Fig.15	480	–	495	µs
t_{DSE}	strobe period EEPROM data	see Fig.20	200	488	1150	µs
t_{DSW}	data strobe pulse width	see Fig.15	230	–	250	µs
t_{TDO}	data output transition time	C_L = 10 pF; see Fig.15	–	–	100	ns
t_{DOS}	data output set-up time	see Fig.15	–	–	135	µs
t_{DOH}	data output hold time	see Fig.15	115	–	–	µs
t_{BYD}	consecutive byte delay		1210	–	1225	µs
t_{CWD}	inter-codeword delay	1200 bits/s numeric message	3420	–	–	µs
t_{ST}	start condition set-up time	see Fig.15	4750	–	–	µs
t_{SP}	stop condition set-up time	see Fig.15	595	–	615	µs
t_{STL}	start bit period OL output		480	–	495	µs
t_{SPL}	stop bit period OL output		480	488	495	µs
t_{SDD}	SPF output delay	see Fig.20	1	–	10	ms

TIMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = –2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only Pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating frequency dependent						
f_{osc}	oscillator frequency	SPF03 = 0	–	32768	–	Hz
		SPF03 = 1	–	76800	–	Hz
t_{TDI}	data input transition time		–	–	100	µs
t_{DI1}	data input logic 1		–	∞	–	
t_{DI0}	data input logic 0		–	∞	–	
f_{DI}	data input rate	SPF02 = 0	–	512	–	bits/s
t_{BIT}	bit period		–	1.9531	–	ms
t_{CW}	codeword duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms
f_{DI}	data input rate	SPF02 = 1; f_{osc} = 76800 Hz	–	1200	–	bits/s
t_{BIT}	bit period		–	833.3	–	ms
t_{CW}	codeword duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
Alert only mode (SPF01 = 0)						
t_{SDB}	switch debounce period		–	62.5	–	ms
Display pager mode (SPF01 = 1); see Figs 6 and 7						
t_{STP}	status set-up time	f_{osc} = 32768 Hz	35	–	–	µs
t_{STD}	status change delay		–	–	35	µs
t_{IEH}	interface enable hold time		35	–	–	µs
t_{STH}	status hold time		35	–	–	µs
t_{SPD}	status pulse duration		35	–	–	µs
t_{STP}	status set-up time	f_{osc} = 76800 Hz	15	–	–	µs
t_{STD}	status change delay		–	–	15	µs
t_{IEH}	interface enable hold time		15	–	–	µs
t_{STH}	status hold time		15	–	–	µs
t_{SPD}	status pulse duration		15	–	–	µs

PROGRAMMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = V_{PG} = −5.0 V; (see notes 1, 2 and 3); V_{ref} = V_{SS}; pins 2 and 3 open-circuit; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder in OFF status.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programming; see Fig.19						
t_{RES}	power-up reset pulse width	note 4	35	–	–	µs
t_{PEW}	erase/write time		10	–	–	ms
f_{EW}	erase/write frequency		1.0	1.5	2.0	MHz
t_{EW}	erase/write cycles		100	10000	–	–
t_{DR}	data retention time	T_{amb} = 85 °C	10	–	–	years
t_{PCH}	data clock HIGH time	note 4	65	–	–	µs
t_{PCL}	data clock LOW time	note 4	65	–	–	µs
t_{PRS}	read set-up time	note 4	–	–	35	µs
t_{PSI}	data set-up time on input	note 4	35	–	–	µs
t_{PSO}	data set-up time on output	note 4	–	–	35	µs
t_{PDH}	data hold time	note 4	35	–	–	µs

Notes

1. V_{SS} = V_{PG} only required during erase/write (t_{PEW} in Fig.19), otherwise $V_{SS(min)}$ = −1.5 V.
2. Maximum voltage for programming (V_{PG}) is −5.5 V.
3. See Section "EEPROM Write operation" and Chapter "Limiting values" for limitations of V_{ref} when programming while the voltage converter is enabled.
4. EEPROM programming is also possible at higher frequencies (76.8 kHz or 153.6 kHz). The timings shown then become proportionally smaller.

APPLICATION INFORMATION

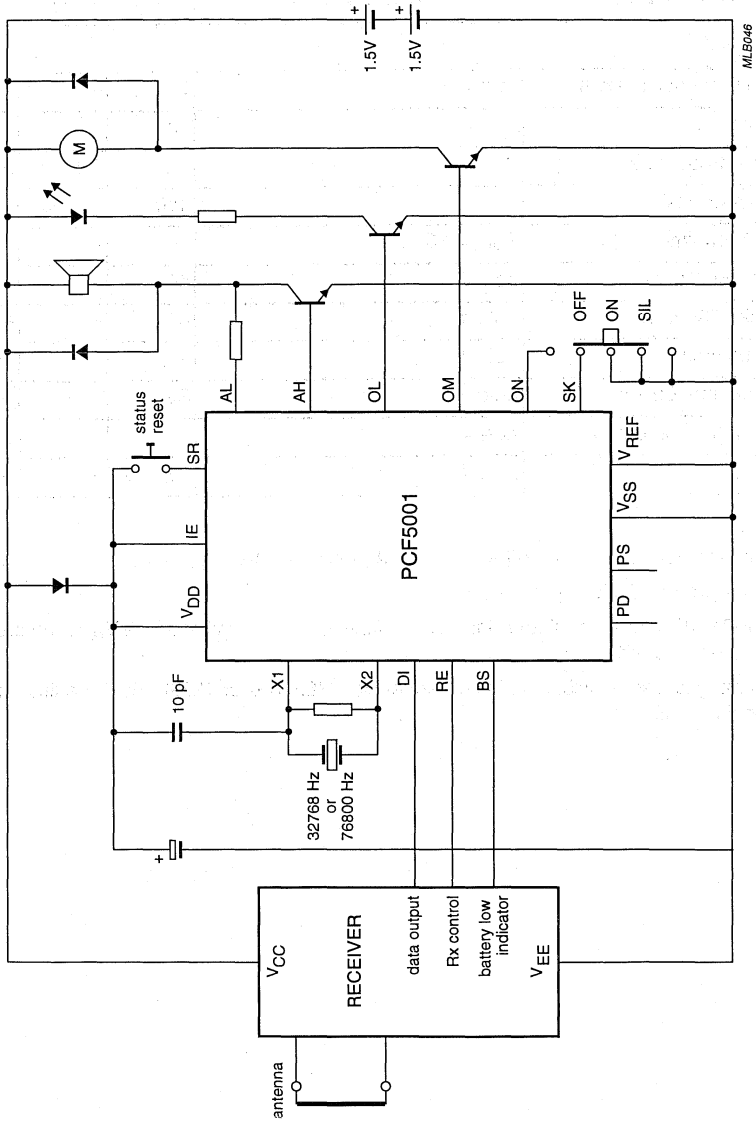


Fig.21 Alert-only pager application example.

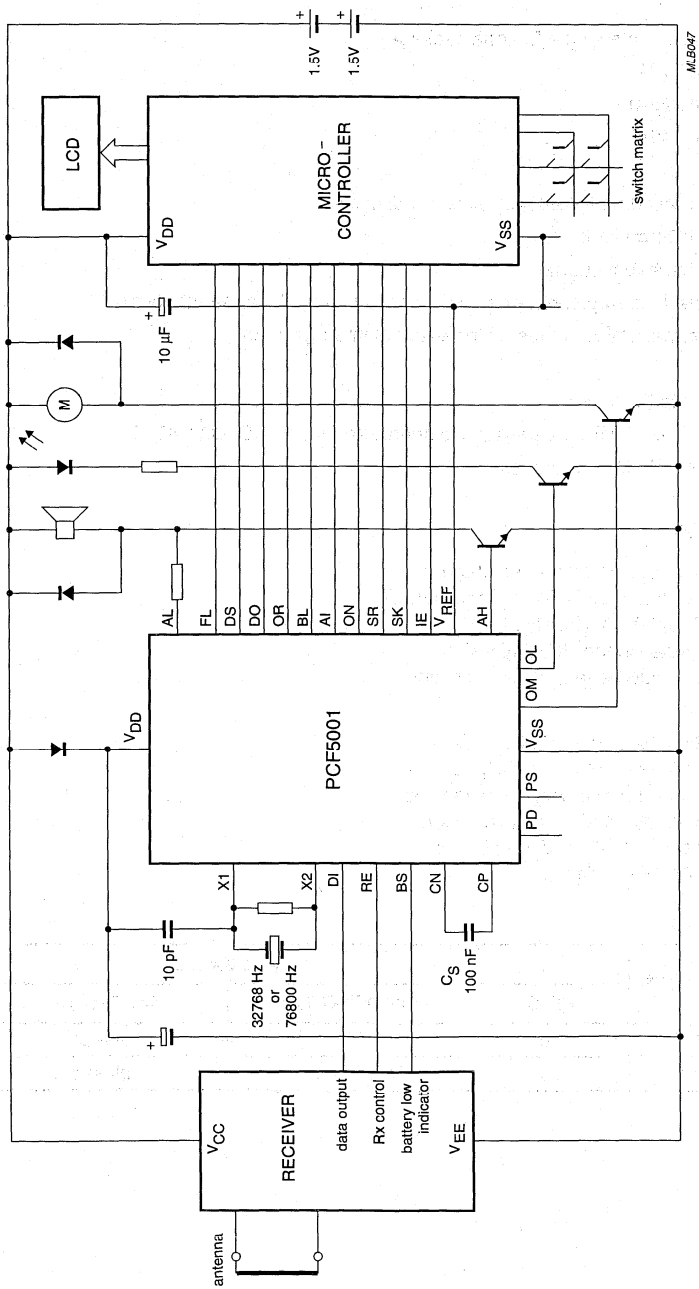


Fig.22 Display-pager application example.

8-bit microcontroller PCF84C12A/22A/42A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead package
- 1k ROM bytes (PCF84C12A)
- 2k ROM bytes (PCF84C22A)
- 4k ROM bytes (PCF84C42A)
- 64 RAM bytes
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 13 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- Two single-level vectored interrupts: external, 8-bit programmable timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- Stop and idle modes
- Logic supply V_{DD}: 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz - Operating temperature range: –40 °C to 85 °C
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C12A, PCF84C22A and PCF84C42A. The shared characteristics of the PCF84CXXXA family of microcontrollers are described in the PCF84CXXXA family data sheet, which should be read in conjunction with this publication.

The PCF84C12A, PCF84C22A and PCF84C42A are general purpose CMOS microcontrollers with 1k, 2k and 4k bytes of program memory, respectively. They include 64 bytes of RAM and 13 I/O port lines. The instruction set is based on that of the MAB8048 and is software compatible with the PCF84CXXXA family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF84C12AP/22AP/42AP	20	DIL	plastic	SOT146
PCF84C12AT/22AT/42AT	20	mini-pack	plastic	SOT163A

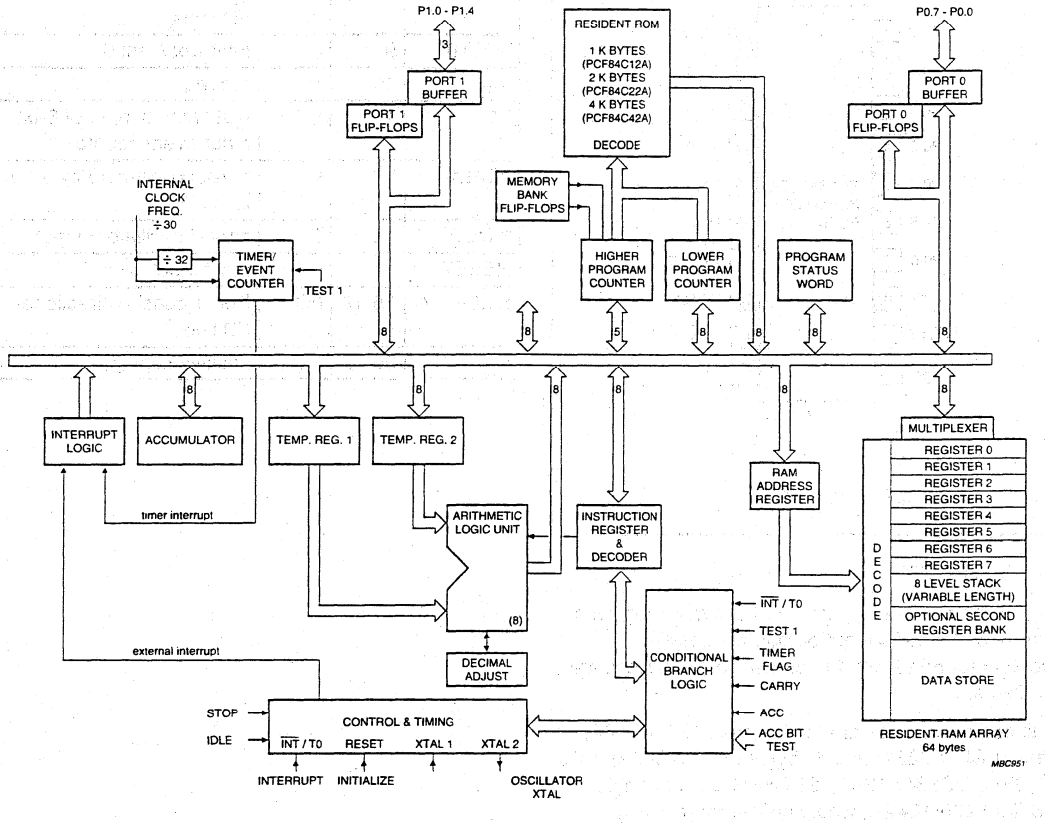


Fig.1 PCF84C12A/22A/42A Block diagram.

PINNING

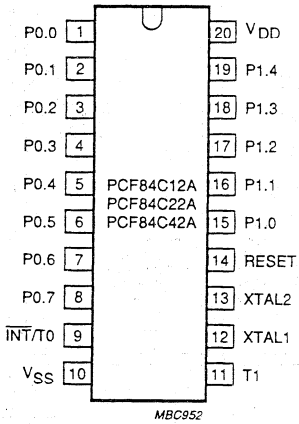


Fig.2 Pinning diagram.

Table 1 Pin description

SYMBOL	PIN	TYPE	FUNCTION
P0.0-P0.7	1-8	I/O	Port 0: quasi-bidirectional I/O lines
INT/T0	9	I	interrupt / test 0
V_{SS}	10	P	ground
T1	11	I	test 1/count input of 8-bit timer/event counter 1
XTAL1	12	I	crystal oscillator / external clock
XTAL2	13	O	crystal oscillator output
RESET	14	I	reset input
P1.0-P1.4	15-19	I/O	Port 1:quasi-bidirectional I/O lines
V_{DD}	20	P	positive supply

INSTRUCTION SET

Since serial I/O interface, port 2 and derivative logic are not provided, the serial input/output, the parallel input/output for port 2 and the derivative instructions are not available.

ROM space being restricted to 1k bytes (PCF84C12A), 2k bytes (PCF84C22A) and 4k bytes (PCF84C42A), SEL MB1/2/3 (for PCF84C12A and PCF84C22A) and SEL MB2/3 (for PCF84C42A) would define non-existing program memory banks and should therefore be avoided.

RAM space being restricted to 64 bytes, care should be taken to avoid accesses to non-existing RAM locations.

See PCF84CxxxA Family Specification for a complete description of the instruction set.

Universal LCD driver for low multiplex rates

PCF8566

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

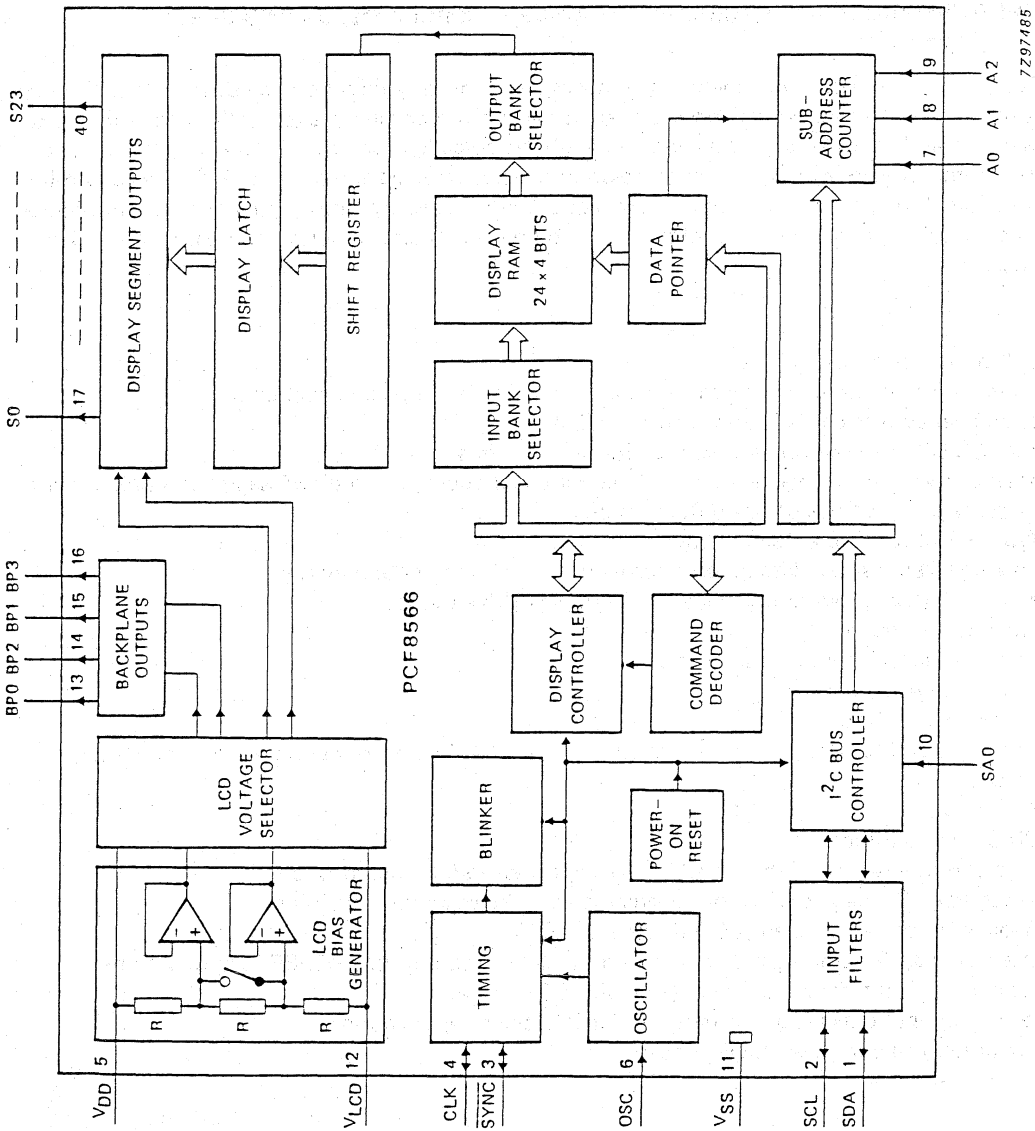


Fig. 1 Block diagram.

LCD row driver for dot matrix displays PCF8568

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

FEATURES

- Single chip LCD row driver with 16 outputs
- Low power consumption
- Selectable multiplex rate 1:8, 1:16, 1:24, 1:32
- Cascadable to 1:24 or 1:32 multiplex rates
- Internally generated intermediate LCD bias voltages
- LCD column bias voltages available at pins VO3 and VO4
- Minimizes display system power requirements
- On-chip oscillator, requires only one external resistor
- Power-on reset blanks display
- Logic voltage range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9.0 V
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring
- Available in 28-lead plastic DIL or space saving mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- General instrumentation
- Consumer products.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	+2.5	-	+6.0	V
V_{LCD}	LCD supply voltage range voltage	V_{DD} −9	-	V_{DD} −3.5	V
I_{DD2}	supply current with internal clock (R_{OSC} = 330 kΩ)	-	67	150	µA
T_{amb}	operating ambient temperature range	−40	-	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8568P	28	DIL	plastic	SOT117
PCF8568T	28	SO28	plastic	SOT136A
PCF8568U/7	(28 pads)	die: bumped chip on tape	-	-

GENERAL DESCRIPTION

The PCF8568 is a low power LCD row driver, designed to drive dot matrix graphic displays with multiplex rates of 1:8 or 1:16. The device has 16 row outputs. Two devices may be cascaded to drive displays with multiplex rates of 1:24 or 1:32. The PCF8568 is optimised for use with the PCF8569 and PCF8579 LCD dot matrix column drivers. Intermediate LCD bias voltages are internally generated. LCD column bias voltages are available at pins VO3 and VO4 for connection to the column drivers. The PCF8568 is compatible with most microcontrollers and communicates via a two- line bidirectional bus (I²C).

LCD row driver for dot matrix displays PCF8568

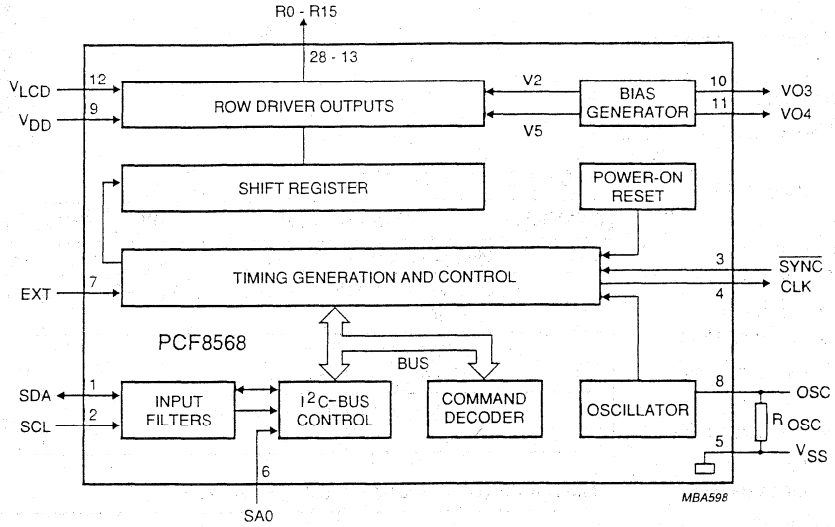


Fig.1 Block diagram.

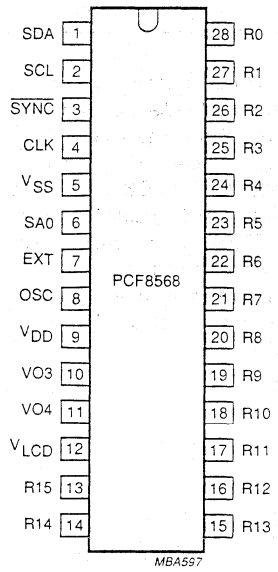


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	clock output
V_{SS}	5	ground (logic)
SA0	6	I²C-bus slave address input (bit 0)
EXT	7	external clock select pin
OSC	8	oscillator or external clock input pin
V_{DD}	9	positive supply voltage
VO3	10	LCD bias voltage output (V3)
VO4	11	LCD bias voltage output (V4)
V_{LCD}	12	LCD supply voltage
R15 to R0	13 to 28	LCD row driver outputs

LCD column driver for dot matrix graphic displays

PCF8569

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

GENERAL DESCRIPTION

The PCF8569 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8 or 1:16. The device has 40 outputs and can drive 16 x 40 dots in a 16 row multiplexed LCD. Up to 16 PCF8569s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8568/78/79 family of LCD row/column drivers. Together the PCF8568, PCF8578 and PCF8569 form a general LCD dot matrix driver chip set, capable of driving displays of up to 20 480 dots. The PCF8569 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

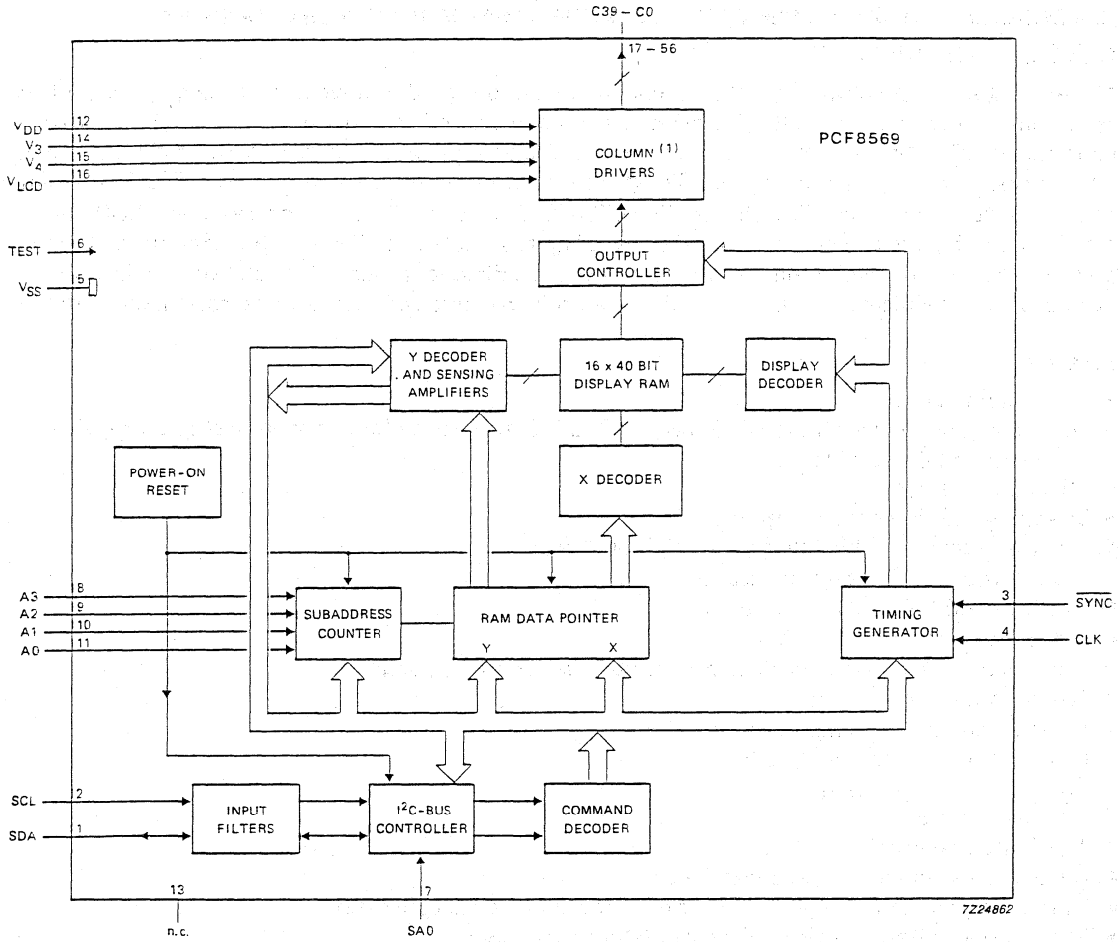
- LCD column driver
- Used in conjunction with the PCF8568 or PCF8578, this device forms part of a chip set capable of driving up to 20 480 dots.
- 40 column outputs
- Selectable multiplex rates; 1:8 or 1:16
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications
- 640-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack or 64-lead tab module

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8569T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8569V: 64-lead tape-automated-bonding (tab) module (SOT267).



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram (pin numbers shown for VSO56; SOT190).

Remote 8-bit I/O expander for I²C-bus PCF8574

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 μA maximum
- I²C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O Port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- DIP16, space-saving SO16 or SSOP20 package.

GENERAL DESCRIPTION

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C).

The device consists of an 8-bit quasi-bidirectional Port and an I²C interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and PCF8574A versions differ only in their slave address as shown in Fig.9.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8574P; PCF8574AP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
PCF8574T; PCF8574AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCF8574TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

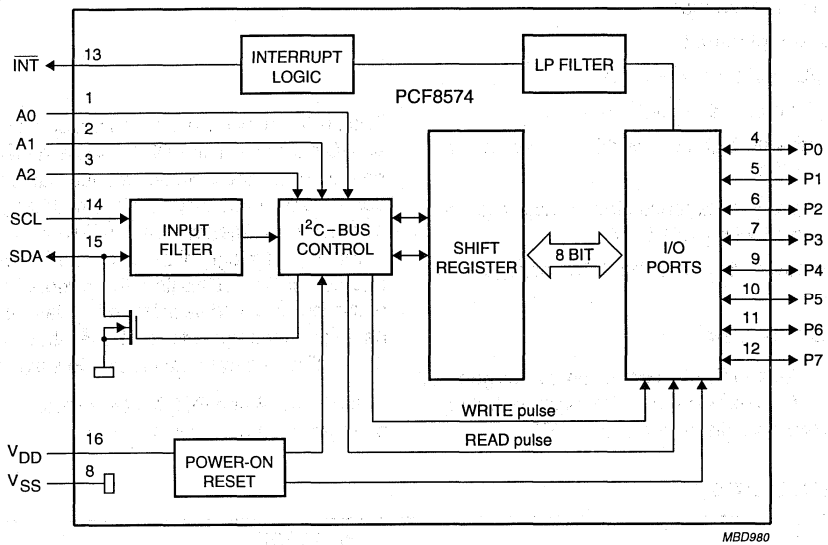


Fig.1 Block diagram (SOT38-1 and SOT162-1).

Universal LCD driver for low multiplex rates

PCF8576

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24-segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO56) or 64-lead tape-automated-bonding (TAB) module (SOT267A)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray.
PCF8576U/10: chip-on-film frame carrier (FFC).
PCF8576V: 64-lead tape-automated-bonding module (SOT267A).

Universal LCD driver for low multiplex rates

PCF8576

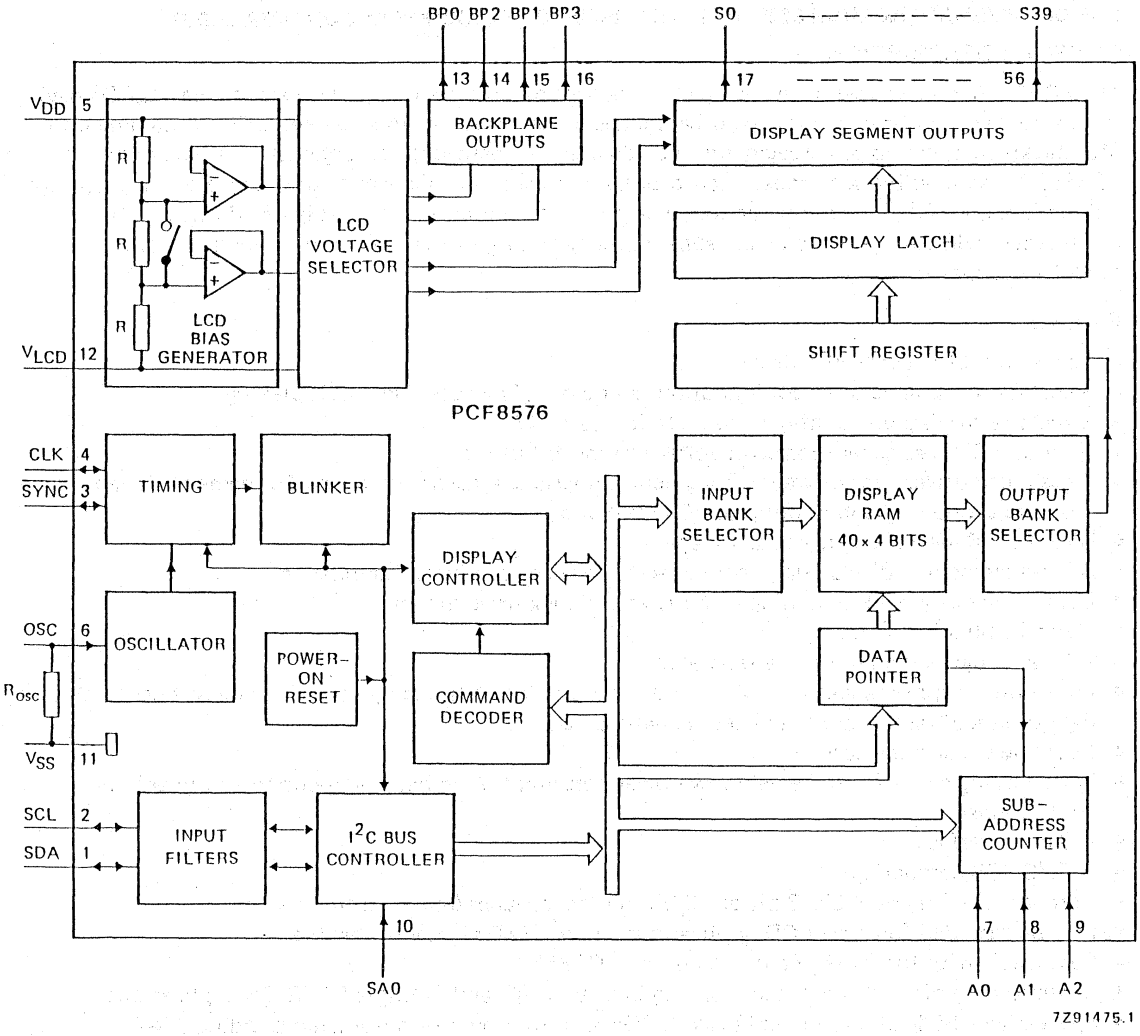


Fig.1 Block diagram; VSO56; SOT190.

LCD row/column driver for dot matrix graphic displays

PCF8578

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

FEATURES

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology.

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

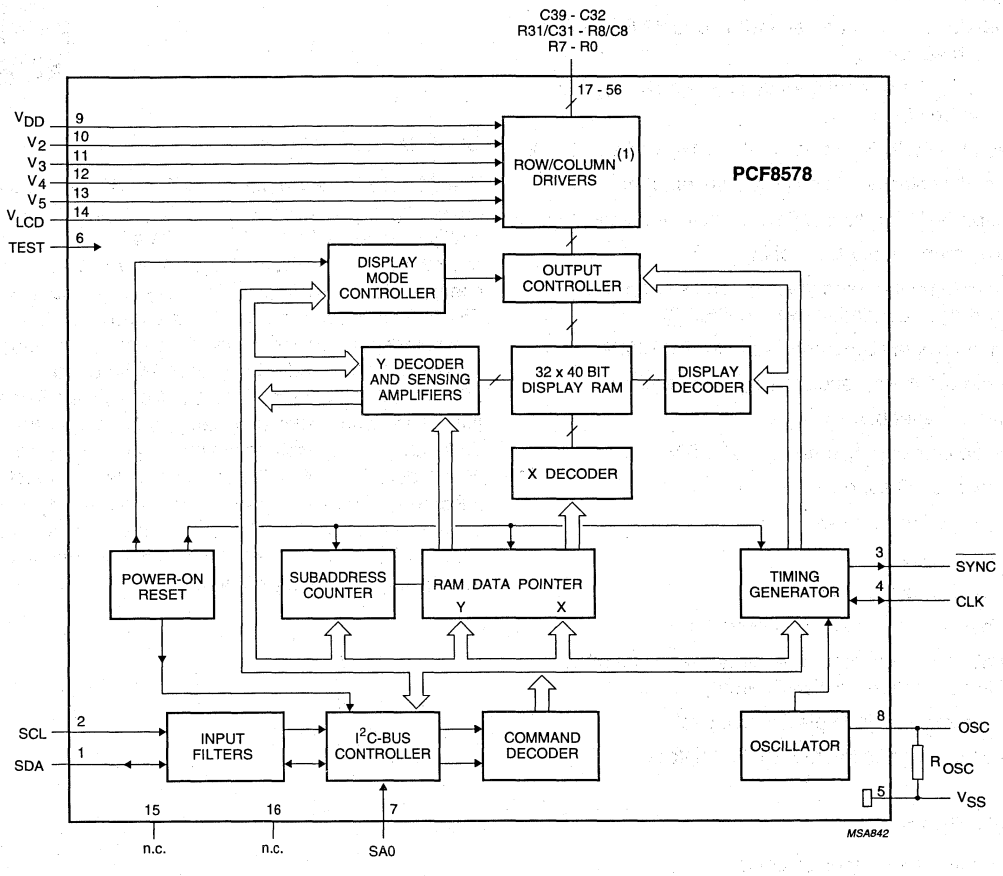
APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8578T	56	VSO56	plastic	SOT190
PCF8578U7	–	chip with bumps on-tape	–	–

BLOCK DIAGRAM



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization output
CLK	4	external clock input/output
V_{SS}	5	ground (logic)
TEST	6	test pin (connect to V_{SS})
SA0	7	I²C-bus slave address input (bit 0)
OSC	8	oscillator input
V_{DD}	9	positive supply voltage
V_2 to V_5	10 to 13	LCD bias voltage inputs
V_{LCD}	14	LCD supply voltage
n.c.	15, 16	not connected
C39 to C32	17 to 24	LCD column driver outputs
R31/C31 to R8/C8	25 to 48	LCD row/column driver outputs
R7 to R0	49 to 56	LCD row driver outputs

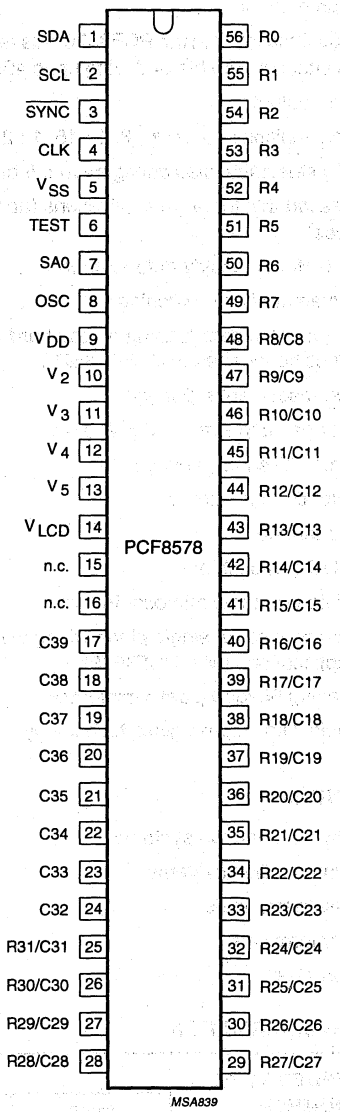


Fig.2 Pin configuration.

LCD column driver for dot matrix graphic displays

PCF8579

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

FEATURES

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

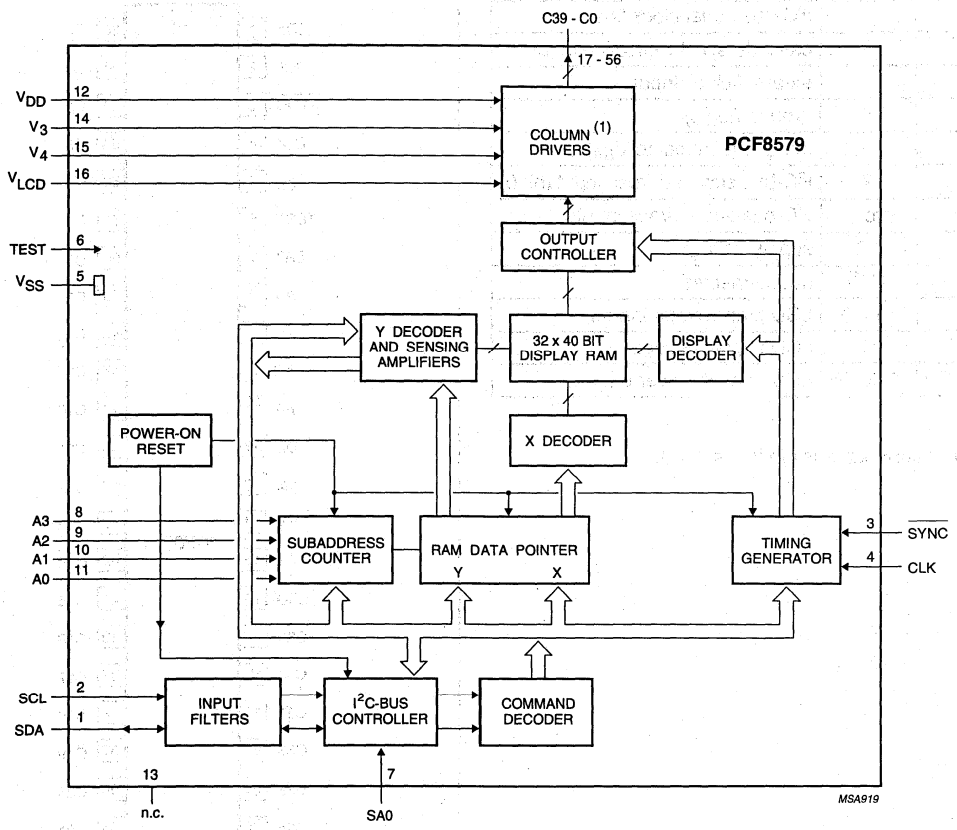
GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 × 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8579T	56	VSO56	plastic	SOT190
PCF8579U7	–	chip with bumps on-tape	–	–

BLOCK DIAGRAM



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization input
CLK	4	external clock input
V_{SS}	5	ground (logic)
TEST	6	test pin (connect to V_{SS})
SA0	7	I²C-bus slave address input (bit 0)
A3 to A0	8 to 11	I²C-bus subaddress inputs
V_{DD}	12	supply voltage
n.c.	13(1)	not connected
V_3, V_4	14, 15	LCD bias voltage inputs
V_{LCD}	16	LCD supply voltage
C39 to C0	17 to 56	LCD column driver outputs

Note

1. Do not connect, this pin is reserved.

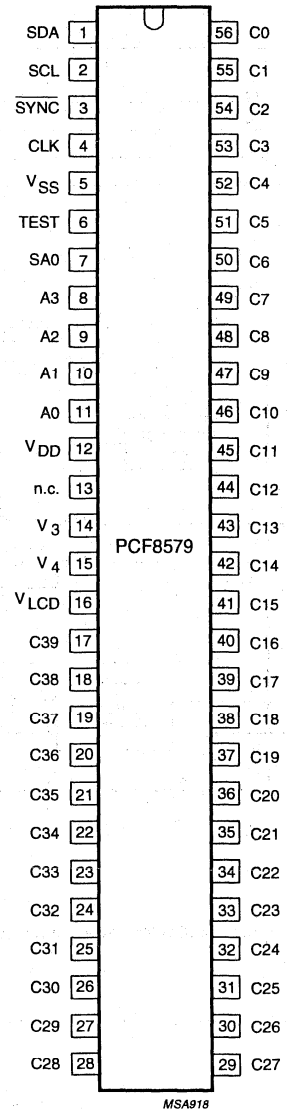


Fig.2 Pin configuration.

8-bit A/D and D/A converter PCF8591

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

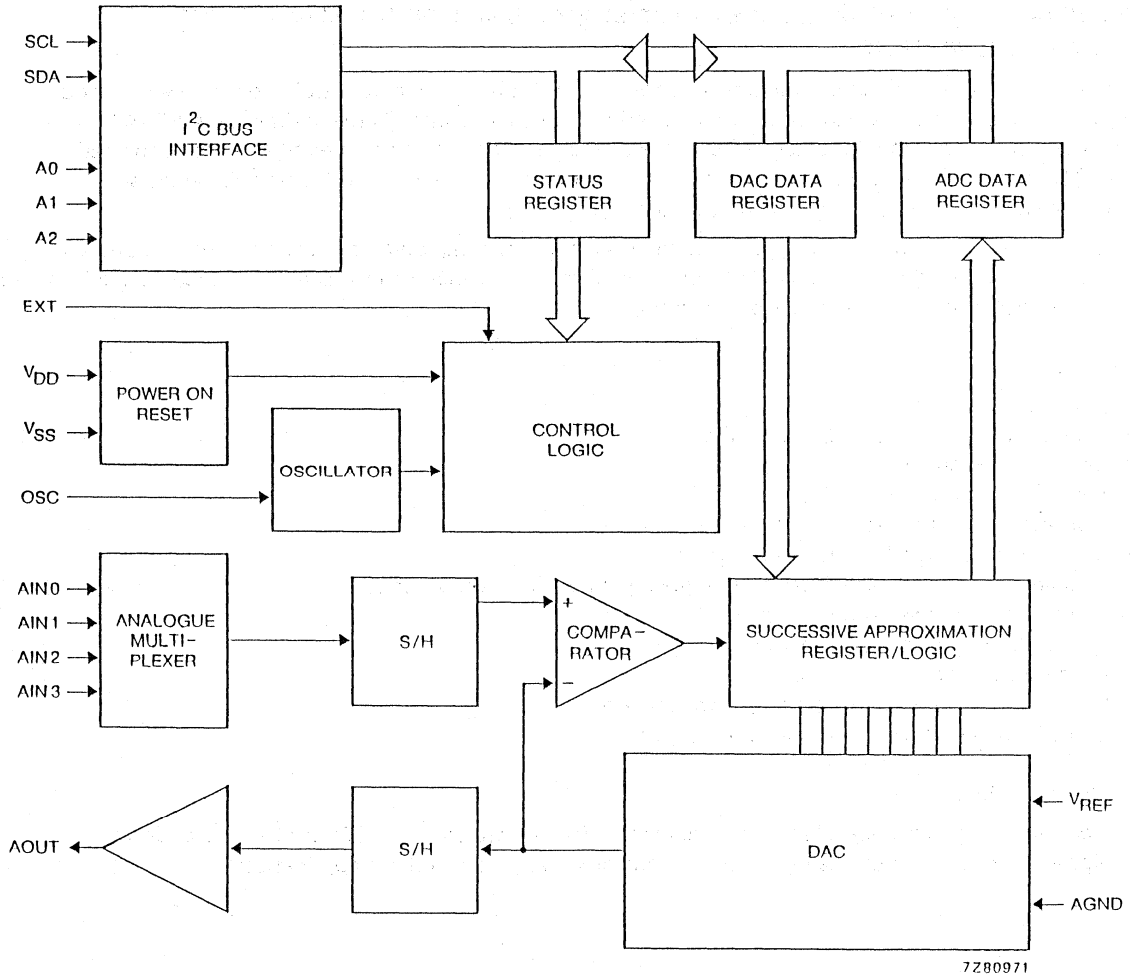


Fig. 1 Block diagram.

Low power clock calendar PCF8593

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

FEATURES

- I²C-bus interface operating supply voltage: 2.5 to 6.0 V
- Clock operating supply voltage (T_{amb} = 0 to +70 °C): 1.0 to 6.0 V
- Data retention voltage: 1.0 to 6.0 V
- External $\overline{\text{RESET}}$ input pin
- Operating current (f_{scl} = 0 Hz, 32 kHz time base, V_{DD} = 2.0 V): typ. 1 µA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C-bus)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Space-saving SO8 package
- Slave address:
  - READ A3H
  - WRITE A2H.

GENERAL DESCRIPTION

The PCF8593 is a CMOS Real-time clock/calendar optimized for low power consumption. Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. The built-in 32.768 kHz oscillator circuit and the first 8 registers are used for the clock/calendar and counter functions. The next 8 registers may be programmed as alarm registers or used as free RAM space.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	6.0	V
		I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz	–	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	4.0	15.0	µA
		f_{scl} = 0 Hz; V_{DD} = 2 V	1.0	8.0	µA
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8593P	8	DIL	plastic	SOT97-1
PCF8593T	8	SO8	plastic	SOT96-1

Low power clock calendar PCF8593

BLOCK DIAGRAM

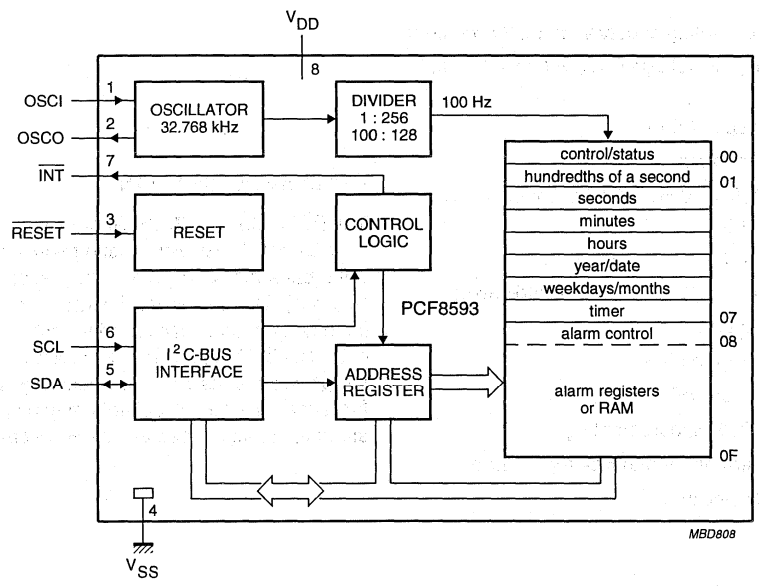


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
$\overline{\text{RESET}}$	3	reset input (active LOW)
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
$\overline{\text{INT}}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

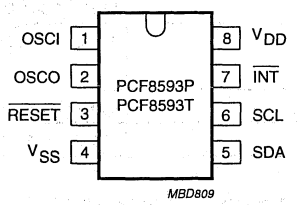


Fig.2 Pin configuration.

Low-voltage GSM front-end transceiver SA1620

DESCRIPTION

The SA1620 is a combined receive (Rx) and transmit (Tx) front-end for GSM cellular telephones. The receive path contains two low noise amplifiers (LNA1 and LNA2) with four switchable attenuation steps. A Gilbert Cell mixer in the receive path down-converts the RF signal to a first IF of 70MHz to 500MHz. A second Gilbert Cell in the transmit path transposes a GMSK or phase modulated IF to RF by image reject mixing. A buffered LO signal is fed to Rx and Tx mixers. Rx or Tx path or the entire circuit may be powered-down.

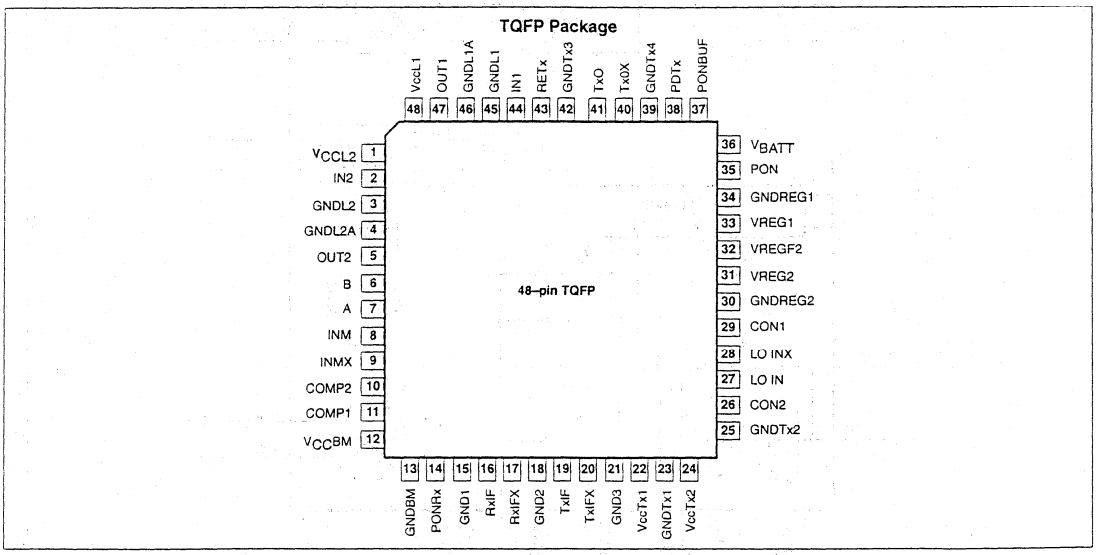
FEATURES

- Excellent noise figure: <2dB for the LNAs at 950MHz
- LNAs matched to 50Ω
- LNAs with gain control, 59dB dynamic range in four discrete steps
- Gain stability ±0.5dB within -40 to 85°C
- Absolute gain tolerance in the Rx path: ±2dB (active mode)
- Feedthrough attenuation LNA1 to Rx mixer ≥ 32dB
- Tx power adjustable from -3 to +12dBm by external resistor
- Direct supply: 2.7V to 5.5V
- Battery supply voltage V_{BATT} = 3.3V to 7.5V or direct supply
- Two DC regulators programmable for 2.9V, 3.3V, 3.6V or 5V
- Low current consumption: 25mA for Rx or 65mA for Tx
- Fully compatible with SA1638 GSM IF Digital I/Q circuit

APPLICATIONS

- 900MHz front end for GSM hand-held units
- Portable radio, TDMA systems

PIN CONFIGURATION



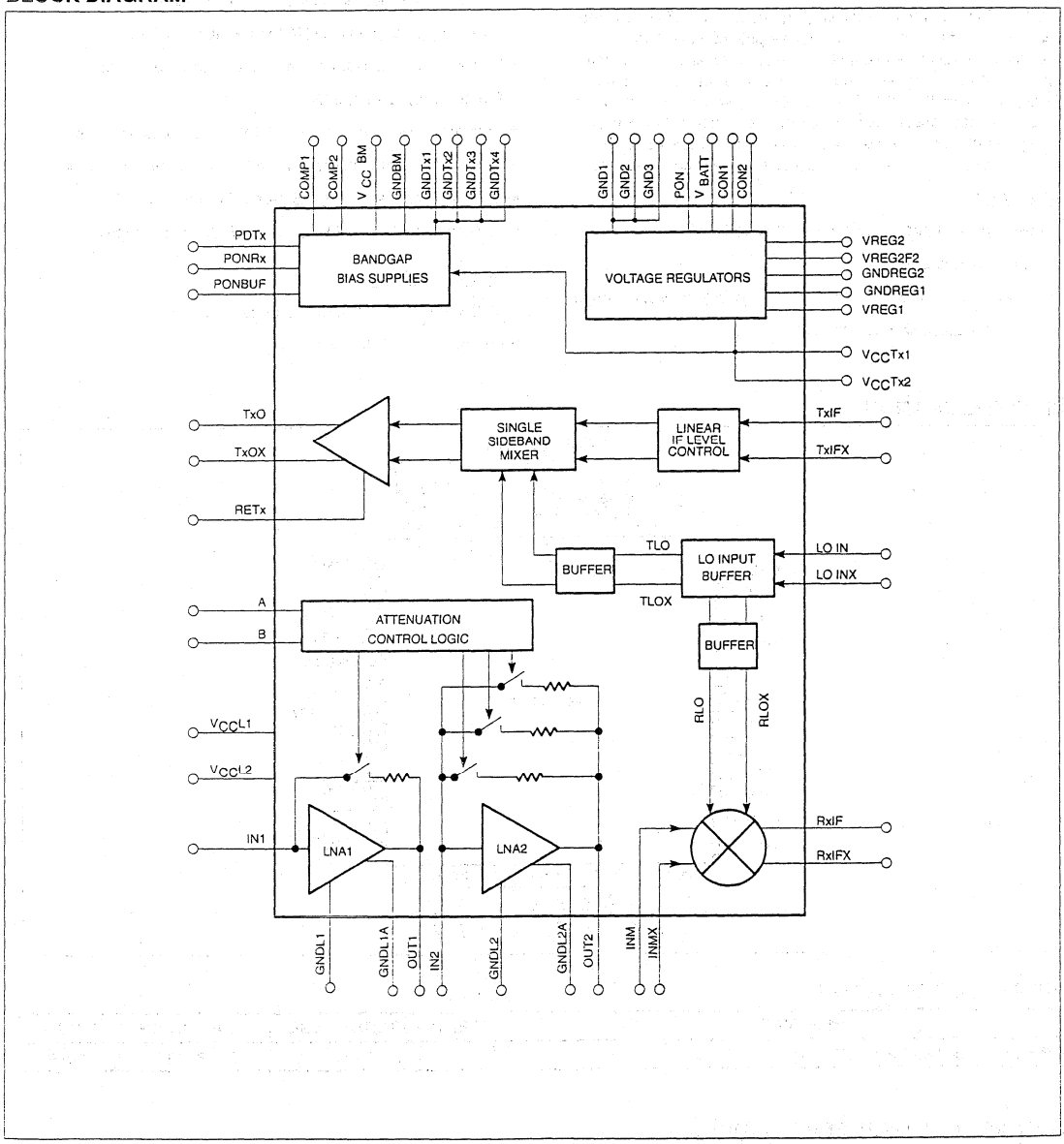
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (TQFP)	-40 to +85°C	SA1620BE	1706B

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	2.7 to 5.5	V
V_{BATT}	Battery voltage	3.3 to 7.5	V
T_A	Operating ambient temperature range	-40 to +85	°C

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	Description
DC Regulators		
15	GND1	Ground of regulator supply
18	GND2	Ground of regulator supply
21	GND3	Ground of regulator supply
26	CON2	Control 2, voltage select for regulator 1 and 2
29	CON1	Control 1, voltage select for regulator 1 and 2
30	GNDREG2	Ground of regulator 2
31	VREG2	Output of regulator 2
32	VREG2F2	Feedback of regulator 2
33	VREG1	Output of regulator 1
34	GNDREG1	Ground of regulator 1
35	PON	Power-on input of regulators
36	V_{BATT}	Input of regulator 1 and 2
Rx Path		
1	$V_{CC}L2$	Positive supply for LNA2
2	IN2	Input LNA2
3	GNDL2	Ground L2 for LNA2
4	GNDL2A	Ground L2A for LNA2
5	OUT2	Output LNA2
6	B	Attenuation select B for LNA1 and LNA2
7	A	Attenuation select A for LNA1 and LNA2
8	INM	RF input for Rx mixer, open emitter
9	INMX	Inverse RF input for Rx mixer, open emitter
10	COMP2	Capacitor for bias stabilization
11	COMP1	Capacitor for bias stabilization
12	$V_{CC}BM$	V_{CC} for Rx Bias and Rx mixer
13	GNDBM	Ground for Rx Bias and Rx mixer
14	PONRx	Power on input for Rx bias supply
16	RxIF	IF output, open collector
17	RxIFX	Inverse IF output, open collector
44	IN1	Input to LNA1
45	GNDL1	Ground L1 for LNA1
46	GNDL1A	Ground L1A for LNA1
47	OUT1	Output LNA1
48	$V_{CC}L1$	Positive supply for LNA1
Tx Path		
19	TxIF	IF input for Tx
20	TxIFX	Inverse IF input for Tx
22	$V_{CC}Tx1$	Positive supply for Tx input
23	GNDTx1	Ground for Tx input
24	$V_{CC}Tx2$	Positive supply for LO and Tx input
25	GNDTx2	Ground for LO and Tx input
38	PDTx	Power down Tx input
39	GNDTx4	Ground for Tx output
40	TxOX	Inverse Tx output, open collector
41	TxO	Tx output, open collector
42	GNDTx3	Ground 1 for Tx output side
43	RETx	Reference resistor for Tx output current
Elements for Tx and Rx Path		
27	LO IN	Input for Local Oscillator signal
28	LO INX	Inverse input for LO or AC ground
37	PONBUF	Power on first stage LO input buffer and bias

NOTES:
1. There are no ESD protection diodes at Pins 16, 17, 40 and 41. Thus, open-collector outputs may have increased DC voltage or higher AC peak voltage.
2. Pins 15, 18 and 21 are connected to each other and to a separate ground in REG1 and REG2.
3. Pins 23, 25, 42 and 39 are connected to each other and to the Tx path, LO buffer and associated bias supplies.
4. Pins 22 and 24 are connected to each other providing a sense input. They are also connected to the Tx path, LO buffer and associated bias supplies.
5. Pins 30 and 34 are not internally connected. They must be connected to external grounds.
6. Pins 48, 1, and 12 are not internally connected and have no ESD protection diodes between them. Power may be saved by connecting $V_{CC}L1$ or $V_{CC}L2$ to ground if LNA1 or LNA2 are not needed.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{BATT}	Battery voltage	-0.3 to +8.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CCXX}+0.3)	V
ΔV	$V_{CC}Tx1,2$ pins to $V_{CC}BM$	-0.3 to +1	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	800	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	−65 to +150	°C
V_{TXO}, V_{TXOX}	Positive RF peak voltage at Tx outputs	6	V
V_{RXIF}, V_{RXIFX}	Positive IF peak voltage at Rx mixer outputs	6	V

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}. 48-pin TQFP: θ_{JA} = 67°C/W.

DC REGULATORS

Two low drop regulators (REG1 and REG2) are included on the chip and may be used to deliver the supply voltage of the main circuitry (e.g., 2.9V) out of the battery (at V_{BATT} = 3.3 to 7.5V) as shown in Figure 2 and in Table 1.

REG1 is intended to supply, at least, the internal functions of the SA1620. Both regulators may also be used for external circuitry. For this application, different voltages may be programmed as shown in Table 1.

The transmitter supply pins (V_{CC}Tx1,2) also operate as a sensor connection in the feedback loop of REG1 and must be externally connected to pin VREG1. For REG2, the sensor pin VREGF2 must be connected to VREG2.

All ground pins are internally bonded to the header except for pins GNDL1, GNDREG1 and GNDREG2.

When both regulators are not used, connect pins V_{BATT}, PON, CON1, CON2, VREG1, VREG2 and VREG2F2 to ground.

Table 1. DC Regulator Output Voltage Control Pins

CON1	CON2	VREG1	VREG2	UNITS
L	L	2.9 ±5%	2.9 ±5%	V
L	H	3.3 ±5%	3.3 ±5%	V
H	L	3.6 ±5%	3.6 ±5%	V
H	H	5.0 ±5%	5.0 ±5%	V

NOTES:
1. The 2.9V setting allows ±5% and 55mV headroom above the 2.7V limit.
2. Logic levels at CON1 and CON2:
   H – Open circuit. Pin must not be connected externally. Logic high level supplied on chip.
   L – Connected to ground.
3. Currents at CON1 and CON2:
   H – 0µA
   L (PON = H) – 50µA
   L (PON = L) – <1µA

Table 2. DC Regulators

SYMBOL	PARAMETER		RATING	UNITS
V_{BATT}	Common positive input voltage at both regulators		3.3 to 7.5	V
VREG1, VREG2	Output voltages of regulators 1 and 2		See Table 1	V
I_{INT1}	Internal current of REG1 in power-on mode		4 + I_{VREG1}/10	mA
I_{INT2}	Internal current of REG2 in power-on mode		2.5 + I_{VREG2}/10	mA
I_{INT01}, I_{INT02}	Internal current in power-down mode		<15	µA
$I_{VREG1MAX}$[5]	Max output current at VREG1		100	mA
$I_{VREG2MAX}$[5]	Max output current at VREG2		30	mA
C13[4]	Capacitor at pin VREG1		0.1 to 1000	µF
C14[4]	Capacitor at pin VREG2		0.1 to 500	µF
BW[6]	V_{BATT} = 3.3V, I_{REG1} = 0.1mA		0.03	kHz
	V_{BATT} = 3.3V, I_{REG1} = 100mA		60	
	V_{BATT} = 7.5V, I_{REG1} = 100mA		80	
F_{REG}[8]	f	≤100kHz	≤–50	dB
		10MHz	≤–25	
		100MHz	tbd	
		400MHz	≤–30	

NOTES:
1. Power-on pin of Regulator 1 and 2: PON
2. Input currents at PON: <1µA. There are no pull-up or pull-down resistors.
3. Feedthrough attenuation from the logic input PON to the outputs VREG1 and VREG2: ≥40dB.
4. Recommended load capacitors: In every case C13 = C14 = 100nF to ground with series resistance ≤0.1Ω. Additional capacitor optional ≤1000µF with series resistance ≤5Ω.
5. At T_j ≥ 150°C a thermal switch reduces the output current.
6. Typical open loop bandwidths of regulator 1 at V_{REG1} = 2.9V and C13 = 100nF.
7. Switch on times: tbd
8. Feedthrough attenuation (at the indicated frequency f) from the input V_{BATT} to the outputs V_{REG1} and V_{REG2} at V_{BATT} = 3.3V, (CON1=CON2=L): F_{REG} (f) = V_{REG} (f) / V_{BATT} (f).

DC ELECTRICAL CHARACTERISTICS

V_{CCxxx} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Transmitter						
$I_{VCCTX1,2}$	Current at pins V_{CC}Tx1,2	Tx active	35	44	58	mA
R1	External resistor[1]		200	250		Ω
V_{R1}	Internal supply at pin RETx	V_{CC}Tx1,2 = 2.7V		0.4		V
		V_{CC}Tx1,2 = 5.5V		0.4		
I_{R1}	Current at pin RETx	R1 = 250Ω, V_{CC}Tx1,2 = 2.7V		1.6		mA
		R1 = 250Ω, V_{CC}Tx1,2 = 5.5V		1.6		
I_{TXO}+ I_{TXOX}	Current sum at pins TxO + TxOX	R1 = 250Ω, V_{CC}Tx1,2 = 2.7V		16		mA
		R1 = 250Ω, V_{CC}Tx1,2 = 5.5V		18		
Low noise amplifiers						
I_{VCC}L1	Current at pin V_{CC}L1	G1hi mode		3.5		mA
I_{VCC}L2	Current at pin V_{CC}L2	G2hi mode		3.5		mA
Rx mixer						
I_{RxIF}	Output current at pin RxIF			5		mA
I_{RxIFX}	Output current at pin RxIFX			5		mA
I_{VCC}BM	Current at pin V_{CCBM}	PONBUF = H		0.8		mA
Logic levels[2]						
V_{IH}	Logic 1 level		2.0		V_{CCBM}	V
V_{IL}	Logic 0 level		0		0.8	V
I_I	Input logic current				1	µA
C_{Ia}	Input logic capacitance			1.7		pF

NOTES:

1. The output current I_{TXO} + I_{TXOX} is adjustable by the external resistor R1. I_{TXO} + I_{TXOX} = 10 * I_{R1}, IR1 = V_{R1}/R1.
2. Thresholds are independent of supply voltages. Thus the SA1620 is compatible with SA1638 and with the power down inputs of usual external voltage regulators.

AC ELECTRICAL CHARACTERISTICS

V_{CCXX} = +3V, T_A = 25°C; RF = 925-960MHz; IF=400MHz, f_{LO}=RF + IF; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Low Noise Amplifier LNA1[1]						
S_{21}	Gain	G1hi mode		10		dB
		G1hi mode, RF = 1800MHz		-2.5		
		G1lo mode		-9		
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	G1hi mode		0.003		dB/°C
		G1lo mode		0.0140		
$\Delta S_{21}/\Delta V_{CCL1}$	Gain/voltage sensitivity			0.1		dB/V
$\Delta S_{21}/\Delta f$	Gain frequency variation			0.01		dB/MHz
S_{12}	Reverse isolation	G1hi mode		-20		dB
S_{11}	Input match[2]	50Ω		-10		dB
S_{22}	Output match[2]	50Ω		-12		dB
P_{-1dB}	Input 1dB gain compression	G1hi mode	-15			dBm
IIP3	Input third order intercept		-4.5			dBm
NF	Noise figure			1.7	2	dB
t_{ON}	Turn-on time			7		µs
t_{OFF}	Turn-off time			0.5		µs
Low Noise Amplifier LNA2[1]						
S_{21}	Gain	G2hi mode		11		dB
		G2hi mode, RF = 1800MHz		0.5		dB
		G2lo1 mode	-7	-5	-3	dB
		G2lo2 mode	-21	-19	-17	
		G2lo3 mode	-31	-29	-27	
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	G2hi mode		0.003		dB/°C
		G2lo1,2,3 modes		0.014		
$\Delta S_{21}/\Delta V_{CCL2}$	Gain/voltage sensitivity			0.1		dB/V
$\Delta S_{21}/\Delta f$	Gain frequency variation			0.01		dB/MHz
S_{12}	Reverse isolation	G2hi mode		-20		dB
S_{11}	Input match[2]	50Ω		-10		dB
S_{22}	Output match[2]	50Ω		-12		dB
P_{-1dB}	Input 1dB gain compression	G2hi mode	-16			dBm
IIP3	Input third order intercept		-5.4			dBm
NF	Noise figure			1.7	2	dB
t_{ON}	Turn-on time			7		µs
t_{OFF}	Turn-off time			0.5		µs
Rx Mixer						
VG_C	Voltage conversion gain			19.3		dB
PG_C	Power conversion gain	R3=R4 = 800Ω		+8.5		dB
		RF = 1800MHz		0		
$PG_C/\Delta T$	Gain temperature sensitivity			0		dB/°C
$PG_C/\Delta f$	Gain frequency variation			0		dB/MHz
S_{11}	Mixer input match at ports INM and INMX[3]			-13		dB
NF_M	SSB combined noise figure			9	9.5	dB
P_{-1dB}	Input 1dB compression	R3 = R4 = 800Ω		-6		dBm
IIP3	Input third order intercept		+2.5			dBm
IIP2	Input second order intercept			tbd		dBm
G_{RFM-IF}	RF feedthrough	400MHz		-30	-25	dB
$G_{LOfloor}$	LO floor feedthrough	400MHz		-30	-25	dB
G_{LO-IF}	LO feedthrough to IF	1.3GHz		-8		dB

AC ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Rx Mixer (cont.)						
G_{LO-RFM}	LO to mixer input feedthrough	1.3GHz		-30		dB
G_{LO-RF1}	LO to RF LNA1 input feedthrough	1.3GHz		-40		dB
G_{LNA1-2}	LNA1 output to LNA2 input feedthrough	400MHz 1290-1760MHz			-36 -24	dB
G_{LNA2-M}	LNA2 output to mixer input feedthrough	1290-1760MHz			-24	dB
G_{LNA1-M}	LNA1 output to mixer input feedthrough	400MHz 1290-1760MHz			-24 -32	dB
LO input						
Z_{IN}	Input impedance (each single-ended input)	1.3GHz		35-j97		Ω
P_{IN}	Input power			-10		dBm
$A_{LO\ IN}$	Recommended input amplitude between pins LO IN and LO INX		100	150	250	mV
A_{SAT}	Transistor saturation limit, max input amplitude			500		mV
Tx IF input						
$\|Z_{IN}\|$	Input impedance	400MHz		2		kΩ
P_{IN}	Input power			-25		dBm
A_{TXIF}	Recommended input amplitude between pins TxIF and TxIFX		100	150	220	mV
Tx RF output						
P_{OUT}	R1 = 250Ω, R5 = R6 = 200Ω, V_{CC}Tx1,2 = 2.7V		7	7.5	8	dBm
	R1 = 250Ω, R5 = R6 = 200Ω, V_{CC}Tx1,2 = 5.5V		8	8.5	9	dBm

NOTES:
1. If the LNA1 is not needed, connect pin V_{CC}L1 and IN1 to GND. If the LNA2 is not needed, connect pin V_{CC}L2 and IN2 to GND.
2. Simple L/C elements are needed to achieve specified return loss.
3. The mixer RF inputs (emitters of a Gilbert Cell) may be driven by a symmetrical matching network.
4. Input symmetry suppression is such that the product 6*RF–4*LO is to be suppressed by at least 66dB relative to the wanted IF output when the input to the mixer is at –32dBm.

Table 3. Power-Down and Tx/Rx Control Logic

No.	PONBUF	PDTX	PONRX	MODE	RESULT
1	H	H	L	Standby	LO buffer active, Tx and Rx path inactive
2	H	L	L	Transmit	LO buffer active, Tx path active, Rx path inactive (LNAs + mixer)
3	H	H	H	Receive	Tx path inactive, LO buffer and Rx path active (LNAs + mixer)
4	H	L	H	Calibrate	Tx path and Rx LNAs inactive, LO buffer and Rx mixer active
5	L	x	x	Power-Down	Tx- and Rx-path, LO buffers and Bias inactive

NOTES:
1. Logic levels of PONBUF, PDTx and PONRx: TTL, see DC Electrical Characteristics.
2. Logic levels / polarities are compatible with Philips Semiconductors Power Amp Controller PCA5075 and synthesizers UMA1019 or SA8025.
3. First stage of LO buffer and parts of bias supply are powered on by PONBUF.
4. Tx- or Rx-paths may be activated for special timeslots. Lines 1 and 4 show options to support DC offset calibrations at baseband mixers, following in the receiver chain (SA1638).
5. Feedthrough attenuation PONBUF, PDTx, and PONRx to outputs: [tbd]

Table 4. Gain Control Logic for LNA1 and LNA2

INPUT		ATTENUATION STEP	GAIN		POWER CONSUMPTION	
a	b		LNA1	LNA2	LNA1	LNA2
H	H	0	G1hi	G2hi	on	on
H	L	1	G1hi	G2lo1	on	off
L	H	2	G1hi	G2lo2	on	off
L	L	3	G1lo	G2lo3	off	off

NOTES:
1. Logic levels of a and b: TTL
2. For values of G1hi and G1lo, G2hi, G2lo1, G2lo2 and G2lo3 see LNA1 and LNA2 AC Electrical Characteristics.
3. Feedthrough attenuation A and B to outputs: tbd.

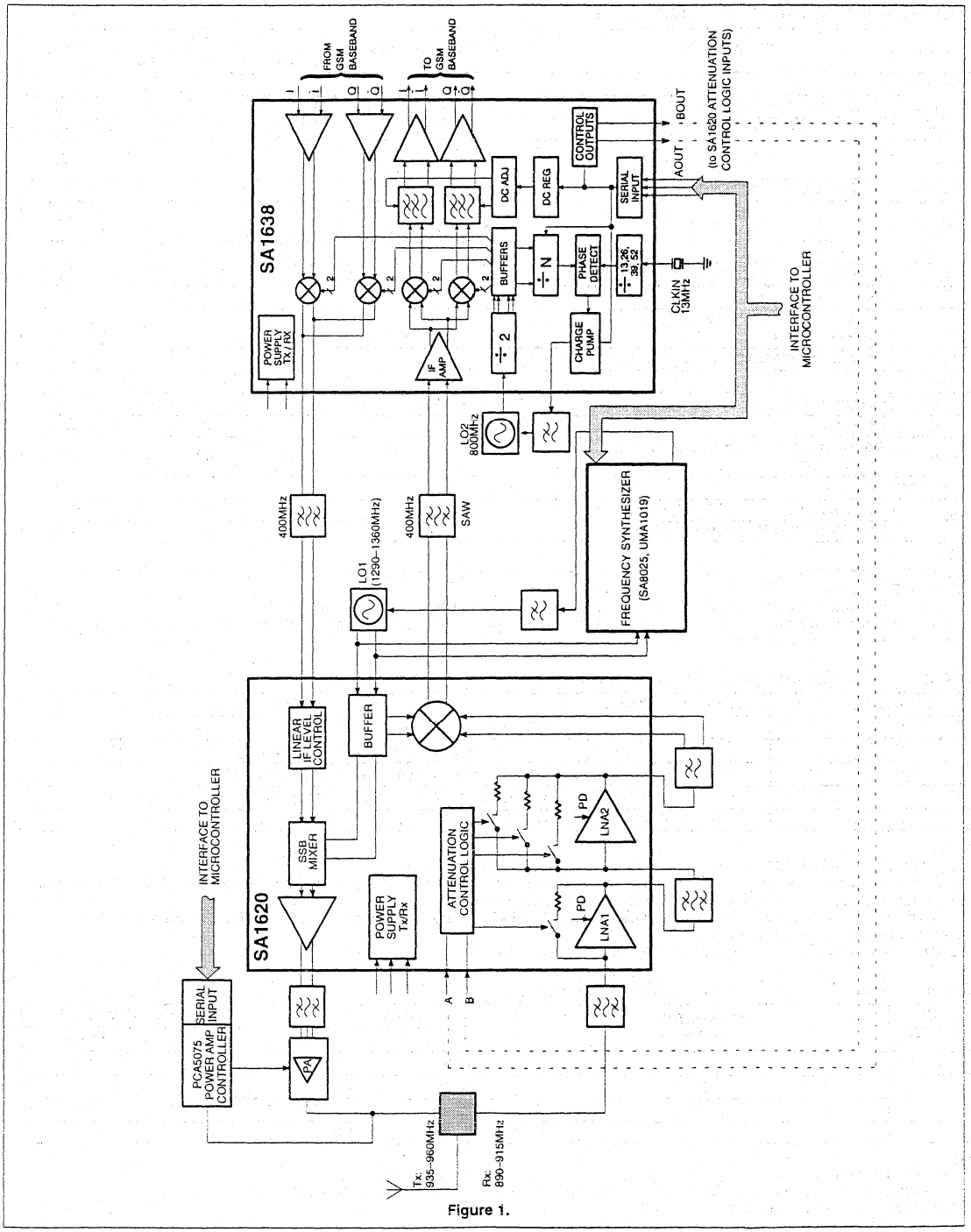

FROM GSM BASEBAND
TO GSM BASEBAND
SA1638
POWER SUPPLY TX/RX
IF AMP
BUFFERS
DC ADJ
DC REG
CONTROL OUTPUTS
SERIAL INPUT
PHASE DETECT
CHARGE PUMP
CLKIN 13MHz
AOUT
BOUT
(to SA1620 ATTENUATION CONTROL LOGIC INPUTS)
INTERFACE TO MICROCONTROLLER
LO2 800MHz
400MHz
SAW
LO1 (1290–1360MHz)
FREQUENCY SYNTHESIZER (SA8025, UMA1019)
SA1620
LINEAR LEVEL CONTROL
BUFFER
SSB MIXER
ATTENUATION CONTROL LOGIC
POWER SUPPLY Tx/Rx
LNA2
LNA1
PD
A
B
INTERFACE TO MICROCONTROLLER
SERIAL INPUT
PCA5075 POWER AMP CONTROLLER
PA
Tx: 935–960MHz
Rx: 890–915MHz

Figure 1.

Overview of Dual GSM/PCN Architecture

The SA1620 RF front-end and SA1638 IF transceivers form a dual conversion architecture which uses a common IF and standard I/Q baseband interface for both transmit and receive paths. This approach avoids the screening difficulties of direct modulation in the transmit direction and the mass production and practical performance issues related to direct conversion in the receive direction. The time division multiplex nature of the GSM system permits integration of the transmit and receive functions together on the one RF and one IF chips. This simplifies the distribution of local oscillator signals, maximizes circuitry commonality, and reduces power consumption.

The SA1620 and SA1638 allow considerable flexibility to optimize the transceiver design for particular price/size/performance requirements, through choice of appropriate RF and IF filters. The IF may be chosen freely in the range 70–500MHz. The same IF can be used in the transmit and receive directions. Alternately, different IFs can be used if the SA1638 synthesizer frequency is switched between transmit and receive timeslots. The comparison frequency of the SA1638 PLL is high in order to provide fast switching time.

With suitable choice of the IF, an identical SA1638 IF receiver design can be used for both 900MHz GSM and 1800MHz PCN (DCS1800) equipment.

General Benefits/Advantages

- 2.7V operation. Compatible with 3V digital technology and portable applications. (Higher voltage operation also possible, if desired.)
- Excellent dynamic range. The availability of two LNAs allows flexibility in receiver dynamic design for portable and mobile GSM spec. applications with appropriate filters. If for a particular application a GaAs or discrete front-end is desired, one of the LNAs can be left unpowered. The placing of the AGC gains switches at the front means that for most of the time some attenuation will be inserted, further increasing typical dynamic performance beyond that specified by GSM.
- High power transmit output driver, delivering +7.5dBm output. This is sufficient to drive a filter and power amplifier input, without a driver amplifier. To avoid unnecessary current consumption the output power can be reduced, if not required, by appropriate choice of an external resistor.
- DC offsets generated in the receive channel are independent of the AGC setting, and correctable by software to prevent erosion of signal handling dynamic range by DC offsets. Independence of DC from AGC setting is achieved by putting the gain switches in the RF front-end.
- Minimal high-quality filter requirements. As a result of the integration in the SA1638 of high quality channel selectivity filters, only sufficient filtering is needed in the receive path to provide blocking protection for the second mixers. This reduces receiver cost and size.
- Operation at a high IF allows RF image reject filters to be relaxed. For example, at a 400MHz IF, the natural gain roll-off in the LNAs and mixer suppresses the image signal in the 1800MHz band by typically 28dB below the desired 900MHz band signal.

Receive Path

Multiple LNAs allow the flexibility to exploit the best choice of currently available filters (on performance, size, or cost grounds). This approach is preferable to a single high-gain stage as the stray cross-coupling effects between pins remain manageable. In a single stage amplifier this would limit the amount of rejection of out-of-band signals that could be achieved, and would also limit the amount of AGC attenuation that could be practically implemented.

The LNAs are powered up only when PONBUF, PDTx and PONRx are high, to allow a high degree of battery economy. If greater sensitivity is required for an application, an external preamplifier circuit can be used instead of LNA1, and LNA1 left unconnected.

A special mode is provided with just the IF output related circuitry active in order to allow calibration of the DC offset at the SA1638 baseband receive outputs. This offset contains a contribution due to coupling effects between the second local oscillator and the IF circuitry, and therefore the receiver is set up in the receive state (but with incoming signals excluded) to allow accurate offset calibration.

Gain Control

Gain control is implemented in the SA1620 RF front-end. This avoids the disruption of the DC offset at the baseband IQ outputs that is typically caused by changes in the AGC. The SA1620 and SA1638 are designed so that the GSM dynamic range requirements can be met with the AGC remaining on the maximum gain setting.

These gain steps scale the dynamic range of the received signal (e.g., 90dB for GSM) into the dynamic range of the baseband processing device.

The absolute gain tolerances may be measured together with the attenuation tolerances of external filters during production of the receiver equipment. After software calibration switching from one dynamic range to another will cause only minor errors.

Tx Path

TXIF and TXIFX are differential IF inputs for phase modulated signals (e.g., GMSK). There is an IF level control loop which provides a constant amplitude to an image reject up mixer. Thus, this mixer operates linearly in the IF path, independent of IF level tolerances.

The single sideband up mixer is sufficient in quadrature to achieve the typical performance indicated in Table 6 over an IF range of 250 to 500MHz. The mixer is operating in switching mode by well matched 0° and 90° LO signals, optimized for 1.1 to 1.5GHz.

The Tx output stage operates in switching mode. Thus, parasitic AM at the IF is not transferred. The outputs TXO and TXOX may be used symmetrically or single-ended. Some spurious emissions will be very low when a symmetrical output signal is used.

$P_{OUT} = 6.25 * (R_5 + R_6) * (I_{R1})^2$

with $R_5 = R_6$ according to Figure 2 and $I_{R1} = V_{R1}/R1$ according to DC Electrical Characteristics. P_{OUT} is adjustable with R1 and is accurate to within ±1dB over the full voltage range 2.7 to 5.5V, and ±0.5dB from a given supply voltage. The absolute limit of the negative peak voltage swing at pins TxO and TxOX is $V_{SAT} = V_{CC}Tx1,2 - 1V$. The absolute limit of the positive peak voltage is +6V.

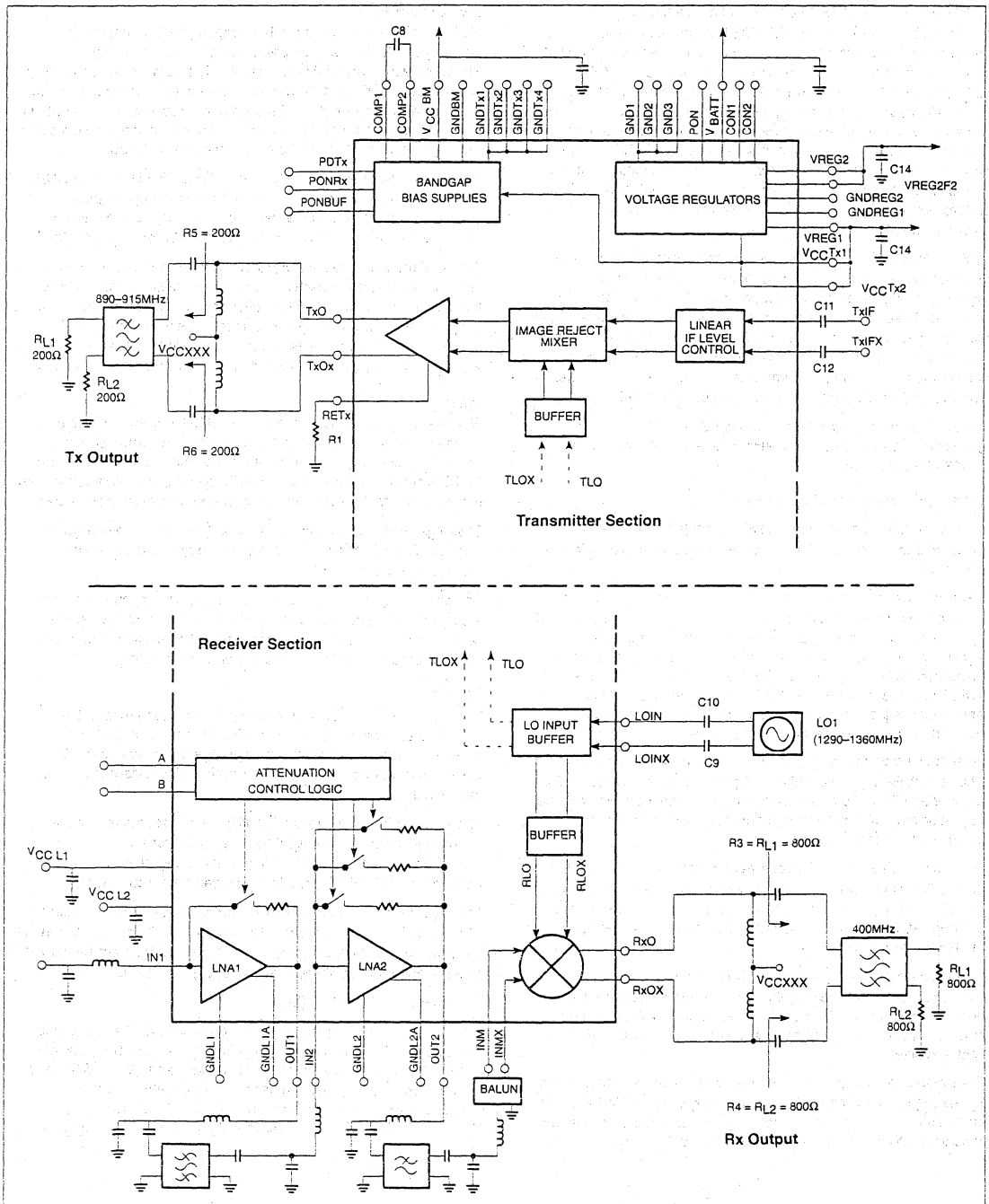


Figure 2. Application Circuit

LO Input

The LO input is used in Tx- and in Rx-mode.

Only one synthesizer PLL is necessary to supply the LO input with different frequencies in Tx and Rx timeslots.

The LO input buffer should only be set in power-down mode together with the PLL. As further buffering is included on chip there will be no influence on the PLL in active mode when the SA1620 Rx- or Tx-path is power On or Off. Current consumption can thus be saved by powering on the Rx- and Tx-circuitry just before it is required, without disruption of the LO circuitry. LO input pins LO IN and LO INX may be used single-ended or symmetrically.

Table 5. GSM/DSC1800 Frequency Specification

(GSM 05.05, Version 4.2.0, April 1992) Mobile Stations Frequency Bands

	GSM	EGSM	DCS1800	Unit
Tx	890 to 915	880.2 to 915	1710 to 1785	MHz
Rx	935 to 960	925.2 to 960	1805 to 1880	MHz

Table 6. Tx Output Frequency and Tx Mixer Products

IF=400MHz, symmetrical load at pins TxO, TxOX.

No.	SPECTRAL LINE f=n*IF+m*LO MHz			Order		RELATIVE POWER OF SPECTRAL LINE			REMARKS
	LO = 1280MHz	LO = 1300MHz	LO = 1315MHz	n	m	min dBc	typ dBc	max dBc	
1	80	100	115	–3	1		–43	–36	
2	160	200	230	–6	2		–69	–50	
3	320	300	285	4	–1		–70	–50	
4	400	400	400	1	0		–59	–32	IF
5	480	500	515	–2	1		–62	–50	
6	560	600	630	–5	2		–71	–50	
7	720	700	685	5	–1		–49	–36	
8	800	800	800	2	0		–47	–40	2)
9	880	900	915	–1	1		0	0	1)
10	960	1000	1030	–4	2		–49	–45	3)
11	1020	1100	1185	6	–1		–50	–45	
12	1200	1200	1200	3	0		–68	–50	
13	1280	1300	1315	0	1		–57	–40	LO
14	1360	1400	1430	–3	2		–55	–36	
15	1440	1500	1545	–6	3		–61	–50	
16	1600	1600	1600	4	0		–67	–50	
17	1680	1700	1715	1	1		–29	–15	4) 5)
18	1760	1800	1830	–2	2		–50	–40	3)
19	1840	1900	1945	–5	3		–29	–20	3)
20	2000	2000	2000	5	0		–62	–40	
21	2080	2100	2115	2	1		–67	–40	
22	2160	2200	2230	–1	2		–56	–40	
23	2240	2300	2345	–4	3		–63	–40	
24	2400	2400	2400	6	0		–69	–40	
25	2480	2500	2515	3	1		–51	–40	
26	2560	2600	2630	0	2		–52	–40	2LO

NOTE:

1. Desired Tx output frequency LO–IF corresponding to EGSM Tx band in Table 5.
2. (LO+IF)–(LO–IF) = 2 * IF
3. See Rx bands in Table 5
4. LO+IF = mixer image frequency
5. See Tx bands in Table 5

Table 7. Tx Output Noise Floor

Measured 10MHz away from spectral lines of Table 6.

Frequency MHz		dBc/Hz			REMARKS
		MIN	TYP	MAX	
< 860				–101	
860 to 880				–124	
880.2 to 890				–124	EGSM TX extension
890 to 915				–124	GSM TX
915 to 925				–124	
925.2 to 935				–133	EGSM RX extension
935 to 960				–145	GSM RX
960 to 1000				–126	
1000 to 1710				–87	
1710 to 1785				–87	DCS1800 TX
1785 to 1805				–87	
1805 to 1880				–129	DCS1800 RX
1880 to 12750				–87	
>12750				tbd	

Tx Noise Density at Adjacent Channel

Measured 200kHz away from Tx–RF: ≤–115dBc/Hz

Low-voltage IF I/Q transceiver SA1638

DESCRIPTION

The SA1638 is a combined Rx and Tx IF I/Q circuit. The receive path contains an IF amplifier, a pair of quadrature down-mixers, and a pair of baseband filters and amplifiers. A second pair of mixers in the transmit path transposes a quadrature baseband input up to the IF frequency. An external VCO signal is divided down internally and buffered to provide quadrature local oscillator signals for the mixers. A further divider chain, reference divider and phase detector are provided to avoid the need for an external IF synthesizer. Rx or Tx path or the entire circuit may be powered down by logic inputs. On-board voltage regulators are provided to allow direct connection to a battery supply.

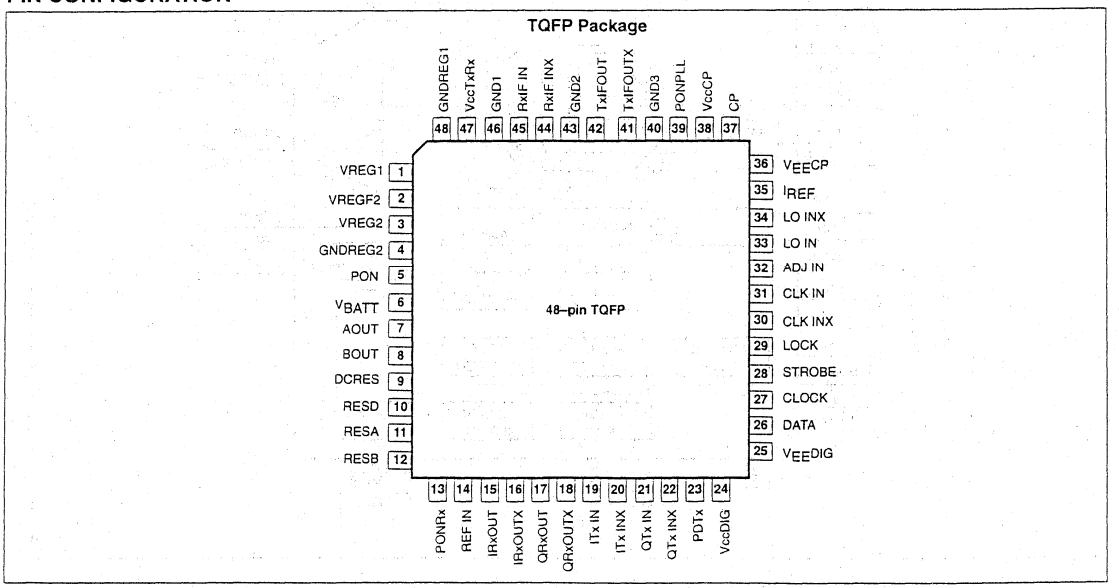
FEATURES

- Direct supply: 3.3V to 7.5V
- Two DC regulators giving 2.9V output
- Low current consumption: 14mA for Rx or 18mA for Tx
- Input/output IF frequency from 70-500MHz
- Internal IF PLL for synthesizing the local oscillator signal
- High performance on-board integrated receive filters with bandwidth tunable between 50kHz to 1MHz
- Switchable alternative bandwidth setting available to allow channel bandwidth flexibility in operation
- Designed for a widely-used I and Q baseband GSM interface
- Control registers power up in a default state
- Optional DC offset trim capability to <100mV
- Receive input impedance programmable
- Only a standard reference input frequency required, choice of 13, 26, 39 or 52MHz
- Fully compatible with SA1620 GSM RF front-end

APPLICATIONS

- IF circuitry for GSM 900MHz hand-held units
- IF circuitry for PCN (DCS1800) hand-held units
- Quadrature up and down mixer stage

PIN CONFIGURATION



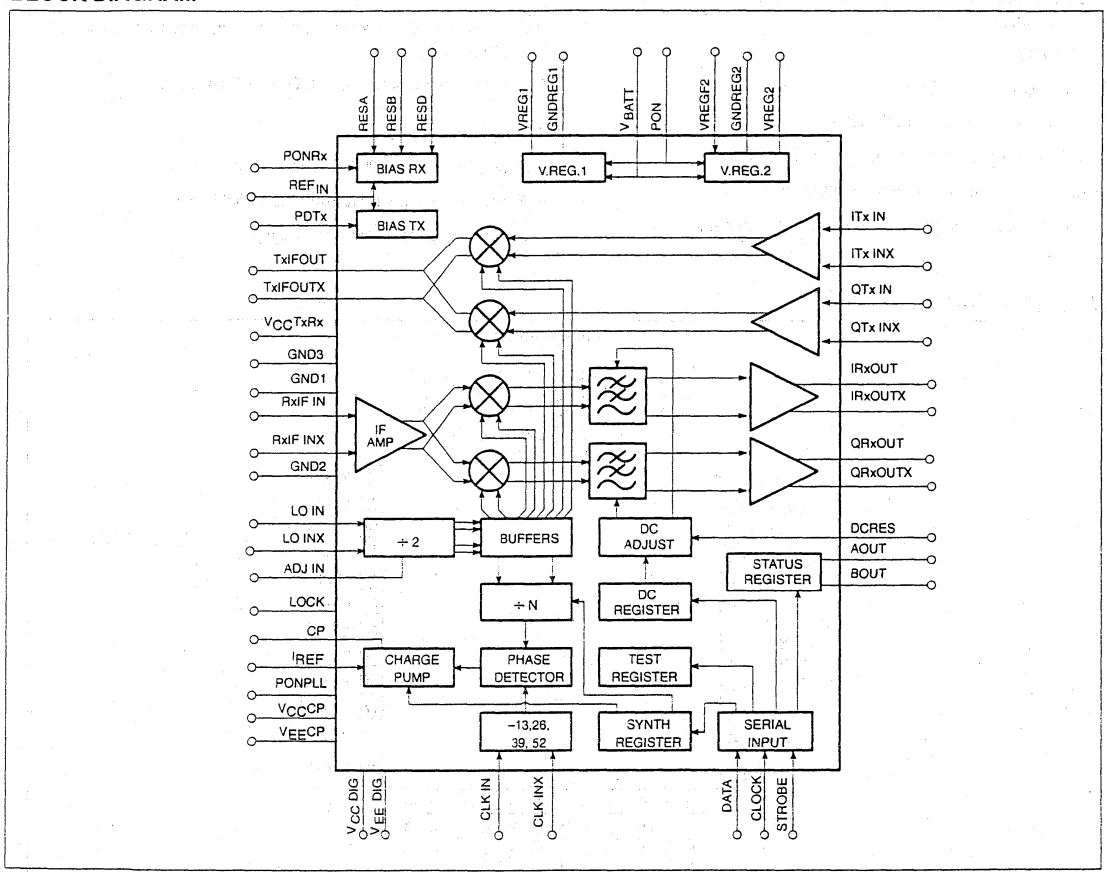
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (TQFP)	-40 to +85°C	SA1638BE	1706B

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXXX}	Supply voltages	2.7 to 5.5	V
$V_{CC}CP$	Charge pump supply voltage	2.9 to 5.5	V
V_{BATT}	Battery voltage	3.3 to 7.5	V
T_A	Operating ambient temperature range	-40 to +85	°C

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VREG1	Output voltage of regulator 1
2	VREGF2	Feedback of regulator 2
3	VREG2	Output voltage of regulator 2
4	GNDREG2	Ground of regulator 2
5	PON	Power-on input for voltage regulators 1 and 2 (active high)
6	V_{BATT}	Input voltage for regulators 1 and 2
7	AOUT	Control output (for SA1620 attenuation select A pin)
8	BOUT	Control output (for SA1620 attenuation select B pin)
9	DCRES	Reference resistor for DC offset circuit
10	RESD	Additional external current defining resistor for filters
11	RESA	Principal external current defining resistor for filters
12	RESB	Principal external current defining resistor for filters
13	PONRx	Power-on input for Rx (active high)
14	Ref IN	Reference voltage input
15	IRxOUT	In-phase differential receive baseband output
16	IRxOUTX	In-phase differential receive baseband output
17	QRxOUT	Quadrature differential receive baseband output
18	QRxOUTX	Quadrature differential receive baseband output
19	ITx IN	In-phase differential transmit baseband input
20	ITx INX	In-phase differential transmit baseband input
21	QTx IN	Quadrature differential transmit baseband input
22	QTx INX	Quadrature differential transmit baseband input
23	PDTx	Power-on for transmitter (active low)
24	V_{CC}DIG	Digital circuit supply
25	V_{EE}DIG	Digital ground
26	DATA	Data input for synthesizer
27	CLOCK	Clock input for synthesizer data
28	STROBE	Strobe input for synthesizer data
29	LOCK	Test control/synthesizer lock indicator
30	CLK INX	Differential reference input for synthesizer
31	CLK IN	Differential reference input for synthesizer
32	ADJ IN	External control for ÷2 trigger level
33	LO IN	Differential LO input
34	LO INX	Differential LO input
35	I_{REF}	Reference current for charge pump
36	V_{EE}CP	Charge pump ground
37	CP	Charge pump output
38	V_{CC}CP	Charge pump circuit supply
39	POnPLL	Power-on input for synthesizer circuits (active high)
40	Gnd3	Ground (internal connection to GND1 and GND2)
41	TxIFOUTX	Differential transmit IFoutput
42	TxIFOUT	Differential transmit IFoutput
43	GND2	Ground (internal connection to GND1 and GND3)
44	RxIF INX	Differential receive IF input
45	RxIF IN	Differential receive IF input
46	GND1	Ground (internal connection to GND2 and GND3)
47	V_{CC}TxRx	Analog circuit supply voltage
48	GNDREG1	Ground of regulator 1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{BATT}	Battery voltage	-0.3 to +8.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CCXX}+0.3)	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	300	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}. 48-pin TQFP: θ_{JA} = 67°C/W.

Table 1. DC Regulators

V_{BATT} = 3.3V, T_A = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNITS
V_{BATT}	Common positive input voltage at both regulators		3.3 to 7.5	V
VREG1, VREG2	Output voltages of regulators 1 and 2		2.9 ±5%	V
IREG1	Supply current of REG1 in power-on mode	No load		mA
IREG2	Supply current of REG2 in power-on mode	No load		mA
IREG1, IREG2	Supply current in power-down mode	No load		μA
$I_{VREG1MAX}$[2]	Max output current at VREG1		30	mA
$I_{VREG2MAX}$[2]	Max output current at VREG2		30	mA
C13[1]	Capacitor at pin VREG1		0.1 to 1000	μF
C14[1]	Capacitor at pin VREG2		0.1 to 500	μF
BW	Bandwidth of VREG1 and VREG2		100	kHz
PSR[3]	Power supply rejection	at DC	–48	dB

NOTES:
1. Recommended load capacitors: In every case C13 = C14 = 100nF to ground with series resistance ≤0.1Ω. Additional capacitor optional ≤1000μF with series resistance ≤5Ω.
2. At $T_j \geq$ 150°C a thermal switch reduces the output current.
3. PSR measured from the input V_{BATT} to the outputs VREG1 and VREG2.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}XXX$ = PONRx = PONPLL = +3V; $V_{EE}XXX$ = GND1 = GND2 = GND3 = PDTx = 0V; f_{LO} = 800MHz; T_A = 25°C unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current					mA
	Rx and IF synthesizer active	PONRx = PONPLL = PDTx = Hi		14	17	
	Tx and IF synthesizer active	PONRx = PDTx = Low; PONPLL = Hi		18	21	
	Power-down mode	PONRx = PONPLL = Low; PDTx = Hi		.008	0.015	
CMOS Logic inputs (PDTx, POnRx, POnPLL, DATA, CLOCK, STROBE)						
V_{IH}	Input logic 1 level		2.0		V_{CC}	V
V_{IL}	Input logic 0 level		0		0.8	V
I_I	Input logic current				1	µA
C_I	Input logic capacitance				4	pF
CMOS Logic outputs (AOUT, BOUT and LOCK)						
V_{OH}	Output logic 1 level		V_{CC}DIG–0.6			V
V_{OL}	Output logic 0 level				0.55	V
Regulator (POn) Logic inputs						
V_{IH}	Input logic 1 level	Regulators 1,2 output ON	2.4			V
V_{IL}	Input logic 0 level	Regulators 1,2 output OFF			0.6	V
I_I	Input logic current				1	µA

AC ELECTRICAL CHARACTERISTICS

$V_{CC}XXX$ = PONRx = PONPLL =+3V; $V_{EE}XXX$ = GND1 = GND2 = GND3 = PDTx = 0V; f_{LO} = 800MHz; T_A = 25°C unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
IF Transmit Modulator						
BW	Input modulation of bandwidth	200Ω source impedance		2		MHz
	Input signal amplitude	Centered on REF_{IN} (V)		±REF_{IN}/2	±REF_{IN}/1.75	V
THD	Total harmonic distortion	Input signal amplitude = ±REF_{IN}/2		-50		dBc
R_{INTx}	Input resistance	Between pins: ITxIn and ITxInX	10			kΩ
C_{INTx}	Input capacitance	Between pins: ITxIn and ITxInX or QTxIn and QTxInX			10	pF
	Input offset voltage			5		mV
	Mean output voltage	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = ±REF_{IN}/2	V_{CC}–0.5			V
	Mean output current	Per collector		2.0		mA
	Output current DC offset				20	µA
	Output differential current			1.0		mA_{RMS}
	Output differential voltage	71Ω tuned load (dynamic impedance)		100		mV_{P-P}
f_{LO-IF}	LO feedthrough	Differential output			10	mA_{RMS}
	Channel matching: Gain Phase	f_{OUT} = 400MHz		 0.2 1.0		 dB degrees
	Equivalent input noise	At 10kHz		TBD		nV/√Hz
ΔG	Gain stability				2.0	dB
t_{ON}	Turn-on time			5		µs
t_{OFF}	Turn-off time			5		µs

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
IF Receiver						
RInRx	Differential input impedance	f_{IN} = 400MHz		5		kΩ
ROutRx	Output impedance			1		kΩ
	Output common mode voltage			REF_{IN}		V
f3dB	Low pass filter -3dB bandwidth	68kΩ resistor between pins RESA and RESB	72	80	88	kHz
	Low pass filter attenuation: 200kHz 400kHz 600kHz 6.5MHz 13.0MHz	68kΩ external resistor between RESA and RESB		 34 64 80 >80 >80		dB
VG	Voltage gain	Differential output PD into GSM baseband relative to 1200Ω source EMF	54		69	dB
NF	Noise figure at minimum gain	1200Ω source and external matching resistor and inductor		5.8		dB
	Channel matching: Gain Phase			 1.0 5.0		 dB degrees
	Output DC offset	Differential		200		mV
IIP2	Input second order intercept	1200Ω source EMF		-11		dBV
P_{-1dB}	Input 1dB compression point: In band 200kHz 400kHz 600kHz	1200Ω source EMF		 -60 -44 -41 -41		dBV
t_{ON}	Turn-On time	POnRx = V_{EE}		5		µs
t_{OFF}	Turn-off time	POnRx = V_{EE}		5		µs
IF Synthesizer						
f_{LO}	Local oscillator input frequency range		140		1000	MHz
Z_{LOIN}	Differential input impedance	Between pins LO_{IN} and $LO_{IN}X$		500 ll 0.5		Ω ll pF
	LO input sensitvity	Referred to 50Ω	300		550	mV_{p-p}
	Equivalent input noise	at 800MHz		tbd		nV / Hz
	Programmable divider: Division range Step size		64	 1	511	
f_{CLK}	Reference clock input frequency			13, 26, 39 or 52		MHz
Z_{CLKIN}	Differential input impedance	Between pins ClkIn and ClkInX		10 ll 1.0		kΩ ll pF
	CLK input sensitivity	Referred to 50Ω		200		mV_{p-p}
	Equivalent input noise	at 13MHz		tbd		nV / Hz
f_C	Phase detector comparison frequency			1		MHz
I_{REF}	Charge pump input reference current			31.2		µA
I_{CP}	Charge pump output current: C0...C2 = 000 C0...C2 = 111 Step size	I_{REF} =31.2µA, V_{CP} = V_{CC}CP/2		 0.5 1.0 0.071		mA
$\frac{\Delta I_{CP}}{I_{CP}}$	Relative output current variation[1]	I_{REF} =31.2µA			±10	%
ΔI_{CP_M}	Output current matching[2]	I_{REF} =31.2µA, V_{CP} = V_{CC}CP/2			±10	µA

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
IF Synthesizer						
	Output current tolerance with programmed step with temperature with output voltage	CP between 0.8V and $V_{CC}CP$ - 0.8V		 ±10 ±10 ±5		%
	Output leakage current			tbd		nA

NOTES:

1. The relative output current variation is defined thus:

$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|}$$; with $V_1 = 0.7V$, $V_2 = V_{DDA} - 0.8V$ (see Figure 1).

2. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on.

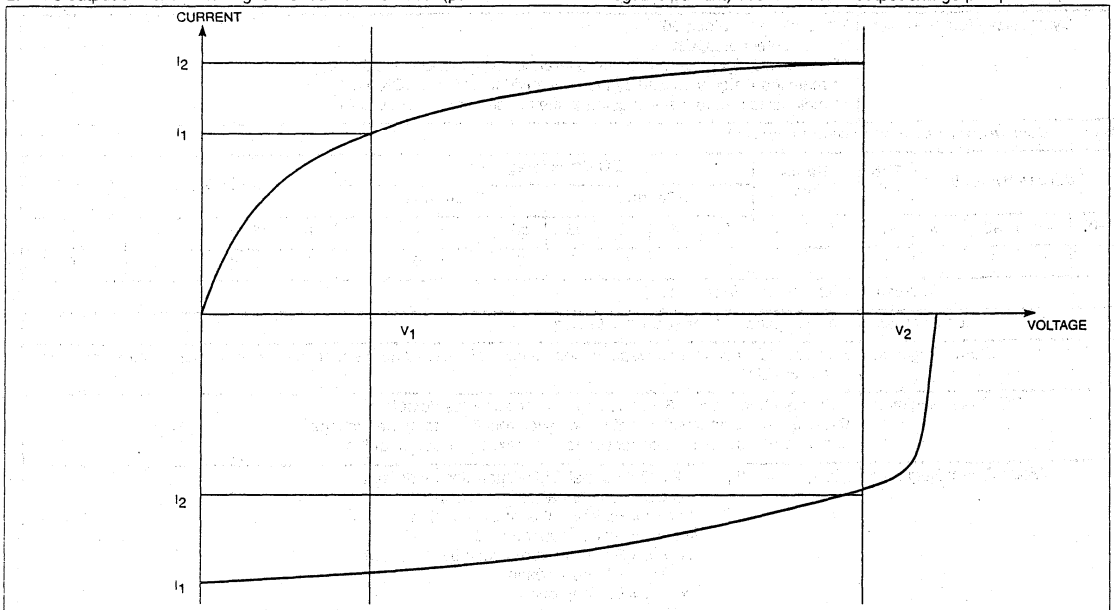


Figure 1. Relative Output Current Variation

Table 2. Definition of SA1638 Serial Registers

First data word: (loaded with default values)

Address SA1638				Sub Adr	N-Divider									Ref ÷ Reg		Charge-Pump			Synth Test	
a0	a1	a2	a3	sa	n0	n1	n2	n3	n4	n5	n6	n7	n8	r0	r1	c0	c1	c2	x0	x1
1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	1	1	1	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 0 for first data word
N-Divider:	9 bits, n0...n8, values 64 (00100 0000) to 511 (111111111) allowed for IF-choice, default 400
Reference ÷ Register:	2 bits, r0...r1, 00 = ÷13, 01 = ÷26, 10 = ÷39, 11 = ÷52. Default: 00
Charge-Pump Register:	3 bits, c0...c2, controls charge pump current, values 000 = minimum current to 111 = maximum current default maximum charge pump current
Synthesizer-Test Register:	2 bits, x0...x1, default 00 00 lock detect at LOCK pin 10 reference signal divided by the reference divider ratio at LOCK pin 01 main input signal divided by the main divider ratio at LOCK pin 11 main divider output signal going to the phase detector at LOCK pin

Second data word: (loaded with default values)

Address SA1638				Sub Adr	Status Reg		DC Offset Register								Mode Select Register					
							I-Channel				Q-Channel									
a0	a1	a2	a3	sa	s0	s1	i0	i1	i2	i3	q0	q1	q2	q3	t0	t1	t2	t3	t4	t5
1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 1 for second data word
Status Register:	2 bits, s0...s1, controls gain/attenuation settings of SA1620 data sheet, see Table 4. Gain Control Logic for LNA1 and LNA2.
DC Offset Register:	4 bits per channel, i0...i3 and q0...q3, no correction as default i0 and q0 switches offset polarity, 0 to lower voltage, 1 to higher voltage il...i3 and q1...q3, 000 no correction to 111 max. correction enabled
Mode Select Register:	6 bits, t0...t5, 000000 = normal GSM-Operation as default 0xxxxx = Rx internal path AC coupled 1xxxxx = Rx internal path DC coupled x0xxxx = Rx LO input applied x1xxxx = Rx LO input replaced by DC offset xx00xx = 90° loop closed xx01xx = 90° loop open xx10xx = 90° loop phase error medium external tune (ADJ IN) xx11xx = 90° loop phase error fine external tune (ADJ IN) xxxx00 = Rx LP filter 3dB BW = 80kHz (GSM) xxxx11 = Rx LP filter 3dB BW = 580kHz

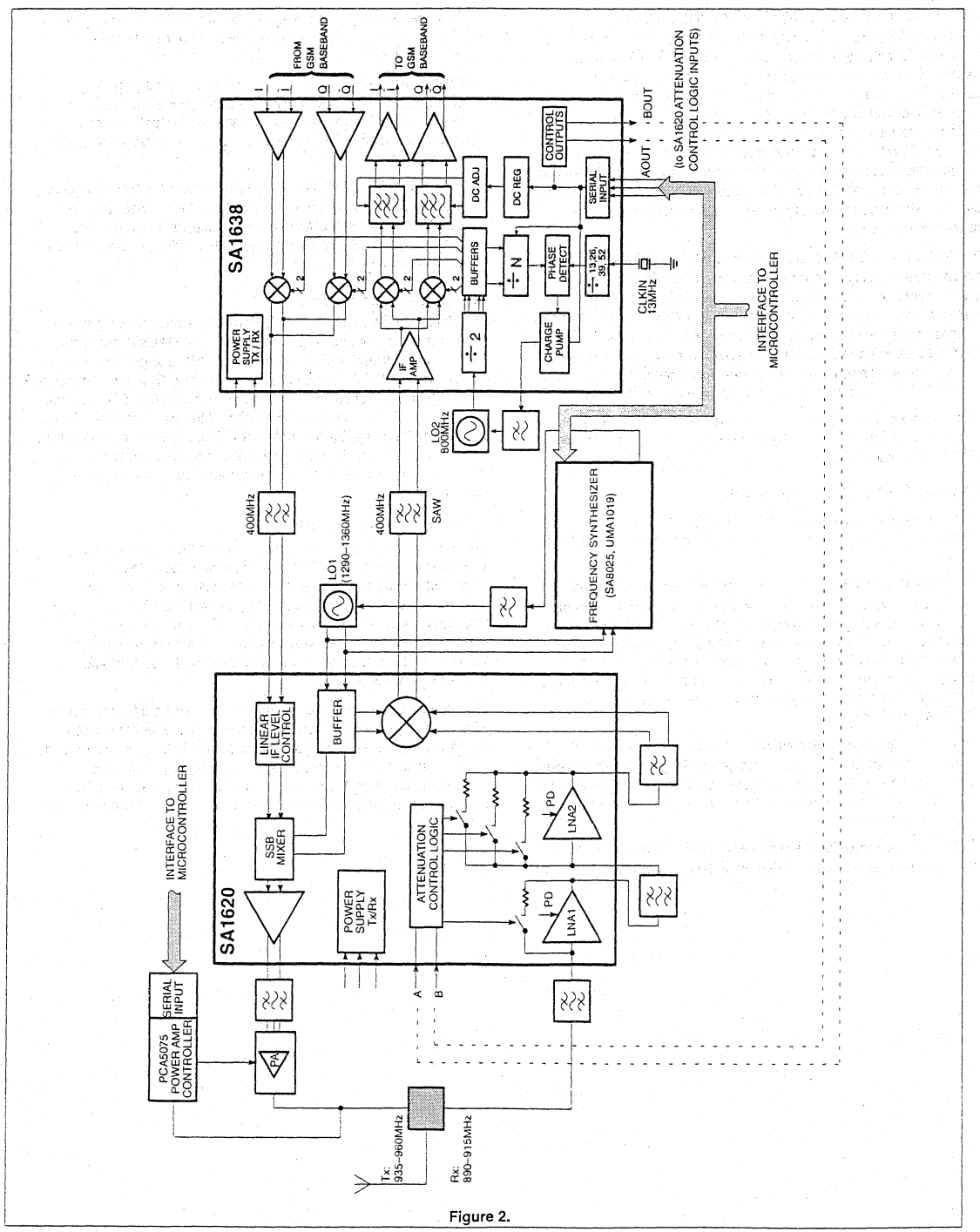

FROM GSM BASEBAND
TO GSM BASEBAND
SA1638
POWER SUPPLY TX/RX
IF AMP
÷ 2
BUFFERS
÷ N
PHASE DETECT
÷ 13,26, 39, 52
CHARGE PUMP
DC ADJ
DC REG
CONTROL OUTPUTS
SERIAL INPUT
AOUT
BOUT
(to SA1620 ATTENUATION CONTROL LOGIC INPUTS)
CLKIN 13MHz
INTERFACE TO MICROCONTROLLER
LO2 800MHz
400MHz
SAW
400MHz
LO1 (1290–1360MHz)
FREQUENCY SYNTHESIZER (SA8025, UMA1019)
SA1620
LINEAR IF LEVEL CONTROL
BUFFER
SSB MIXER
POWER SUPPLY Tx/Rx
ATTENUATION CONTROL LOGIC
PD
LNA2
PD
LNA1
A
B
INTERFACE TO MICROCONTROLLER
SERIAL INPUT
PCA5075 POWER AMP CONTROLLER
PA
Tx: 935–960MHz
Rx: 890–915MHz

Figure 2.

Overview of Dual GSM/PCN Architecture

The SA1620 RF front-end and SA1638 IF transceivers form a dual conversion architecture which uses a common IF and standard I/Q baseband interface for both transmit and receive paths. This approach avoids the screening difficulties of direct modulation in the transmit direction and the mass production and practical performance issues related to direct conversion in the receive direction. The time division multiplex nature of the GSM system permits integration of the transmit and receive functions together on the one RF and one IF chips. This simplifies the distribution of local oscillator signals, maximizes circuitry commonality, and reduces power consumption.

The SA1620 and SA1638 allow considerable flexibility to optimize the transceiver design for particular price/size/performance requirements, through choice of appropriate RF and IF filters. The IF may be chosen freely in the range 70–500MHz. The same IF can be used in the transmit and receive directions. Alternately, different IFs can be used if the SA1638 synthesizer frequency is switched between transmit and receive timeslots. The comparison frequency of the SA1638 PLL is high in order to provide fast switching time.

With suitable choice of the IF, an identical SA1638 IF receiver design can be used for both 900MHz GSM and 1800MHz PCN (DCS1800) equipment.

General Benefits/Advantages

- 2.7V operation. Compatible with 3V digital technology and portable applications. (Higher voltage operation also possible, if desired.)
- Excellent dynamic range. The availability of two LNAs in the SA1620 allows flexibility in receiver dynamic design for portable and mobile GSM spec. applications with appropriate filters. If for a particular application a GaAs or discrete front-end is desired, one of the LNAs can be left unpowered. Placing the AGC gain switches at the front results in some attenuation most of the time, further increasing typical dynamic performance beyond that specified by GSM.
- High power transmit output driver, delivering +7.5dBm output. This is sufficient to drive a filter and power amplifier input, without a driver amplifier. To avoid unnecessary current consumption, the output power can be reduced to an appropriate level by choice of an external resistor.
- DC offsets generated in the receive channel are independent of the AGC setting, and correctable by software to prevent erosion of signal handling dynamic range by DC offsets. Independence of DC from AGC setting is achieved by putting the gain switches in the RF front-end.
- Minimal high-quality filter requirements. As a result of the integration in the SA1638 of high quality channel selectivity filters, only sufficient filtering is needed in the receive path to provide blocking protection for the second mixers. This reduces receiver cost and size.
- Operation at a high IF allows RF image reject filter requirements to be relaxed. For example, at a 400MHz IF, the natural gain roll-off in the SA1620 LNAs and mixer suppresses the image signal in the 1800MHz band by typically 28dB below the desired 900MHz band signal.

DC Offset Correction

DC offset correction is provided by two DACs each feeding into one of the two Rx channels. The step size of both DACs is set by the value of the external resistor between DCRES and ground. With a resistor value of 120kΩ, the step size is 200mV. The actual offset of each DAC is controlled independently by 4 bits within a DC register. For each DAC 1 bit controls the polarity of the offset and the other 3 bits control the magnitude of the offset. Thus any original offset less than 1.5V magnitude in either channel can be reduced to the specified level by selecting the appropriate DAC setting via the serial interface.

Integrated Receive Filters

The low-pass characteristics of the Rx channel are determined by two low-pass responses. The first of these is the output of the quadrature mixers and the second is the low-pass filters which follow the post-mixer amplifiers. These specifications refer only to the response of the default state, but this may be switched by the control register to an alternative setting with a nominal 3dB point of 792kHz. In this alternative bandwidth setting, the performance of the circuit is not specified.

The corner frequency of the low pass filters can be adjusted over a wide range by varying the value of the external resistor between RESA and RESB. The range of feasible corner frequencies extends at least between 50kHz and 500kHz. As with the alternative bandwidth setting on the mixer outputs, the performance of the circuit is not specified when the alternative low-pass filter bandwidth is active.

Audio processor-companding, VOX and amplifier section

SA5752

DESCRIPTION

The SA5752 is a high performance low power audio signal processing system especially designed to meet the requirements for small size and low voltage operation of hand-held equipment. The SA5752 subsystem includes a low noise microphone preamplifier with adustable gain, a noise cancellation switching amplifier with adjustable threshold, a voice operated transmitter (VOX) switch, VOX control, an audio compressor with buffered input, audio expandor, and an internal bandgap voltage regulator with power down capability. When used with Philips Semiconductors' SA5753, the complete audio processing function of an AMPS or TACS cellular telephone is easily implemented. The system also meets the requirements of the proposed NAMPS or NTACS specifications. The SA5752 can also be used without the SA5753 in a wide variety of radio communications applications.

FEATURES

- Operating voltage range: 2V to 5.5V
- Miniature SSOP and SO packages
- High performance
- Adjustable VOX and noise cancellation threshold
- Adjustable gain preamplifier
- Audio companding
- ESD protected
- Open collector VOX output
- Logic inputs CMOS compatible
- Power down mode
- Few external components
- Meets AMPS/TACS/NAMPS/NTACS requirements

BENEFITS

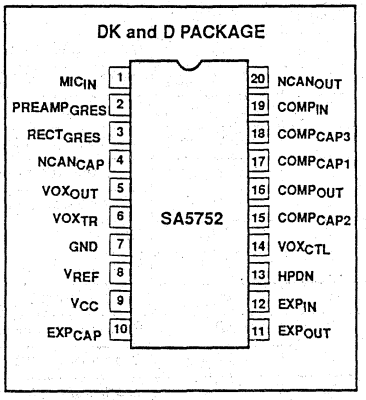
- Very compact applications
- Long battery life in portable equipment
- Complete cellular audio function with the SA5753

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION

DK and D PACKAGE



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package	-40 to +85°C	SA5752D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA5752DK	1563

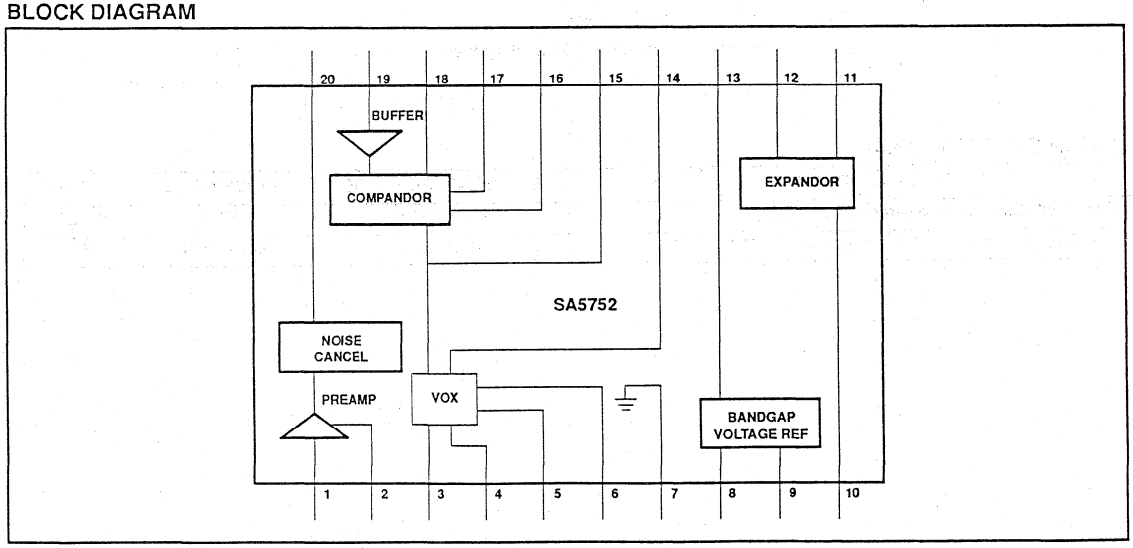
Audio processor-companding, VOX and amplifier section

SA5752

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	MIC_{IN}	Microphone input
2	$PREAMP_{GRES}$	Preamplifier gain resistor
3	$RECT_{GRES}$	Rectifier gain resistor
4	$NCAN_{CAP}$	Noise cancellation timing capacitor
5	VOX_{OUT}	Voice operated transmission output
6	VOX_{TR}	Voice operated transmission threshold resistor
7	GND	Ground
8	V_{REF}	Reference voltage
9	V_{CC}	Positive supply
10	EXP_{CAP}	Expandor timing capacitor
11	EXP_{OUT}	Expandor output
12	EXP_{IN}	Expandor input
13	HPDN	Hardware power-down
14	VOX_{CTL}	Voice operated transmission control
15	$COMP_{CAP2}$	Compressor capacitor 2 DC block
16	$COMP_{OUT}$	Compressor output
17	$COMP_{CAP1}$	Compressor timing capacitor 1
18	$COMP_{CAP3}$	Compressor capacitor 3 DC block
19	$COMP_{IN}$	Compressor input
20	$NCAN_{OUT}$	Noise cancellation output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage range	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature	-40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +3.0V, 0dB = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		2.7[4]	3.0	5.5	V
I_{CC}	Supply current	No signal Power down mode		3.1 125	4.0	mA µA
Z_L	Load impedance pins $NCAN_{OUT}$, EXP_{OUT}		50			kΩ
	$COMP_{OUT}$[1]		10			kΩ
Z_{IN}	Input impedance $COMP_{IN}$, MIC_{IN}		40	50	60	kΩ
	EXP_{IN}[2]		2.0			kΩ
	Noise cancellation current	Pin 6		25		µA
V_{OS}	DC offset $NCAN_{OUT}$[3]		-50	–3.0	50	mV

NOTES:
1. Compressor is tested in production with 50kΩ load.
2. Not tested in production.
3. Offset values are identical for both gain states of noise reduction circuit.
4. Operational down to V_{CC} = 2V.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +3.0V, 0dB level = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Preamplifier gain range Preamplifier voltage gain 0dB Preamplifier voltage gain 40dB	 Pin 2 open Pin 2 AC ground	0 -1.0 39.0	 0 40	40 1.0 41.0	dB dB dB
	Preamplifier noise density	Pin 2 AC grounded RS = 50kΩ unweighted 20Hz-20kHz		7		nV/√Hz
		weighted CCIR DIN45405 20-20kHz		8		nV/√Hz
	Switch amplifier gain		9	10	11	dB
Compandor 1kHz, all tests[1]						
$COMP_{OUT}$	Compressor error at -21dB output level	Input level = -42dB	–1.0	–0.16	1.0	dB
$COMP_{OUT}$	Compressor error at -10dB output level	Input level = -20dB	-1.0	–0.11	1.0	dB
$COMP_{OUT}$	Compressor error at 0dB output level	Input level = 0dB	-1.5	+0.1	1.5	dB
$COMP_{OUT}$	Compressor error at +5dB output level	Input level = +10dB	-1.0	+0.04	1.0	dB
$COMP_{OUT}$	Compressor error at +10dB output level	Input level = +20dB	-1.0	+0.02	1.0	dB
EXP_{OUT}	Expandor error at -42dB output level	Input level = -21dB	–1.0	–0.12	1.0	dB
EXP_{OUT}	Expandor error at -21dB output level	Input level = -10.5dB	-1.0	+0.1	1.0	dB
EXP_{OUT}	Expandor error at -10dB output level	Input level = -5dB	-1.0	+0.03	1.0	dB

AC ELECTRICAL CHARACTERISTICS (Contineud)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
EXP_{OUT}	Expandor error at 0dB output level	Input level = 0dB	-1.5	–0.2	1.5	dB
EXP_{OUT}	Expandor error at +10dB output level	Input level = +5dB	-1.0	+0.03	1.0	dB
EXP_{OUT}	Expandor error at +20dB output level[2]	Input level = +10dB	-1.0	–0.1	1.0	dB
EXP_{OUT}	Expandor V_{OS}	No signal	-50.0	+3.0	50.0	mV
EXP_{OUT}	Expandor output DC shift	No signal to 0dB	-100	+2.0	100	mV
	Timing capacitors compandor			2200		nF
THD	Total harmonic distortion					
	Compressor	1kHz, 0dB BW=300-3kHz		0.2	1	%
	Expandor	1kHz, 0dB BW=300-3kHz		0.1	1	%
	$NCAN_{OUT}$	1kHz. Pin 2 open output level = 0dB		0.02	1	%
		1kHz, Pin 2 open output level = +20dB		0.06	1	%
VOX_{OUT}	Sink current				0.5	mA
	Low level High level	Open collector I_L = 0.5mA		 V_{CC}	0.4	V V
VOX_{CTL}	Input current Low		-50	–6.6	0	µA
	High		-10	–0.02	+10	µA
	Input level Low High		0 $0.7V_{CC}$		$0.3V_{CC}$ V_{CC}	V V
H_{PDN}	Input current Low		-10	–4.1	+10	µA
	High		-10	–0.2	+10	µA
	Input level Low High		0 $0.7V_{CC}$		$0.3V_{CC}$ V_{CC}	V V
	Reference filter capacitor			10		µF

NOTE:
1. Measurements are relative to 0dB output.
2. Measurement is indicative of the output dynamic range capability.

Audio processor-companding, VOX and amplifier section

SA5752

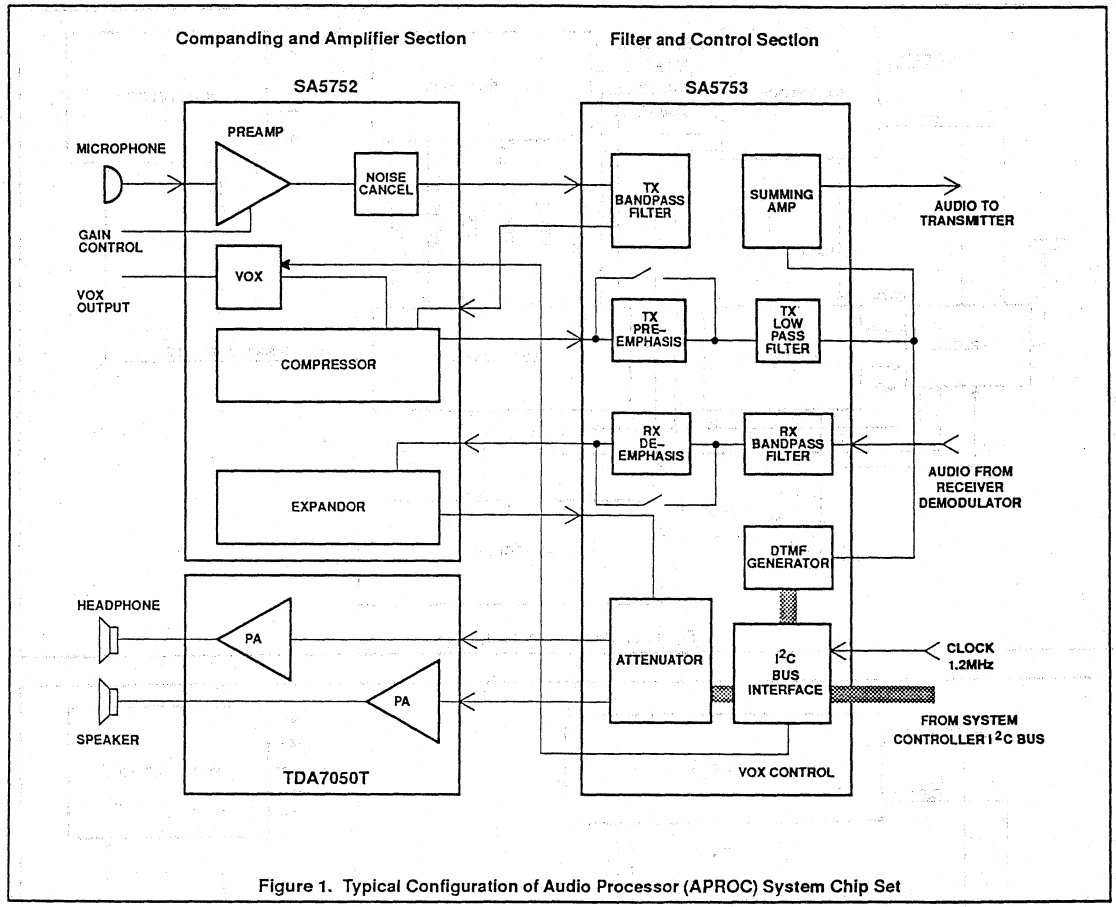


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

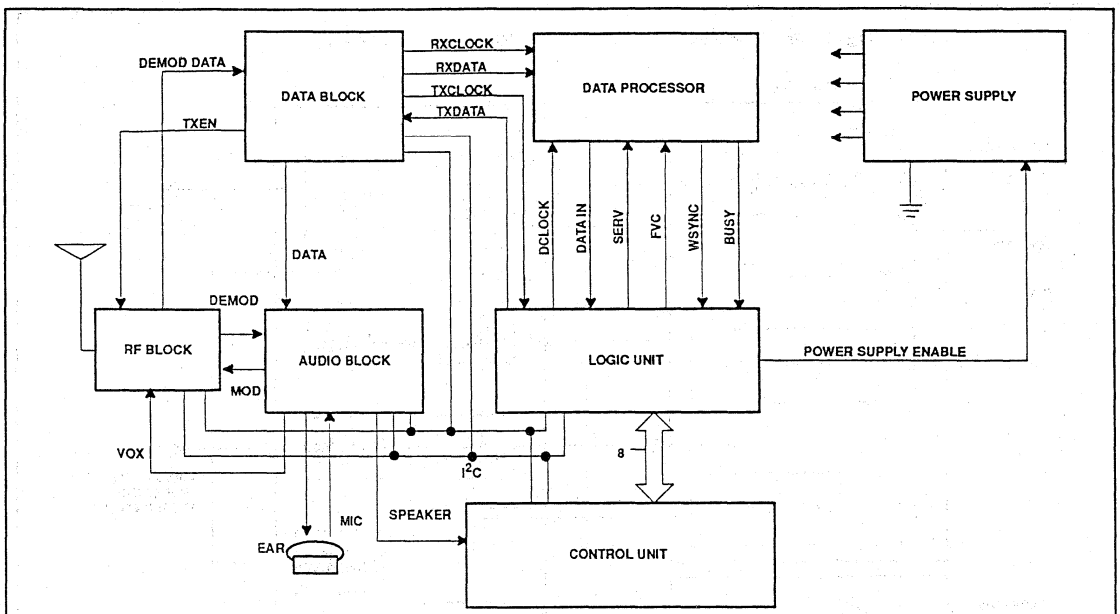


Figure 2. Cellular Radio System

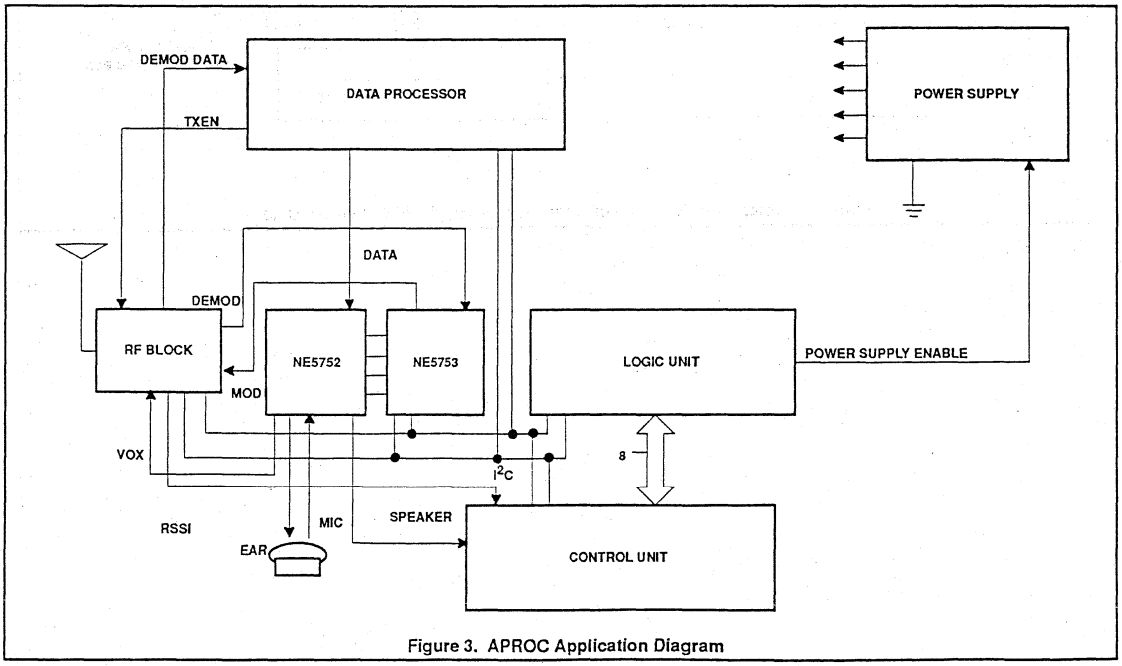


Figure 3. APROC Application Diagram

Audio processor-companding, VOX and amplifier section

SA5752

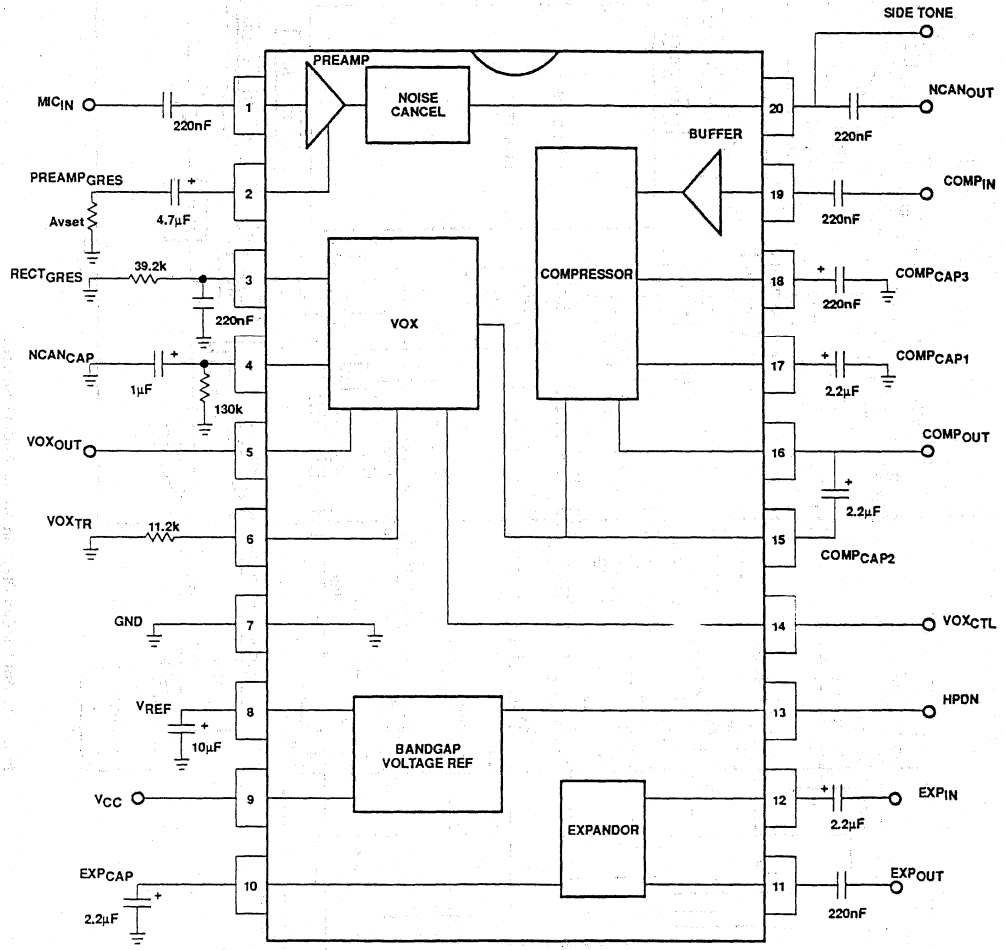


Figure 4. SA5752 Test and Application Circuit

Audio processor-companding, VOX and amplifier section

SA5752

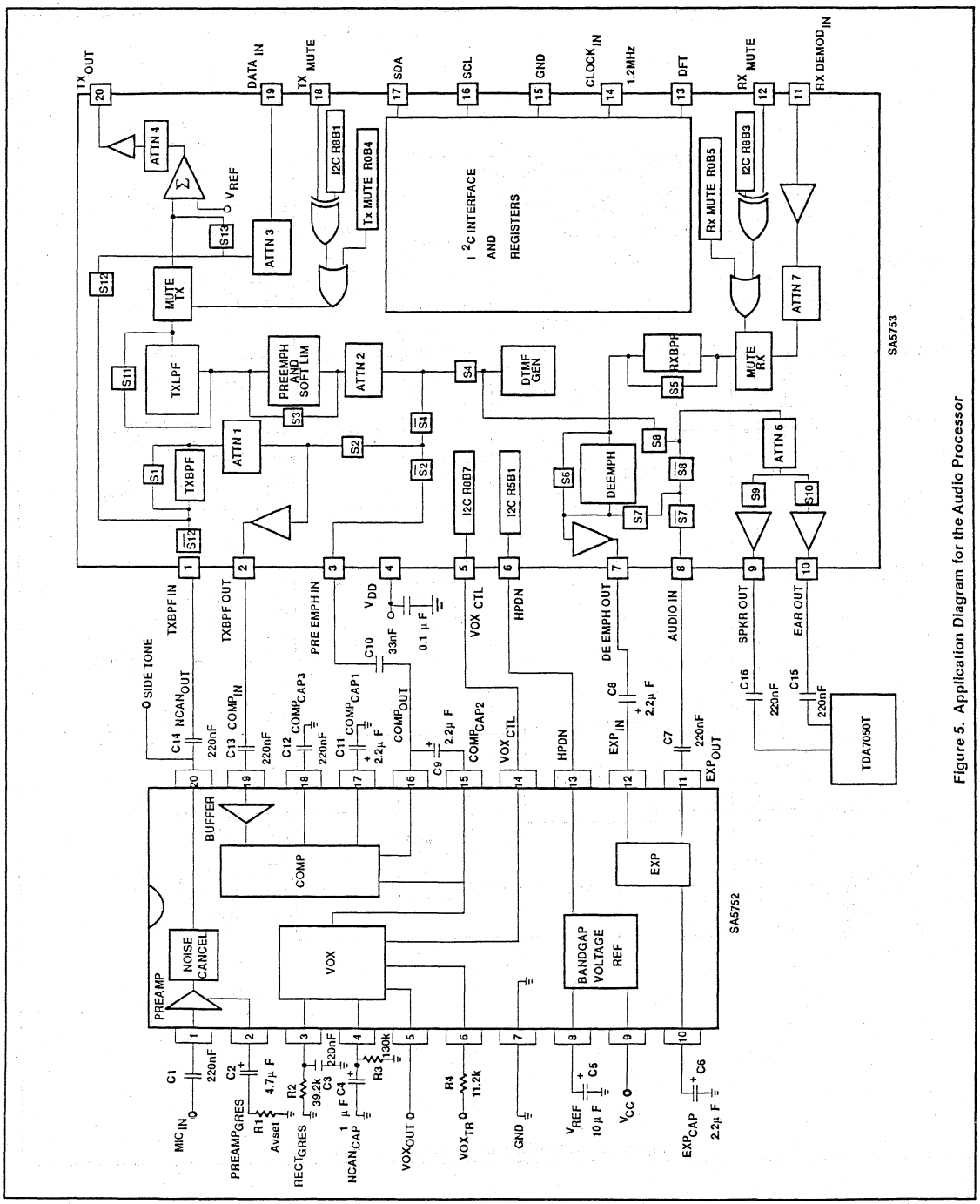
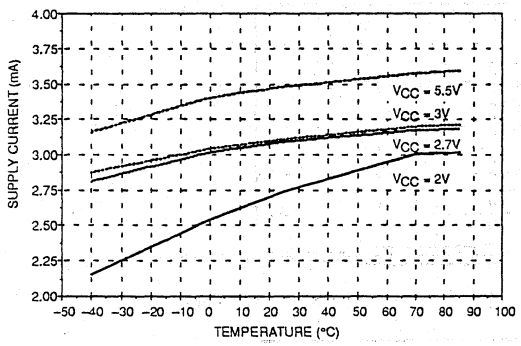


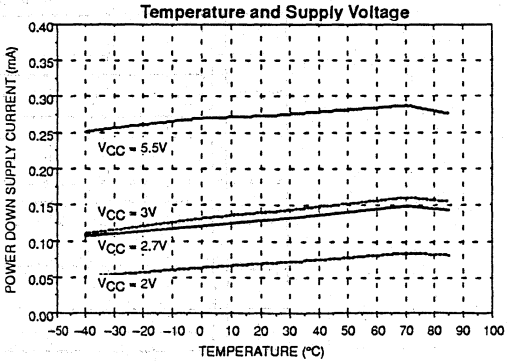
Figure 5. Application Diagram for the Audio Processor

TYPICAL PERFORMANCE CHARACTERISTICS

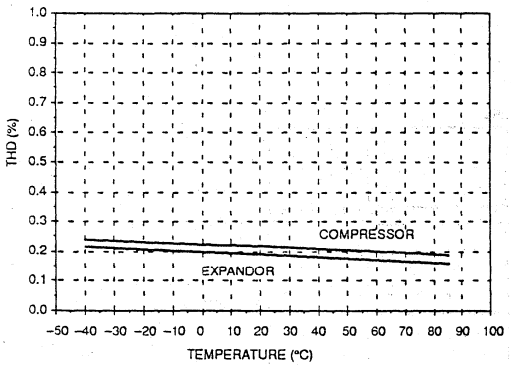
Supply Current vs Temperature and Supply Voltage



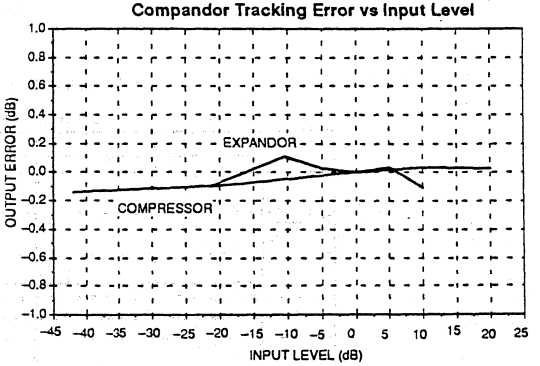
Power Down Supply Current vs Temperature and Supply Voltage



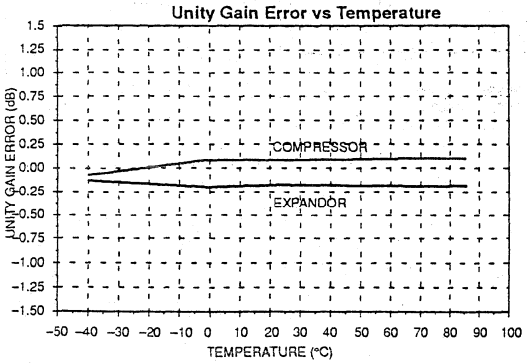
THD vs Temperature for 3V Supply



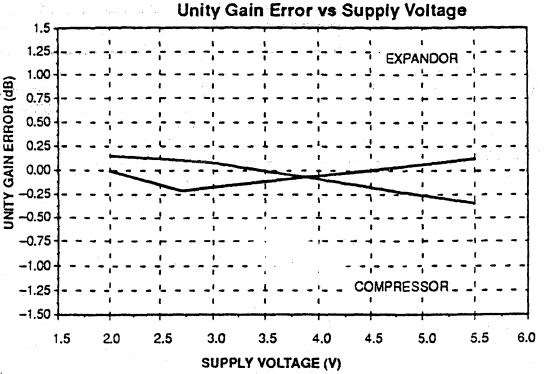
Compandor Tracking Error vs Input Level



Unity Gain Error vs Temperature

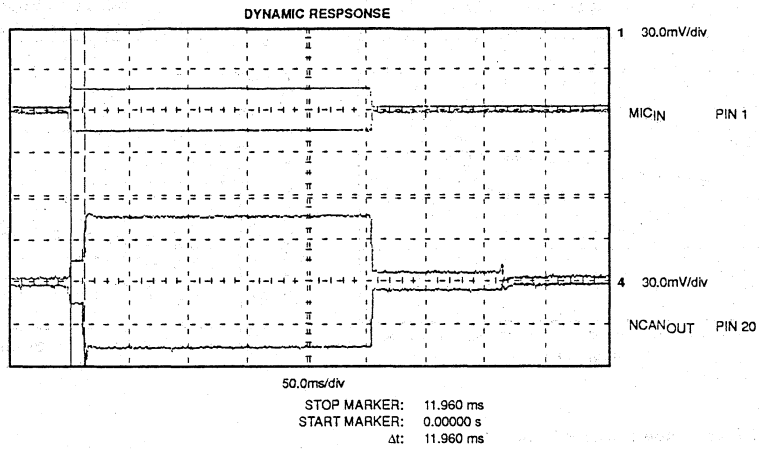


Unity Gain Error vs Supply Voltage

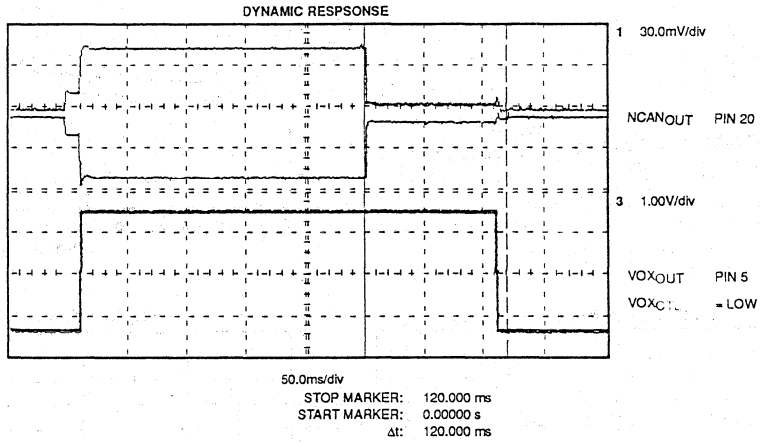


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Noise Cancellation Switching Amplifier



Voice Activated Transmitter (VOX)



Audio processor-filter and control section

SA5753

DESCRIPTION

The SA5753 is a high performance low power CMOS audio signal processing system especially designed to meet the requirements for small size and low voltage operation of hand-held equipment. The SA5753 subsystem includes complementary transmit/receive voice band (300-3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, digitally controlled attenuators for signal level and volume control, audio path mute switches, a programmable DTMF generator, power-down circuitry for low current standby, power-on reset capability, and an I^2C interface. When the SA5753 is used with an SA5752 (companding function), the complete audio processing system of an AMPS, TACS, NAMPS or NTACS cellular telephone is easily implemented.

The system also meets the requirements of the proposed NAMPS or NTACS specification, and can be used in cordless telephone applications.

The SA5753 can be operated without the I^2C bus interface by pulling DFT (Pin 13) HIGH.

FEATURES

- Low 3V supply
- Miniature SSOP package
- Low power
- High performance
- Built-in programmable DTMF generator
- Built-in digitally controlled attenuators for modulation and volume control
- Built-in peak-deviation limiter
- I^2C Bus controlled
- Power-on reset
- Power down capability
- Programmable mute control
- Meets AMPS/TACS/NAMPS/NTACS requirements

BENEFITS

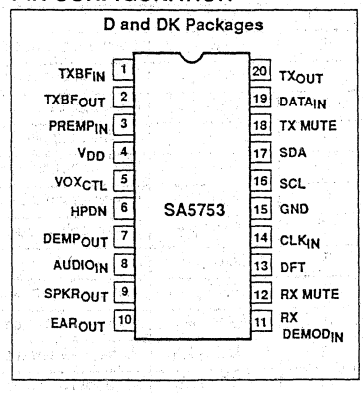
- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5752

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION

D and DK Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	-40 to +85°C	SA5753D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA5753DK	1563

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	$TXBF_{IN}$	Transmit bandpass filter input
2	$TXBF_{OUT}$	Transmit bandpass filter output
3	$PREMP_{IN}$	Pre-emphasis input
4	V_{DD}	Positive supply
5	VOX_{CTL}	Vox control output
6	HPDN	Power-down I/O
7	$DEMP_{OUT}$	De-emphasis output
8	$AUDIO_{IN}$	Audio input
9	$SPKR_{OUT}$	Audio output to speaker
10	EAR_{OUT}	Audio output to earpiece
11	RX $DEMOD_{IN}$	Rx demodulated audio signal input
12	RX MUTE	RX audio signal mute input
13	DFT	Default input, non-I^2C or stand-alone operation
14	CLK_{IN}	Clock input (1.2MHz)
15	GND	Ground
16	SCL	I^2C serial clock line
17	SDA	I^2C serial data line
18	TX MUTE	Tx audio signal mute input
19	$DATA_{IN}$	Data input
20	TX_{OUT}	Transmit output

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Power supply voltage range	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to V_{DD}+0.3	V
	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature	-40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +3.0V, unless otherwise specified. See test circuit, Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Power supply voltage		2.7	3.0	5.5[1]	V
I_{DD}	Supply current	Operating IDLE Power Down (PWDN)		2.7 600 200		mA µA µA
I_{IH}	Input current high TX MUTE, RX MUTE, HPDN DFT	$V_{IN} = V_{DD}$	 –10 0	 0 +10	 +10 +30	 µA µA
I_{IL}	Input current low TX MUTE, RX MUTE, HPDN, DFT	V_{IN} = GND	 –30 –10	 –10 0	 0 +10	 µA µA
V_{IH}	Input voltage high		$0.7V_{DD}$		V_{DD}	V
V_{IL}	Input voltage low		0		$0.3V_{DD}$	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +3.0V. See test circuit, Figure 1. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV_{RMS} = -20dBm, unless otherwise specified. All gain control blocks (Attenuators) = 0dB gain, NAMPS and VCO bits set to 0.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		100		kΩ
	RX BPF gain with de-emphasis	f = 1kHz	-0.5	0	0.5	dB
	RX BPF gain with de-emphasis	f = 100Hz		-30		dBm0
	RX BPF gain with de-emphasis	f = 300Hz	9.0	9.6	11.0	dBm0
	RX BPF gain with de-emphasis	f = 3kHz	-11.0	-10.0	-9.0	dBm0
	RX BPF gain with de-emphasis	f = 5.9kHz		-58		dBm0
	RX BPF noise with de-emphasis	300Hz-3kHz		200		μV_{RMS}
	RX dynamic range	with deemphasis		80		dB
	$DEMP_{OUT}$ output impedance	f = 1kHz			40	Ω
	$DEMP_{OUT}$ output swing (1%)	2kΩ to $V_{DD/2}$; f = 1kHz		2.4		V_{P-P}
	$SPKR_{OUT}$ ouput swing (1%)	50kΩ to$V_{DD/2}$; f = 1kHz	V_{DD} -1	2.4		V_{P-P}
	EAR_{OUT} output swing (1%)	50kΩ to $V_{DD/2}$; f = 1kHz	V_{DD} -1	2.4		V_{P-P}
	$SPKR_{OUT}$ noise / EAR_{OUT} noise			200		μV_{RMS}
	CLK_{IN} high		2.1		3.0	V
	CLK_{IN} low		0		1.0	V
	TX BPF anti alias rejection	f > 50kHz		40		dB
	TX BPF input impedance	f = 3kHz		100		KΩ
	TX BPF noise	300 - 3000kHz		200		μV_{RMS}
	TX LPF gain	f = 5.9kHz		-39	-36	dBm0
	TX LPF gain with pre-emphasis	f = 1kHz, 0dBV		2.43		dB
	TX LPF gain with pre-emphasis	f = 100Hz		-19		dBm0
	TX LPF gain with pre-emphasis	f = 300Hz		-10.45		dBm0
	TX LPF gain with pre-emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre-emphasis	f = 5900Hz		-28		dBm0
	TX LPF gain with pre-emphasis	f = 9kHz		-48		dBm0
	TX overall gain	1kHz		2.43		dB
	TX overall gain	100Hz		-58	-45	dBm0
	TX overall gain	300Hz	-11	-10.4	-9	dBm0

NOTES:
1. Tx noise performance is optimized for operation with $V_{CC} \leq 4.2V$.

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		-52	-45	dBm0
	TX BPF dynamic range			TBD		dB
	$PREMP_{IN}$ input impedance	f = 3kHz		100		kΩ
	TX_{OUT} Slew rate	C_L = 15pF		0.75		V/µs
	Output impedance	f = 3kHz			40	Ω
	Output swing (limiting)			1.2		V_{P-P}
	Output swing (1% THD)	5kΩ load (25°C)		1.0		V_{P-P}
	Tx DTMF signal with TXLPF and pre-emphasis			0.45		V/kHz
	Rx DTMF sidetone		-0.8		5.2	dBm0
	Time delay to mute from RX MUTE or TX MUTE transition	$V_{IN} = V_{IL}$ to V_{IH} $V_{IN} = V_{IH}$ to V_{IL}		0.5 0.5		µs µs

Table 1. Gain Control Blocks (Bit 0 is Least Significant Bit)

SYMBOL	Bits	TYPICAL STEP (dB)	TYPICAL GAIN (dB) MIN	TYPICAL GAIN (dB) MAX
A1	4	–0.8	–12.0	0
A2a	5	±0.25	–3.75	+3.75
A2b	2	–6, (–12 on first)	–24.0	0
A3	4	–1.0	–17.0	–2.0
A4	4	±0.5	–3.5	+3.5
A6	4	–2.0	–30.0	0
A7	4	±0.5	–3.5	+3.5
NAMPS	1		+1.9 in A2b –7.6 in A4	
VCO	1		+6.0 in A4	
For A2a, A4 and A7:		MSB sets the sign of the gain MSB = 0 for gain MSB = 1 for attenuation		
For all Gain Blocks:		All bits set to 0 = 0dB gain All bits set to 1 = maximum gain or attenuation		

FUNCTIONAL DESCRIPTION

The SA5753 is an audio signal processor designed to meet the requirements of compact low voltage radio telephone equipment. It includes transmit and receive bandpass filters for voiceband (300-3000Hz) with pre-emphasis and de-emphasis respectively, a transmit peak deviation limiter, voice channel mute switches and a data path which can be summed into the transmit channel. An I^2C interface is provided for software programmability of a DTMF generator, mute polarity, selection of different power down and operating modes and control of the gain in both the transmit and receive channels.

Software programmable gain control allows the device to be automatically optimized during equipment production and offers flexibility during normal operation.

Gain Blocks

The programmable gain blocks are shown in Table 1 and Figure 1. The purpose for each block is as follows:

a. A1 compensates for microphone gain variations in the transmit path.

b. A2a compensates for transmitter dynamic range variations due to manufacturing tolerances of the SA5753 and SA5752 compandor companion device. To meet AMPS requirements, the dynamic range between the zero crossing signal level of the compandor and the peak signal allowed by the deviation limiter is adjusted to 12.34dB.

c. A2b allows coarse attenuation to be inserted in the transmit path to eliminate positive feedback effects in hands-free speaker applications. First step is 12dB followed by two steps of 6dB.

d. A3 sets the gain between the $DATA_{IN}$ pin (Pin 19) and the TX_{OUT} pin (Pin 20) and should be adjusted after A2a and A4 have been previously optimized. The SA5753 will interface directly with the UMA1000T data processor (which produces a 2Vpk data signal). For NAMPS applications an additional 10 to 14dB resistive divider must be added at the $DATA_{IN}$ pin (Pin 19) for a 2V data signal.

e. A4 compensates for transmit gain variations due to manufacturing tolerances of the SA5753, SA5752 and VCO

connected to TX_{OUT} (Pin 20). After A2a has been adjusted to set dynamic range then A4 is used to set the peak output voltage at TX_{OUT} (Pin 20) such that a nominal 10kHz/V VCO produces a peak deviation of 12kHz to meet AMPS specifications.

f. A6 is the volume control for both the $SPKR_{OUT}$ and EAR_{OUT}.

g. A7 compensates for manufacturing tolerances in the SA5753 and preceeding demodulator. For AMPS requirements, a 1kHz tone with 2.9kHz deviation should produce an output signal at $DEMP_{OUT}$ (Pin 7) corresponding to the zero crossing signal level of the expandor.

NAMPS and VCO Offsets

For NAMPS applications, a '1' programmed into R5B3 (register 5, bit 3) will offset the transmit gain for NAMPS applications. It is recommended that A2a and A4 be programmed after the NAMPS option is set to compensate for manufacturing tolerances in the NAMPS offset, itself.

When the VCO bit of R5B2 is a '1', an extra gain of 6dB is provided at TX_{OUT} for direct interface to VCOs with a nominal gain of 5kHz/V.

Operation Using the I²C Communications Bus

The SA5753 includes on-chip gain blocks and options which can be programmed through an I²C interface bus. To use this capability, the DFT pin (Pin 13) must be pulled LOW. In this mode, all signal level adjustments can be made through software with no external potentiometers required.

With DFT pulled LOW, the HPDN pin (Pin 6) is an OUTPUT having the same value as the program bit in register 5 bit 1 (R5B1) of the control register bit map. The value at the VOX_{CTL} output (Pin 5) is the same as the program bit in R8B7. The HPDN and VOX_{CTL} outputs can be used to control the state of the SA5752 companion device.

Power On Reset and Power Down Modes

In order to avoid undefined states of the SA5753 when power is initially applied, a power-on-reset circuit is incorporated which defaults RxP and TxP such that the receive and transmit paths are muted if a 'high' voltage is applied to RX MUTE and TX MUTE (Pins 12 and 18). RX MUTE and TX MUTE include on-chip pull up resistors so, during power up, the user may apply a logic '1' to these pins or leave them floating. After power up, the registers can be programmed and the mutes removed by a quick access write to R0.

Three software controlled low power modes are provided on the SA5753. These are POWER DOWN (PWDN), IDLE and DENA and can be selected by programming a '1' into R6B2, R6B1 or R6B0 as follows. In PWDN mode (R6B2=1) both the voice and data channels are powered down with the respective I/O pins at a high impedance. In DENA mode (R6B1=1) the voice channels are powered down, but the data channel (from $DATA_{IN}$ and TX_{OUT}) is fully active. In IDLE mode (R6B1=1, R6B0=1) both voice and data channels are powered down. (See Table on page 8.)

The difference between selecting IDLE and PWDN is that the former maintains the normal operational bias voltages at all voice and data I/O pins and provides a glitch-free transfer from power down to a fully active mode and vice-versa.

Although the POWER DOWN mode exhibits lower power consumption, glitches may occur when transferring to an active mode because of the previous high impedance of the I/O pins.

The VOX_{CTL} and HPDN pins (Pins 5 and 6) still have the same value as R8B7 and R5B1 in all low power modes.

Operation Without Using the I²C Bus

The SA5753 can be operated in a default mode with the I²C bus bypassed. To use this mode, the DFT pin (Pin 13) is pulled HIGH, then the I²C bus is bypassed and the SA5753 operates as if all register bits in the I²C address map table are set to '0' except R1B2 (S13), R0B0 (S10) and R0B1 (S9), which are set to '1' to enable the receiver output. R6B2 (PWDN), which is controlled by the state of the HPDN pin (Pin 6), which is an input in DEFAULT mode.

When HPDN is pulled HIGH, the R6B2 bit is set to '0' and the SA5753 is placed in it's normal operating mode with all Gain Control Blocks set to 0dB except A3, which is set to −2dB.

When HPDN is pulled LOW, the R6B2 bit is set to '1' and the SA5753 enters POWER DOWN.

There is no on-chip pull-up or pull-down structure on the HPDN pin and so it must not be allowed to float in DEFAULT mode since the operating mode of the SA5753 will then be undetermined.

The Tx MUTE and Rx MUTE pins must be pulled LOW to enable the transmit and receive paths, respectively.

The VOXCTL pin (Pin 5) will follow the value of the control bit stored in R8B7 prior to pulling DFT HIGH.

The DTMF is disabled in the DEFAULT mode.

Programming Without the I²C Protocol

In the default mode, with DFT (Pin 13) and HPDN (Pin 6) pulled HIGH, the registers in the control register bit map are chained together so that bit 0 of a register is connected to bit 7 of the preceeding register with R0B6, R0B7, R1B6 and R1B7 bypassed, i.e., R0B5 is connected to R1B0, R1B5 is connected to R2B0, R2B7 is connected to R3B0, etc. Bits can then be loaded as a serial stream through the SDA pin of the I²C bus by the negative edge of a shifting clock applied at the SCL pin of the I²C bus. When a bit is loaded at SDA it will load first into R0B0 and then will be shifted to R8B7 after 68 clock edges.

A total of 68 clock pulses (applied at SCL) are therefore required to completely load the registers.

In this mode of operation the contents of the register map are also shifted out from the VOX_{CTL} pin since it takes the same value as R8B7. After power up there is no reset within the registers so the first 68 bits clock out at the VOX_{CTL} pin will have an indeterminate value.

Summary: To use this capability, the DFT pin and the HPDN pin must be pulled HIGH, the serial bit stream loaded through SCL synchronous with the negative clock edge applied at SCL for 68 clock pulses, and then the DFT pin pulled LOW.

Cordless Telephone Applications

For cordless telephone applications, a switch S12 is provided (R5B0) to route data through the complete transmit path while inhibiting the voice channel. In the receive path, a quick access mode is provided through the I²C to disable both EAR_{OUT} and $SPKR_{OUT}$, by setting R0B0 and R0B1, when data is detected at the $DEMP_{OUT}$ pin (Pin 7).

I²C CHARACTERISTICS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line

(SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. Data transfer may be initiated only when the bus is not busy (both lines HIGH).

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired-AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

For devices operating over a wide range of supply voltages, such as the SA5753, the following levels have been defined for a logical LOW and HIGH;

$V_{ILMAX} = 0.3V_{DD}$ (max. input LOW voltage)
$V_{IHMIN} = 0.7V_{DD}$ (min. input HIGH voltage)

Data Transfer

Data is transferred from a transmitting device to a receiving device with one data bit transferred during each clock pulse on the SCL line. The transmitter also generates the clock once arbitration has given it control of the SCL line. The data on the SDA line must remain stable during the HIGH period of the clock cycle, otherwise it may be interpreted as a control signal.

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

Acknowledgement

Following each byte of data transfered, the receiver must acknowledge successful reception. To do this the transmitter releases the SDA line (allowing it to go HIGH) at the end of each transmitted byte, and it is pulled LOW by the receiver. If this condition is maintained during the next HIGH period of the clock pulse (called the acknowledge clock pulse) then data transfer is resumed. If the receiver does not pull the SDA line LOW, the transmitter will abort the transfer.

I²C Bus Data Configurations

The SA5753 is always a slave receiver in the I²C bus configuration). The slave address consists of eight bits in the serial mode and is internally fixed.

Control Registers

The control register bit map is shown below. Either a quick access or normal address mode can be used, determined by the two MSB bits in the first word following the SA5753 address word. If the quick access mode is used, the registers R0 or R1 can be updated by sending only two bytes of information (address plus update). If R0 or R1 are updated using the address mode, then B7 and B6 of the data word are ignored. In all access modes, incremental register addressing is supported with following words updating the next register until a 'stop' bit is sent.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

High Frequency = 1200kHz/6/HD
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

Low Frequency = 1200kHz/14/LD
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading DTC = 1 in R1, bit 5.

Single tones can be obtained by loading 2 into the unused tone register to silence it.

Loading a value of 1 or 0 into the registers will default the register value to 257 or 256 for high tone or low tone, respectively.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during continuous operation (DTC=1).

I²C Address and Access

S	A7 A6 A5 A4 A3 A2 A1 A0	ACK	F7 F6 F5 F4 F3 F2 F1 F0	ACK	...	P

S = start, A0 = 0, ACK = acknowledge, P = stop, A7–0 = SA5753 address fixed internally at 1000000.
Access mode is determined by F7, F6.

All access modes support incremental addressing.

Mode	F7	F6	Action
quick access	0	0	Load F5–F0 to R0B5 – R0B0
quick access	0	1	Load F5-F0 to R1B5 – R1B0
test mode	1	0	For test only. DO NOT USE.
address mode	1	1	F3–F0 point to register

Address Map

REG	Address				Register Bits							
	F3	F2	F1	F0	B7	B6	B5	B4	B3	B2	B1	B0
R0	0	0	0	0	Y	Y	RxM	TxM	A2bb1	A2bb0	S9	S10
R1	0	0	0	1	Y	Y	DTC	S4	S8	S13	S7	S2
R2	0	0	1	0	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0
R3	0	0	1	1	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
R4	0	1	0	0	A1b3	A1b2	A1b1	A1b0	A4b3	A4b2	A4b1	A4b0
R5	0	1	0	1	A6b3	A6b2	A6b1	A6b0	NAMPS	VCO	HPDN	S12
R6	0	1	1	0	A2ab4	A2ab3	A2ab2	A2ab1	A2ab0	PWDN	IDLE 1	IDLE 0
R7	0	1	1	1	A3b3	A3b2	A3b1	A3b0	A7b3	A7b2	A7b1	A7b0
R8	1	0	0	0	VOX_{CTL}	S3	S5	S6	S11	RxP	TxP	S1

Y = ignored in address mode.
For all bits TRUE = '1'

A1b3–0 = program bits for gain block A1
A2ab4–0 = program bits for gain block A2a
A2bb1–0 = program bits for gain block A2b
A3b3–0 = program bits for gain block A3
A4b4–0 = program bits for gain block A4
A5b2–0 = program bits for gain block A5
A6b3–0 = program bits for gain block A6
A7b3–0 = program bits for gain block A7
HD7–0 = high tone DTMF
LD7–0 = low tone DTMF
NAMPS = program bit for NAMPS offset
VCO = 6dB higher TX_{OUT}
RxM = receive mute
TxM = transmit mute
RxP = receive mute polarity
TxP = transmit mute polarity
DTC = DTMF continuous
S1 = bypass TXBPF
S2 = bypass compressor in TX path, inhibit pre-emph input
S3 = bypass pre-emp and limiter in Tx path
S4 = enable DTMF to TX path and inhibit $PREMP_{IN}$ and S2.
S5 = bypass RXBPF
S6 = bypass de-emph in RX path
S7 = bypass expandor in RX path, inhibit audio input
S8 = enable DTMF to RX path and inhibit $AUDIO_{IN}$ and S7.
S9 = enable $SPKR_{OUT}$
S10 = enable EAR_{OUT}
S11 = bypass TXLPF
S12 = cordless data option established
S13 = enable data path
VOX_{CTL} = enable VOX of compandor/expander circuit. This bit appears at the VOX_{CTL} pin (Pin 5) of the SA5753.
HPDN = enable power down of compandor circuit. This bit appears at the HPDN pin (Pin 6) of the SA5753
PWDN, IDLE1, IDLE0 see Table below

Low Power Modes (R6B0 – R6B2)

PWDN	IDLE1	IDLE0	
1	X	X	(PWDN) Complete power down except I²C, I/Os high impedance.
0	1	0	(DENA) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} enabled.
0	1	1	(IDLE) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} disabled.
0	0	0	Normal operation.
0	0	1	$DATA_{IN}$ to TX_{OUT} disabled.

X = don't care.

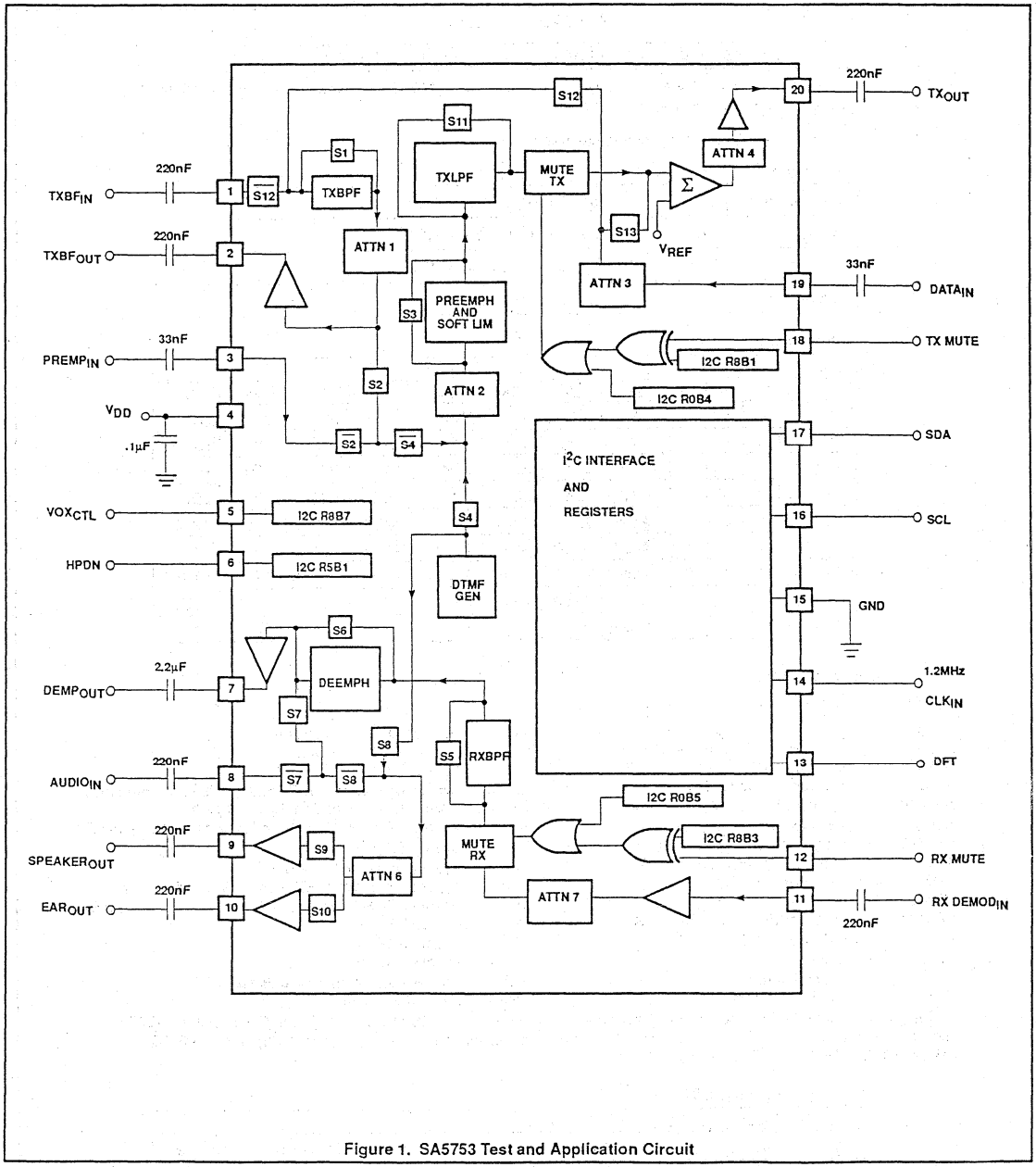


Figure 1. SA5753 Test and Application Circuit

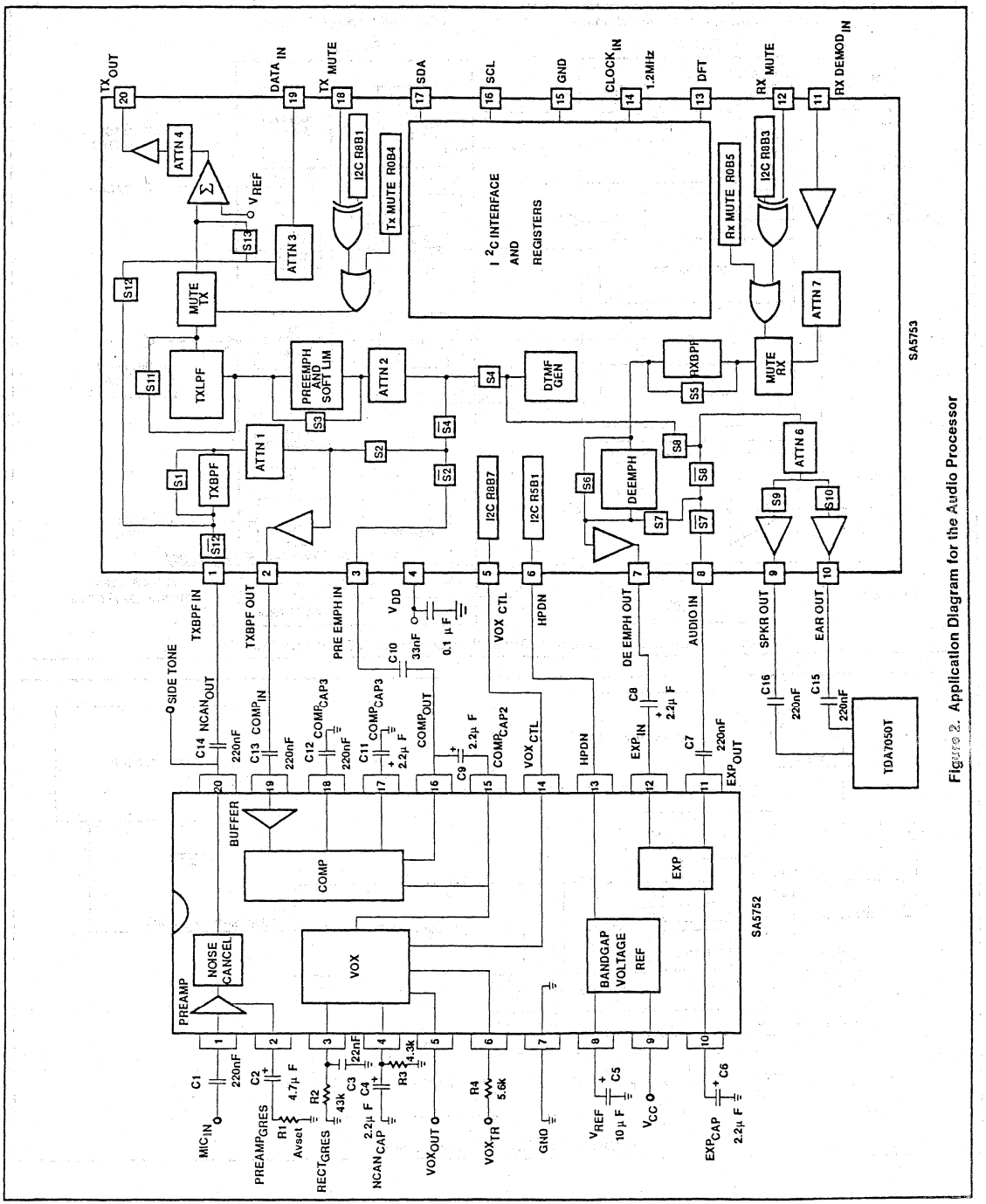


Figure 2. Application Diagram for the Audio Processor

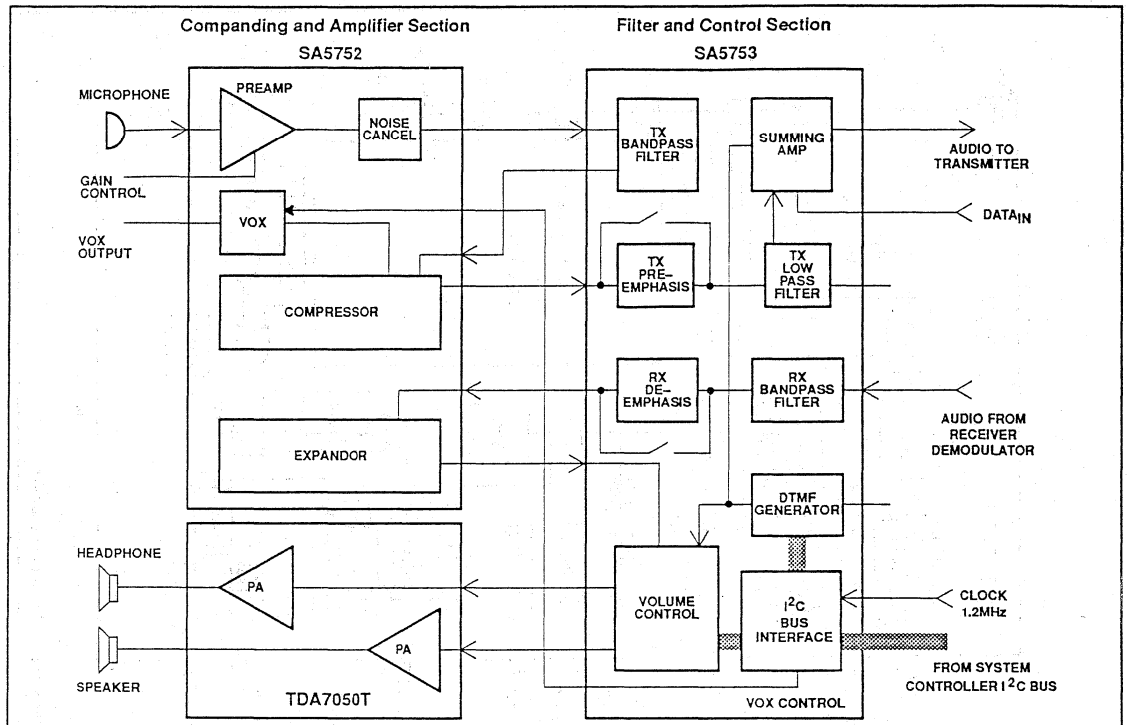


Figure 3. Typical Configuration of Audio Processor (APROC) System Chip Set

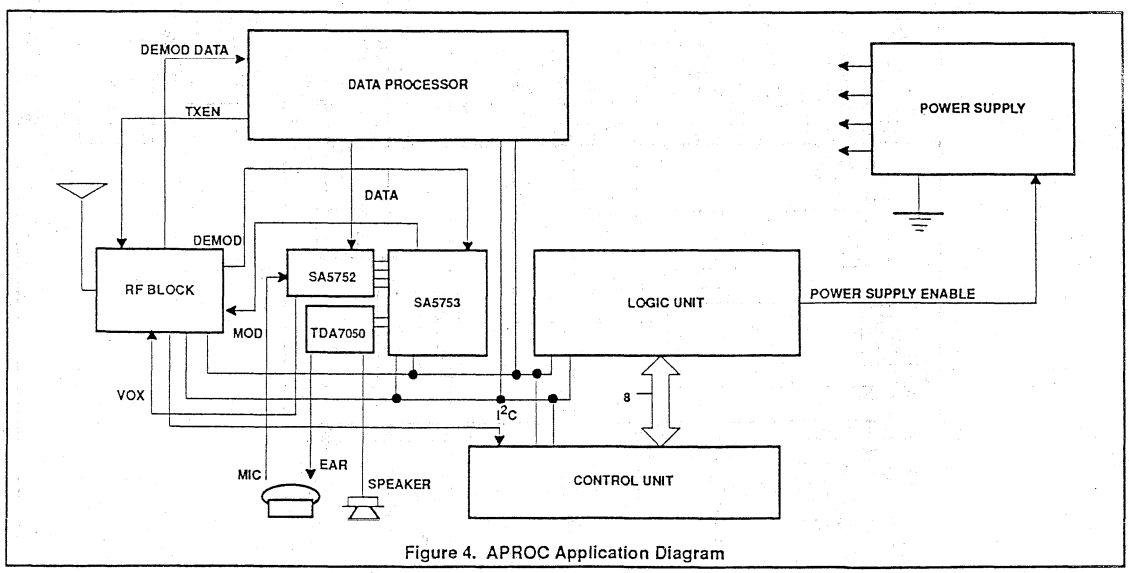
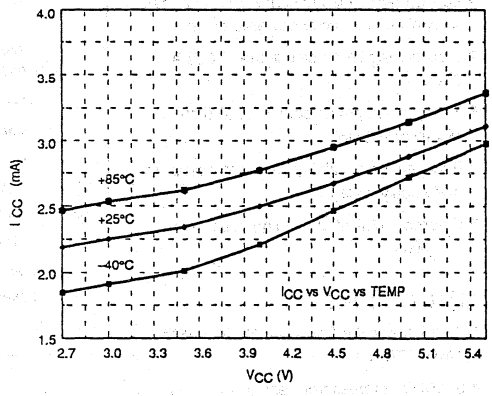
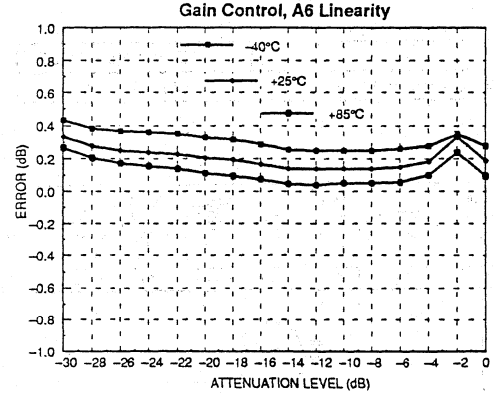


Figure 4. APROC Application Diagram

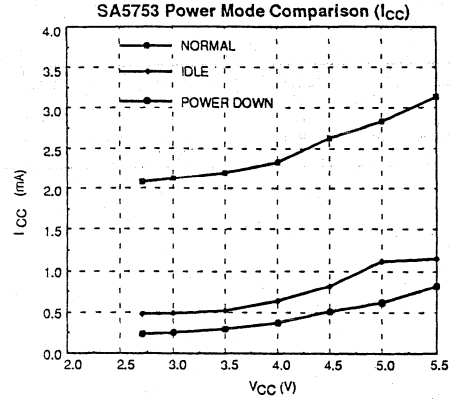
SA5753 Normal Operation



Gain Control, A6 Linearity



SA5753 Power Mode Comparison (I_{CC})



Low-voltage LNA and mixer-1GHz SA601

DESCRIPTION

The SA601 is a combined RF amplifier and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 1.6dB noise figure at 900MHz with 11.5dB gain and an IP3 intercept of -2dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has a 10dB noise figure and IP3 of –2dBm at the input at 900MHz. The nominal current drawn from a single 3V supply is 7.4mA. The Mixer can be powered down to further reduce the supply current to 4.4mA.

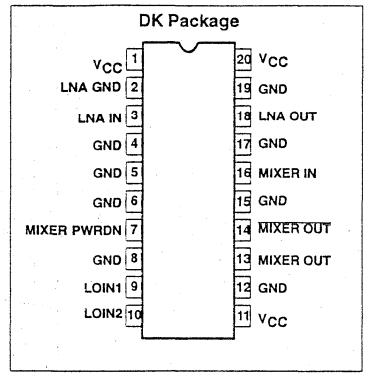
FEATURES

- Low current consumption: 7.4mA nominal, 4.4mA with the mixer powered-down
- Outstanding LNA noise figure: 1.6dB at 900MHz
- High system power gain: 17.5dB (LNA + Mixer) at 900MHz
- Excellent gain stability versus temperature and supply voltage
- External >-7dBm LO can be used to drive the mixer

APPLICATIONS

- 900MHz cellular front-end (NADC, GSM, AMPS, TACS)
- 900MHz cordless front-end (CT1, CT2)
- 900MHz receivers

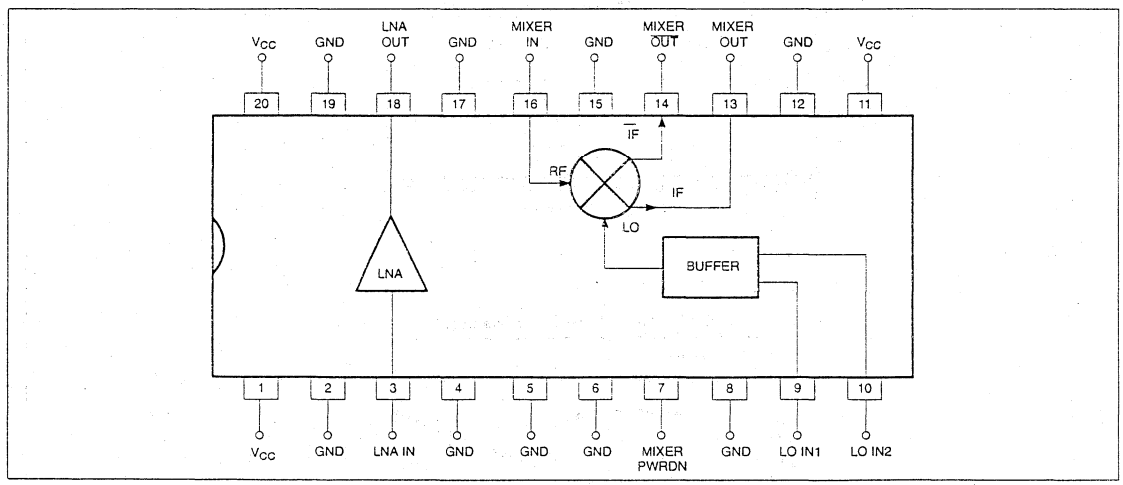
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount, SSOP)	-40 to +85°C	SA601DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[3]

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,
   θ_{JA}: 20-Pin SSOP = 110°C/W
3. Pins 9 and 10 are sensitive to electrostatic discharge (ESD).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current			7.4		mA
		Mixer power-down input low		4.4		
V_{LNA-IN}	LNA input bias voltage			0.78		V
$V_{LNA-OUT}$	LNA output bias voltage			2.1		V
V_{MX-IN}	Mixer RF input bias voltage			0.94		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; LO_{IN} = -7dBm @ 817MHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			-3σ	TYP	+3σ	
S_{21}	Amplifier gain	900MHz	10	11.5	13	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	900MHz		0.003		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz		0.01		dB/MHz
S_{12}	Amplifier reverse isolation	900MHz		-20		dB
S_{11}	Amplifier input match[1]	900MHz		-10		dB
S_{22}	Amplifier output match[1]	900MHz		-10		dB
P_{-1dB}	Amplifier input 1dB gain compression	900MHz		-16		dBm
IP3	Amplifier input third order intercept	$f_2 - f_1$ = 25kHz, 900MHz	-3.5	-2	-0.5	dBm
NF	Amplifier noise figure	900MHz	1.3	1.6	1.9	dB
VG_C	Mixer voltage conversion gain: $R_P = R_L$ = 1kΩ	f_S = 900MHz, f_{LO} = 817MHz, f_{IF} = 83MHz	17.5	19	20.5	dB
PG_C	Mixer power conversion gain: $R_P = R_L$ = 1kΩ	f_S = 900MHz, f_{LO} = 817MHz, f_{IF} = 83MHz	4.5	6	7.5	dB
S_{11M}	Mixer input match[1]	900MHz		-10		dB
NF_M	Mixer SSB noise figure	900MHz	8.5	10	11.5	dB
P_{-1dB}	Mixer input 1dB gain compression	900MHz		-13		dBm
$IP3_M$	Mixer input third order intercept	$f_2 - f_1$ = 25kHz, 900MHz	-3.5	-2	-0.5	dBm
IP_{2INT}	Mixer input second order intercept	900MHz		12		dBm
P_{RFM-IF}	Mixer RF feedthrough	900MHz		-7		dB
P_{LO-IF}	LO feedthrough to IF	900MHz		-25		dB
P_{LO-RFM}	LO to mixer input feedthrough	900MHz		-38		dB
P_{LO-RF}	LO to LNA input feedthrough	900MHz		-40		dB
$P_{LNA-RFM}$	LNA output to mixer input	900MHz		-40		dB
P_{RFM-LO}	Mixer input to LO feedthrough	900MHz		-23		dB
LO_{IN}	LO drive level	817MHz		-7		dBm

NOTE:
1. Simple L/C elements are needed to achieve specified return loss.

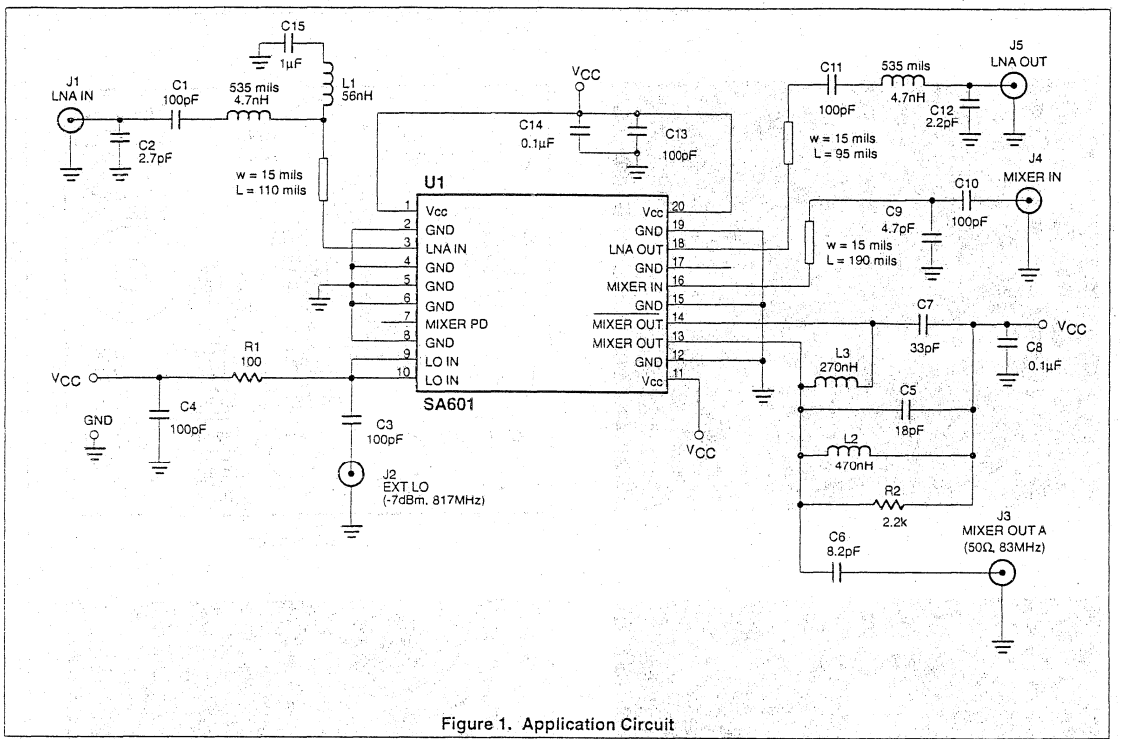


Figure 1. Application Circuit

CIRCUIT TECHNOLOGY

LNA

Impedance Match: Intrinsic return loss at the input and output ports is 7dB and 9dB, respectively. With no external matching, the associated LNA gain is ≈10dB and the noise figure is ≈1.4dB. However, the return loss can be improved at 900MHz using suggested L/C elements (Figure 1) as the LNA is unconditionally stable.

Noise Match: The LNA achieves 1.6dB noise figure at 900MHz when S_{11} = -10dB. Further improvements in S_{11} will slightly decrease the NF and increase S_{21}.

Temperature Compensation: The LNA has a built-in temperature compensation scheme to reduce the gain drift to 0.003dB/°C from –40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 3V to 5V.

LO Drive Level: Resistor R1 can be replaced by an inductor of 4.7nH and C13 should be adjusted to achieve a good return loss at the LO port. Under this condition, the mixer will operate with less than -10dBm LO drive.

IP3 Performance: C9 between Pin 16 and ground can be removed to introduce 3dB mismatch loss, while improving the IP3 to +3dBm. The associated noise figure is 11dB.

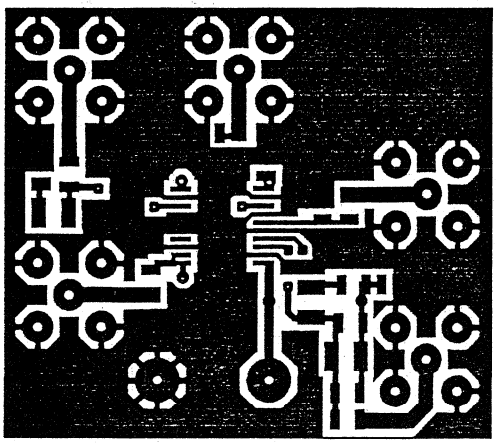
Mixer

Input Match: The mixer is configured for maximum gain and best noise figure. The user needs to supply L/C elements to achieve this performance.

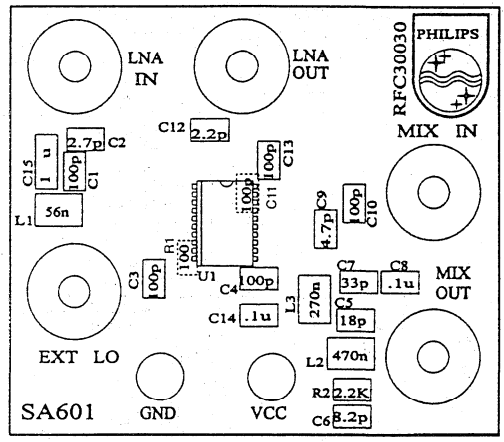
Power Down: The mixer can be disabled by connecting Pin 7 to ground. When the mixer is disabled, 3mA is saved.

Power Combining: The mixer output circuit features passive power combining (patent pending) to optimize conversion gain and noise figure performance without using extra DC current or degrading the IP3. For IF frequencies significantly different than 83MHz, the component values must be altered accordingly.

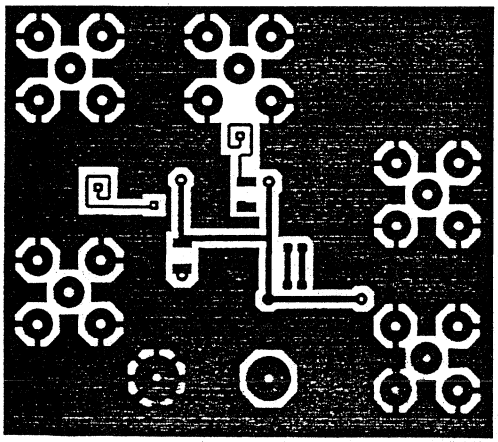
Filter Interface: For system integration where a high impedance filter of 1kΩ is to be cascaded at the mixer IF output, capacitors C5 and C6 need to be changed to 27pF and 1000pF, respectively.



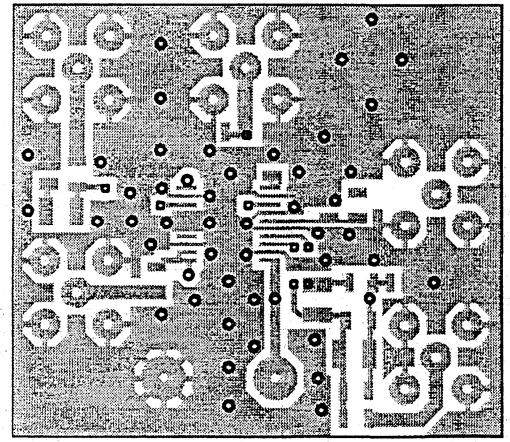
Top View



Silk Screen



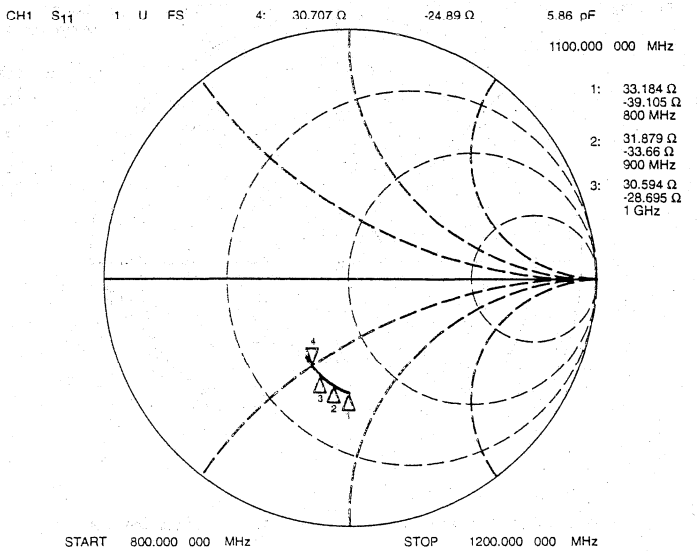
Bottom View



Via Layer

Figure 2. SA601 Demoboard Layout (Not Actual Size)

TYPICAL PERFORMANCE CHARACTERISTICS



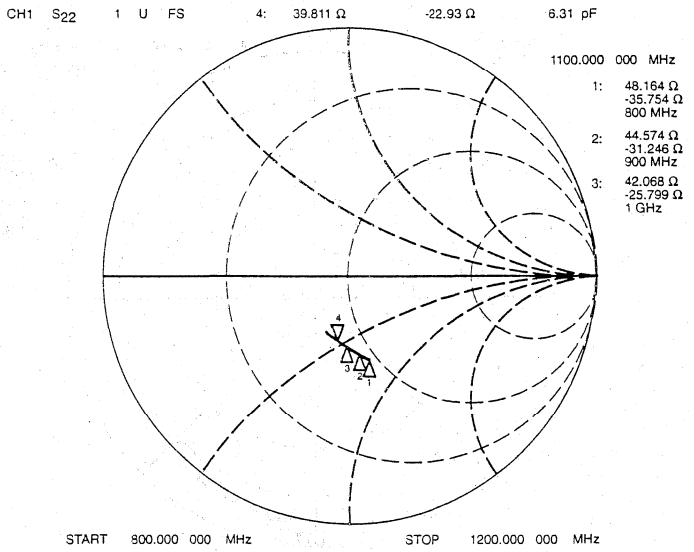


Figure 3. LNA Input and Output Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

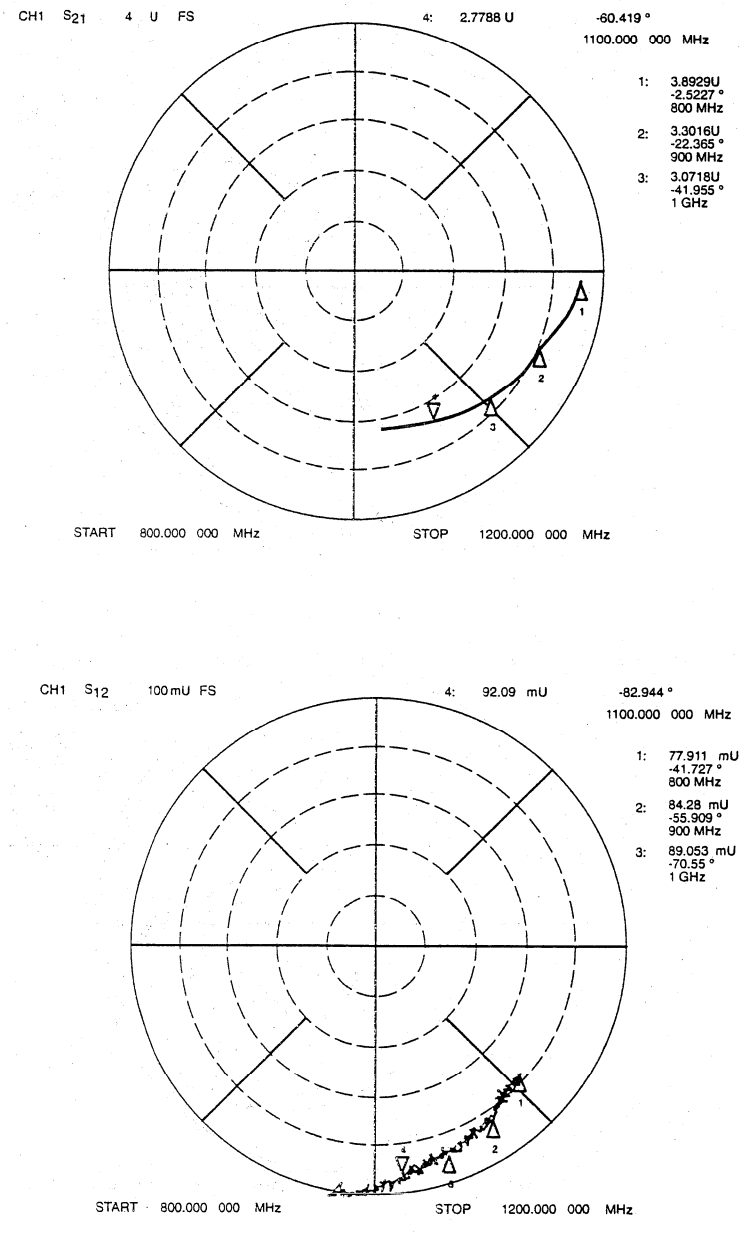


Figure 4. LNA Transmission and Isolation Characteristics (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

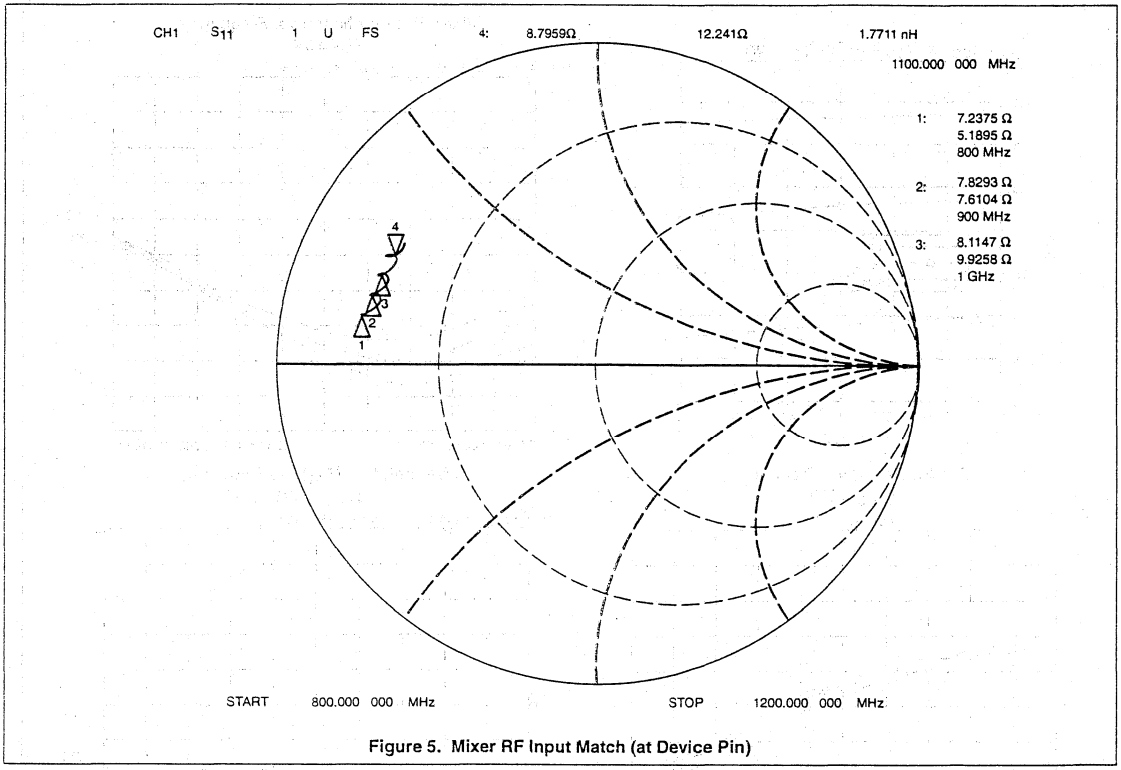
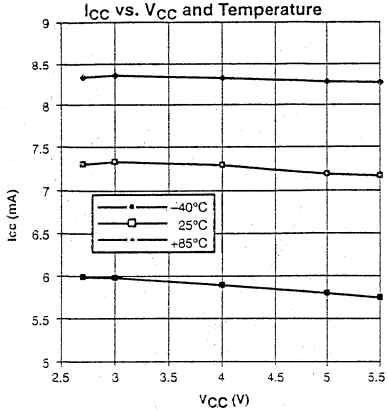


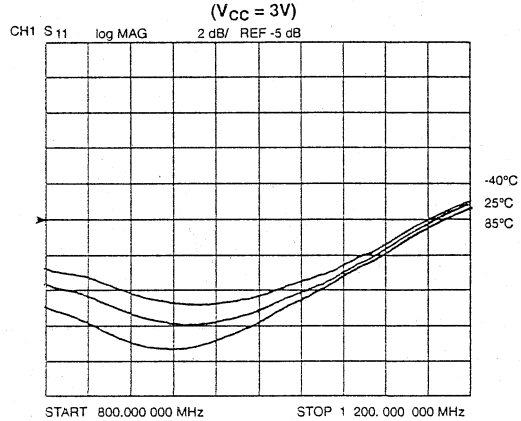
Figure 5. Mixer RF Input Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

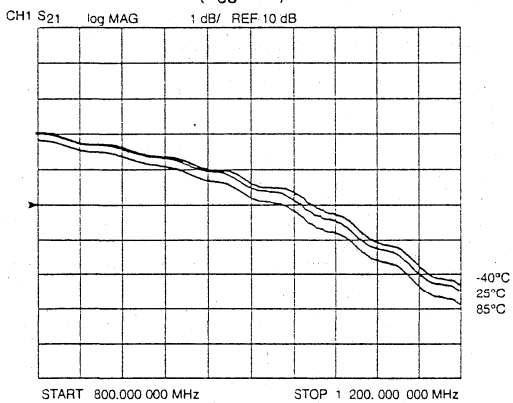
I_{CC} vs. V_{CC} and Temperature



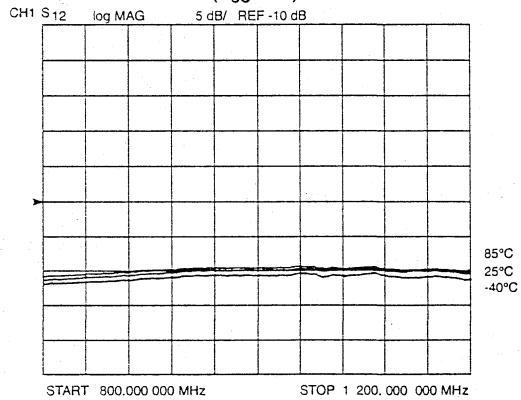
Mixer RF Input Match vs. Frequency (V_{CC} = 3V)



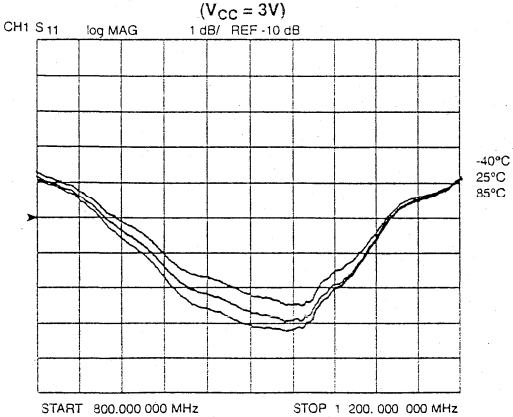
LNA Gain (S_{21}) vs. Frequency (V_{CC} = 3V)



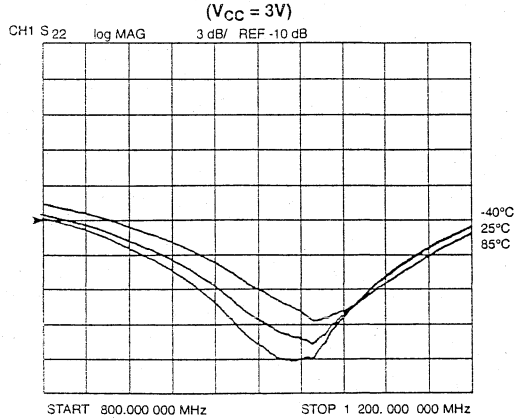
LNA Isolation (S_{12}) vs. Frequency (V_{CC} = 3V)



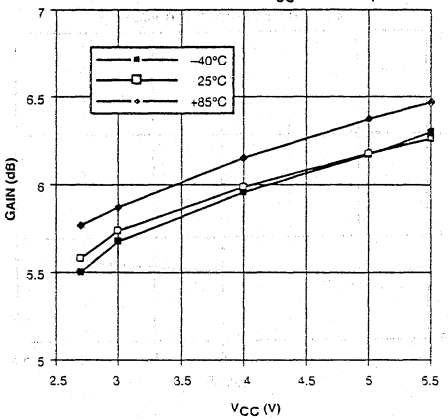
LNA Input Match (S_{11}) vs. Frequency (V_{CC} = 3V)



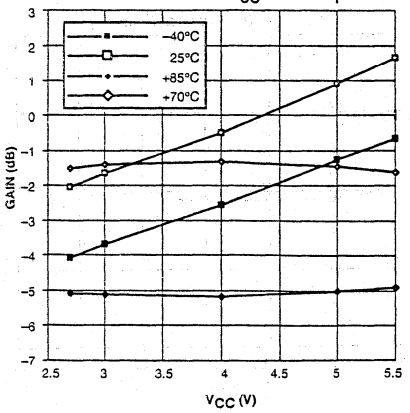
LNA Output Match (S_{22}) vs. Frequency (V_{CC} = 3V)



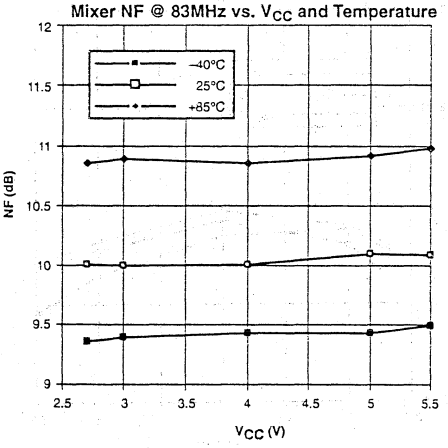
Mixer Gain @ 83MHz vs. V_{CC} and Temperature



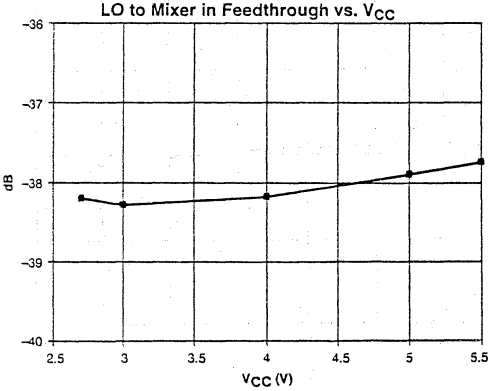
Mixer IP3 @ 83MHz vs. V_{CC} and Temperature



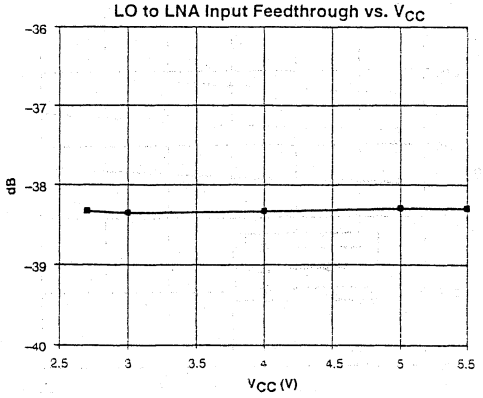
Mixer NF @ 83MHz vs. V_{CC} and Temperature



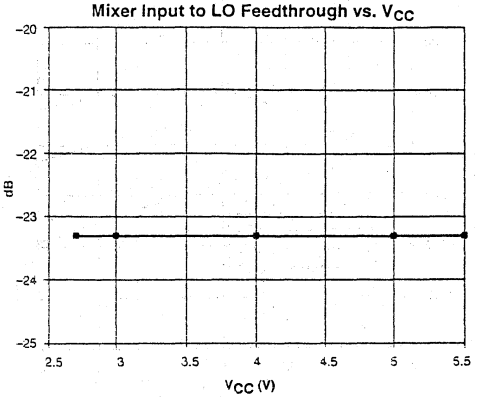
LO to Mixer in Feedthrough vs. V_{CC}

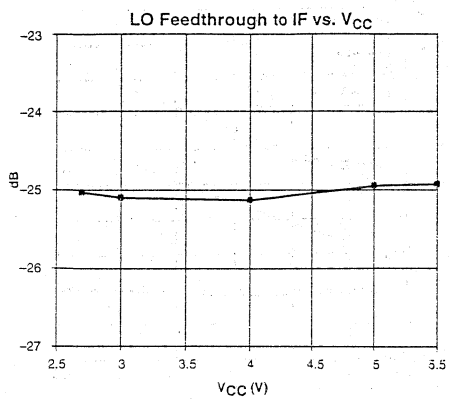


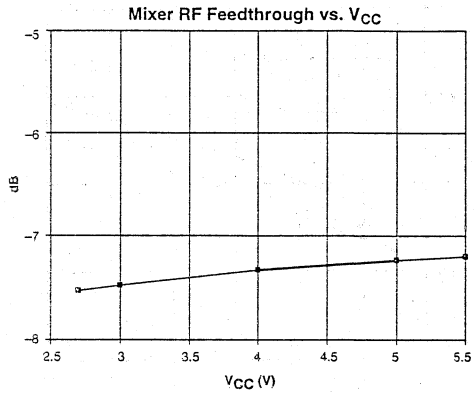
LO to LNA Input Feedthrough vs. V_{CC}

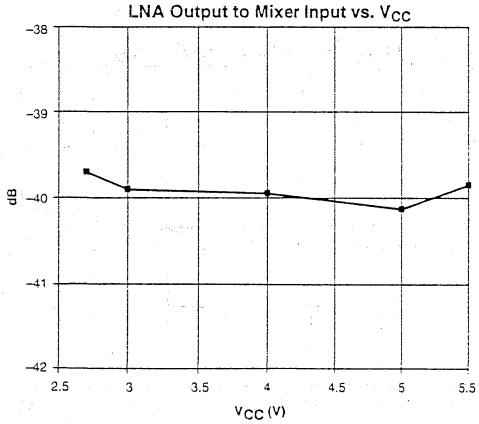


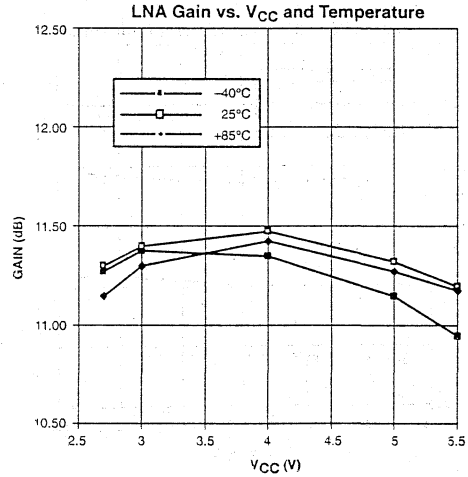
Mixer Input to LO Feedthrough vs. V_{CC}

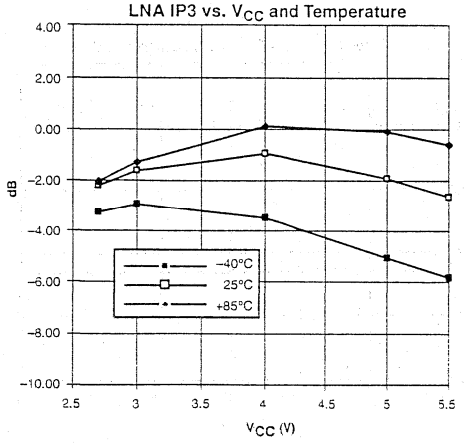


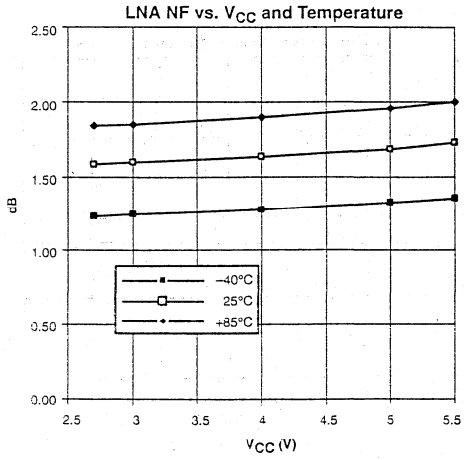

LO Feedthrough to IF vs. V_{CC}
dB
V_{CC} (V)


Mixer RF Feedthrough vs. V_{CC}
dB
V_{CC} (V)


LNA Output to Mixer Input vs. V_{CC}
dB
V_{CC} (V)


LNA Gain vs. V_{CC} and Temperature
GAIN (dB)
V_{CC} (V)
-40°C
25°C
+85°C


LNA IP3 vs. V_{CC} and Temperature
dB
V_{CC} (V)
-40°C
25°C
+85°C


LNA NF vs. V_{CC} and Temperature
dB
V_{CC} (V)
-40°C
25°C
+85°C

Low-voltage high performance mixer FM IF system

SA606

DESCRIPTION

The SA606 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA606 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

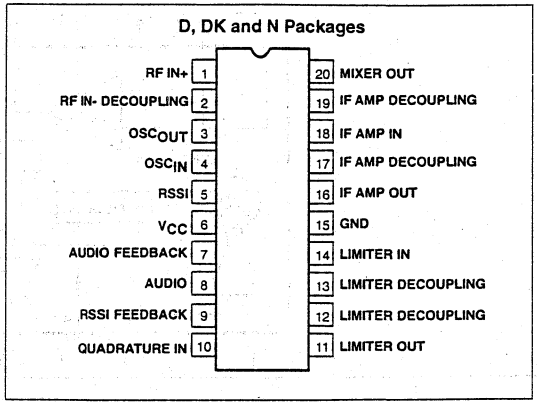
The SA606 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to level adjust the outputs or add filtering.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA606 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs

PIN CONFIGURATION

D, DK and N Packages



- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA606N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA606D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA606DK	1563

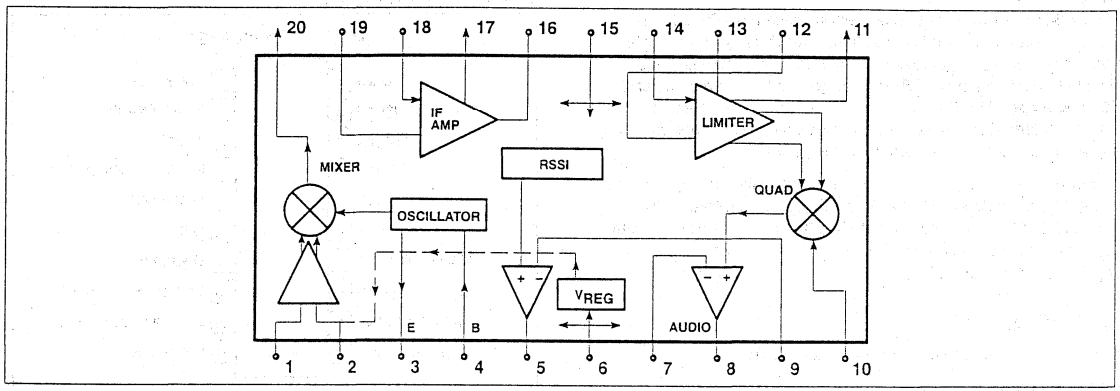
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		7	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range		-40 to +85	°C
θ_{JA}	Thermal impedance	D package DK package N package	90 117 75	°C/W

Low-voltage high performance mixer FM IF system

SA606

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third-order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = -52dBm		-9		dBm
	Conversion voltage gain	Matched 14.5dBV step-up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single-ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting -3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	IF level -110dBm		17		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
THD	Total harmonic distortion		-35	-50		dB
S/N	Signal-to-noise ratio	No modulation for noise		62		dB
	RF RSSI output, R_g = 2kΩ	RF level = -118dBm		0.3	.80	V
		RF level = -68dBm	.70	1.1	1.80	V
		RF level = -23dBm	1.20	1.8	2.50	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = -27dBm		120		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = -27dBm		2.2		V
	System SINAD sensitivity	RF level = -117dBm		12		dB

CIRCUIT DESCRIPTION

The SA606 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of -9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

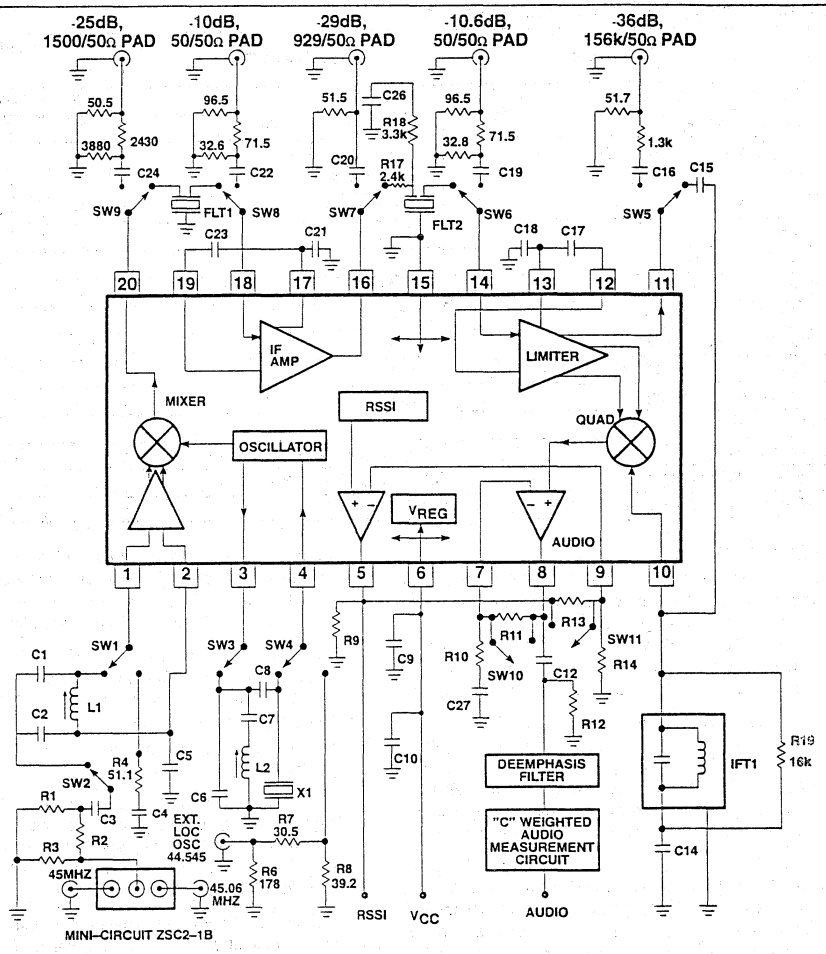
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

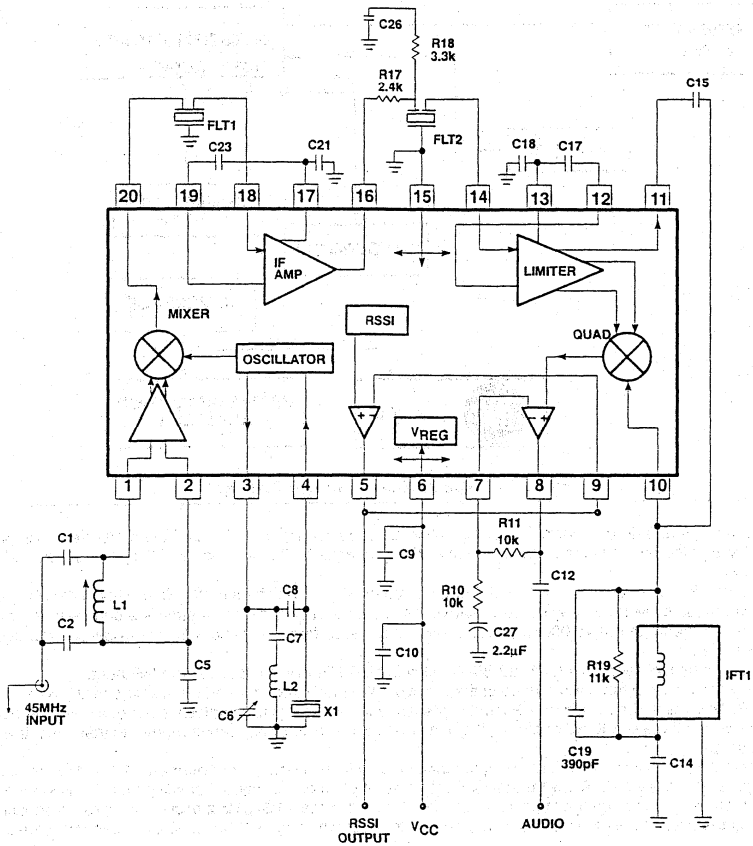


Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	2.2μF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C8	10.0pF NPO Ceramic	L2	0.8μH nominal Toko 292CNS–T1038Z
C9	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C10	10μF Tantalum (minimum) *	R9	2kΩ ±1% 1/4W Metal Film
C12	2.2μF	R10	10kΩ ±1%
C14	100nF ±10% Monolithic Ceramic	R11	10kΩ ±1%
C15	10pF NPO Ceramic	R12	2kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C23	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C25	100nF ±10% Monolithic Ceramic	R19	16kΩ
C26	100nF ±10% Monolithic Ceramic		

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA606 45MHz Test Circuit (Relays as shown)



NE606D/DK Demo Board
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

* NOTE: This value can be reduced when a battery is the power source.

Figure 2. SA606 45MHz Application Circuit

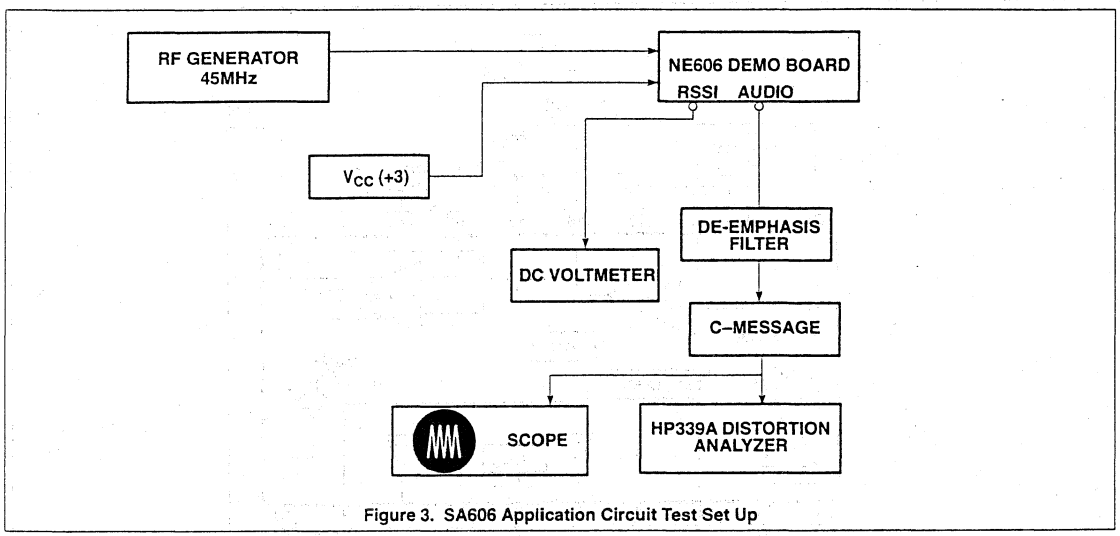


Figure 3. SA606 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or -116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 10kΩ.

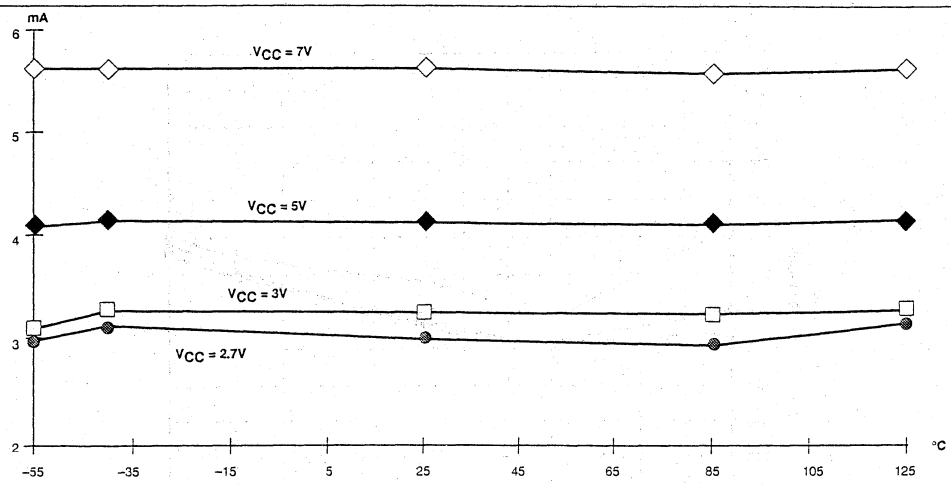


Figure 4. I_{CC} vs Temperature

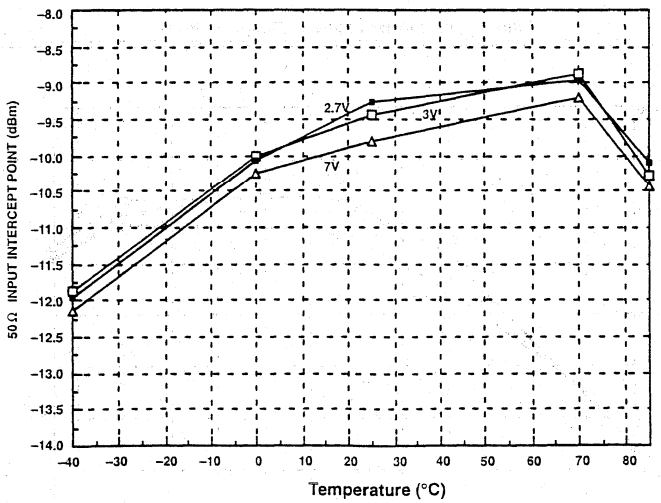


Figure 5. Third Order Intercept Point vs Supply Voltage

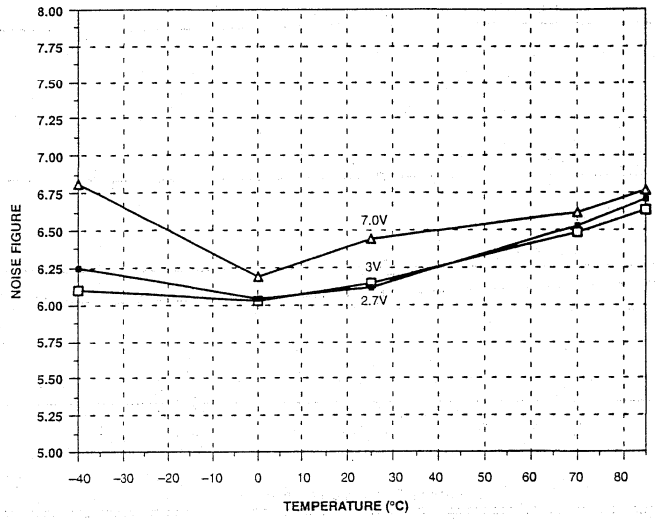


Figure 6. Mixer Noise Figure vs Supply Voltage

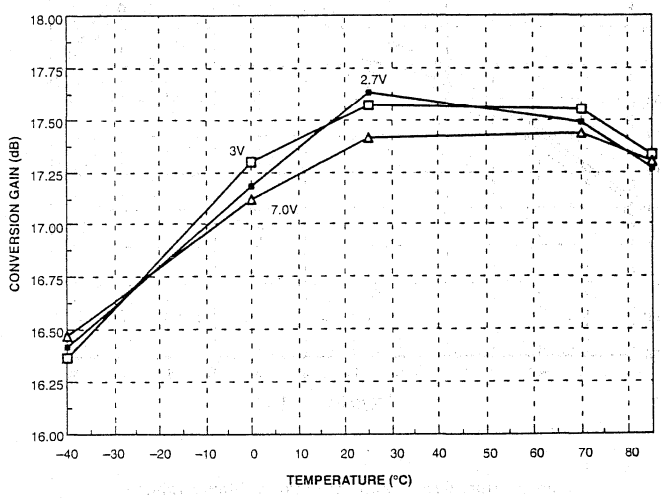


Figure 7. Conversion Gain vs Supply Voltage

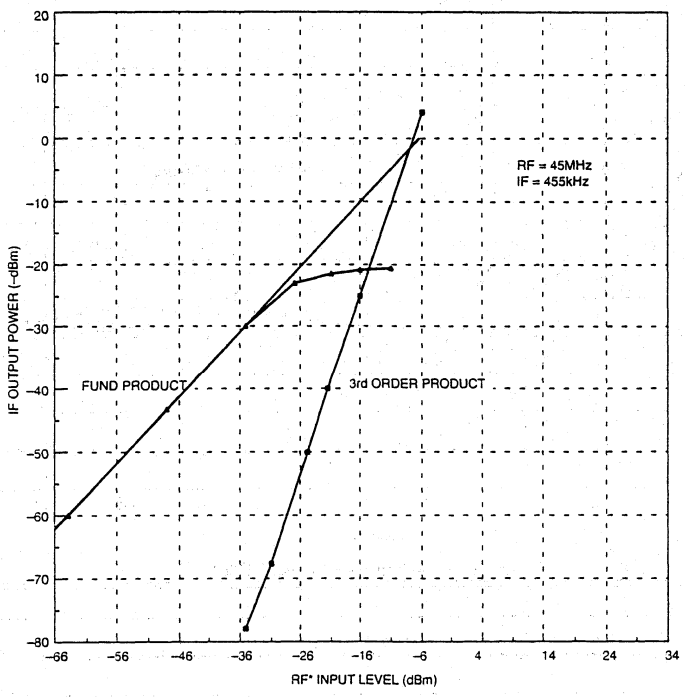


Figure 8. Mixer Third Order Intercept and Compression

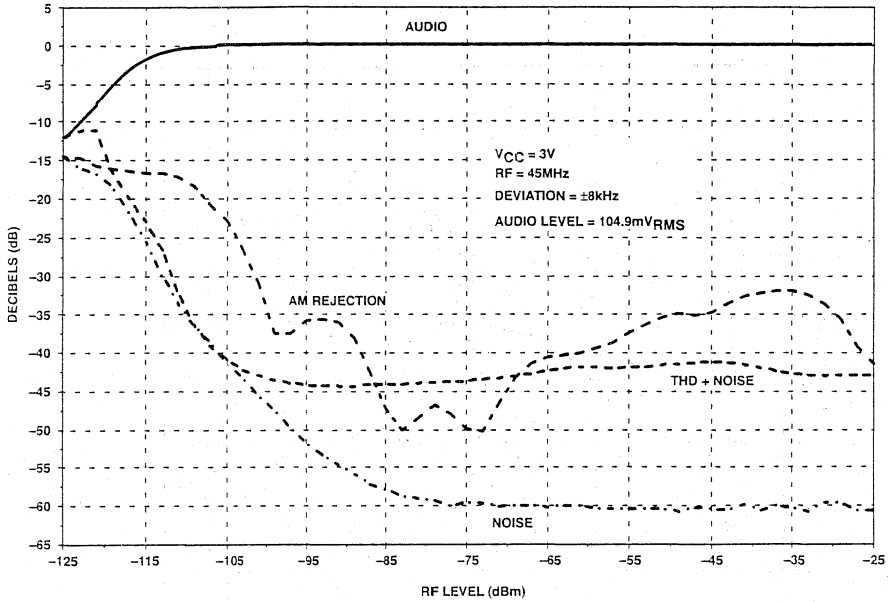


Figure 9. Sensitivity vs RF Level (-40°C)

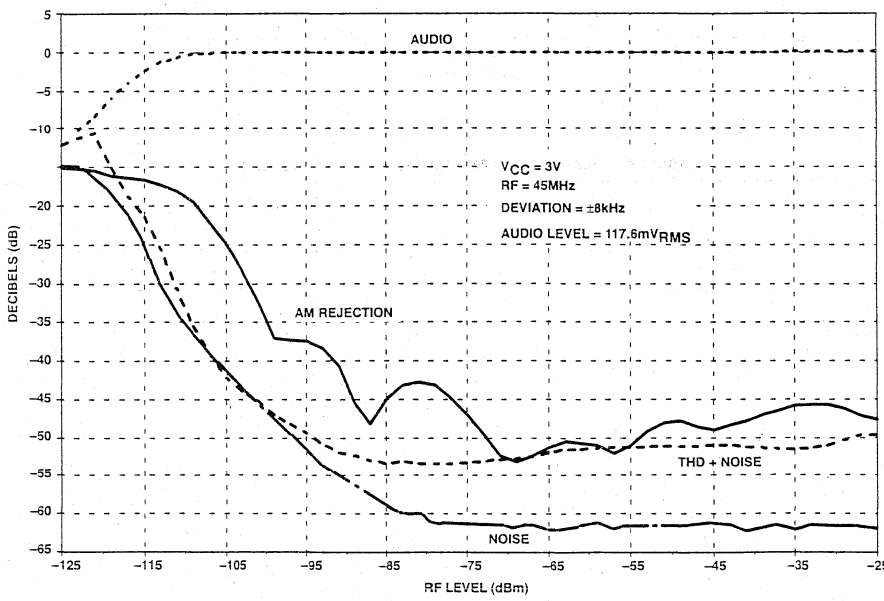


Figure 10. Sensitivity vs RF Level (+25°C)

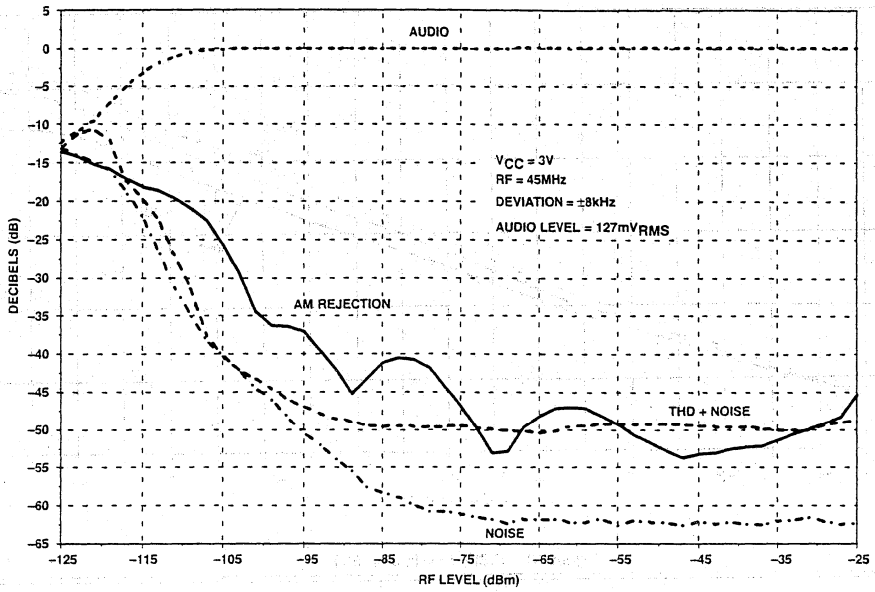


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

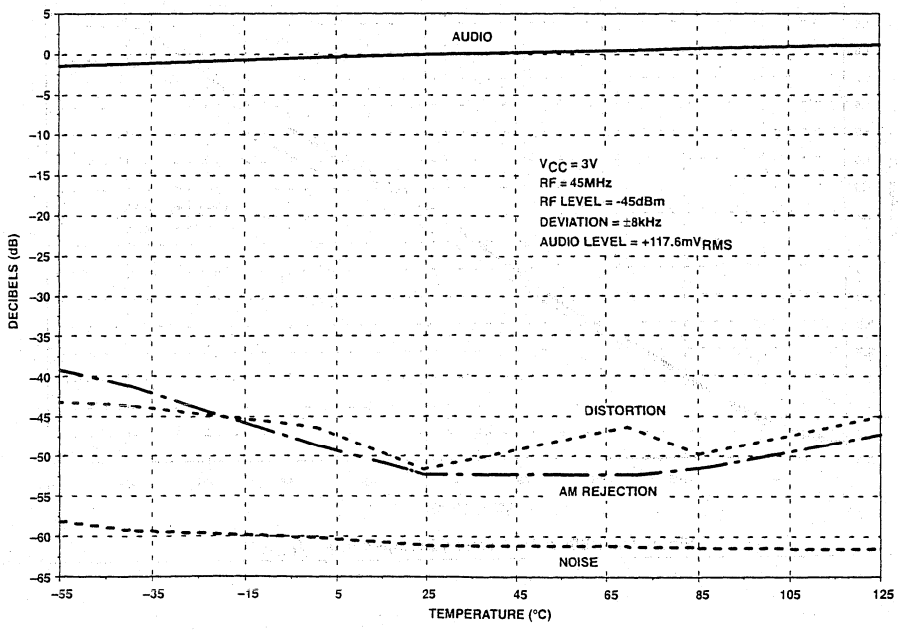


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

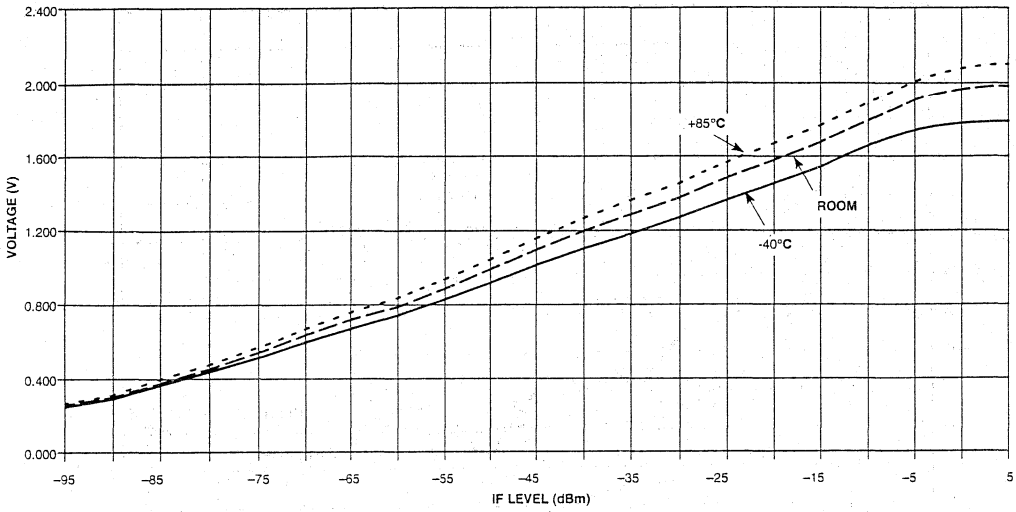


Figure 13. RSSI (455kHz IF @ 3V)

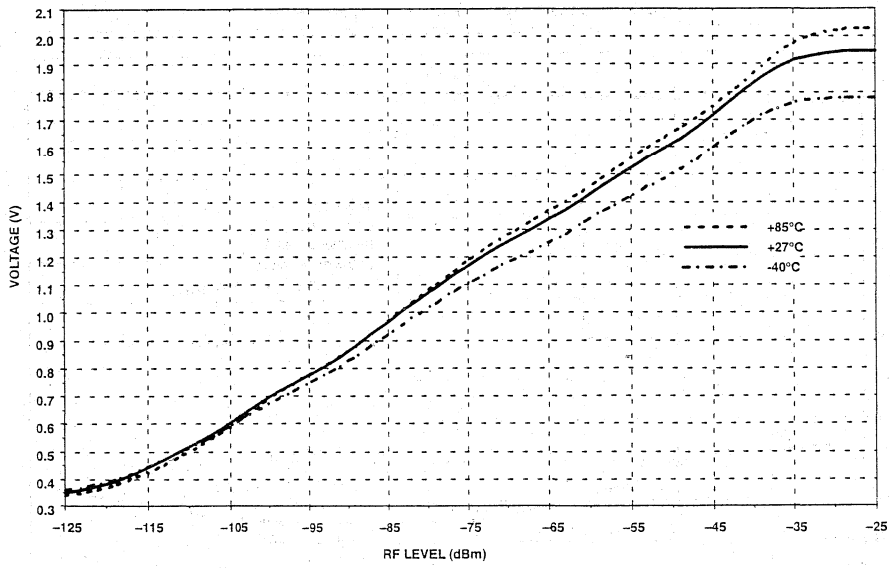


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

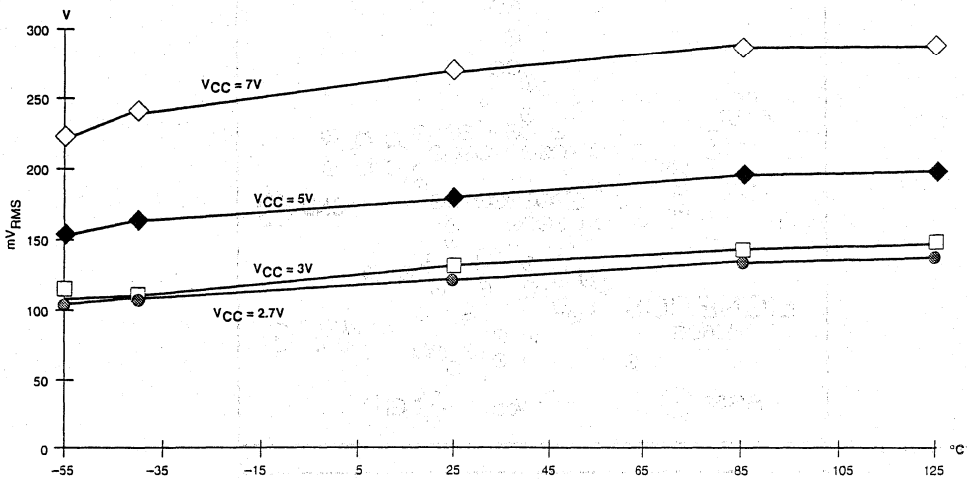
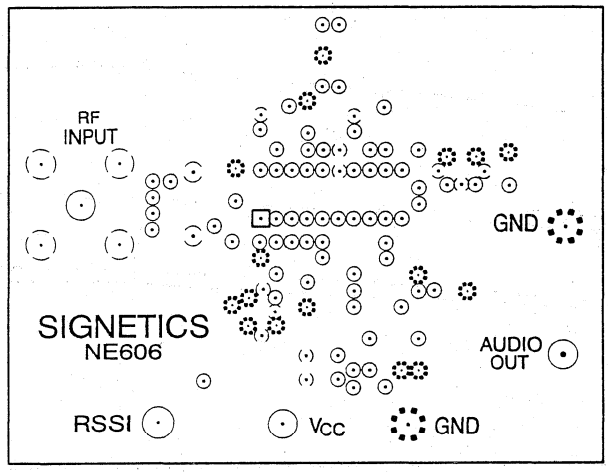


Figure 15. Audio Output vs Temperature



*Applies to Stand-Alone data sheets only.

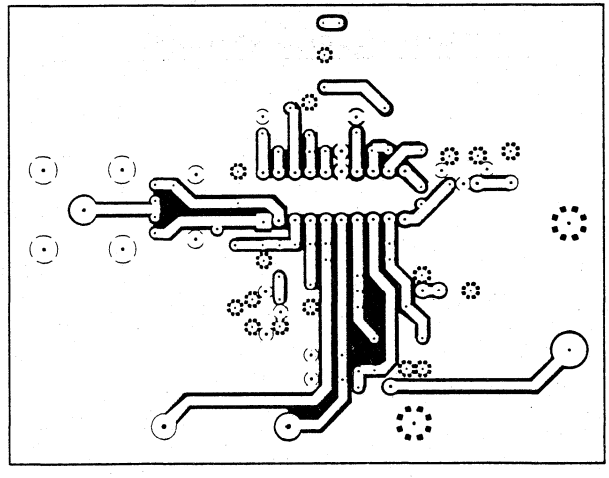
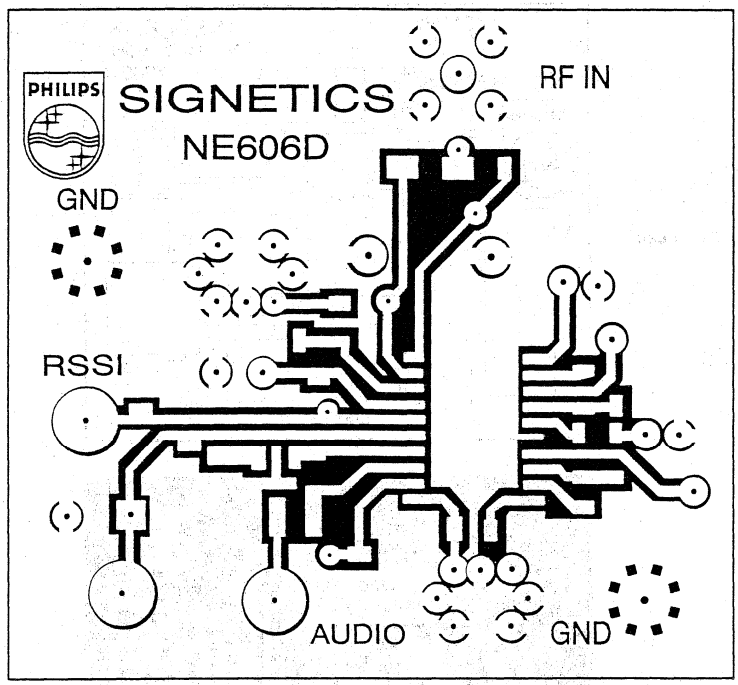


Figure 16. SA606N DIP Product Board Layout (Actual Size* — For Reference Use Only)



*Applies to Stand-Alone data sheets only.

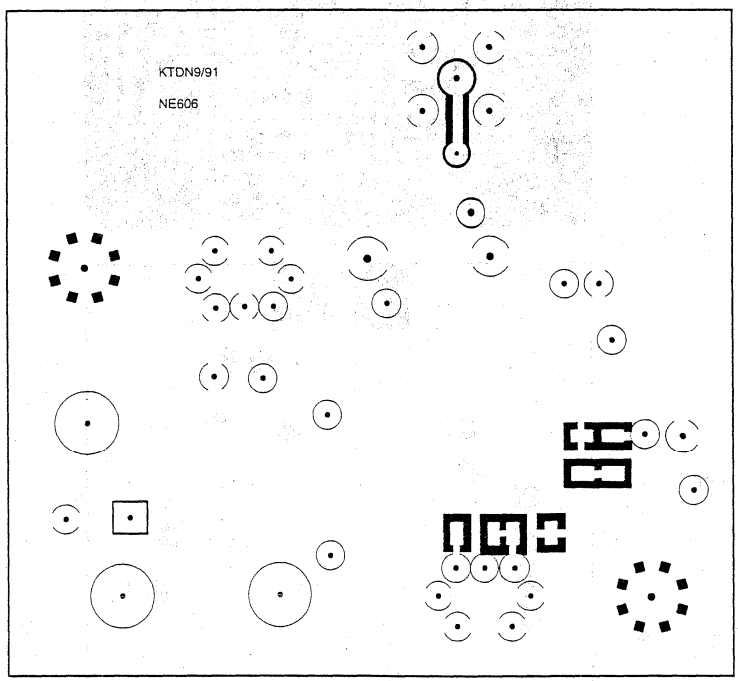
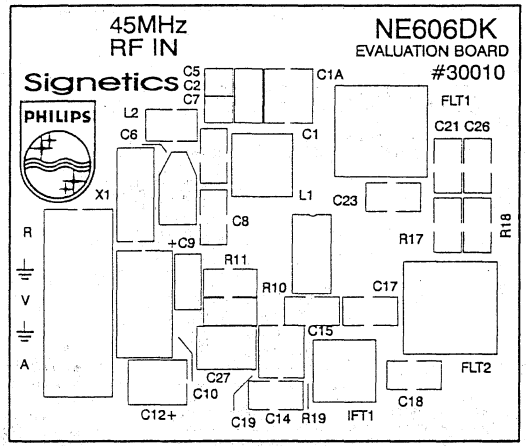
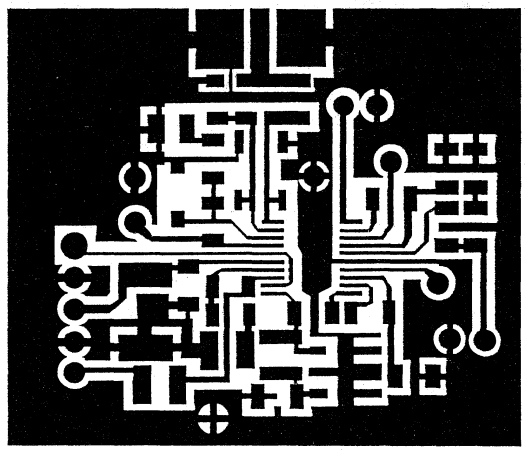


Figure 17. SA606D SOL Product Board Layout (2X Actual Size* — For Reference Use Only)

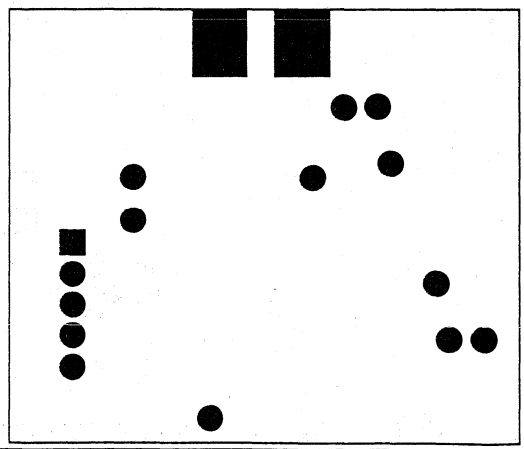
606 Silk Screen



606 TOP



606 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

Low-voltage high performance mixer FM IF system

SA607

DESCRIPTION

The SA607 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA607 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA607 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The SA607 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

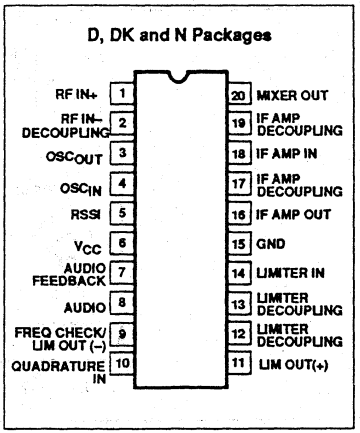
- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA607 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

PIN CONFIGURATION

D, DK and N Packages



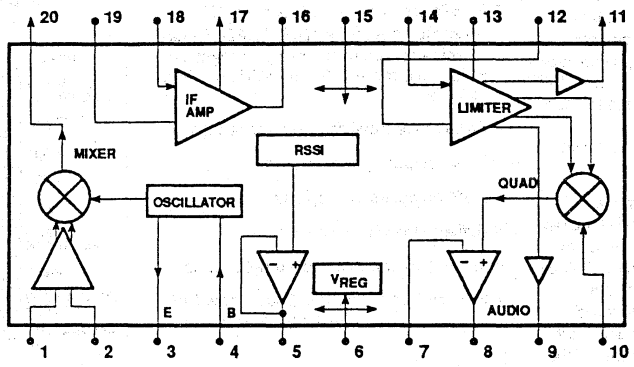
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	-40 to +85°C	SA607N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA607D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA607DK	1563

Low-voltage high performance mixer FM IF system

SA607

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA607	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA607			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA607 MIN	LIMITS SA607 TYP	LIMITS SA607 MAX	UNITS
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) No load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/limiter output impedance	(Pin 9)		200		Ω
	Frequency check/limiter output level	(Pin 9) No load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:
1. The generator source impedance is 50Ω, but the SA607 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA607 input (Pin 18) which is about 21dB less than the "available power" at the generator.

Low-voltage high performance mixer FM IF system

SA607

CIRCUIT DESCRIPTION

The SA607 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

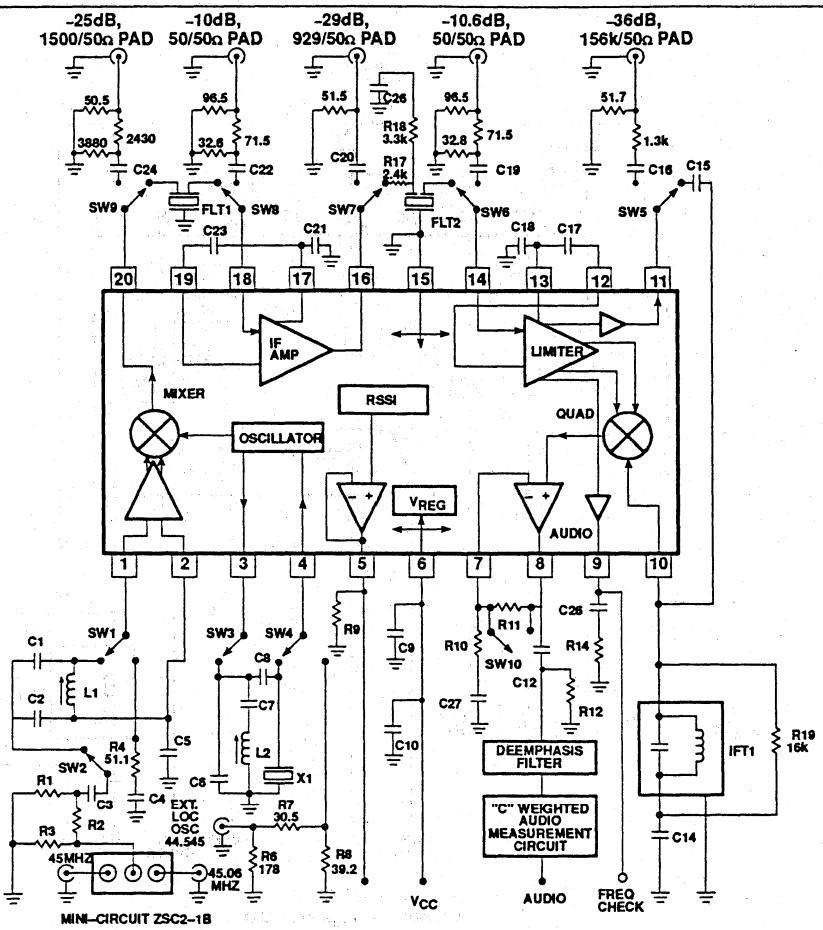
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter output or Frequency Check output has drive capability of a load minimum of 2kΩ or higher to obtain 115mV output level.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

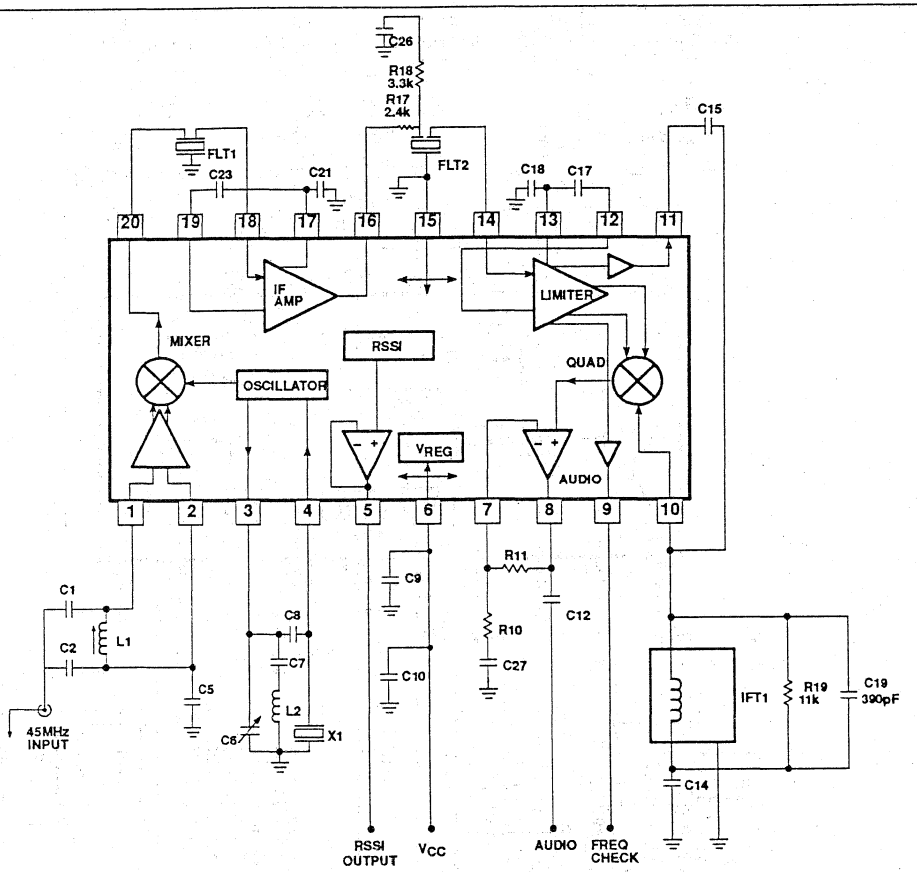


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1µF ±10% Monolithic Ceramic
C27	2.2µF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147–160nH Coilcraft UNI-10/142-04J08S
L2	0.8µH nominal Toko 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R12	2kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA607 45MHz Test Circuit (Relays as shown)



SA607D/DK
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH Coilcraft 1008C S-122
X1	44.545MHz Crystal Hy-Q
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. SA607 45MHz Application Circuit

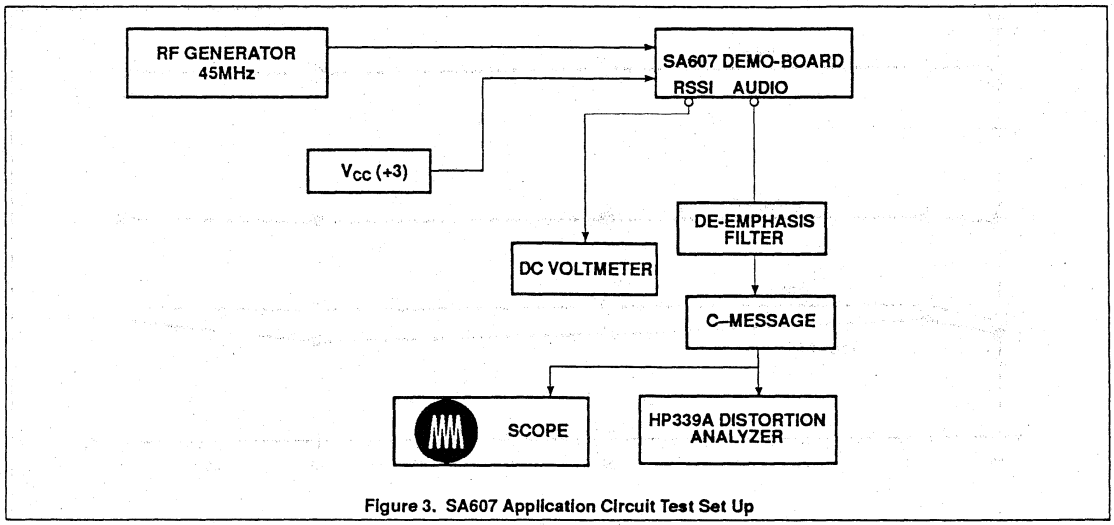


Figure 3. SA607 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

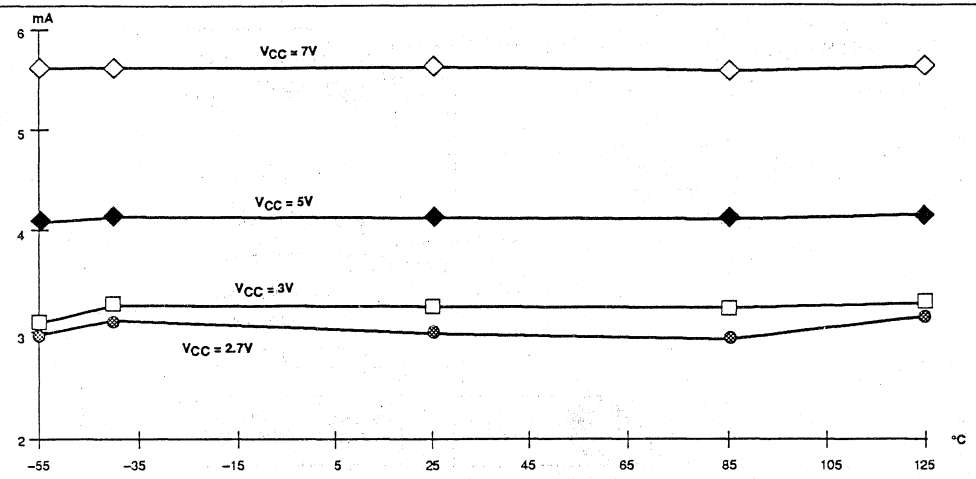


Figure 4. I_{CC} vs Temperature

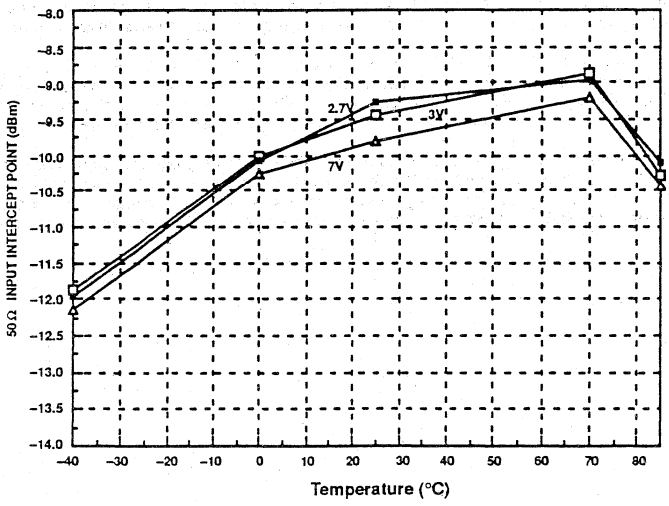


Figure 5. Third Order Intercept Point vs Supply Voltage

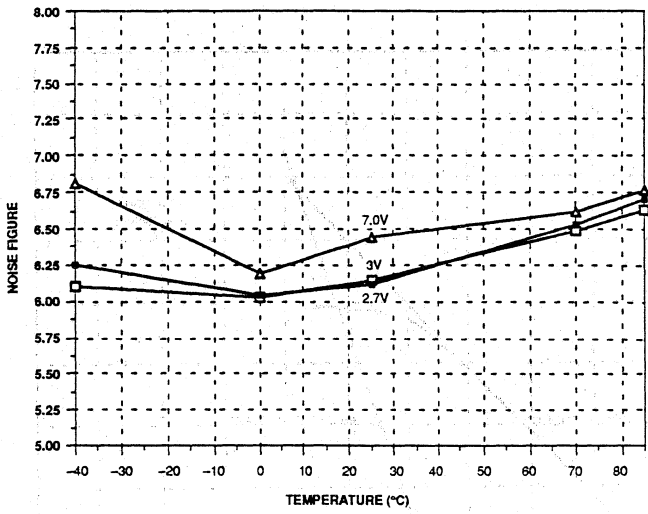


Figure 6. Mixer Noise Figure vs Supply Voltage

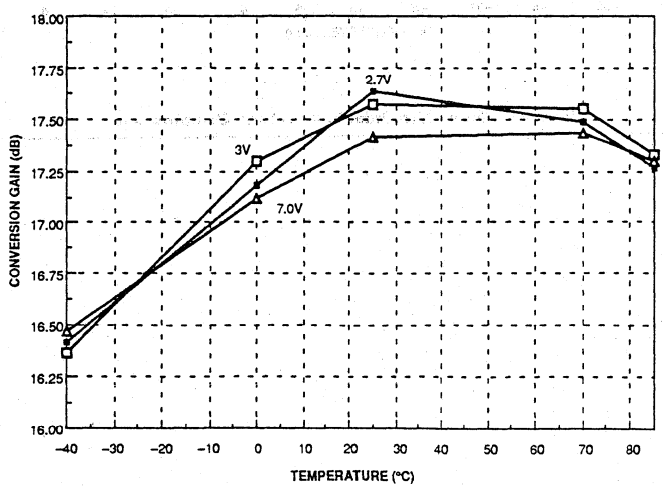


Figure 7. Conversion Gain vs Supply Voltage

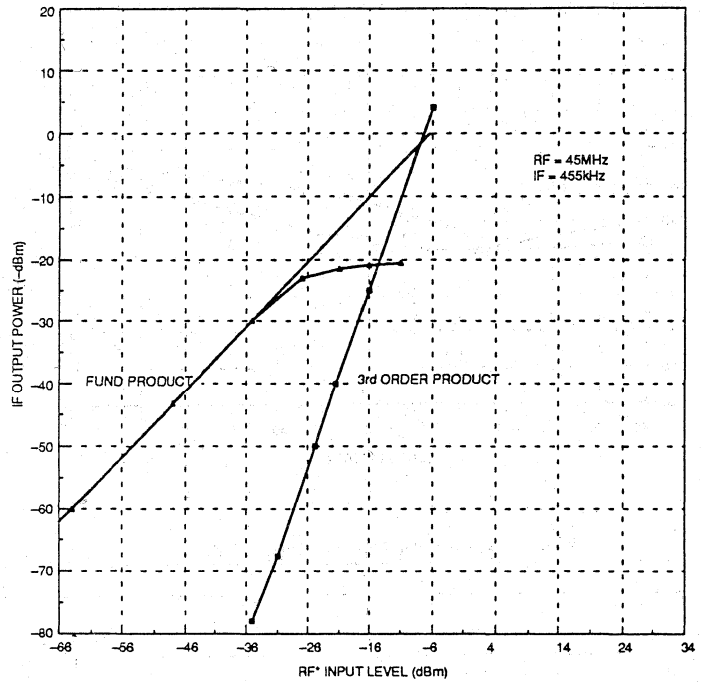


Figure 8. Mixer Third Order Intercept and Compression

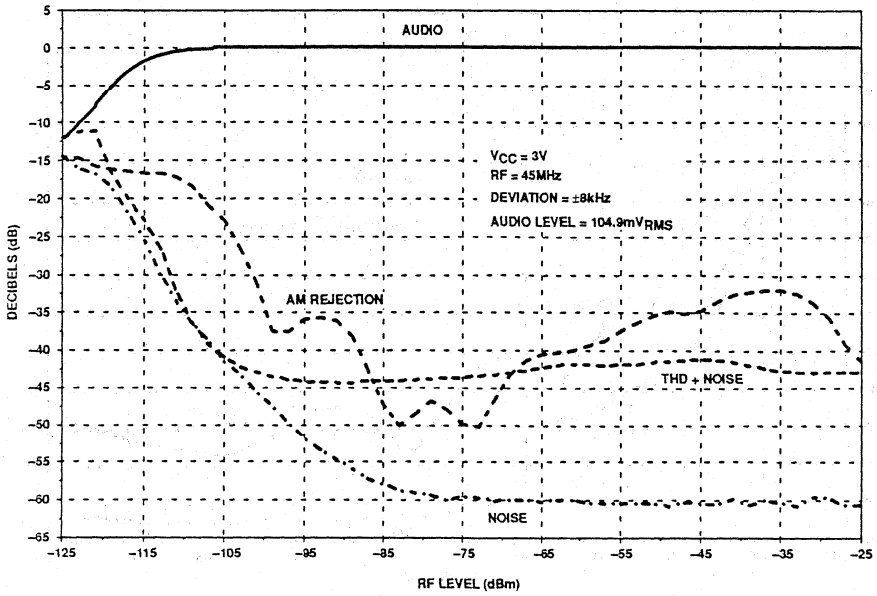


Figure 9. Sensitivity vs RF Level (–40°C)

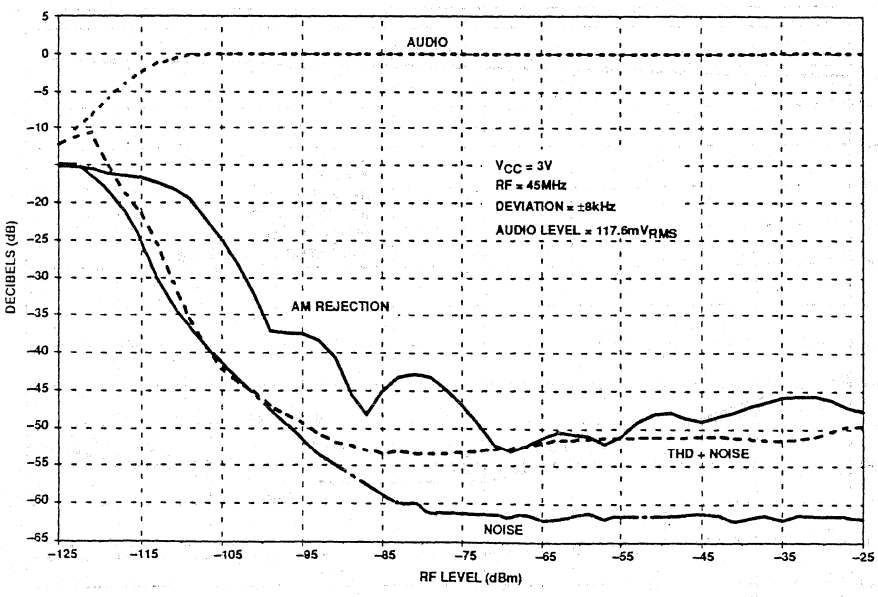


Figure 10. Sensitivity vs RF Level (+25°C)

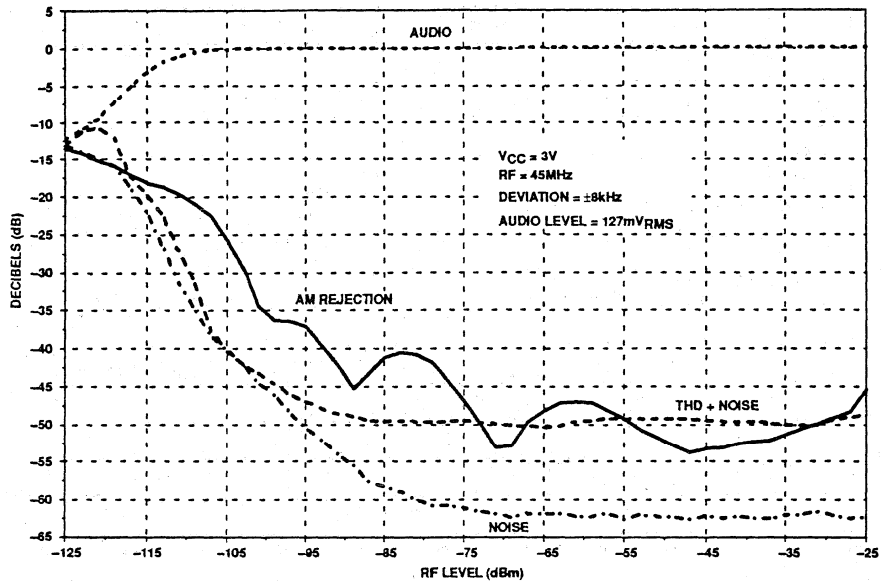


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

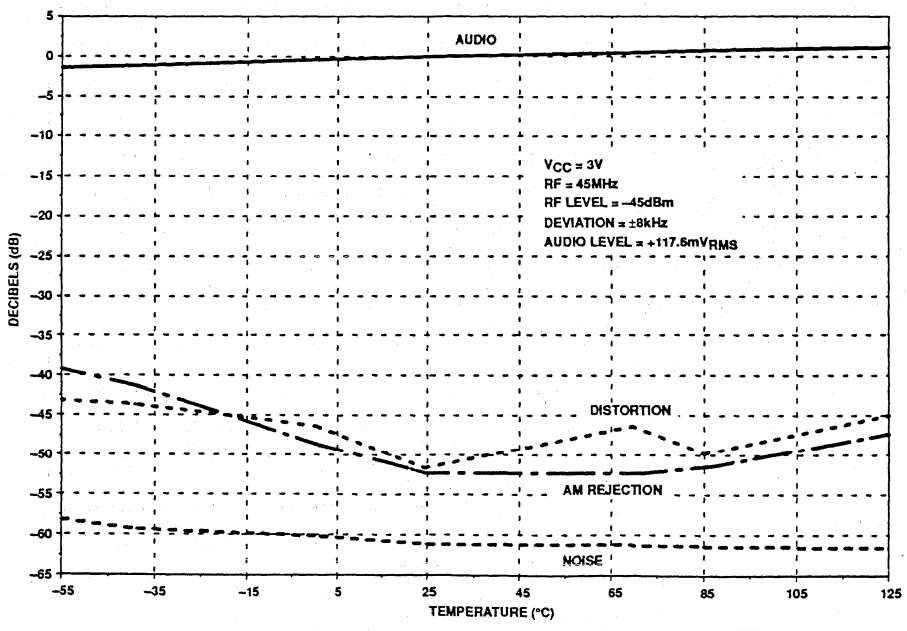


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

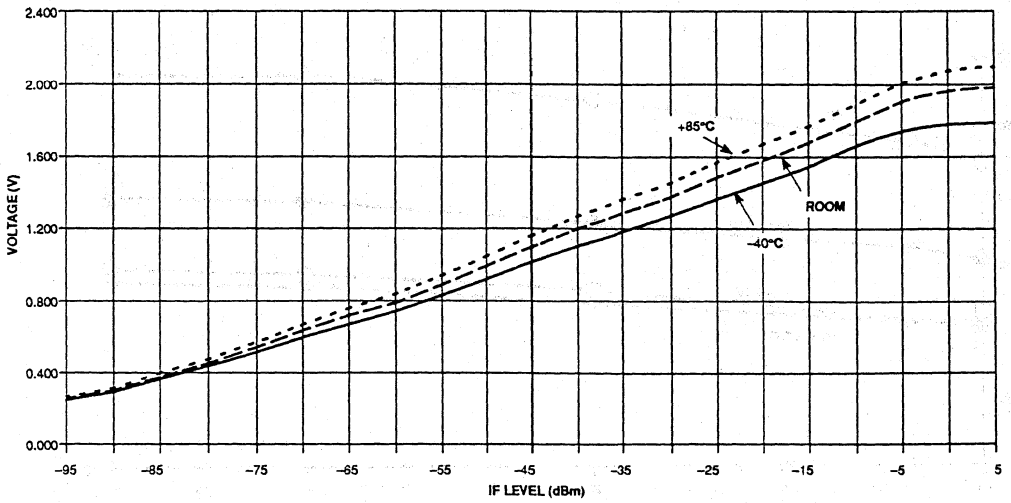


Figure 13. RSSI (455kHz IF @ 3V)

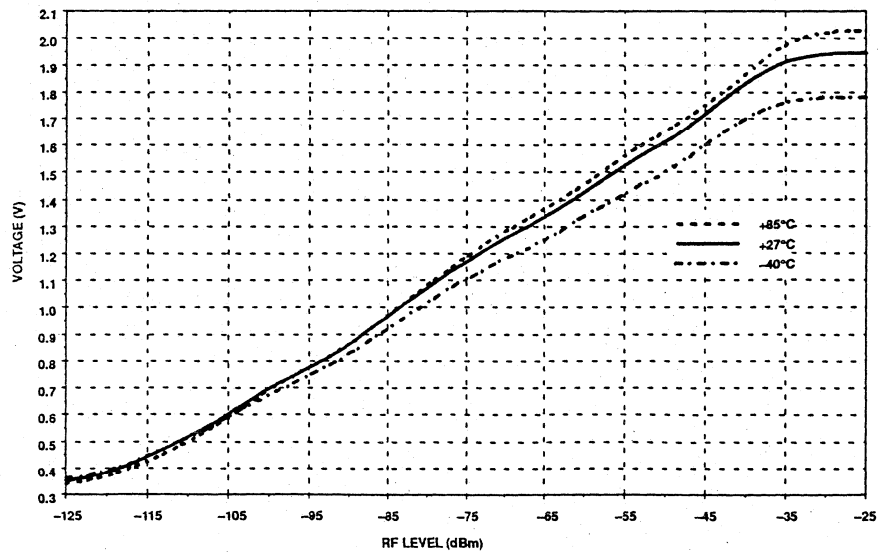


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

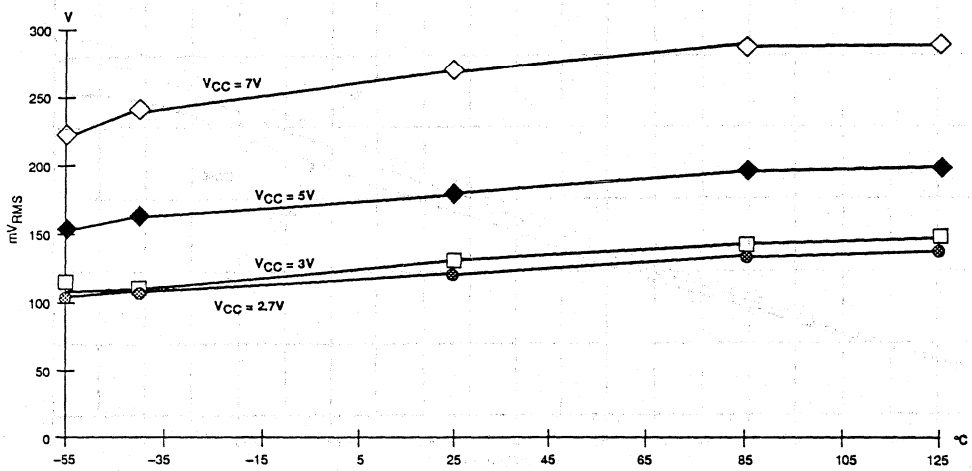
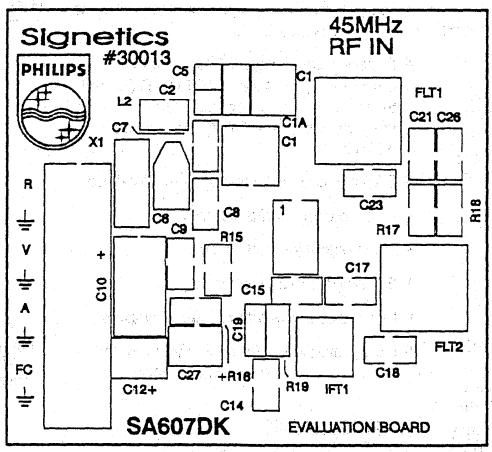
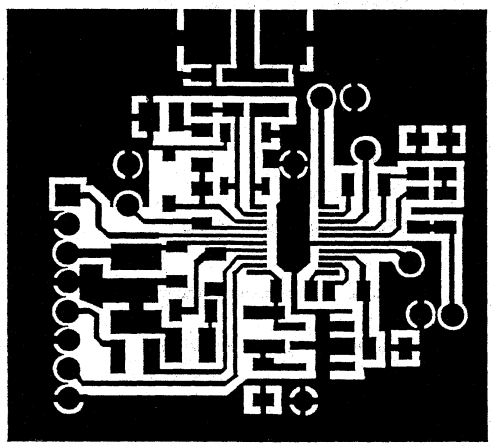


Figure 15. Audio Output vs Temperature

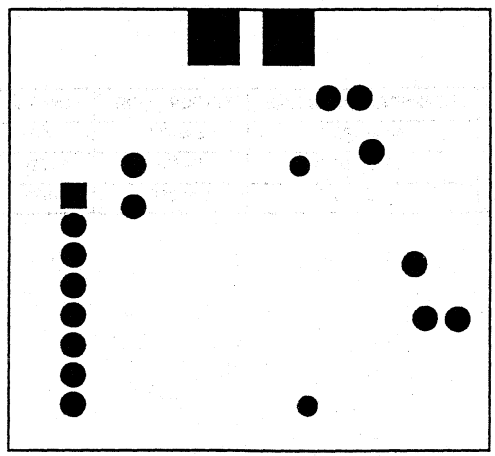
607 Silk Screen



607 TOP



607 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

Low-voltage high performance mixer FM IF system

SA608

DESCRIPTION

The SA608 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA608 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA608 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output is buffered. The RSSI output has an internal amplifier with the feedback pin accessible. The SA608 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

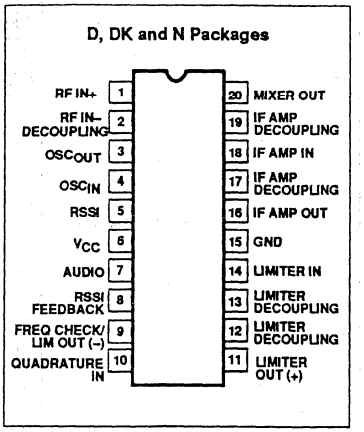
- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA608 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

PIN CONFIGURATION

D, DK and N Packages



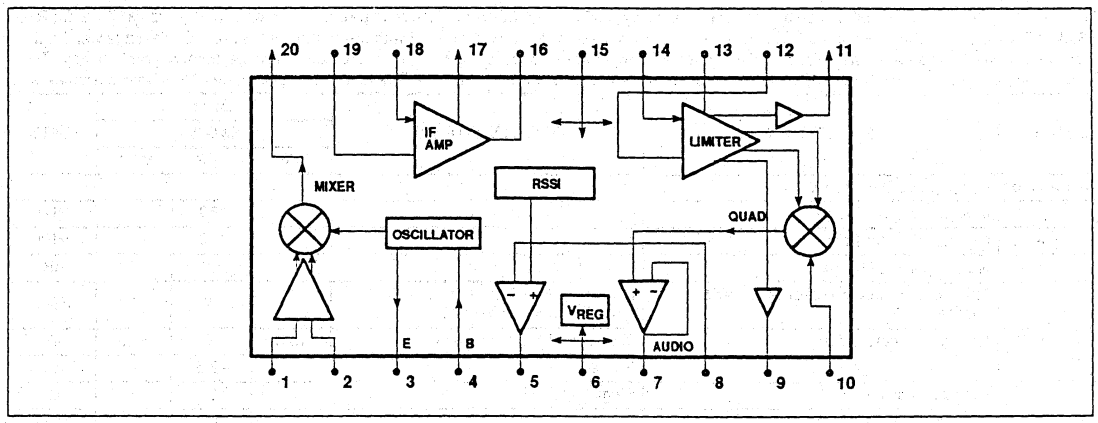
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	-40 to +85°C	SA608N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA608D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA608DK	1563

Low-voltage high performance mixer FM IF system

SA608

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		7	V
T_{STG}	Storage temperature range		–65 to +150	°C
T_A	Operating ambient temperature range SA608		–40 to +85	°C
θ_{JA}	Thermal impedance	D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA608			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA608 MIN	LIMITS SA608 TYP	LIMITS SA608 MAX	UNITS
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level[2]		35	60	80	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) no load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/lim (–) output impedance	(Pin 9)		200		Ω
	Frequency check/lim (–) output level	(Pin 9) no load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA608 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA608 input (Pin 18) which is about 21dB less than the "available power" at the generator.
2. By using 45kΩ load across the Quad detector coil, you will have Audio output at 115mV with –42dB distortion.

Low-voltage high performance mixer FM IF system

SA608

CIRCUIT DESCRIPTION

The SA608 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of −9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

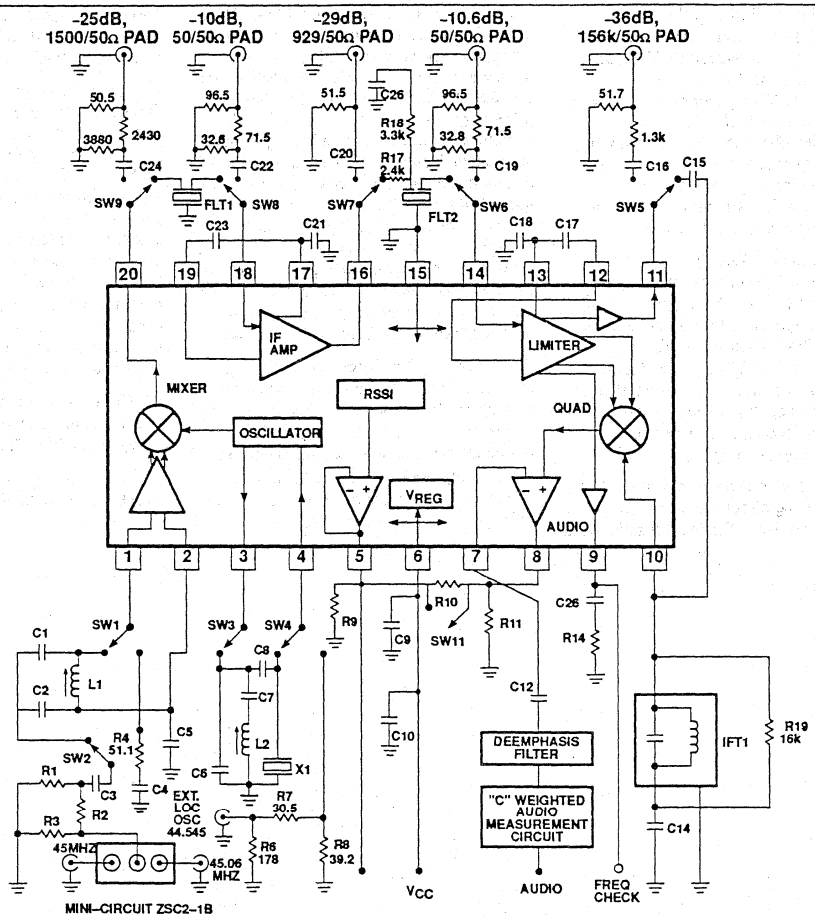
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter or Frequency Check output has drive capability of a 5kΩ minimum or higher in order to obtain 120mV_{RMS} output level.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}

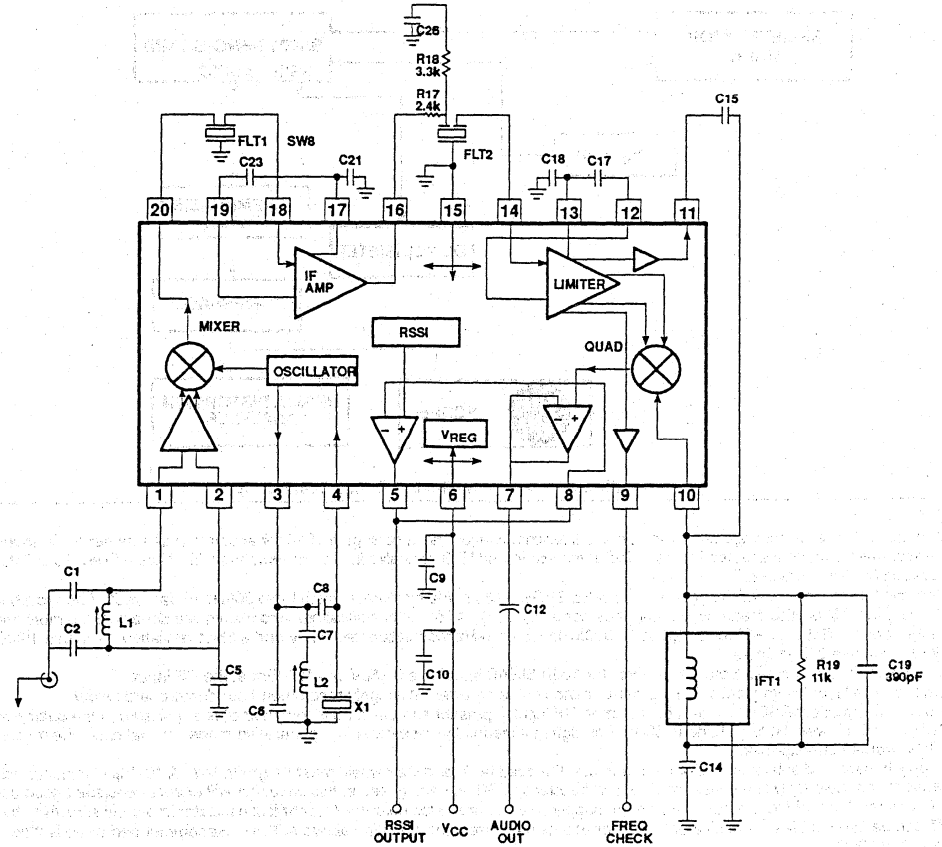


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147–160nH Coilcraft UNI-10/142-04J08S
L2	0.8μH nominal Toko 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	10kΩ ±1%
R11	10kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA607 45MHz Test Circuit (Relays as shown)



Product Board SA608D/DK Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330μH TOKO 303LN–1130
L1	0.33μH TOKO SCB–1320Z
L2	1.2μH Coilcraft 1008CS–122
X1	44.545MHz Crystal Hy-Q
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R14	10kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. SA608 45MHz Test Circuit (Relays as shown)

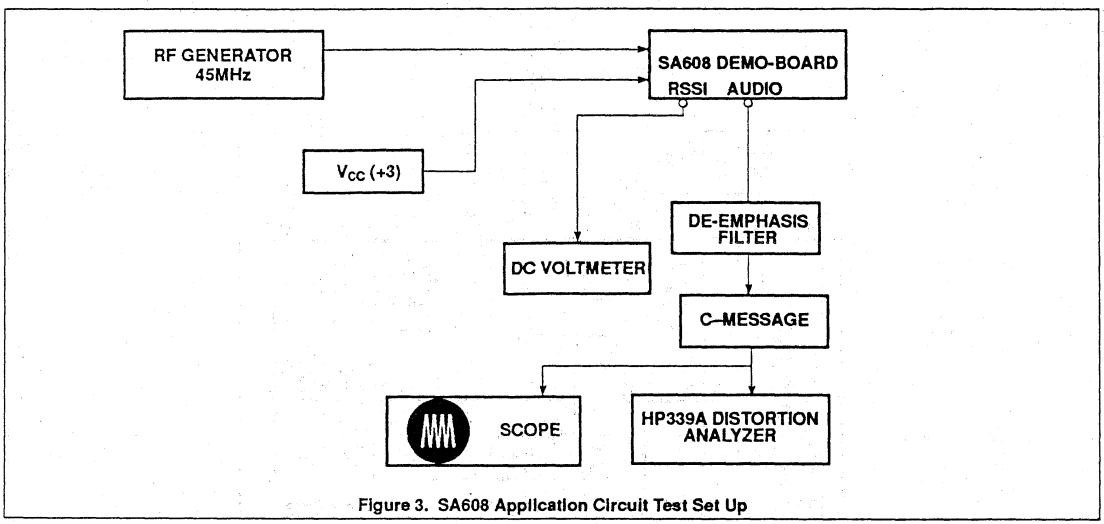


Figure 3. SA608 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

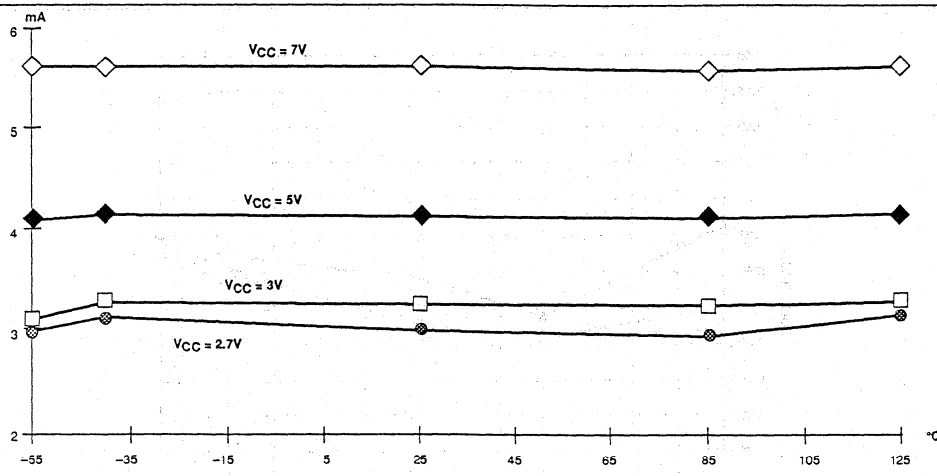


Figure 4. I_{CC} vs Temperature

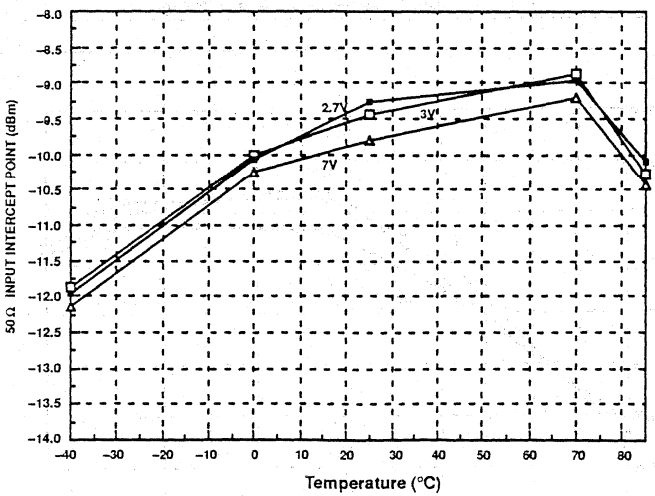


Figure 5. Third Order Intercept Point vs Supply Voltage

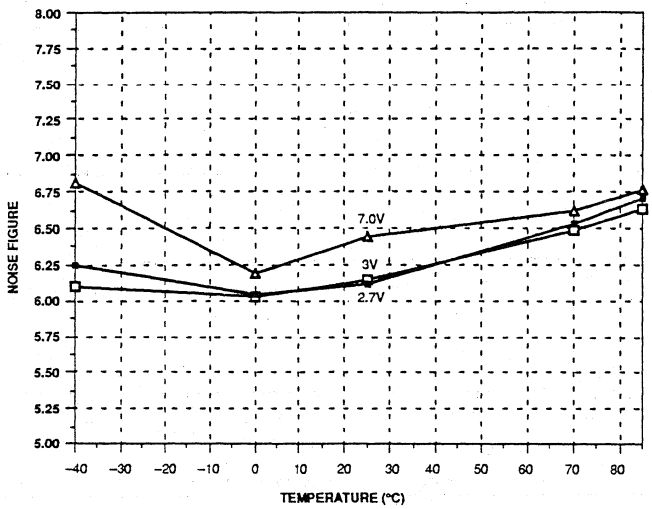


Figure 6. Mixer Noise Figure vs Supply Voltage

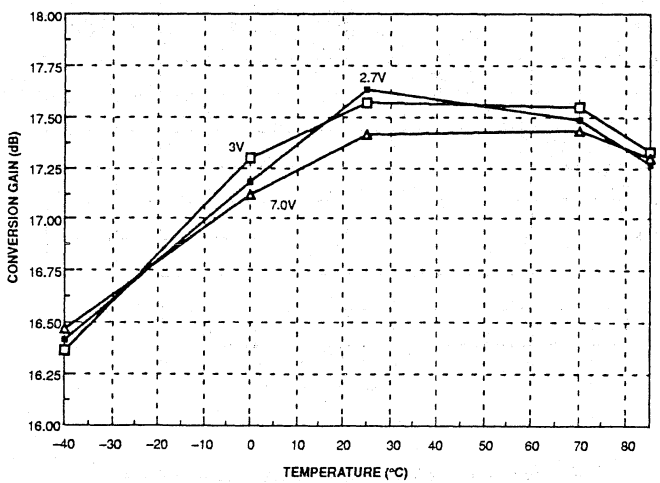


Figure 7. Conversion Gain vs Supply Voltage

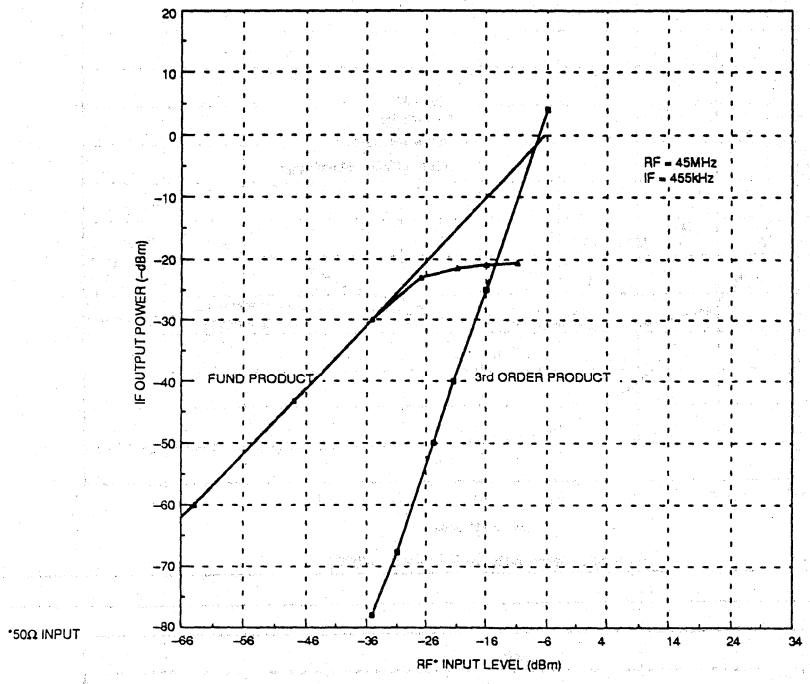


Figure 8. Mixer Third Order Intercept and Compression

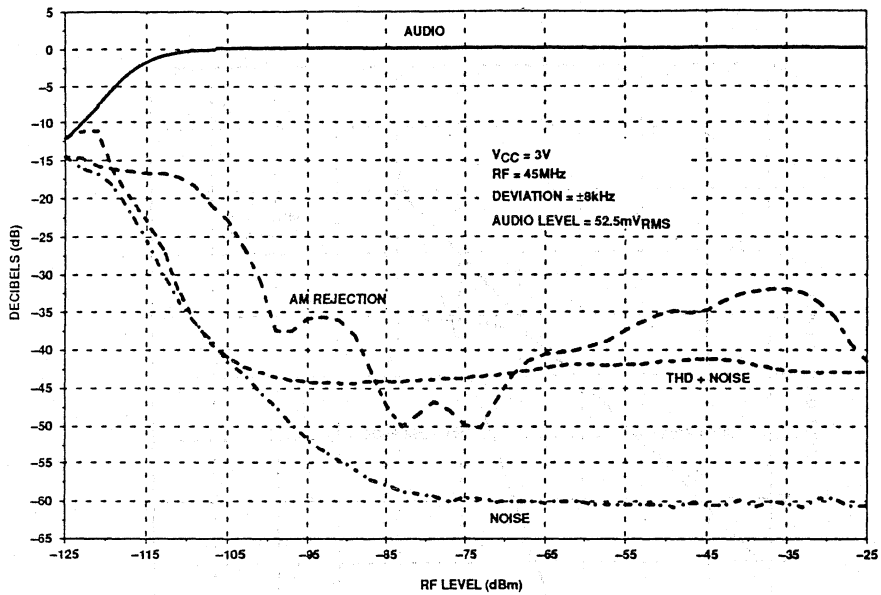


Figure 9. Sensitivity vs RF Level (–40°C)

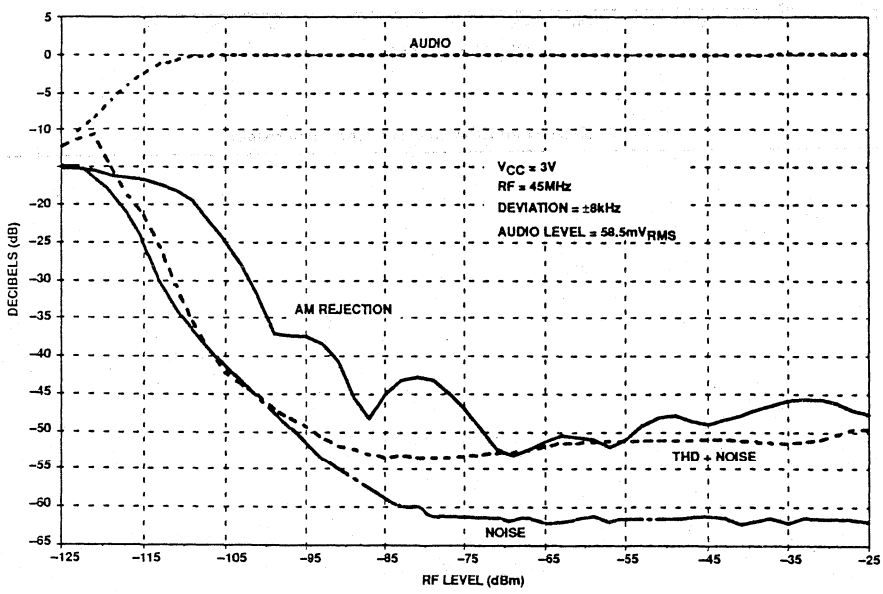


Figure 10. Sensitivity vs RF Level (+25°C)

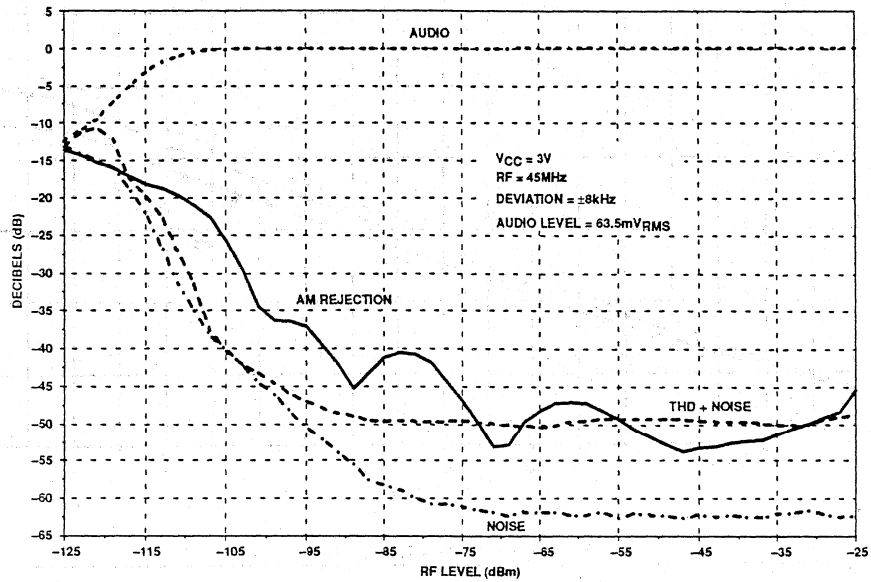


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

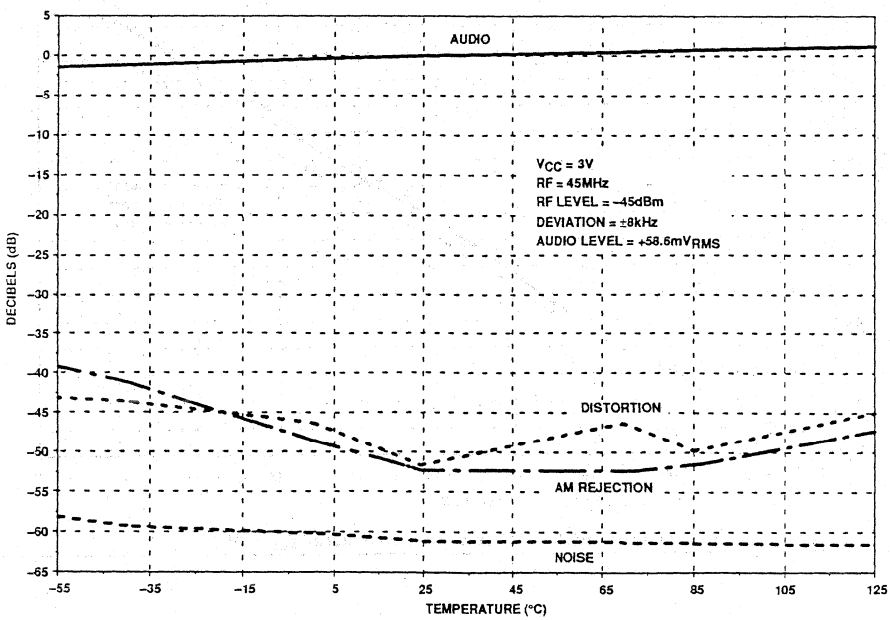


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

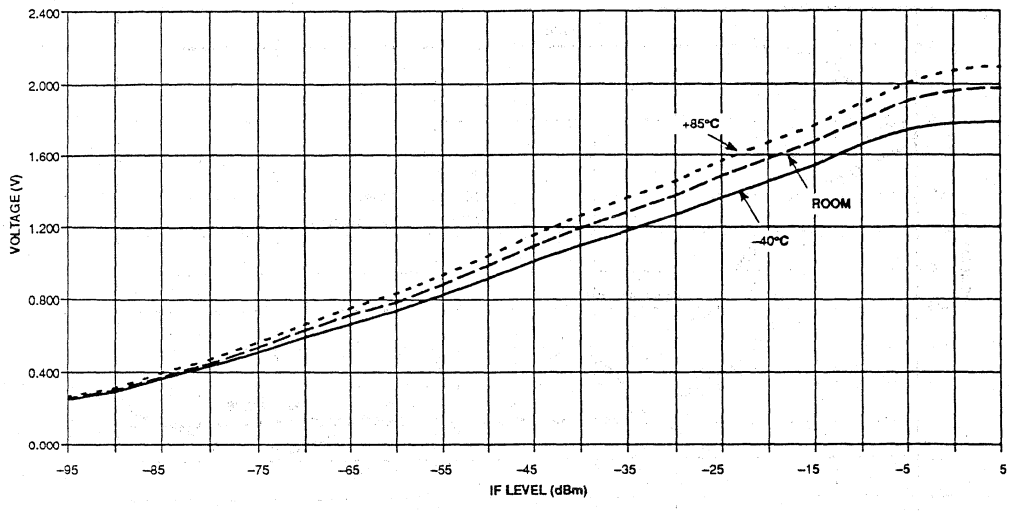


Figure 13. RSSI (455kHz IF @ 3V)

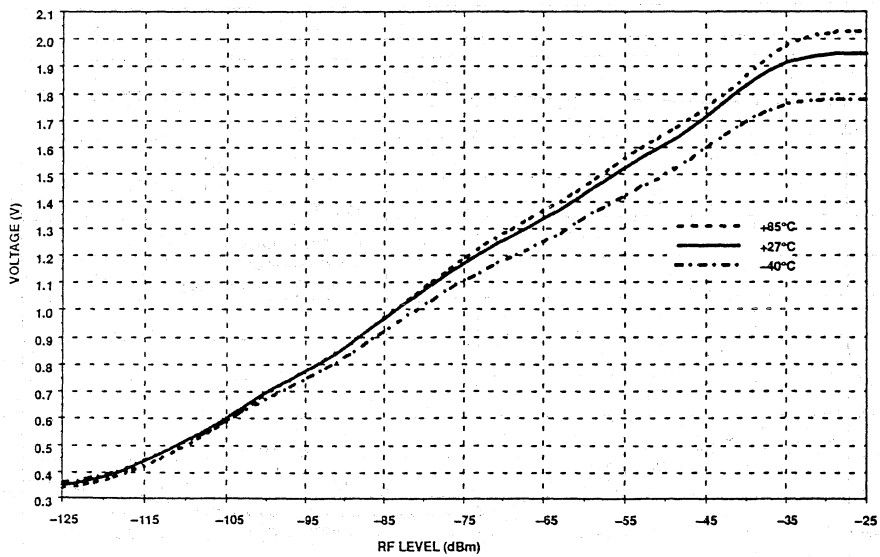


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

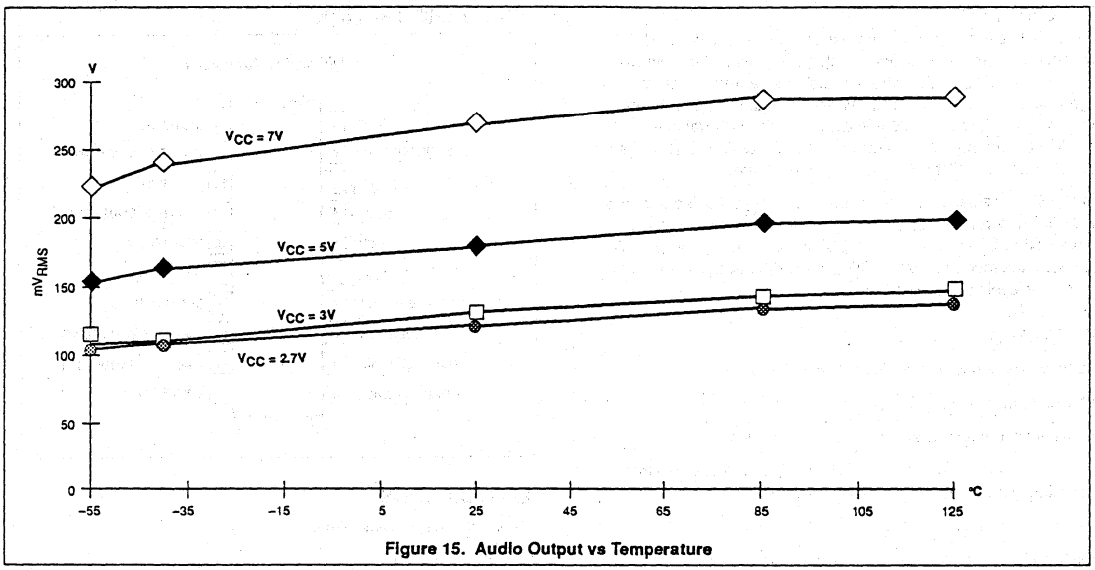


Figure 15. Audio Output vs Temperature

Low-voltage high performance mixer FM IF system

SA616

DESCRIPTION

The SA616 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA616 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

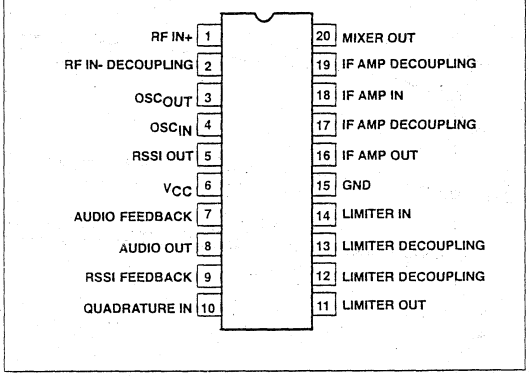
The SA616 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE615. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to adjust the output levels or add filtering.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA616 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

PIN CONFIGURATION

D, DK and N Packages



APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA616N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA616D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA616DK	1563

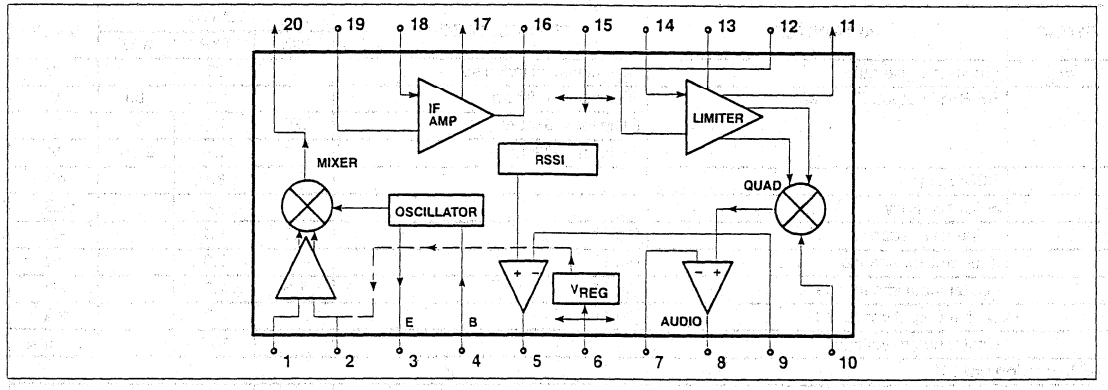
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		7	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range		-40 to +85	°C
θ_{JA}	Thermal impedance	D package DK package N package	90 117 75	°C/W

Low-voltage high performance mixer FM IF system

SA616

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third-order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = -52dBm		-9		dBm
	Conversion power gain	Matched 14.5dBV step-up	11	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single-ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting -3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		-105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	120		mV
	SINAD sensitivity	IF level -110dBm		17		dB
THD	Total harmonic distortion		-30	-45		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S/N	Signal-to-noise ratio	No modulation for noise		62		dB
	RF RSSI output, R_9 = 2kΩ	RF level = -118dBm		0.3	.80	V
		RF level = -68dBm	.70	1.1	2	V
		RF level = -23dBm	1.0	1.8	2.50	V
	RSSI range			80		dB
	RSSI accuracy			±2		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = -27dBm		120		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = -27dBm		2.2		V
	System SINAD sensitivity	RF level = -117dBm		12		dB

CIRCUIT DESCRIPTION

The SA616 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of -9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

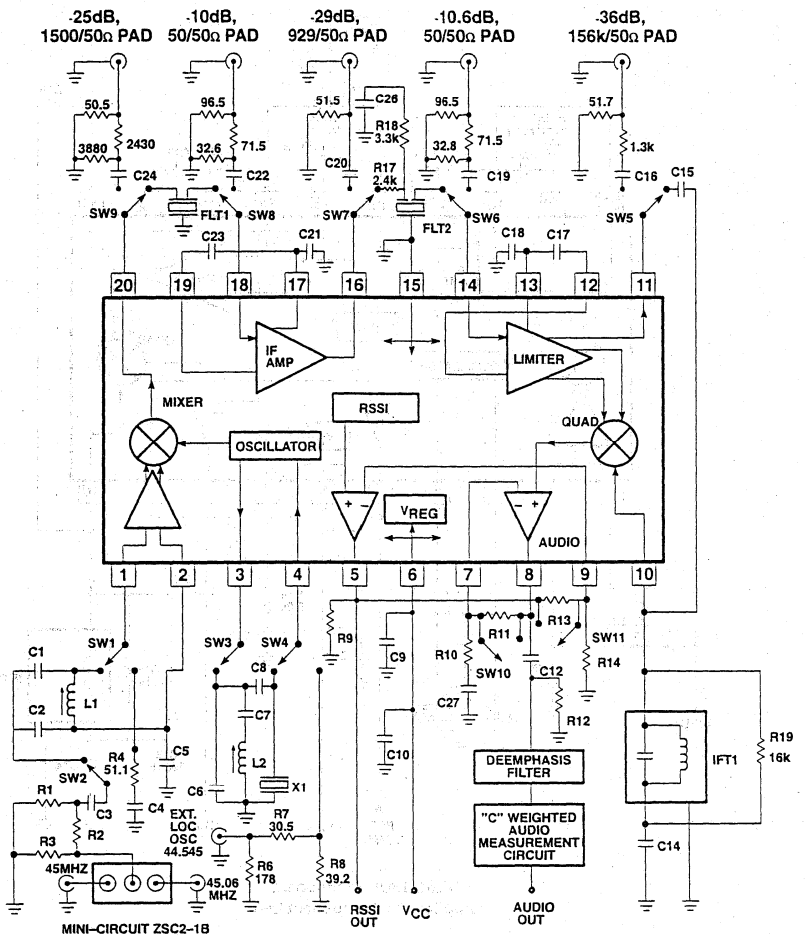
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

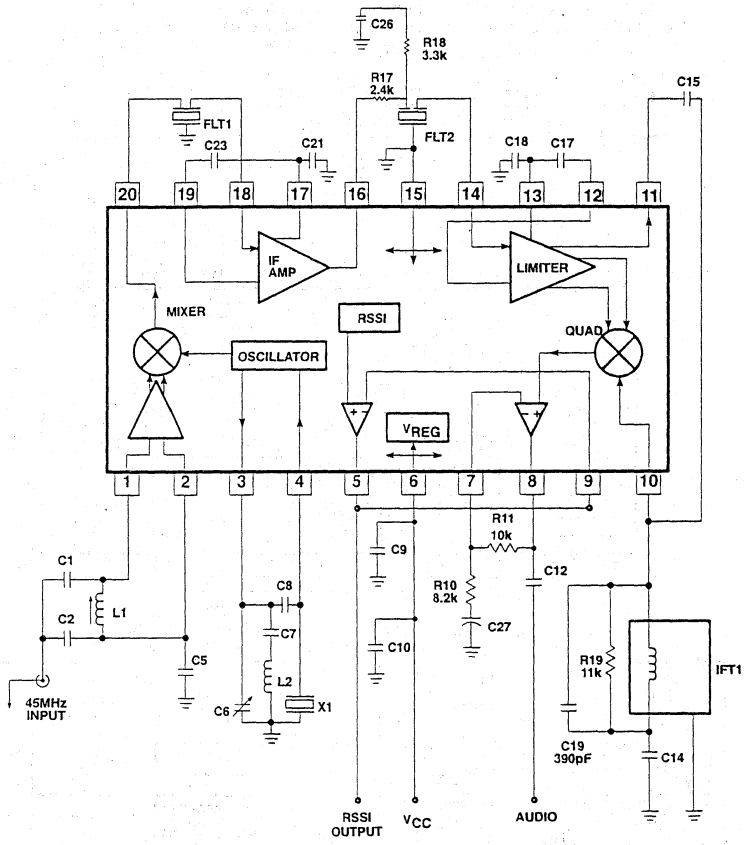
NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
C7	1nF Ceramic	L1	147-160nH Coilcraft UNI-10/142-04J08S
C8	10.0pF NPO Ceramic	L2	0.8µH nominal
C9	100nF ±10% Monolithic Ceramic		Toko 292CNS-T1038Z
C10	15µF Tantalum (minimum)	X1	44.545MHz Crystal ICM4712701
C12	2.2µF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	8.2kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C23	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C26	100nF ±10% Monolithic Ceramic	R19	16kΩ

Figure 1. SA616 45MHz Test Circuit (Relays as shown)



NE616D/DK Demoboard
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15µF Tantalum (minimum)
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

Figure 2. SA616 45MHz Application Circuit

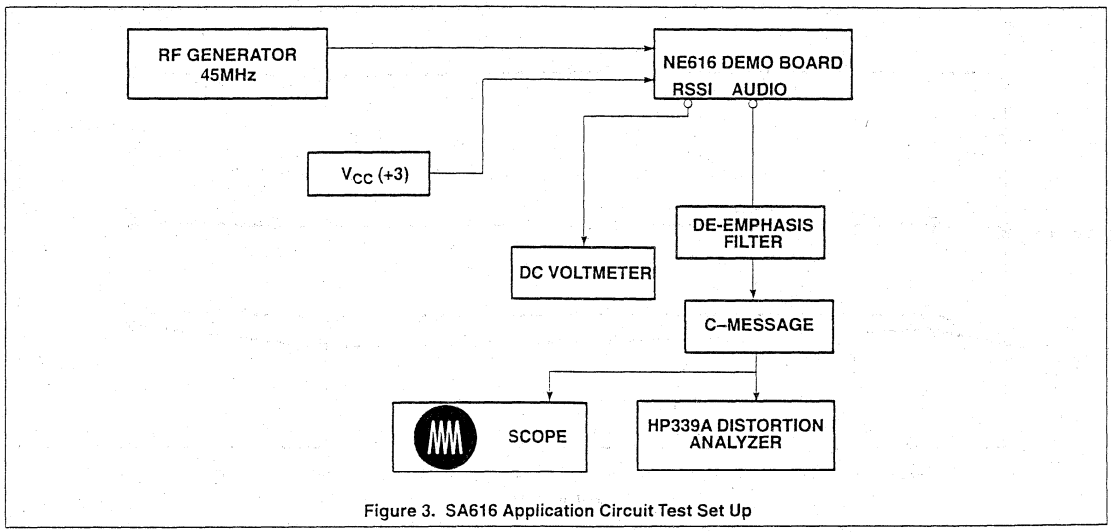


Figure 3. SA616 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or -116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

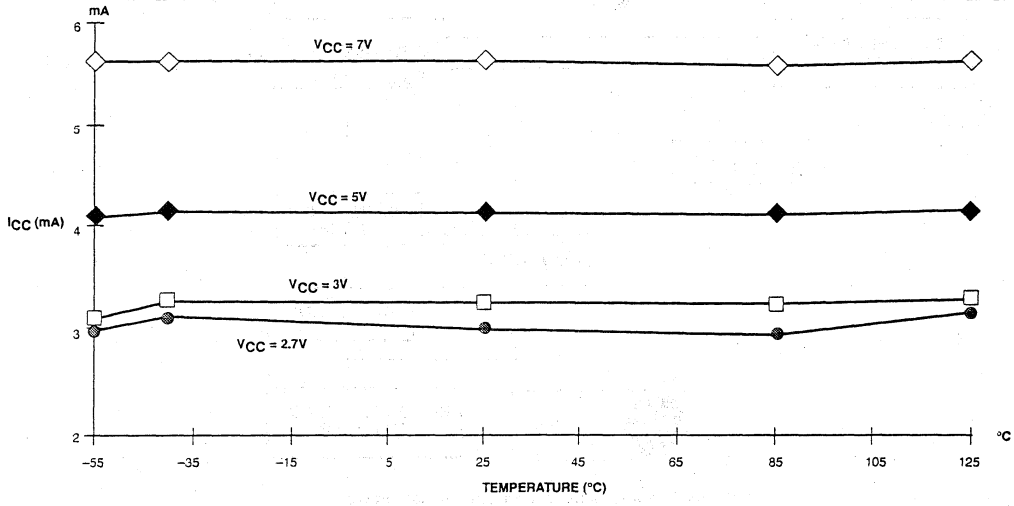


Figure 4. I_{CC} vs Temperature

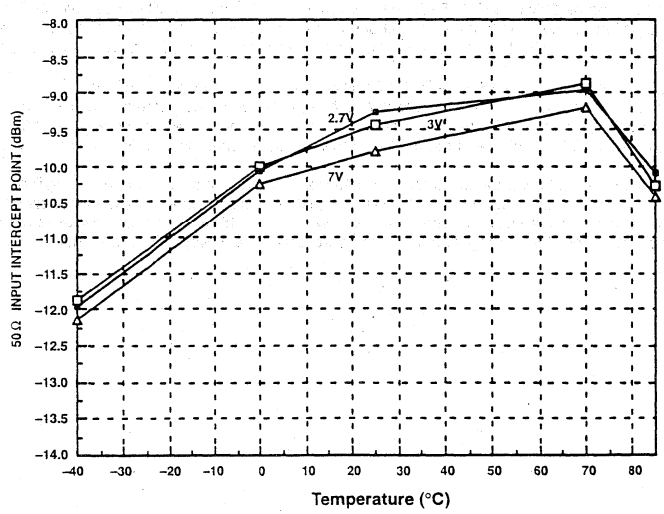


Figure 5. Third Order Intercept Point vs Supply Voltage

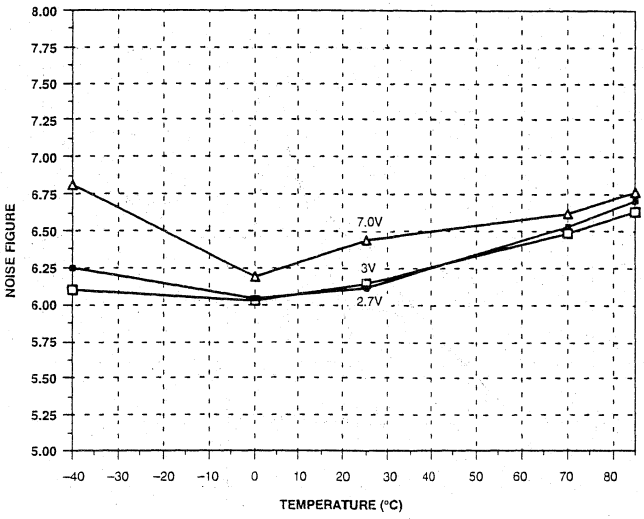


Figure 6. Mixer Noise Figure vs Supply Voltage

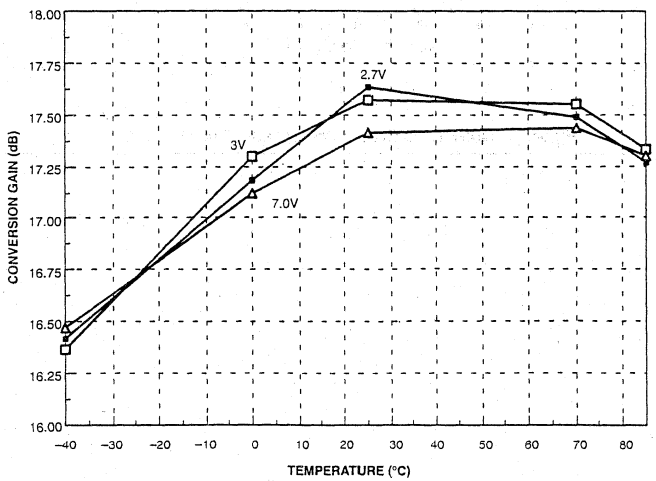


Figure 7. Conversion Gain vs Supply Voltage

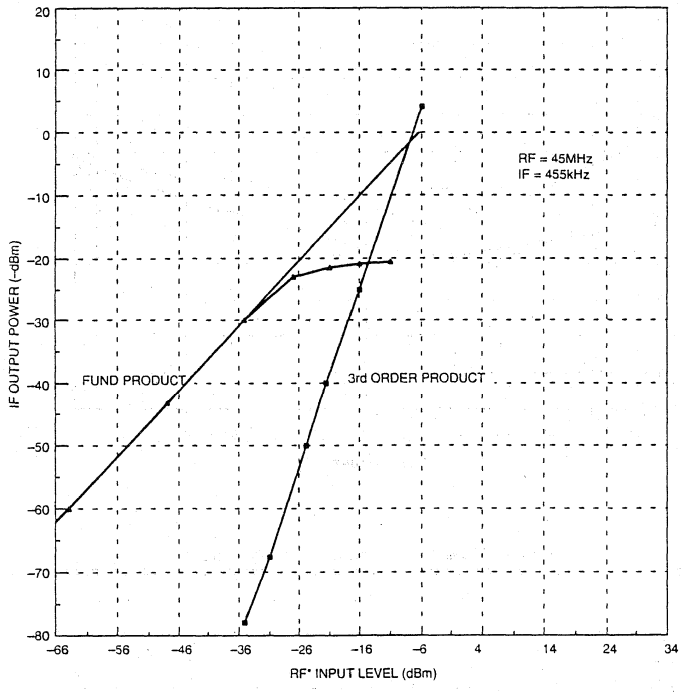


Figure 8. Mixer Third Order Intercept and Compression

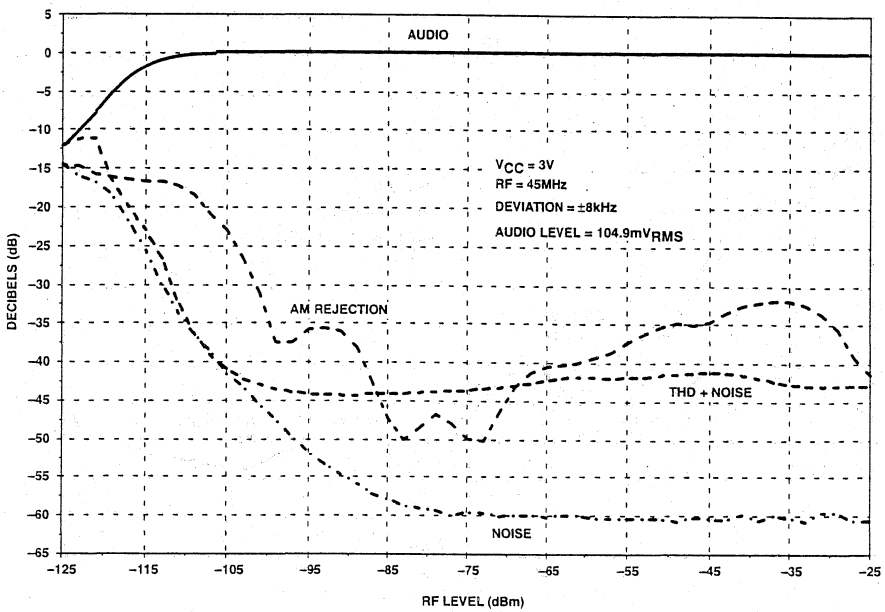


Figure 9. Sensitivity vs RF Level (-40°C)

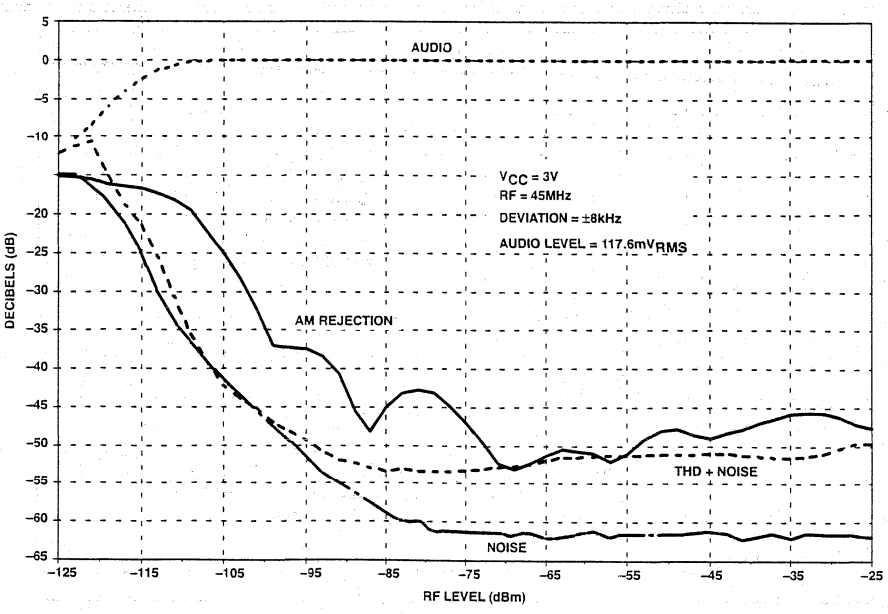


Figure 10. Sensitivity vs RF Level (+25°C)

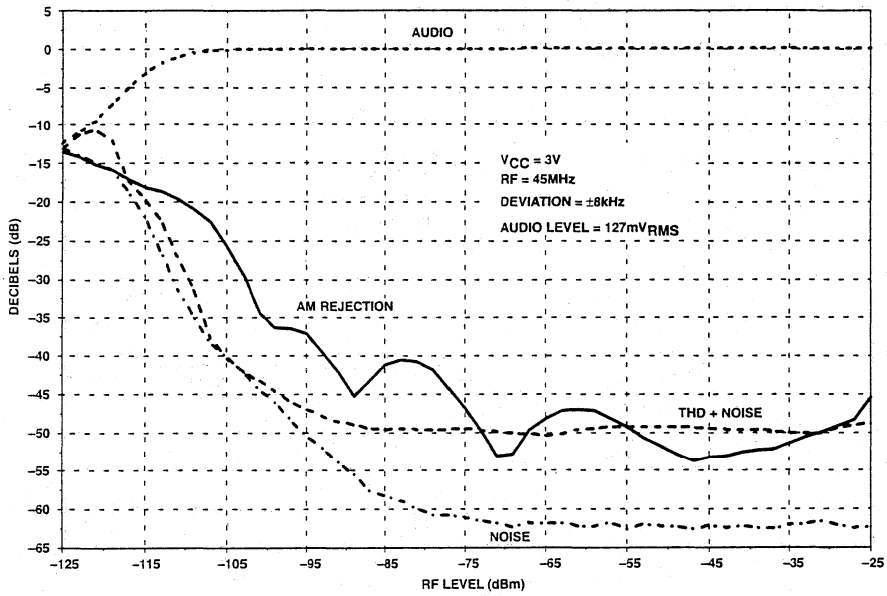


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

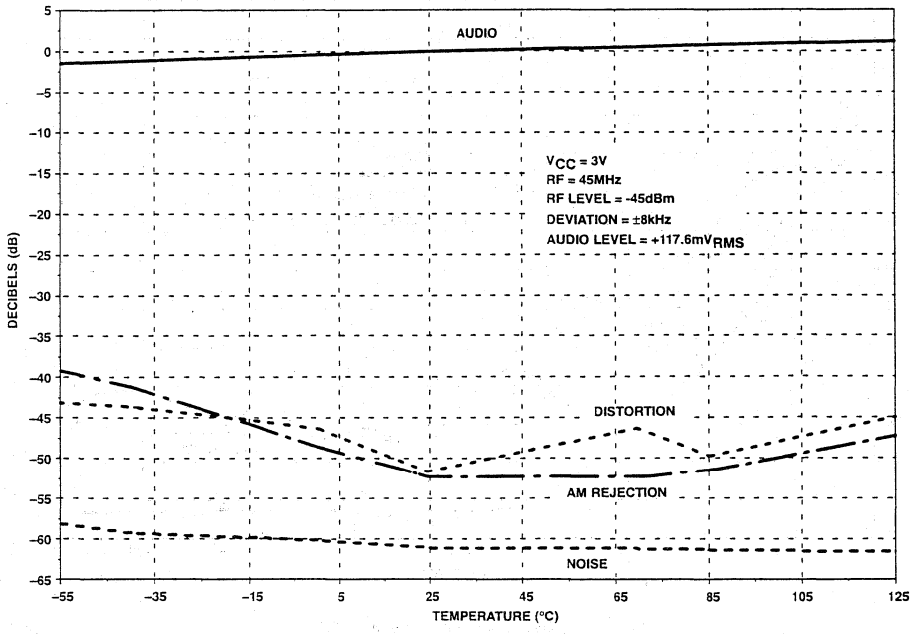


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

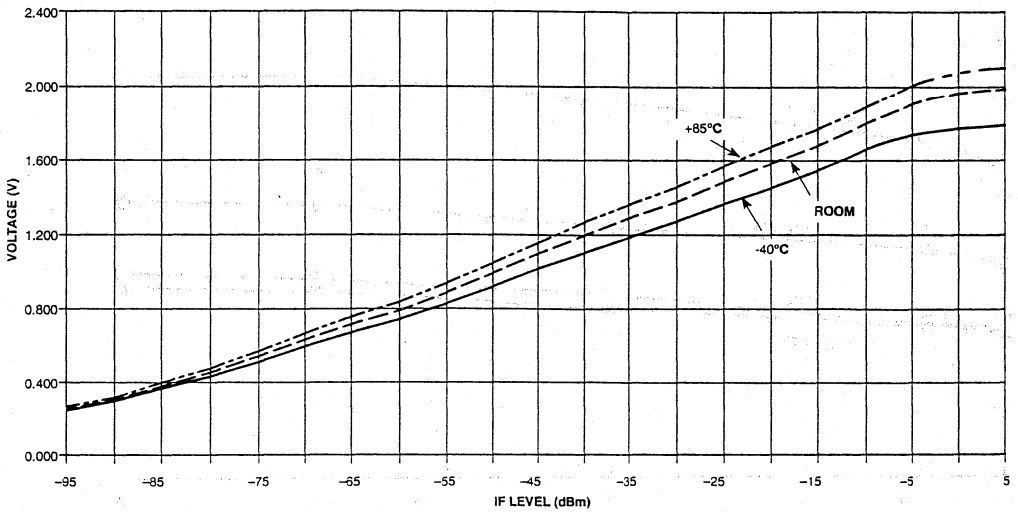


Figure 13. RSSI (455kHz IF @ 3V)

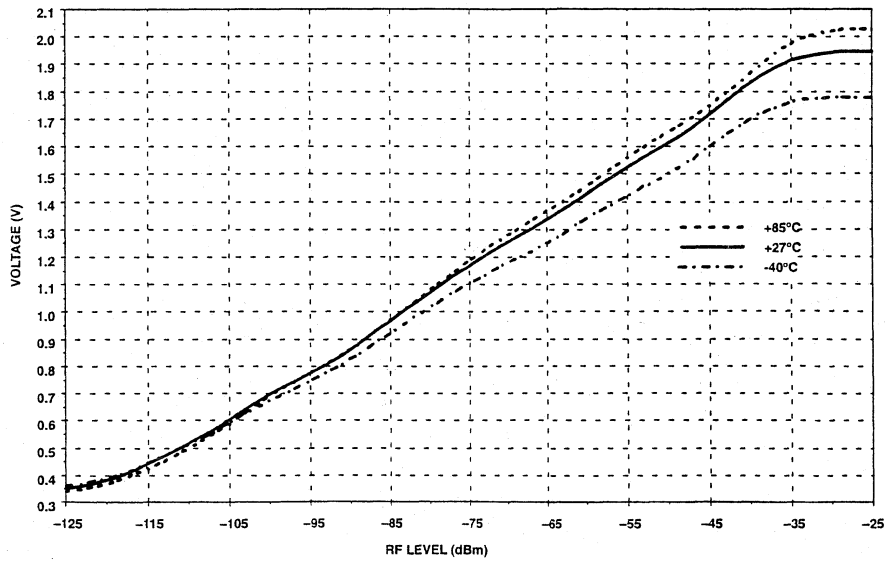


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

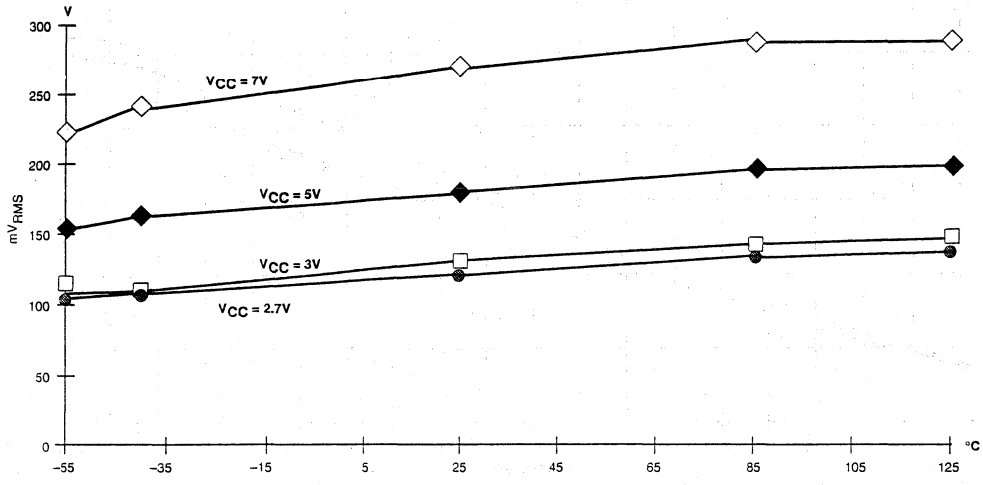
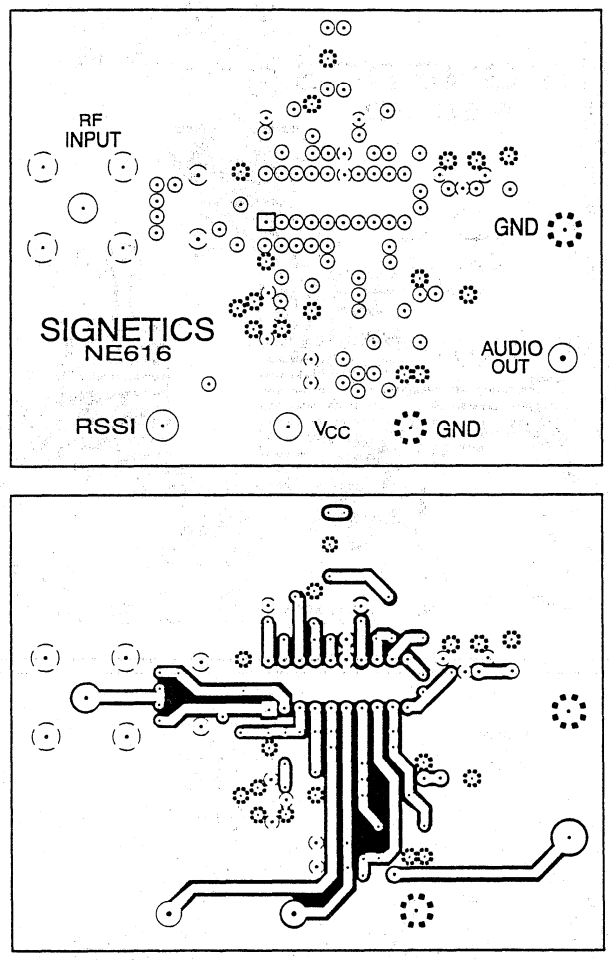
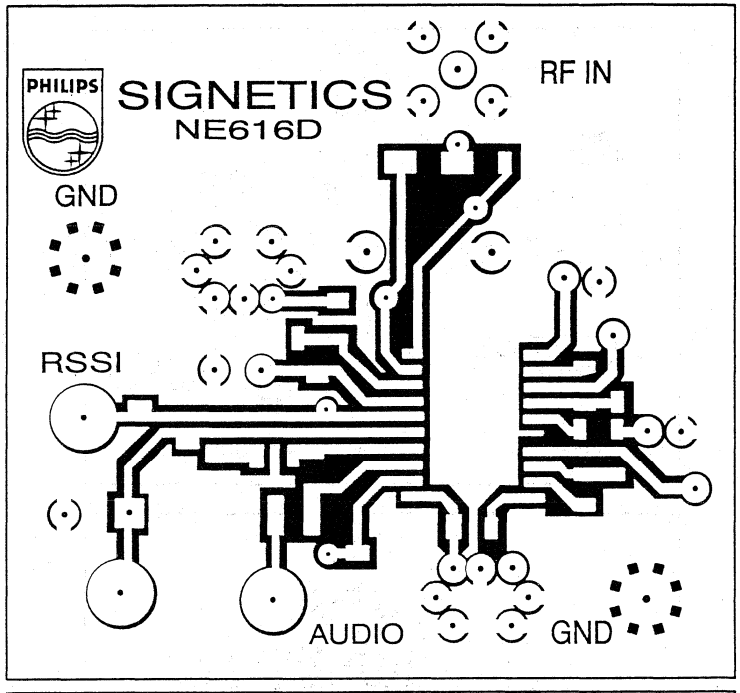


Figure 15. Audio Output vs Temperature



*Applies to Stand-Alone data sheets only.

Figure 16. SA616N DIP Product Board Layout (Actual Size* — For Reference Use Only)



*Applies to Stand-Alone data sheets only.

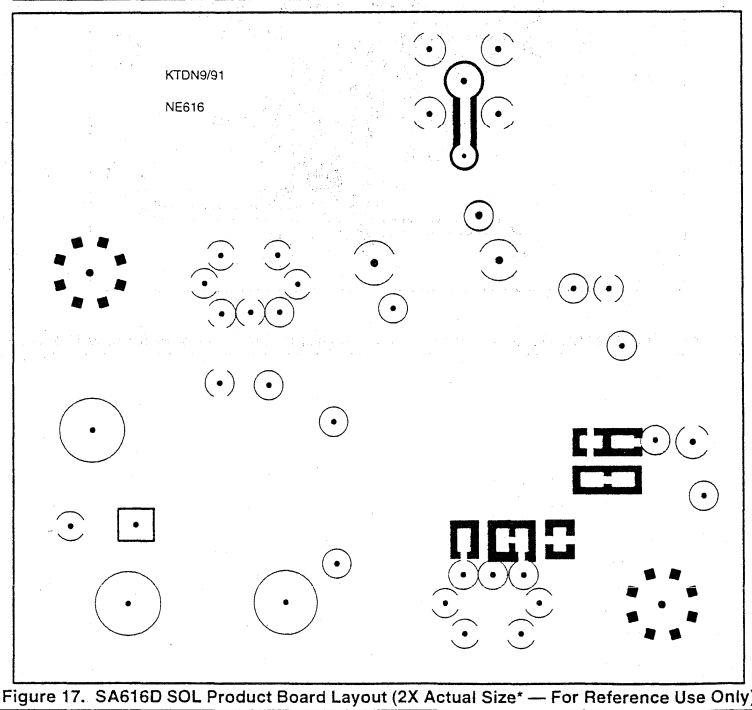
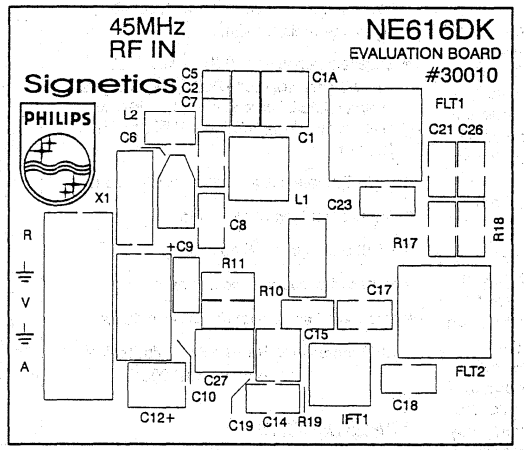
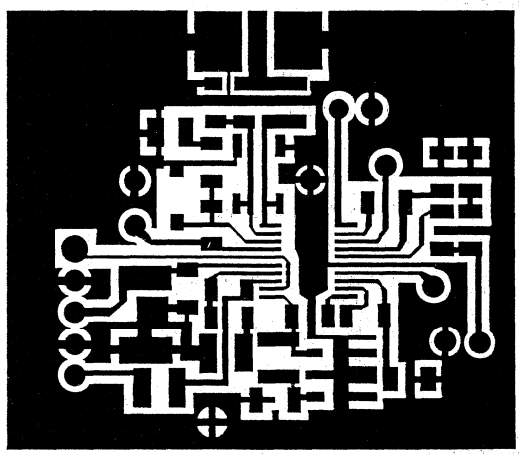


Figure 17. SA616D SOL Product Board Layout (2X Actual Size* — For Reference Use Only)

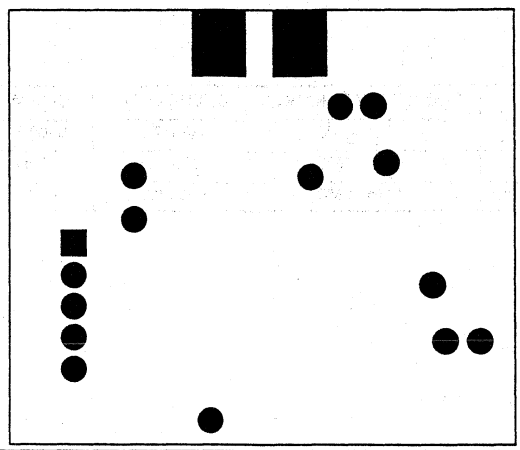
616 Silk Screen



616 TOP



616 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

Low-voltage high performance mixer FM IF system

SA617

DESCRIPTION

The SA617 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA617 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA617 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The SA617 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

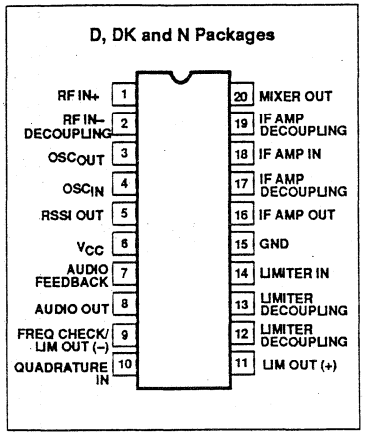
- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA617 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

PIN CONFIGURATION

D, DK and N Packages



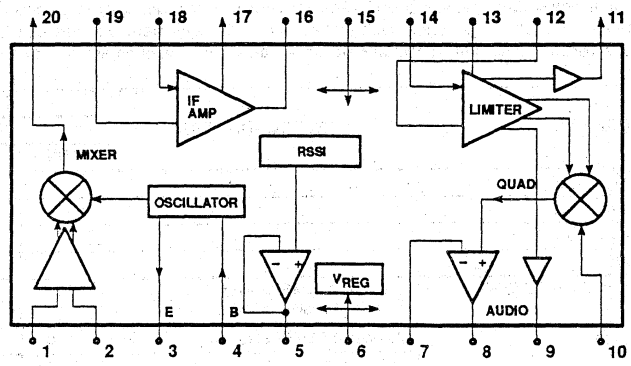
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	-40 to +85°C	SA617N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA617D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA617DK	1563

Low-voltage high performance mixer FM IF system

SA617

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		7	V
T_{STG}	Storage temperature range		–65 to +150	°C
T_A	Operating ambient temperature range SA617		–40 to +85	°C
θ_{JA}	Thermal impedance	D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA617			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit NO TAG. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA617 MIN	LIMITS SA617 TYP	LIMITS SA617 MAX	UNITS
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	11.0	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	114		mV
	SINAD sensitivity	RF level –110dB		13		dB
THD	Total harmonic distortion		–30	–45		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	2.0	V
		IF level = –23dBm	1.0	1.8	2.5	V
	RSSI range			80		dB
	RSSI accuracy			±2.0		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) No load 2.4kΩ load		130 115		mV$_{RMS}$
	Frequency Check/limiter output impedance	(Pin 9)		200		Ω
	Frequency Check/limiter output level	(Pin 9) No load 2.4kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		240		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA617 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA617 input (Pin 18) which is about 21dB less than the "available power" at the generator.

Low-voltage high performance mixer FM IF system

SA617

CIRCUIT DESCRIPTION

The SA617 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

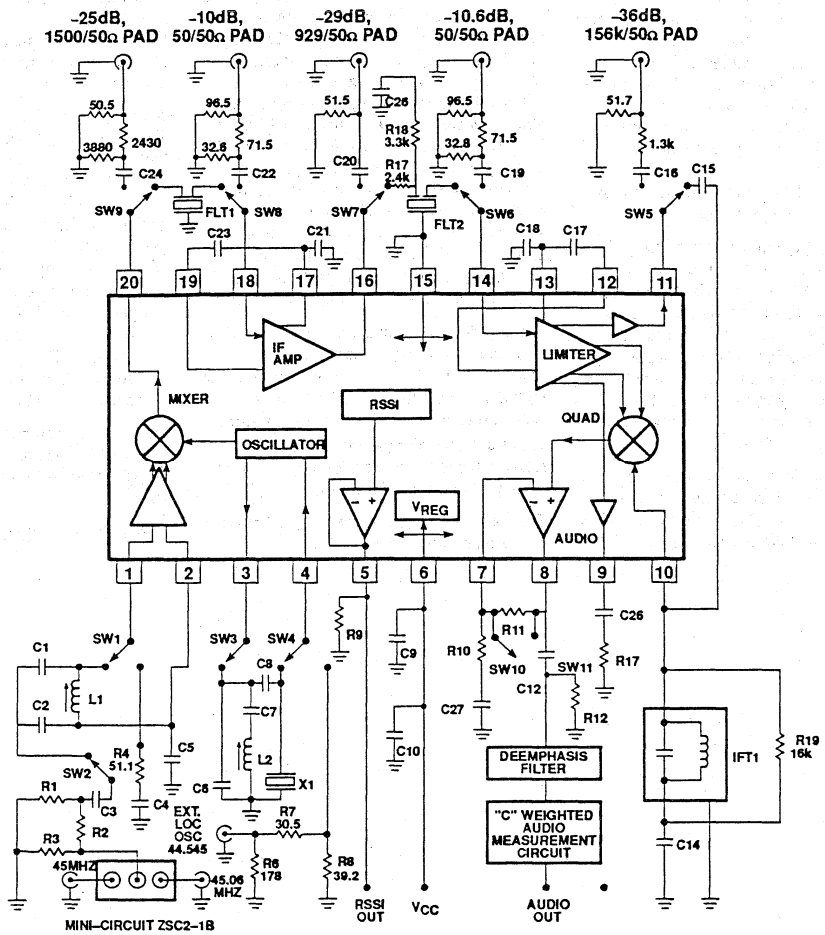
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 2kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter output or Frequency Check output has drive capability of a load minimum of 2kΩ or higher to obtain 115mV output level.

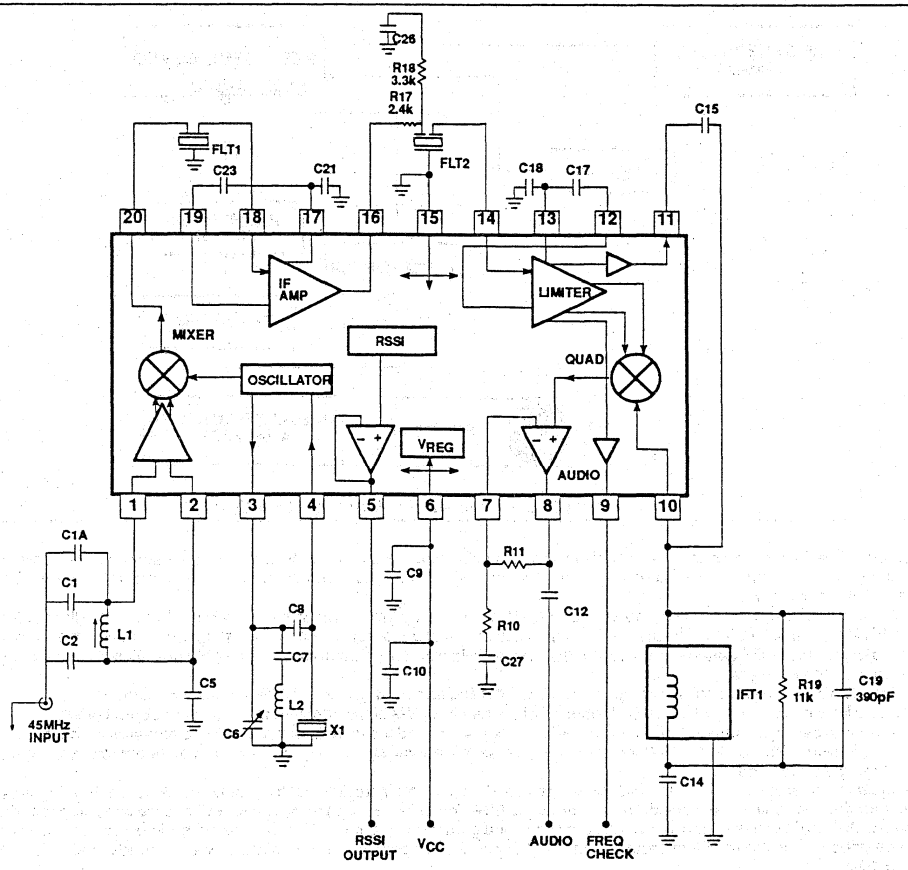
NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147-160nH Coilcraft UNI-10/142-04J08S
L2	3.3μH nominal Toko 292CNS-T1046Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R12	2kΩ ±1%
R14	10kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

Figure 1. SA617 45MHz Test Circuit (Relays as shown)



SA617DK
Application Component List

C1A	18pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C1	33pF NPO Ceramic	C26	100nF ±10% Monolithic Ceramic
C2	220pF NPO Ceramic	C27	2.2µF Tantalum
C5	100nF ±10% Monolithic Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C6	30pF trim cap	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	IFT 1	330µH TOKO 303LN-1130
C8	10.0pF NPO Ceramic	L1	.33µH TOKO SCB-1320Z
C9	100nF ±10% Monolithic Ceramic	L2	1.2µH
C10	15µF Tantalum (minimum)	X1	44.545MHz Crystal ICM4712701
C12	2.2µF ±10% Tantalum	R5	Not Used in Application Board (see Note 8, pg 8)
C14	100nF ±10% Monolithic Ceramic	R10	8.2k ±5% 1/4W Carbon Composition
C15	10pF NPO Ceramic	R11	10k ±5% 1/4W Carbon Composition
C17	100nF ±10% Monolithic Ceramic	R17	2.4k ±5% 1/4W Carbon Composition
C18	100nF ±10% Monolithic Ceramic	R18	3.3k ±5% 1/4W Carbon Composition
C19	390pF ±10% Monolithic Ceramic	R19	11k ±5% 1/4W Carbon Composition
C21	100nF ±10% Monolithic Ceramic		

Figure 2. SA617 45MHz Application Circuit

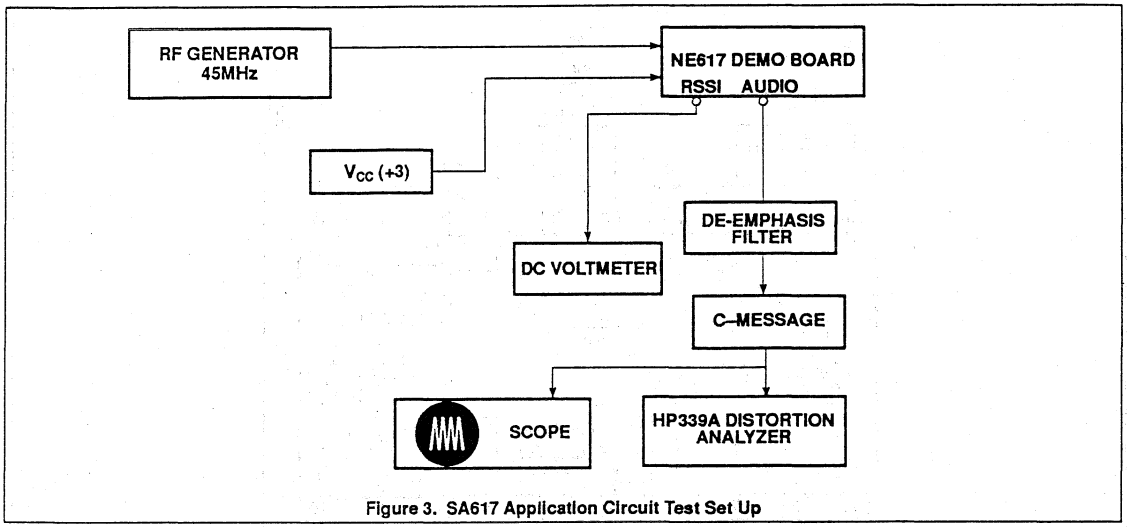


Figure 3. SA617 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

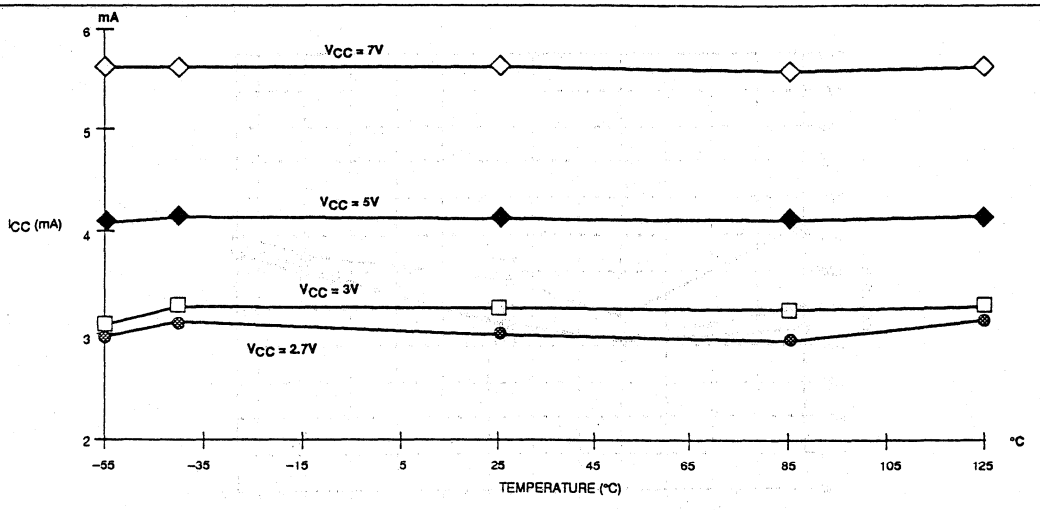


Figure 4. I_{CC} vs Temperature

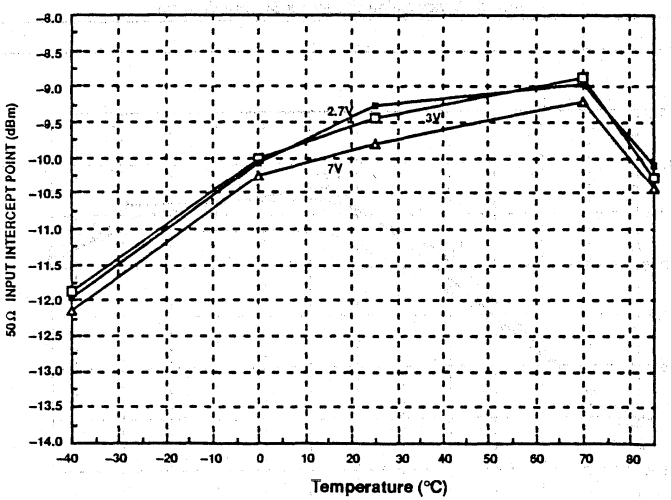


Figure 5. Third Order Intercept Point vs Supply Voltage

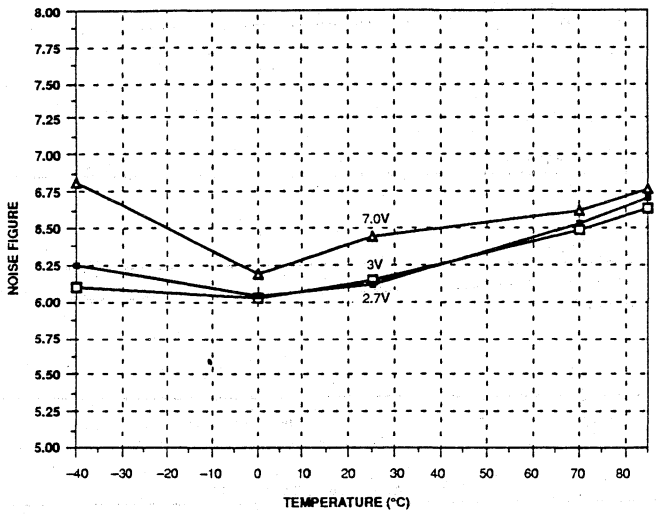


Figure 6. Mixer Noise Figure vs Supply Voltage

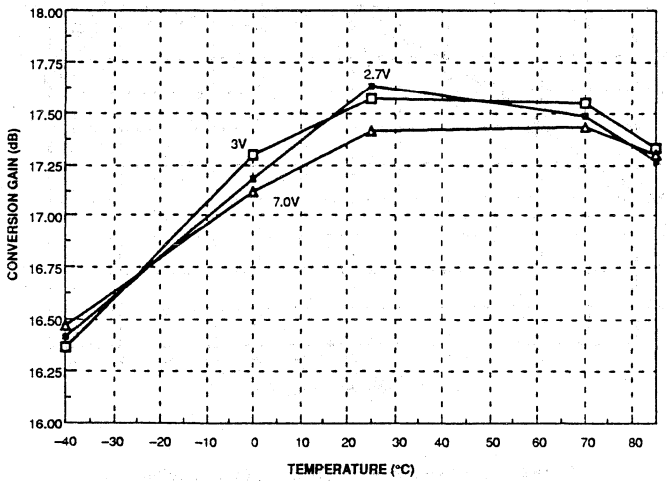


Figure 7. Conversion Gain vs Supply Voltage

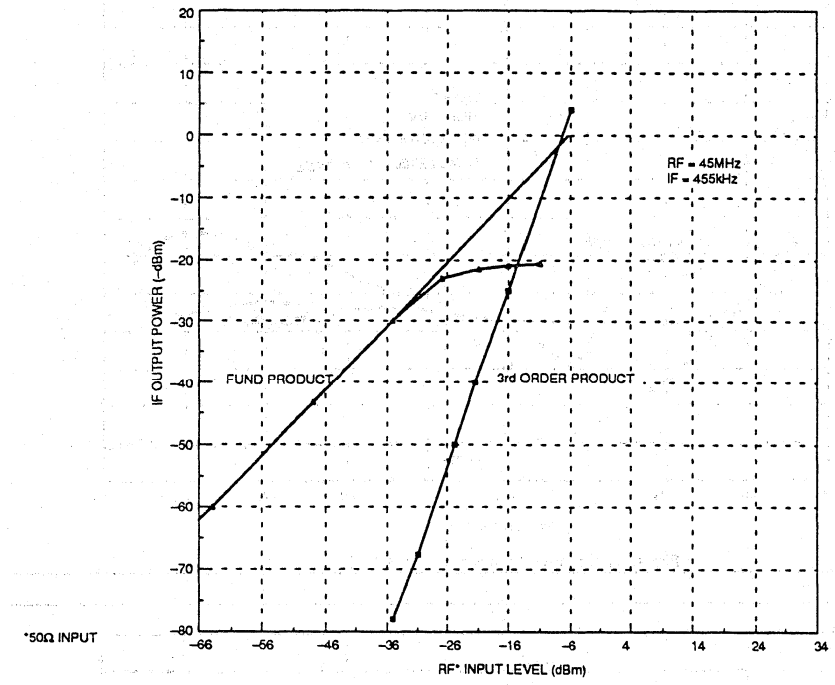


Figure 8. Mixer Third Order Intercept and Compression

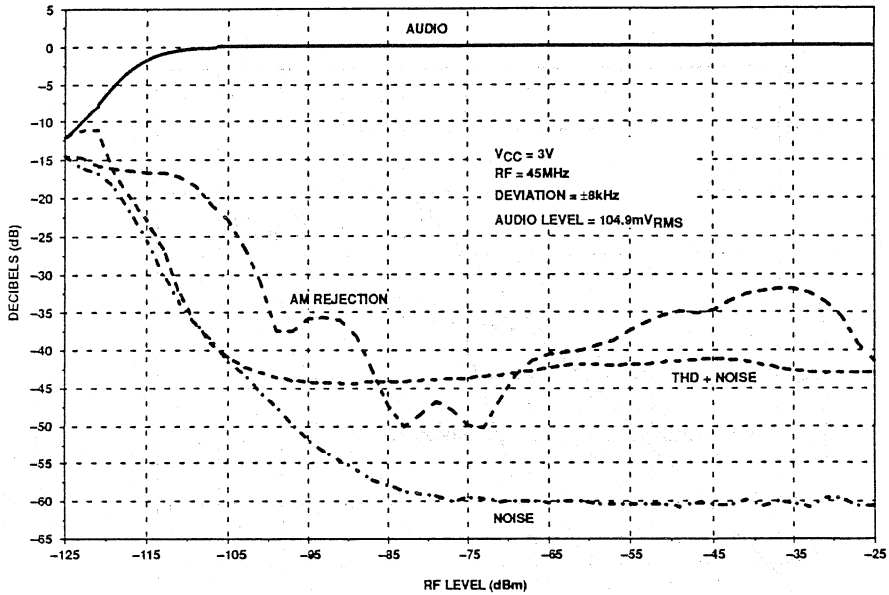


Figure 9. Sensitivity vs RF Level (–40°C)

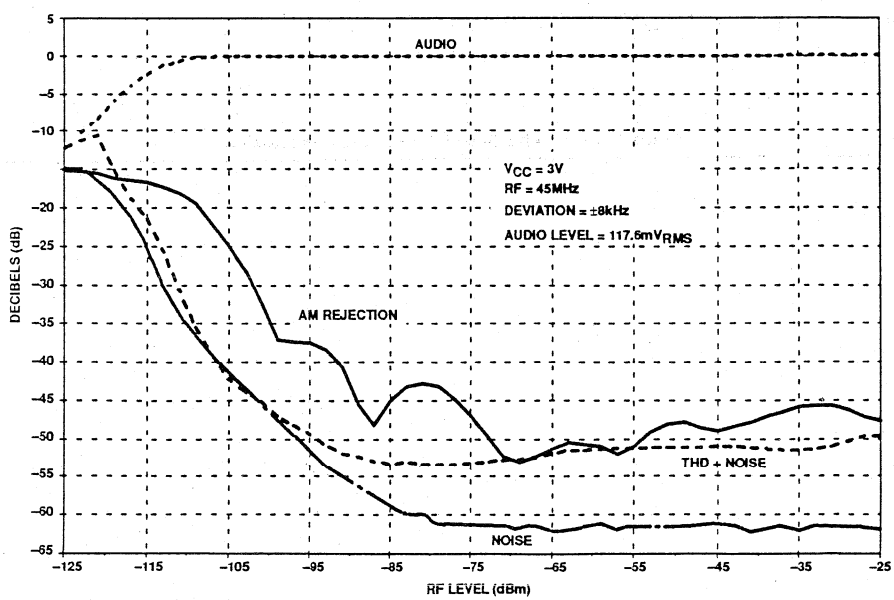


Figure 10. Sensitivity vs RF Level (+25°C)

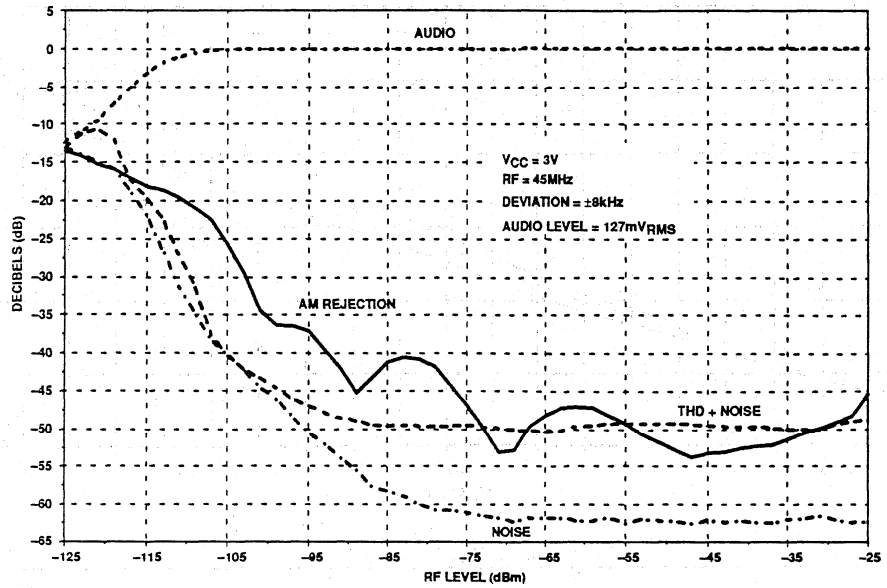


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

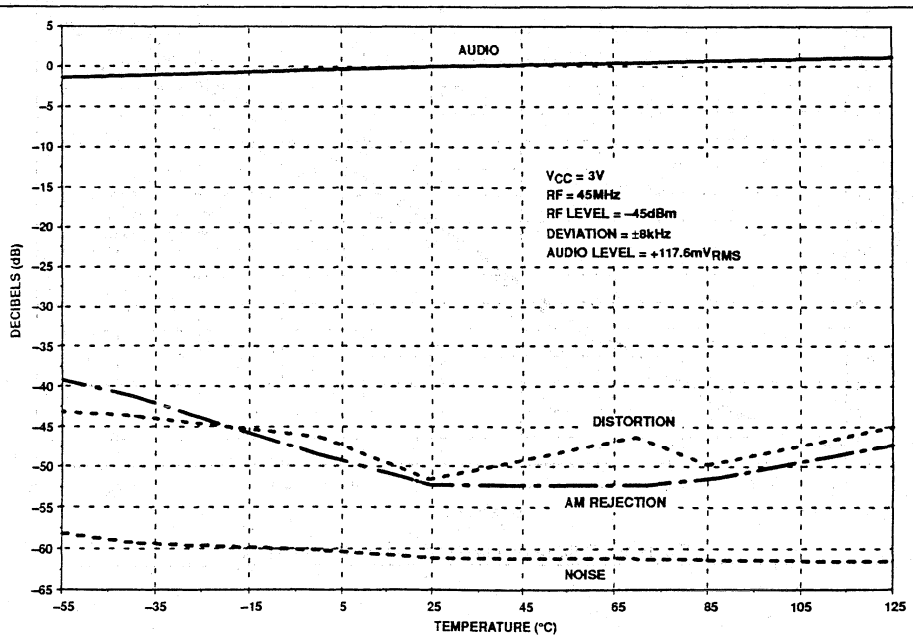


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

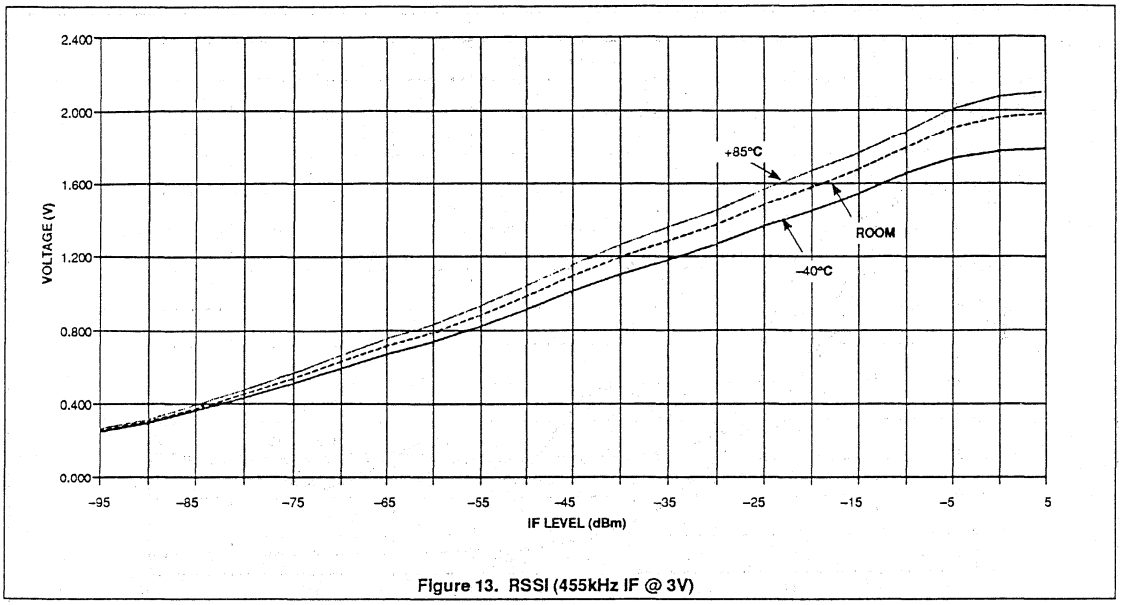


Figure 13. RSSI (455kHz IF @ 3V)

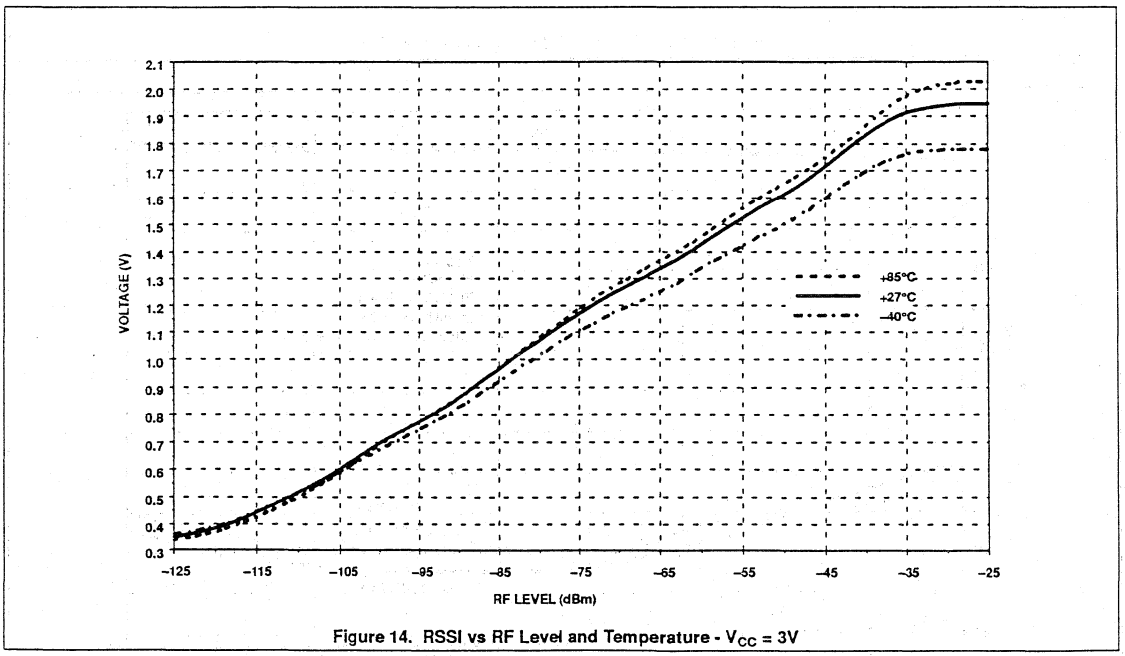


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

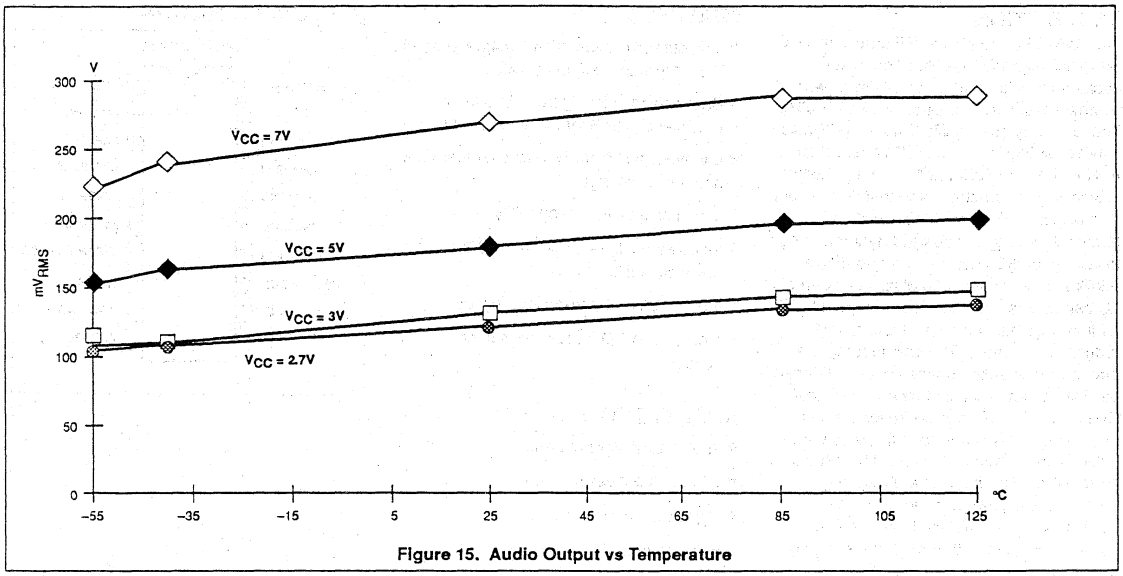


Figure 15. Audio Output vs Temperature

Low-voltage LNA, mixer and VCO-1GHz

SA620

DESCRIPTION

The SA620 is a combined RF amplifier, VCO with tracking bandpass filter and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 1.6dB noise figure at 900MHz with 11.5dB gain and an IP3 intercept of -3dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has an 9dB noise figure and IP3 of –6dBm at the input at 900MHz. An external LO can be used in place of the internal VCO for improved mixer input IP3 and a 3mA reduction in current. The chip incorporates a through-mode option so the RF amplifier can be disabled and replaced by an attenuator (S_{21} = –7.5dB). This is useful for improving the overall dynamic range of the receiver when in an overload situation. The nominal current drawn from a single 3V supply is 10.4mA and 7.2mA in the thru-mode. Additionally, the VCO and Mixer can be powered down to further reduce the supply current to 1.2mA.

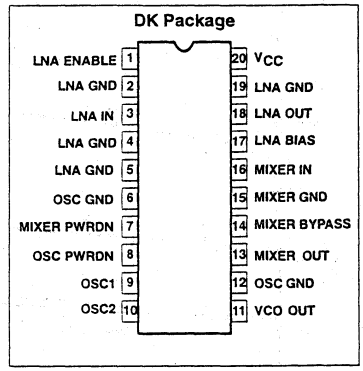
FEATURES

- Low current consumption: 10.4mA nominal, 7.2mA with thru-mode activated
- Outstanding noise figure: 1.6dB for the amplifier and 9dB for the mixer at 900MHz
- Excellent gain stability versus temperature and supply voltage
- Switchable overload capability
- Independent LNA, mixer and VCO power down capability
- Internal VCO automatic leveling loop
- Monotonic VCO frequency vs control voltage

APPLICATIONS

- 900MHz cellular front-end
- 900MHz cordless front-end
- Spread spectrum receivers
- RF data links
- UHF frequency conversion
- Portable radio

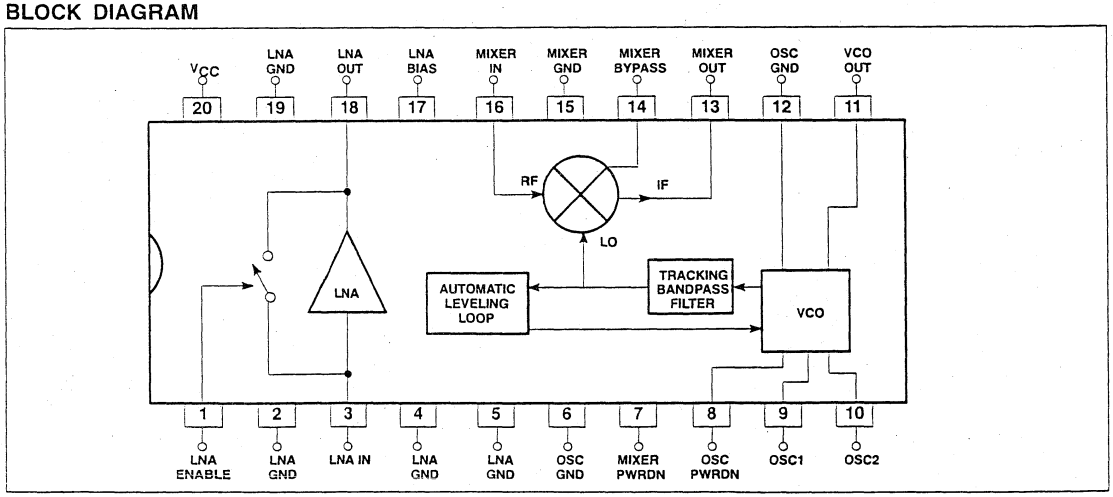
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount, SSOP)	-40 to +85°C	SA620DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}: 20-Pin SSOP = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current	LNA enable input high		10.4		mA
		LNA enable input low		7.2		mA
		VCO power-down input low		7.4		mA
		Mixer power-down input low		7.4		mA
		Full chip power-down		1.2		mA
V_T	Enable logic threshold voltage[NO TAG]		1.2	1.5	1.8	V
V_{IH}	Logic 1 level	RF amp on	2.0		V_{CC}	V
V_{IL}	Logic 0 level	RF amp off	–0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	µA
V_{LNA-IN}	LNA input bias voltage	Enable = 2.4V		0.78		V
$V_{LNA-OUT}$	LNA output bias voltage	Enable = 2.4V		2.1		V
V_B	LNA bias voltage	Enable = 2.4V		2.1		V
V_{MX-IN}	Mixer RF input bias voltage			0.94		V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the SA620 LNA.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; Enable = +3V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			-3σ	TYP	+3σ	
S_{21}	Amplifier gain	900MHz	10	11.5	13	dB
S_{21}	Amplifier gain in through mode	Enable = 0.4V, 900MHz	-9	-7.5	-6	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity in pwr-dwn mode	900MHz		-0.014		dB/°C
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled	900MHz		0.003		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz		0.01		dB/MHz
S_{12}	Amplifier reverse isolation	900MHz		-20		dB
S_{11}	Amplifier input match[1]	900MHz		-10		dB
S_{22}	Amplifier output match[1]	900MHz		-12		dB
P_{-1dB}	Amplifier input 1dB gain compression	900MHz		-16		dBm
IP3	Amplifier input third order intercept	900MHz	-4.5	-3	-1.5	dBm
NF	Amplifier noise figure	900MHz	1.3	1.6	1.9	dB
t_{ON}	Amplifier turn-on time (Enable Lo Hi)	See Figure 1		50		µs
t_{OFF}	Amplifier turn-off time (Enable Hi Lo)	See Figure 1		5		µs
VG_C	Mixer voltage conversion gain: $R_P = R_L = 1k\Omega$,	f_S = 0.9GHz, f_{LO} = 0.8GHz, f_{IF} = 100MHz	14.5	16	17.5	dB
PG_C	Mixer power conversion gain: $R_P = R_L = 1k\Omega$,	f_S = 0.9GHz, f_{LO} = 0.8GHz, f_{IF} = 100MHz	1.5	3	4.5	dB
S_{11M}	Mixer input match[1]	900MHz		-10		dB
NF_M	Mixer SSB noise figure	900MHz	7.5	9	10.5	dB
P_{-1dB}	Mixer input 1dB gain compression	900MHz		-13		dBm
$IP3_M$	Mixer input third order intercept	f_2–f_1 = 1MHz, 900MHz	-7.5	-6	-4.5	dBm
IP_{2INT}	Mixer input second order intercept	900MHz		12		dBm
P_{RFM-IF}	Mixer RF feedthrough	900MHz		-20		dB
P_{LO-IF}	LO feedthrough to IF	900MHz		-25		dBm
P_{LO-RFM}	LO to mixer input feedthrough	900MHz		-30		dBm
P_{LO-RF}	LO to LNA input feedthrough	900MHz		-45		dBm
P_{VCO}	VCO buffer out	900MHz		-16		dBm
	VCO frequency range		300 (min)		1200 (max)	MHz
	VCO phase noise	Offset = 60kHz		-105		dBc/Hz

NOTE:
1. Simple L/C elements are needed to achieve specified return loss.

Low-voltage LNA, mixer and VCO-1GHz SA620

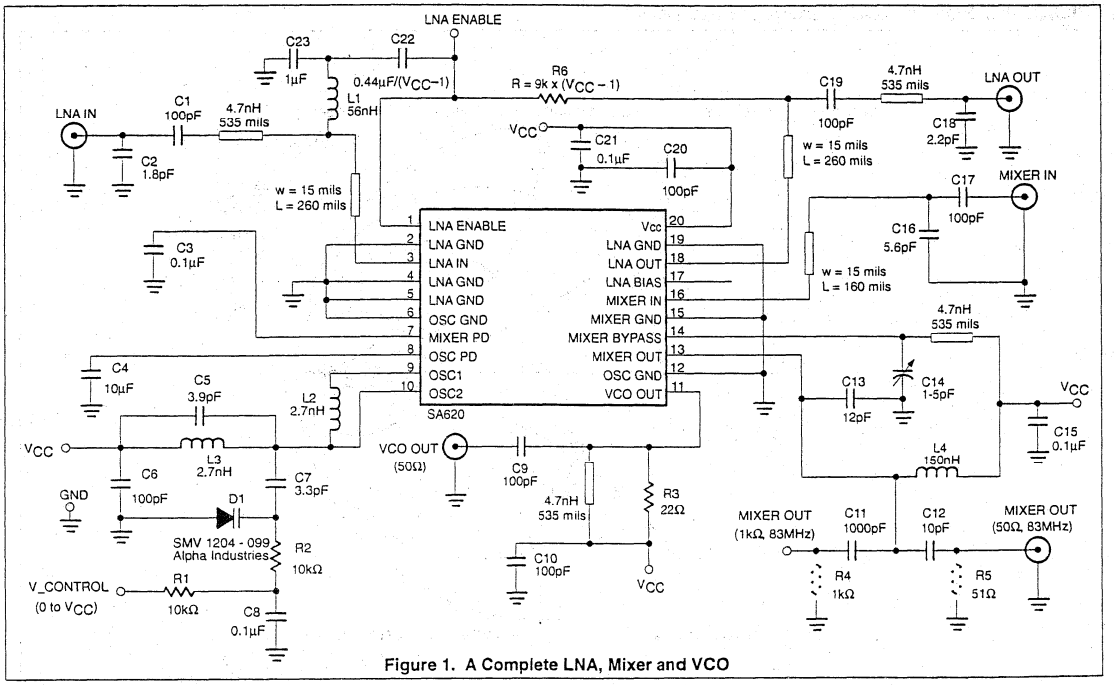


Figure 1. A Complete LNA, Mixer and VCO

CIRCUIT TECHNOLOGY

LNA

Impedance Match: Intrinsic return loss at the input and output ports is 7dB and 9dB, respectively. With no external matching, the associated LNA gain is ≈10dB and the noise figure is ≈1.4dB. However, the return loss can be improved at 900MHz using suggested L/C elements (Figure NO TAG) as the LNA is unconditionally stable.

Noise Match: The LNA achieves 1.6dB noise figure at 900MHz when S_{11} = -10dB. Further improvements in S_{11} will slightly increase the NF and S_{21}.

Thru-Mode: A series switch can be activated to feed RF signals from LNA input to output with an attenuator (S_{21} = –7.5dB). As a result, the power handling is greatly improved and current consumption is decreased by 3.2mA as well. However, if this mode is not required, C23 and R6 can be deleted.

Temperature Compensation: The LNA has a built-in temperature compensation scheme to reduce the gain drift to 0.003dB/°C from –40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 3V to 5V.

Mixer

Input Match: The mixer is configured for maximum gain and best noise figure. The user needs to supply L/C elements to achieve this performance.

Mixer Bypass: To optimize the IP3 of the mixer input, one must adjust the value of C14 for the given board layout. The value typically lies between 1 and 5pF. Once a value if selected, a fixed capacitor can be used. Further improvements in mixer IP3 can be achieved by inserting a resistive loss at the mixer input, at the expense of system gain and noise figure.

Tracking Bandpass Filter: At the LO input port of the mixer there is a second-order bandpass filter (approx. 50MHz bandwidth) which will track the VCO center frequency. The result is the elimination of low frequency noise injected into the mixer LO port without the need for an external LO filter.

Power Down: The mixer can be disabled by connecting Pin 7 to ground. If a Schottky diode is connected between Pin 1 (cathode) and Pin 7 (anode), the LNA disable signal will control both LNA and mixer simultaneously When the mixer is disabled, 3mA is saved.

Test Port: Resistor R5 can be substituted with an external test port of 50Ω input impedance. Since R5 and MIXER OUT have the same output power, the result is a direct power gain measurement.

VCO

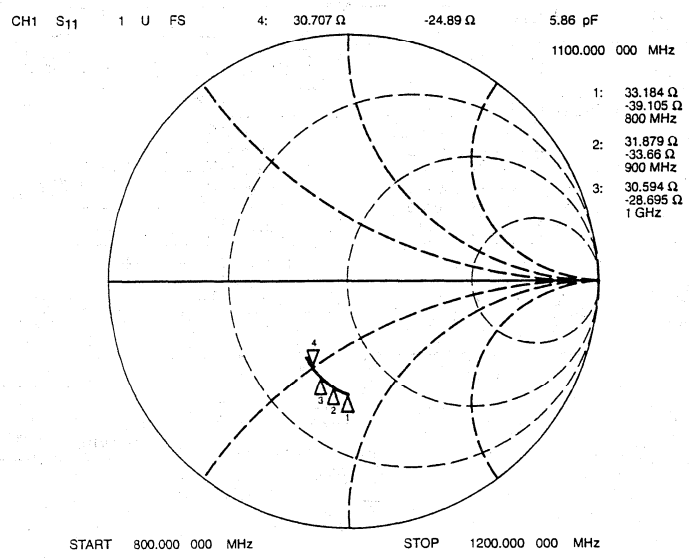
Automatic Leveling Loop: An on-chip detector and loop amplifier will adjust VCO bias current to regulate the VCO amplitude regardless of the Q-factor (>10) of the resonator and varactor diode. However, the real current reduction will not occur until the VCO frequency falls below 500MHz. For a typical resonator the steady-state current is 3mA at 800MHz.

Buffered VCO Output: The VCO OUT (Pin 11) signal can drive an external prescaler directly (see also the Philips SA7025 low voltage, fractional-N synthesizer). The extracted signal levels need to be limited to –16dBm or less to maintain mixer IIP3.

Phase Noise: If close-in phase noise is not critical, or if an external synthesizer is used, C4 (Pin 8) can be decreased to a lower value.

Power-Down: The VCO can be disabled by connecting Pin 8 to ground. If a Schottky diode is connected between Pin 1 (cathode) and Pin 8 (anode), the LNA disable signal will control both LNA and VCO simultaneously. When the VCO is disabled, 3mA is saved.

TYPICAL PERFORMANCE CHARACTERISTICS



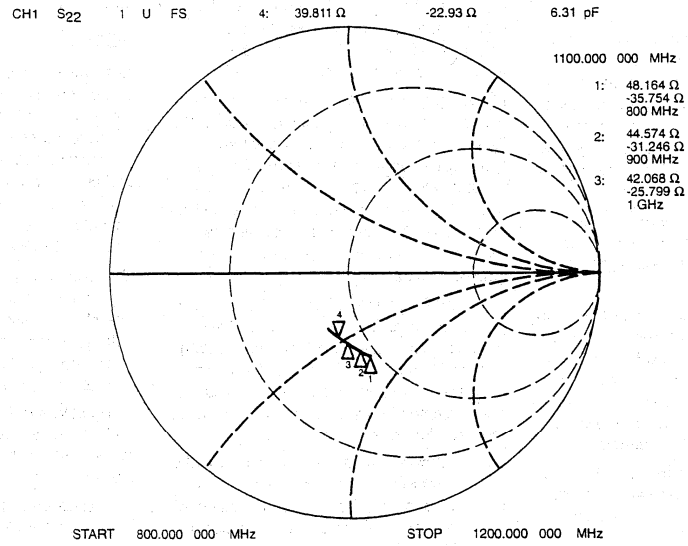
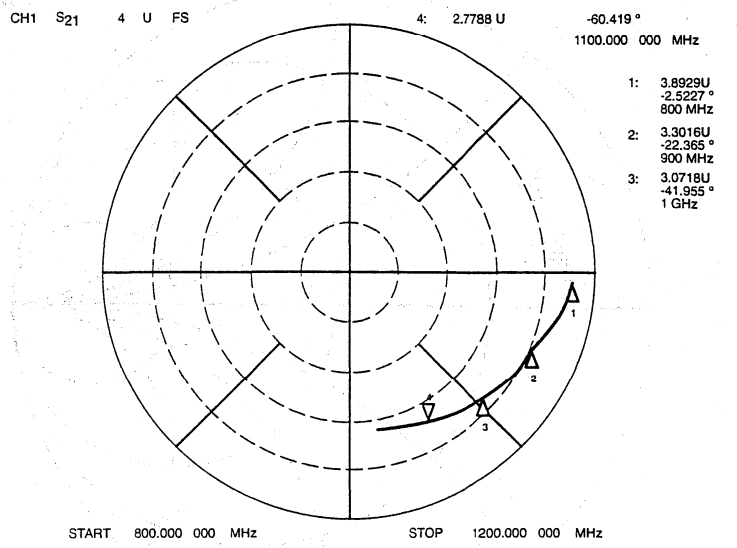


Figure 2. LNA Input and Output Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



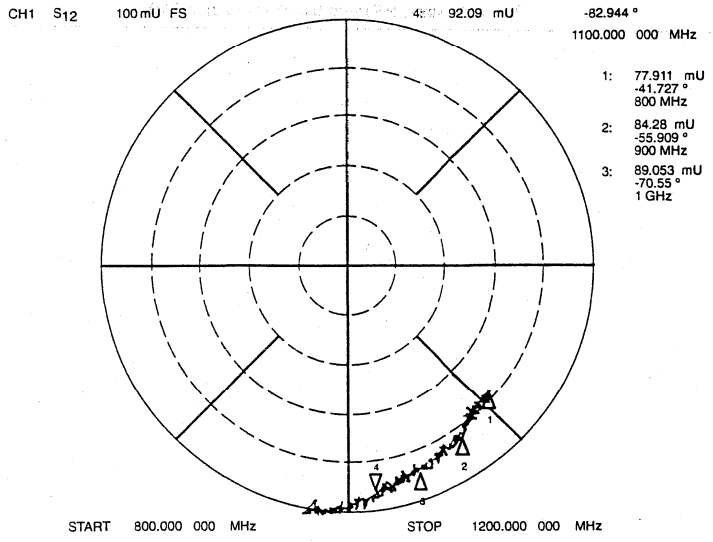


Figure 3. LNA Transmission and Isolation Characteristics (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

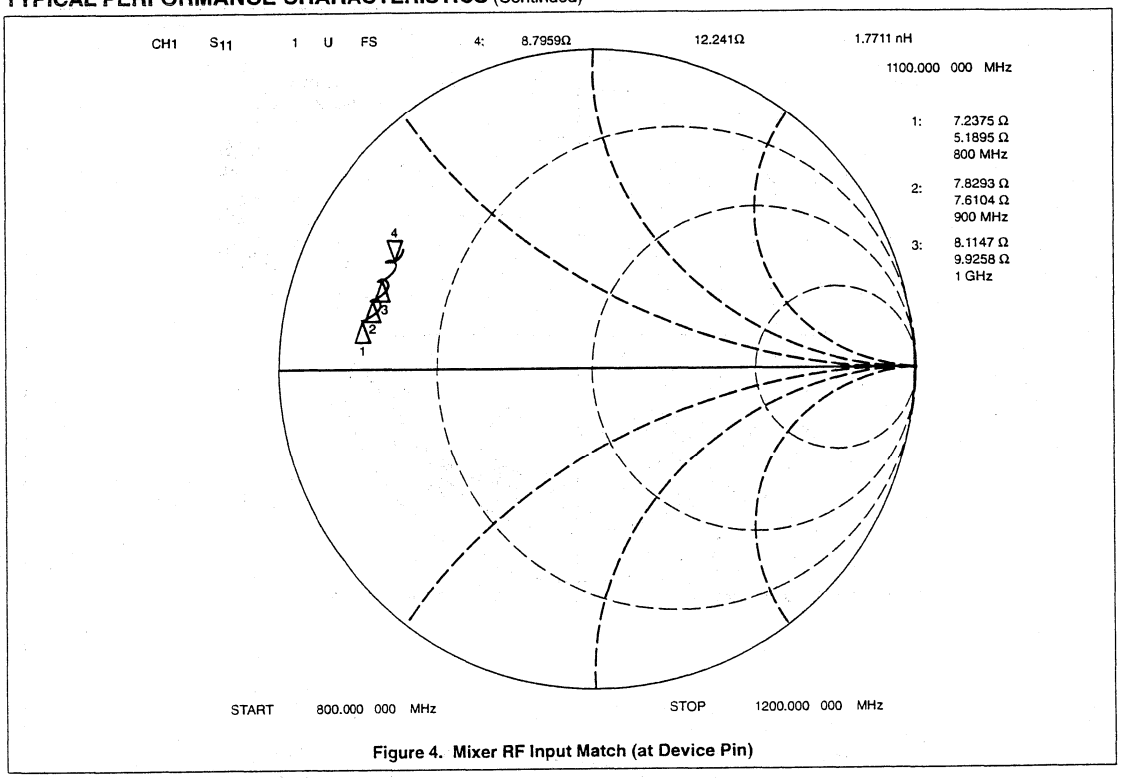
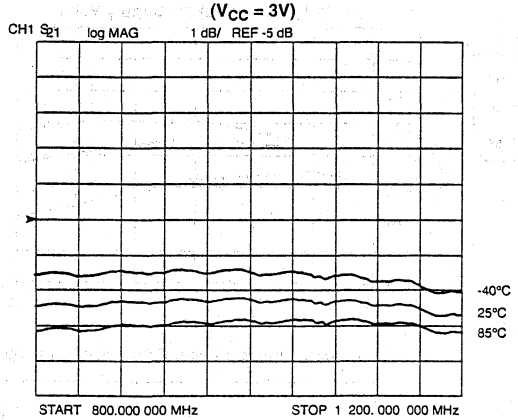


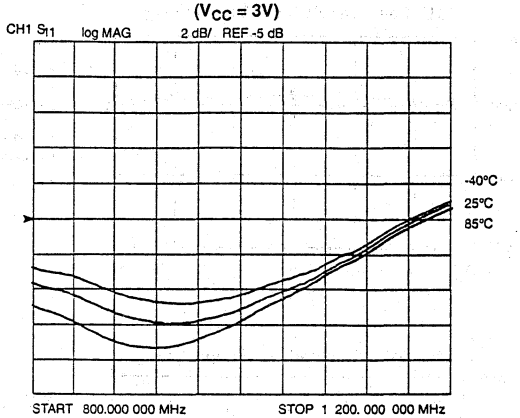
Figure 4. Mixer RF Input Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

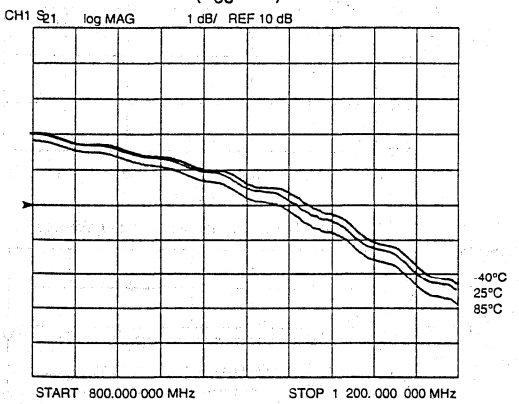
LNA Gain (S_{21}) In Through Mode vs. Frequency (V_{CC} = 3V)



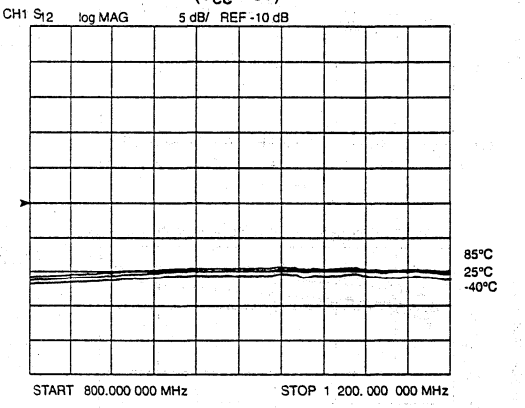
Mixer RF Input Match vs. Frequency (V_{CC} = 3V)



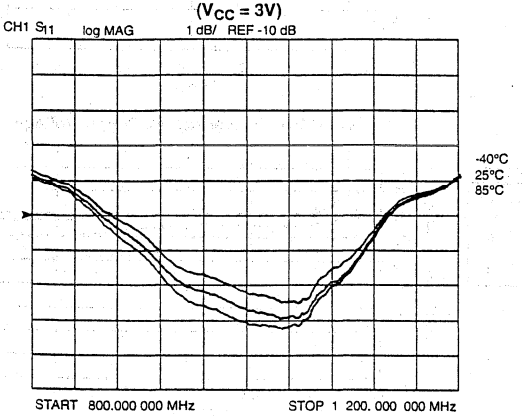
LNA Gain (S_{21}) vs. Frequency (V_{CC} = 3V)



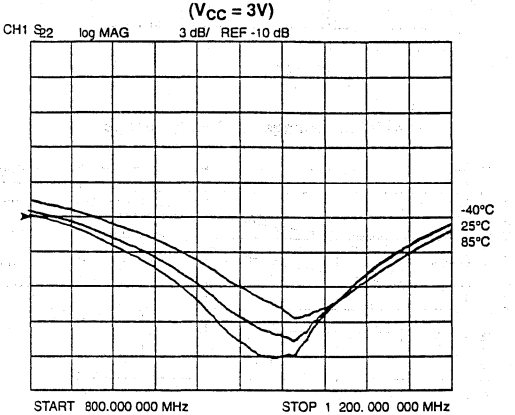
LNA Isolation (S_{12}) vs. Frequency (V_{CC} = 3V)



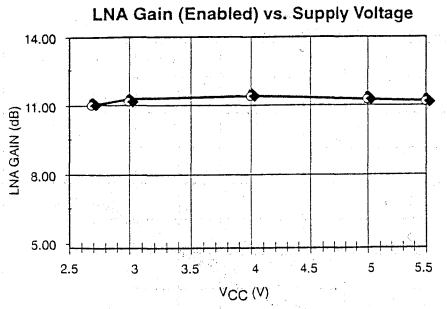
LNA Input Match (S_{11}) vs. Frequency (V_{CC} = 3V)

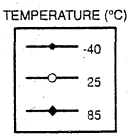


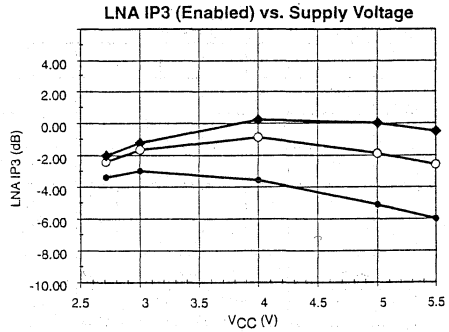
LNA Output Match (S_{22}) vs. Frequency (V_{CC} = 3V)

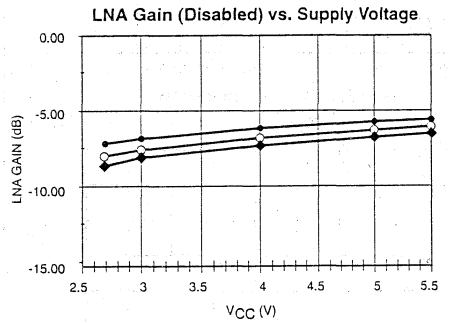


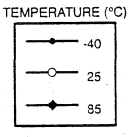
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

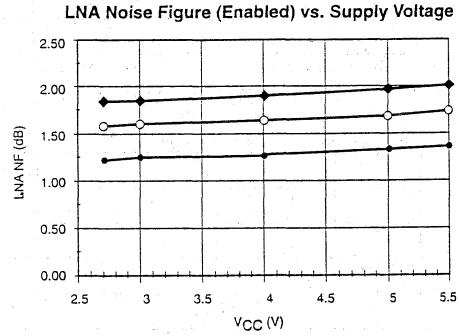


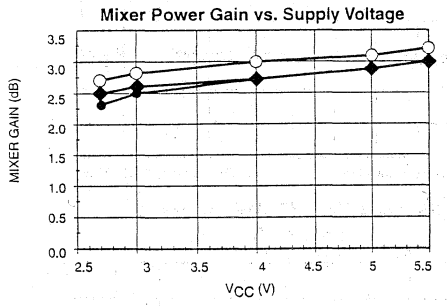


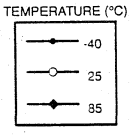


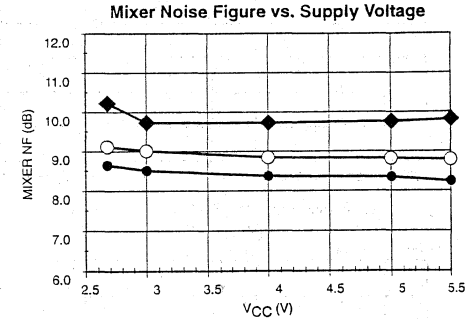


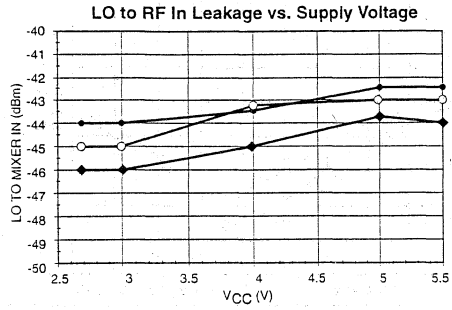


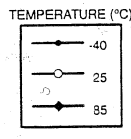


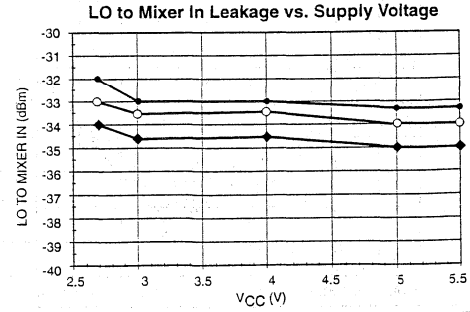




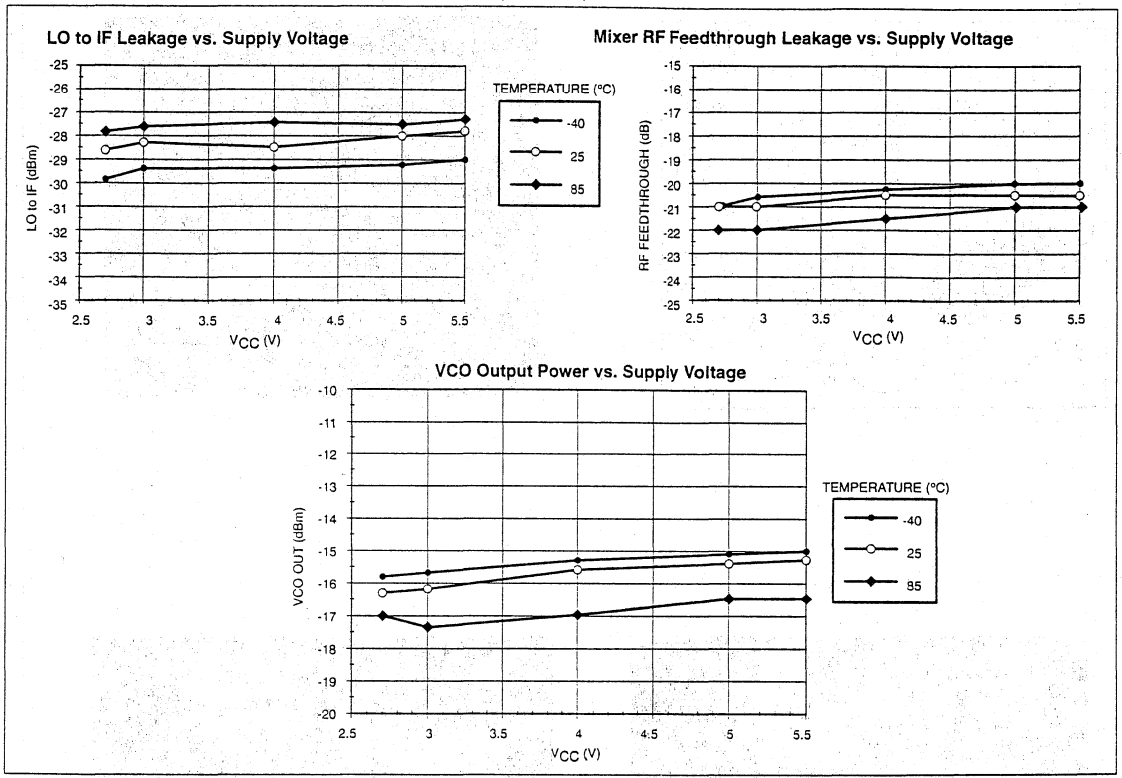


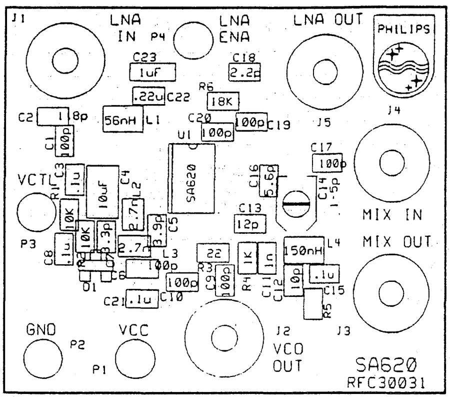


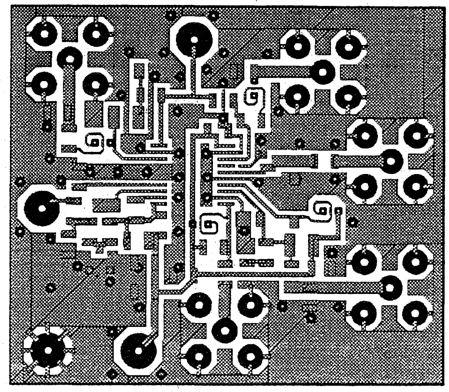


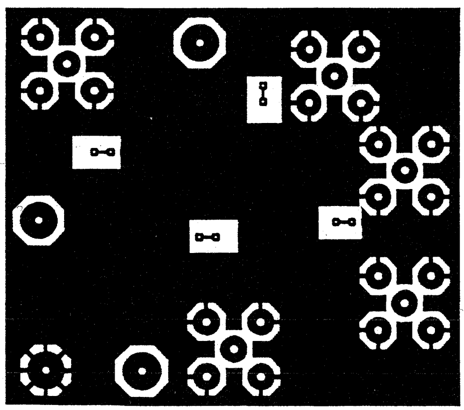


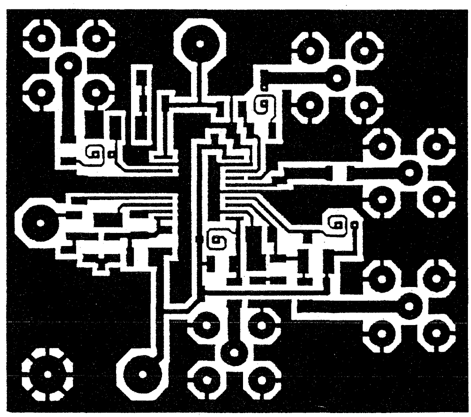
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)




J1
LNA IN
P4
LNA ENA
LNA OUT
PHILIPS
C23
1uF
C18
2.2p
R6
18K
.22u
C22
C2
18p
56nH
L1
C20
100p
C19
U1
J5
J4
C1
100p
C17
100p
VCTL
C3
.1u
10uF
C4
L2
SA620
C16
5.6p
C14
1-5p
R1
10K
C13
12p
MIX IN
MIX OUT
P3
C8
.1u
2.7n
3.9p
C5
3.3p
L3
22
R3
1K
1n
150nH
L4
100p
C10
C9
R4
C11
C12
10p
.1u
C15
R5
D1
C21
GND
P2
VCC
P1
J2
VCO OUT
J3
SA620
RFC30031







Low-voltage high performance mixer FM IF system with high-speed RSSI

SA626

DESCRIPTION

The SA626 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, high speed logarithmic received signal strength indicator (RSSI), voltage regulator and audio and fast RSSI op amps. The SA626 is available in 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The SA626 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio and RSSI outputs have amplifiers. The RSSI output has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

SA626 incorporates a power down mode which powers down the device when Pin 8 is low. Power down logic levels are CMOS and TTL compatible with high input impedance.

APPLICATIONS

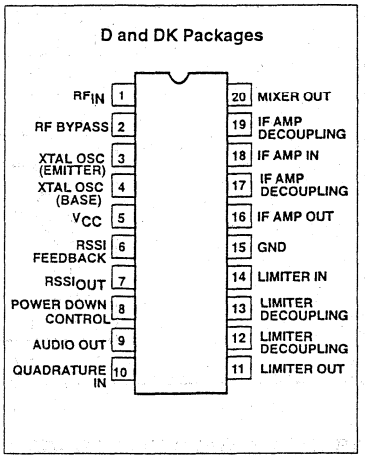
- Digital cordless telephones
- Digital cellular telephones
- Digital cellular base stations
- Portable high performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 6.5mA typ at 3V
- Power down mode (I_{CC} = 200µA)
- Mixer input to >500MHz
- Mixer conversion power gain of 11dB at 240MHz
- Mixer noise figure of 14dB at 240MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz, local oscillator can be injected)
- 92dB of IF Amp/Limiter power gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Audio output internal buffer
- RSSI output internal buffer
- Internal op amps with rail-to-rail outputs
- 10.7MHz filter matching (330Ω) reduces external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.54µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 240MHz and IF at 10.7MHz
- SA626 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

D and DK Packages



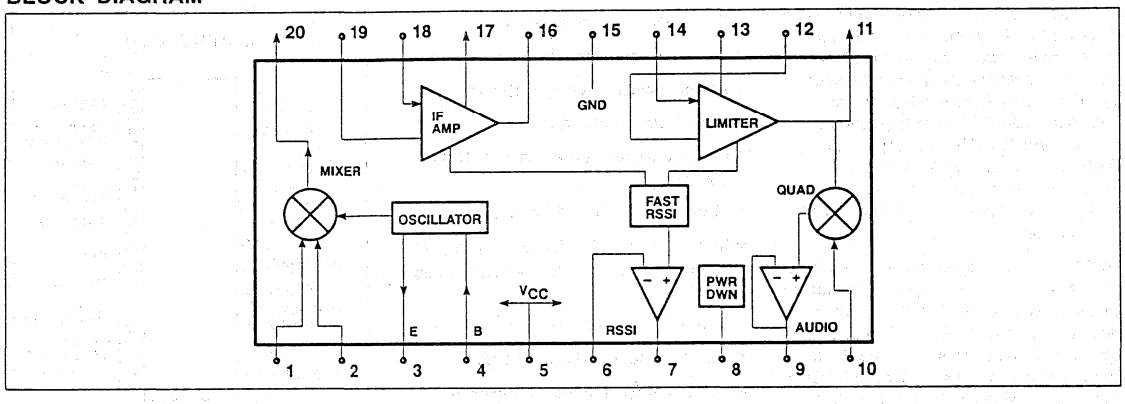
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA626D	0172D
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA626DK	1563

Low-voltage high performance mixer FM IF system with high-speed RSSI

SA626

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		0.3 to 7	V
V_{IN}	Voltage applied to any other pin		–0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range SA626		–40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

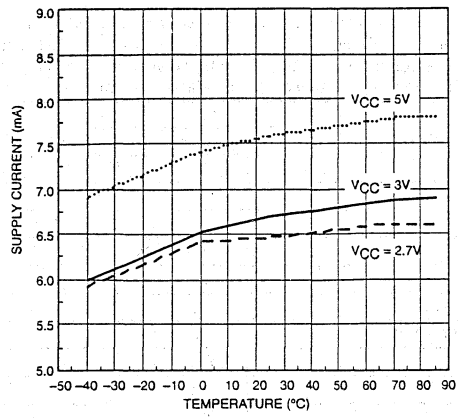
V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA626			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7	3.0	5.5	V
I_{CC}	DC current drain	Pin 8 = HIGH	5.5	6.5	7.5	mA
I_{CC}	Standby	Pin 8 = LOW		0.2	0.5	mA
	Input current	Pin 8 LOW	–10		10	µA
		Pin 8 HIGH	–10		10	µA
	Input level	Pin 8 LOW	0		0.3V_{CC}	V
		Pin 8 HIGH	0.7V_{CC}		V_{CC}	V
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

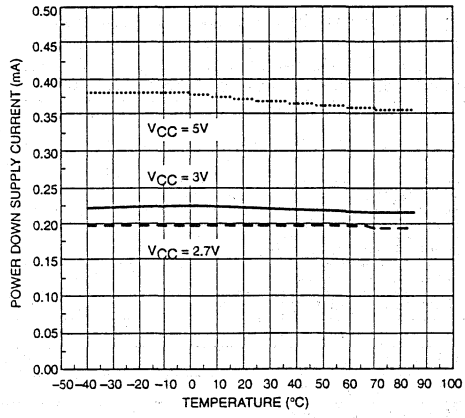
AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 240.05MHz + 14.5dBV RF input step-up; IF frequency = 10.7MHz; RF level = -68dBm; FM modulation = 1kHz with ±125kHz peak deviation. Audio output with C-message weighted filter and de-emphasis filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

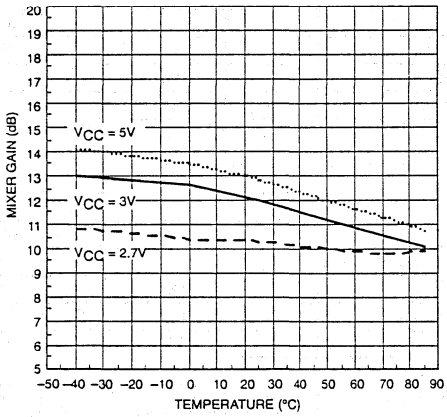
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA626			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 160mV$_{RMS}$)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	External oscillator (buffer)			500		MHz
	Noise figure at 240MHz			14		dB
	Third-order input intercept point	Matched f1=240.05; f2=240.35MHz		-16		dBm
	Conversion power gain	Matched 14.5dBV step-up	8	11	14	dB
	RF input resistance	Single-ended input		700		Ω
	RF input capacitance			3.5		pF
	Mixer output resistance	(Pin 20)		330		Ω
IF section						
	IF amp power gain			38		dB
	Limiter amp power gain			54		dB
	Input limiting -3dB	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		50		dB
	Audio level	Unity gain	120	160	200	mV$_{RMS}$
	Audio DC level	Pin 9, no signal		1.0		V
	SINAD sensitivity	IF level = -111dBm		16		dB
THD	Total harmonic distortion			-43	–38	dB
S/N	Signal-to-noise ratio	No modulation for noise		60		dB
	IF RSSI output with buffer	IF level = -118dBm		0.2	0.5	V
		IF level = -68dBm	0.3	0.6	1.0	V
		IF level = -10dBm	0.9	1.3	1.8	V
	IF RSSI output rise time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		1.2		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		1.1		µs
	IF RSSI output fall time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		2.0		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		7.3		µs
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance			330		Ω
	IF output impedance			330		Ω
	Limiter input impedance			330		Ω
	Limiter output impedance			300		Ω
	Limiter output level with no load			130		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	RF level = -10dBm		160		mV$_{RMS}$
	System RSSI output	RF level = -10dBm		1.4		V
	System SINAD	RF level = -106dBm		12		dB



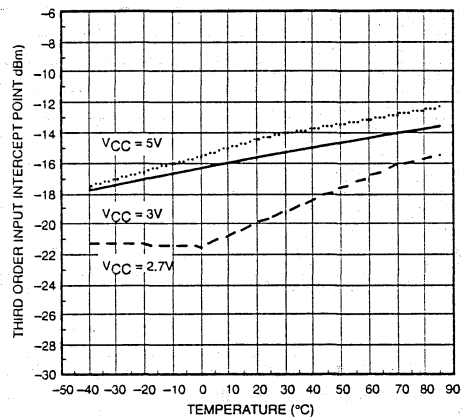
Supply Current vs Temperature and Supply Voltage



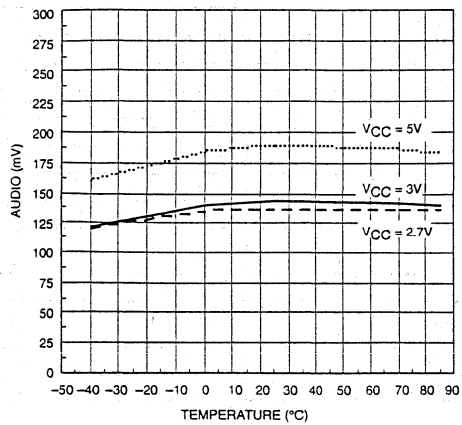
Power Down Supply Current vs Temperature and Supply Voltage



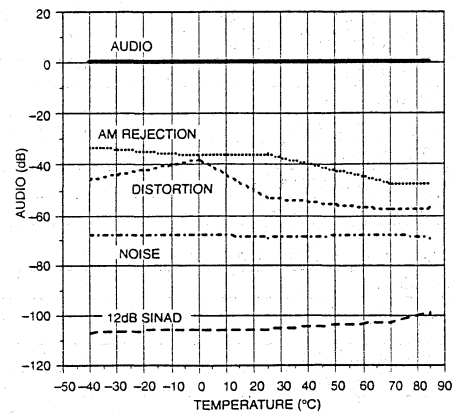
Mixer Power Gain vs Temperature and Supply Voltage



Third Order Input Intercept Point vs Temperature and Supply Voltage



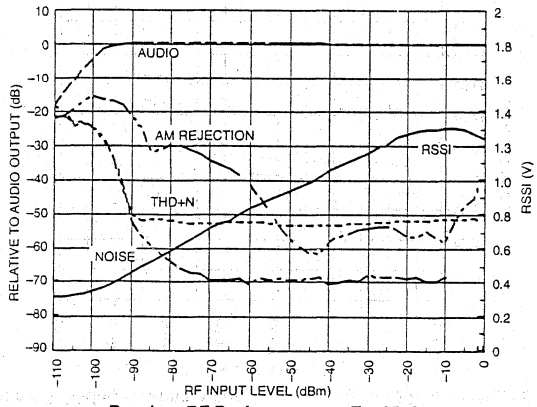
Audio Output Level vs. Temperature and Supply Voltage



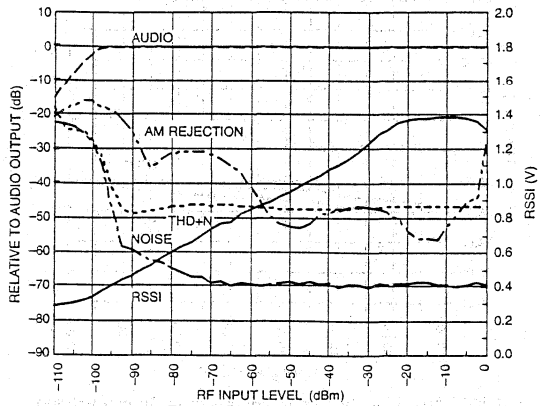
12dB SINAD and Relative Audio, THD, Noise and AM Rejection for VCC = 3V vs Temperature RF = 240MHz, Level = –68dBm, Deviation = 125kHz

Low-voltage high performance mixer FM IF system with high-speed RSSI

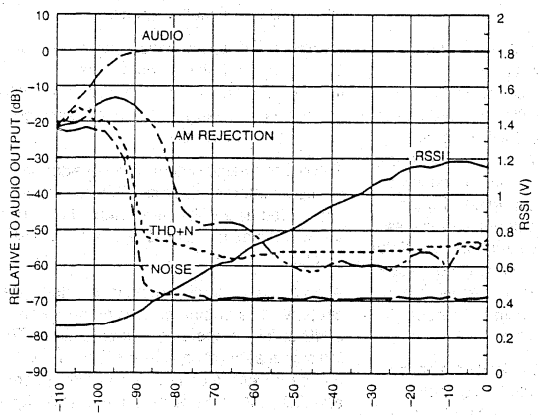
SA626



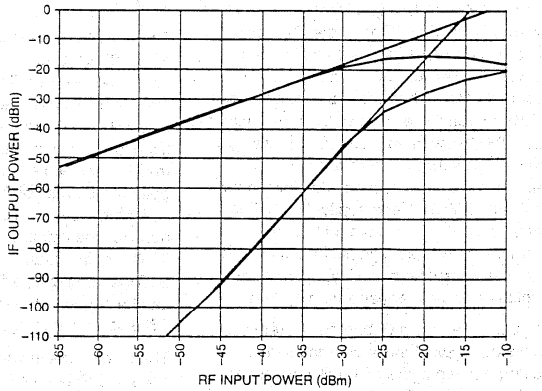
Receiver RF Performance — T = 25°C, Audio Level = 129mV$_{RMS}$



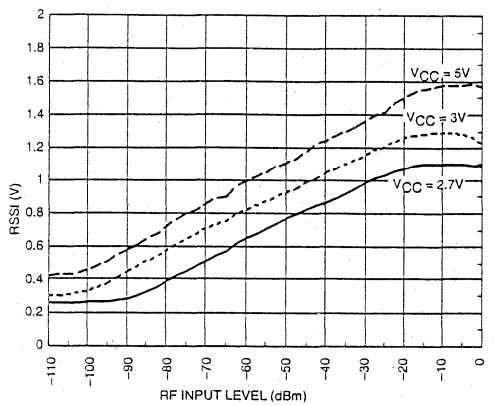
Receiver RF Performance — T = –40°C, Audio Level = 118mV$_{RMS}$



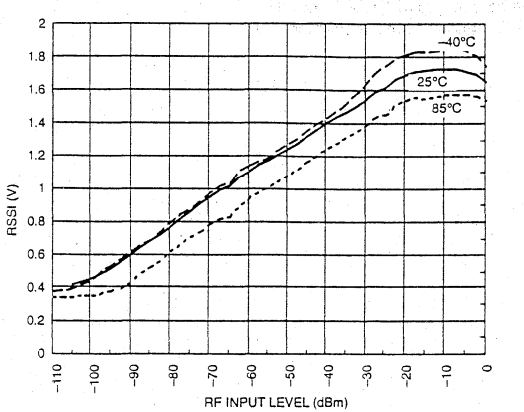
Receiver RF Performance – T = 85°C, Audio Level = 131mV$_{RMS}$



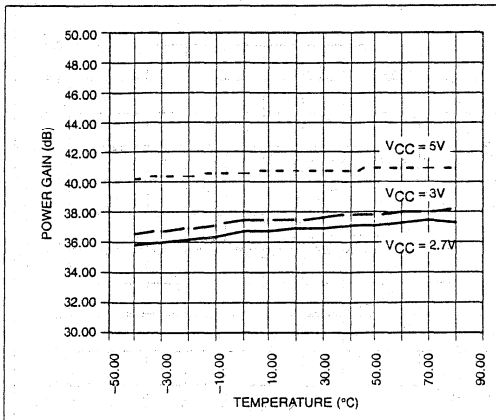
Mixer Third Order Intercept and Compression



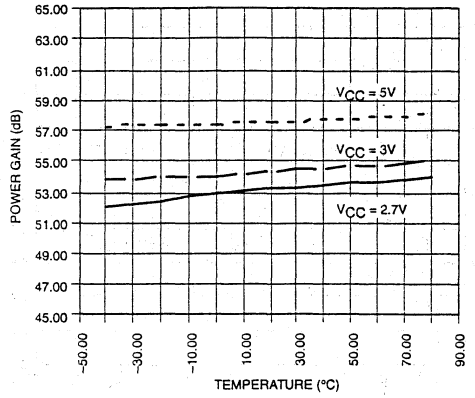
RSSI vs RF Input Level and Supply Voltage



RSSI vs RF Input Level and Temperature



SA626 IF Amplifier Gain vs Temperature vs Supply Voltage



SA626 Limiting Amplifier Gain vs Temperature vs Supply Voltage

CIRCUIT DESCRIPTION

The SA626 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 38dB of power gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 54dB of power gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 10.7MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as cordless and cellular hand-held phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 14dB, conversion power gain of 11dB, and input third-order intercept of -16dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 10.7MHz ceramic filter. The input resistance of the limiting IF amplifiers is also 330Ω. With most 10.7MHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 3dB insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 3dB insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

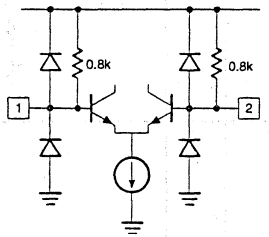
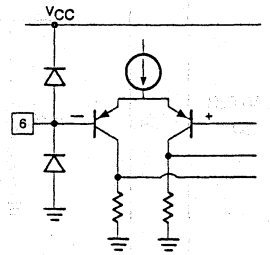
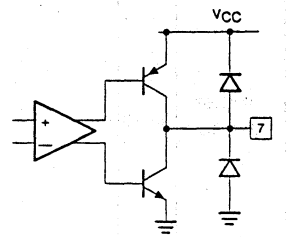
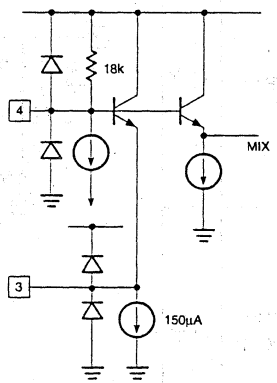
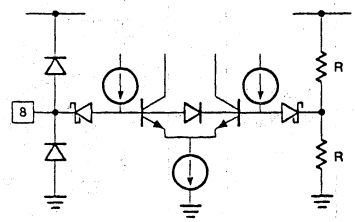
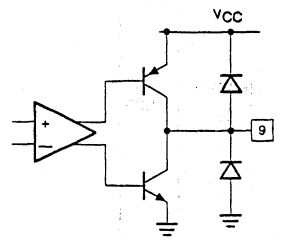
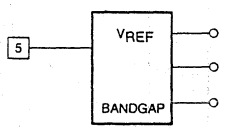
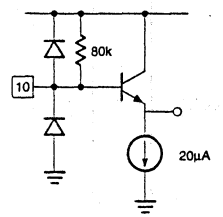
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a power gain of 92dB. For operation at intermediate frequency at 10.7MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

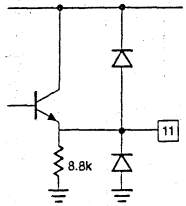
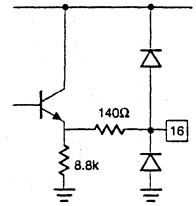
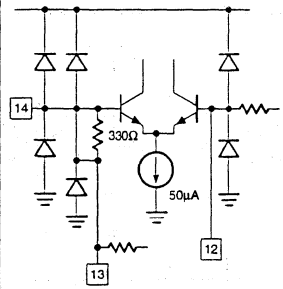
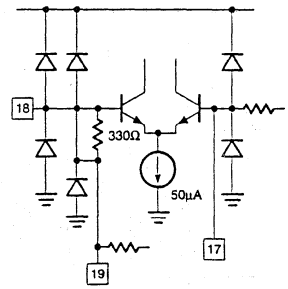
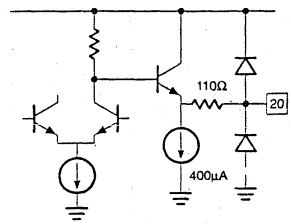
The demodulated output of the quadrature drives an internal op amp. This op amp is configured as a unity gain buffer. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

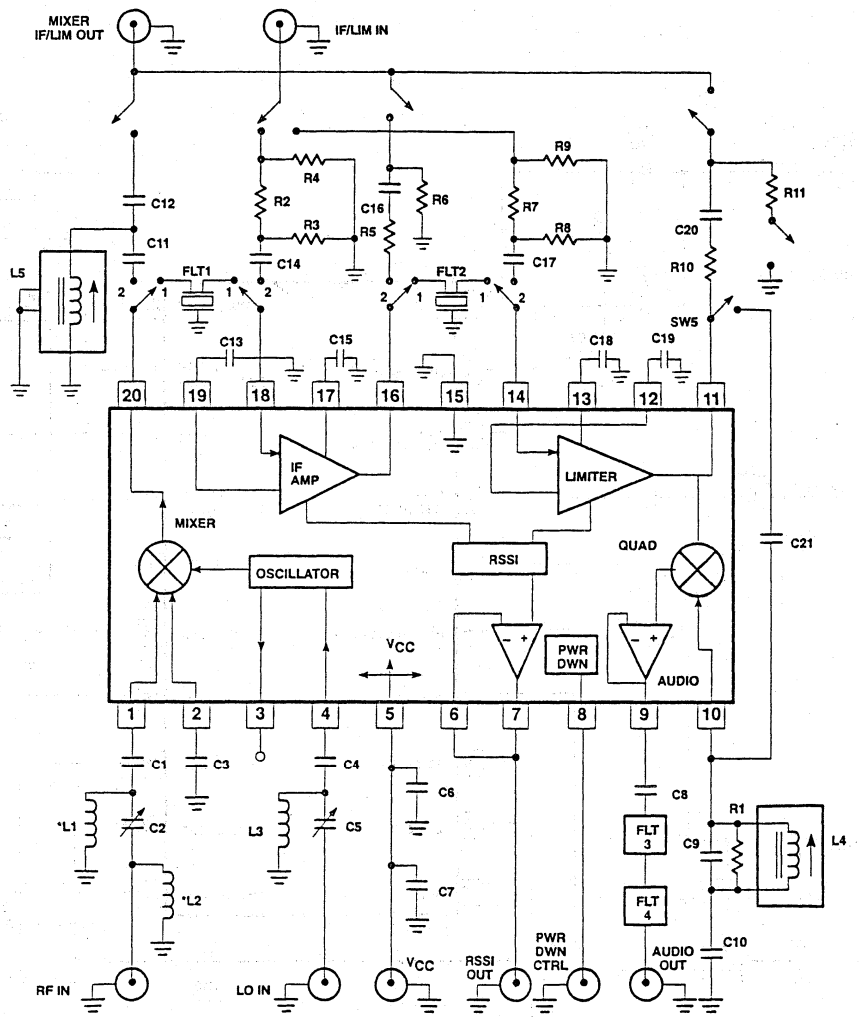
A log signal strength indicator completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone, and RCR-28 cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	+2.75	
4	XTAL OSC	+2.32		9	AUDIO OUT	+1.09	
5	V_{CC}	+3.00		10	QUAD. IN	+3.00	

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	LIMITER OUT	+1.35		16	IF AMP OUT	+1.22	
12	LIMITER DECOUP	+1.23		17	IF AMP DECOUP	+1.22	
13	LIMITER COUPLING	+1.23		18	IF AMP IN	+1.22	
14	LIMITER IN	+1.23		19	IF AMP DECOUP	+1.22	
15	GND	0		20	MIXER OUT	+1.03	



Automatic Test Circuit Component List

R1	8.2kΩ select	C1	0.1µF	C12	160pF select	L1	150nH select for input match
R2	6.42kΩ	C2	1–5pF select for input match	C13	1000pF	L2	22nH select for input match
R3	347.8Ω	C3	0.1µF	C14	0.1µF	L3	47nH select for input match
R4	49.9Ω	C4	0.1µF	C15	1000pF	L4	5.6µH select for input match
R5	1kΩ	C5	1–5pF select for input match	C16	0.1µF	L5	1.27–2.25µH select for mixer output match
R6	49.9Ω	C6	100pF	C17	0.1µF		
R7	6.42kΩ	*C7	6.8µF 10V	C18	1000pF	FLT1	10.7MHz (Murata SFE10.7MA5-A)
R8	347.8Ω	C8	1µF	C19	1000pF	FLT2	10.7MHz (Murata SFE10.7MA5-A)
R9	49.9Ω	C9	39pF select	C20	0.1µF	FLT3	"C" message weighted
R10	1kΩ	C10	0.1µF	C21	1pF	FLT4	Active de-emphasis
R11	49.9Ω	C11	0.1µF				

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA626 240.5MHz (RF) / 10.7MHz (IF) Test Circuit

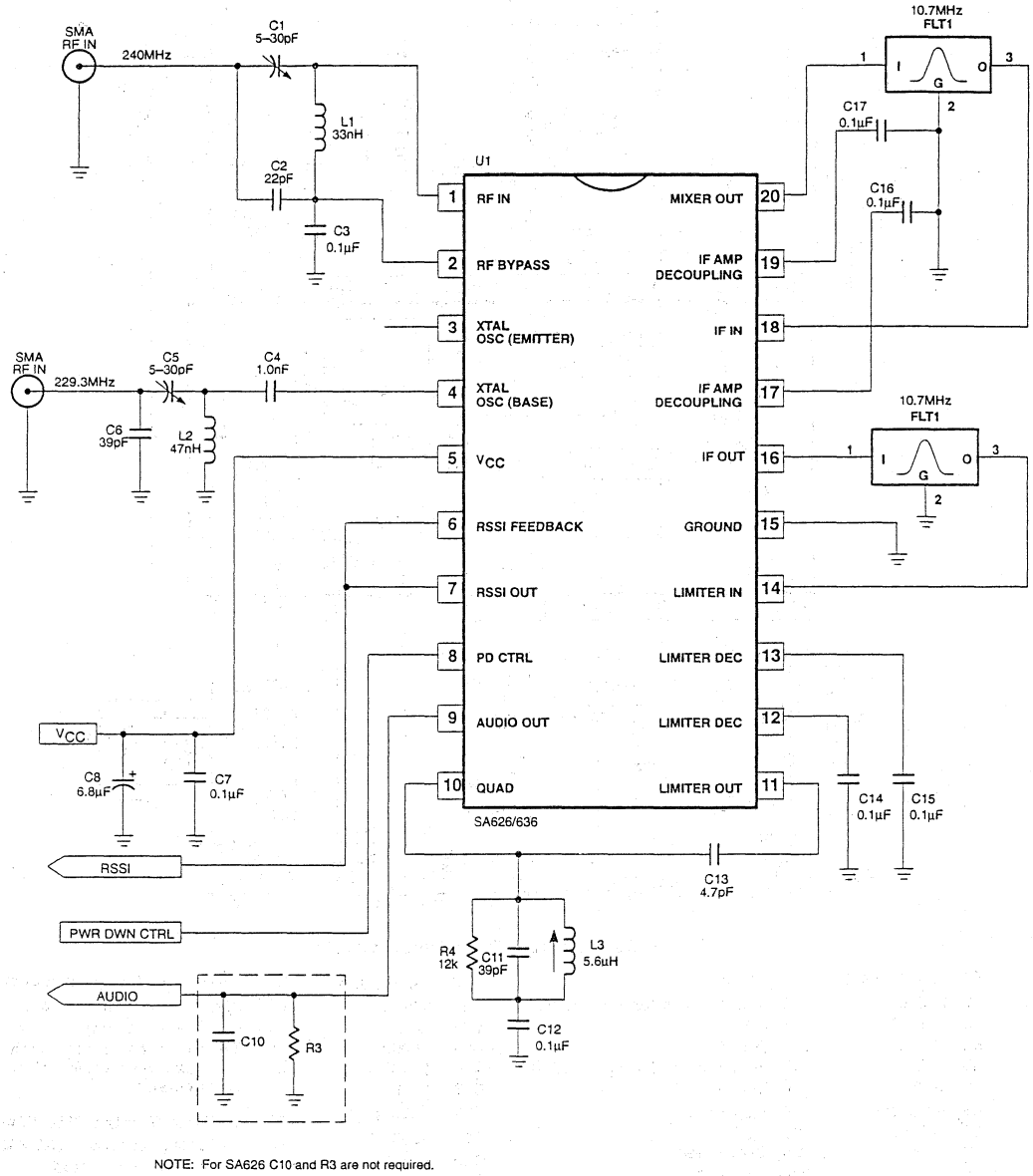


Figure 2. SA626 240MHz (RF) / 10.7MHz (IF) Application Circuit

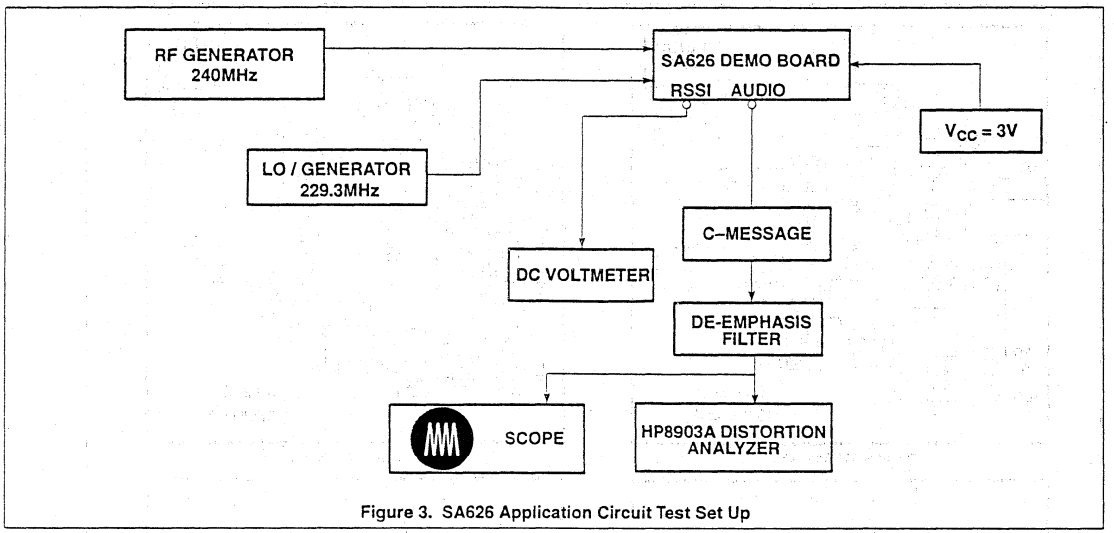
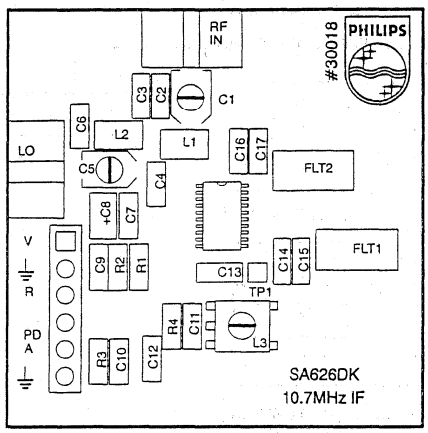


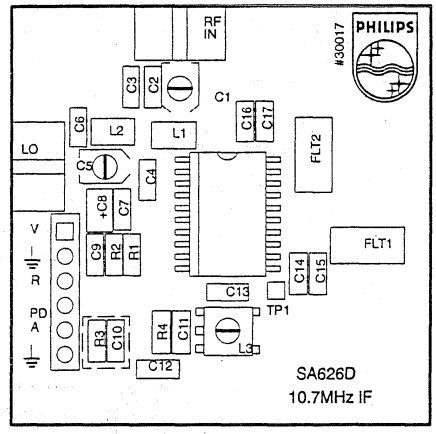
Figure 3. SA626 Application Circuit Test Set Up

NOTES:

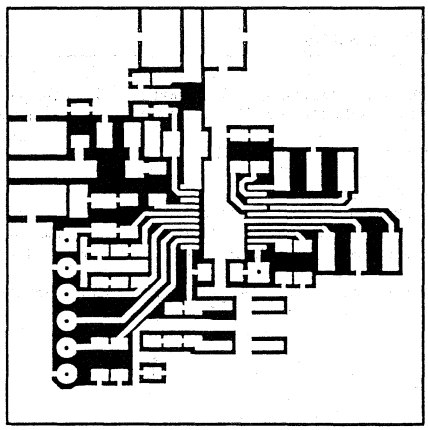
1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP8903A analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filter can be SFE10.7MA5-A made by Murata which has 280kHz IF bandwidth.
3. RF generator: Set your RF generator at 240.000MHz, use a 1kHz modulation frequency and a 125kHz deviation.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.54µV or –112dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1µF bypass capacitor on the supply pin improves sensitivity.



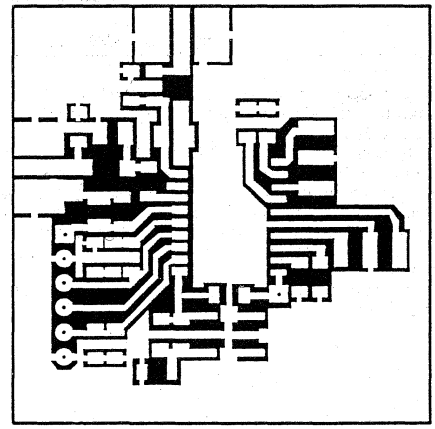
TOP SILK SCREEN (SSOP)



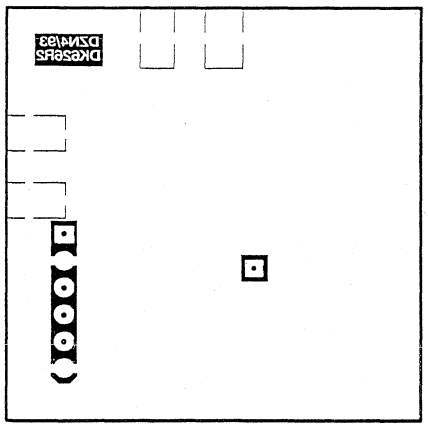
TOP SILK SCREEN (SOL)



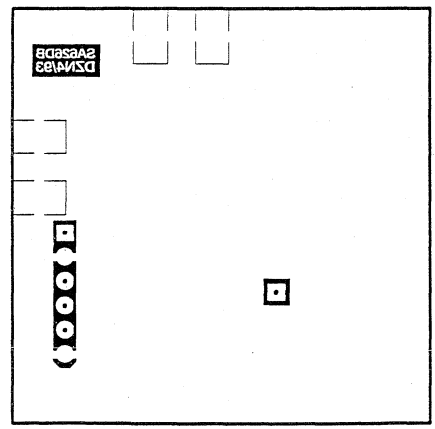
TOP VIEW (SSOP)



TOP VIEW (SOL)



BOTTOM VIEW (SSOP)



BOTTOM VIEW (SOL)

Figure 4. SA626 Demoboard Layout (Not Actual Size)

Low-voltage high performance mixer FM IF system with high-speed RSSI

SA636

DESCRIPTION

The SA636 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator, wideband data output and fast RSSI op amps. The SA636 is available in 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The SA636 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The data output has a minimum bandwidth of 600kHz. This is designed to demodulate wideband data. The RSSI output is amplified. The RSSI output has access to the feedback pin. This enables the designer to adjust the level of the outputs or add filtering.

SA636 incorporates a power down mode which powers down the device when Pin 8 is low. Power down logic levels are CMOS and TTL compatible with high input impedance.

APPLICATIONS

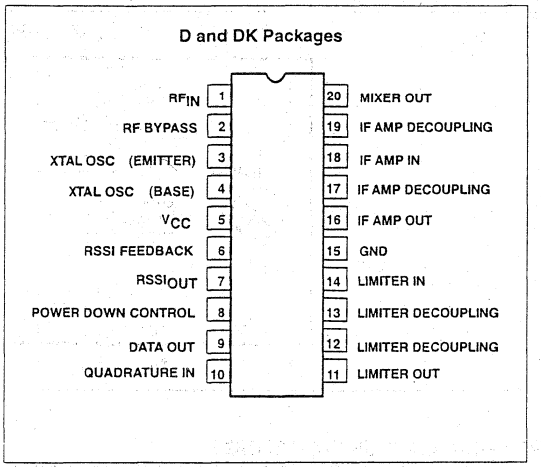
- DECT (Digital European Cordless Telephone)
- Digital cordless telephones
- Digital cellular telephones
- Portable high performance communications receivers
- Single conversion VHF/UHF receivers
- FSK and ASK data receivers
- Wireless LANs

FEATURES

- Wideband data output (600kHz min.)
- Fast RSSI rise and fall times
- Low power consumption: 6.5mA typ at 3V
- Mixer input to >500MHz
- Mixer conversion power gain of 11dB at 240MHz
- Mixer noise figure of 12dB at 240MHz

PIN CONFIGURATION

D and DK Packages



- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 92dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.54μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 240MHz and IF at 10.7MHz
- ESD hardened
- 10.7MHz filter matching (330Ω)
- Power down mode (I_{CC} = 200μA)

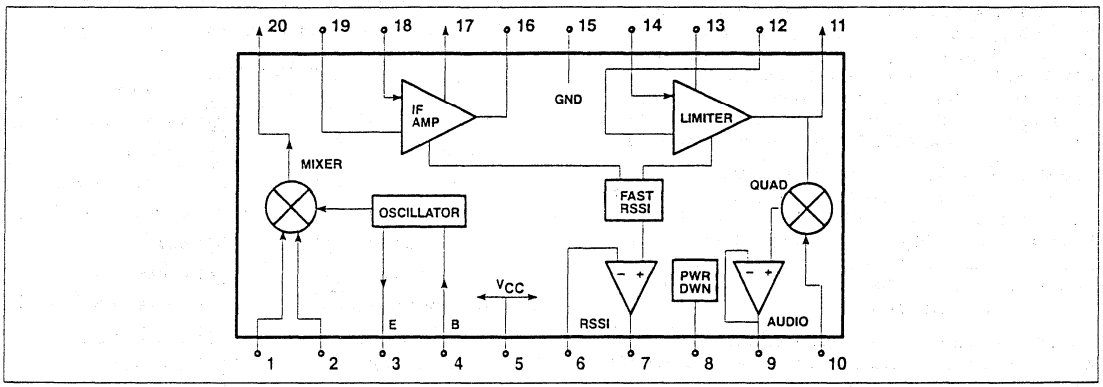
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA636D	0172D
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA636DK	1563–

Low-voltage high performance mixer FM IF system with high-speed RSSI

SA636

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	0.3 to 7	V
V_{IN}	Voltage applied to any other pin	−0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA636	−40 to +85	°C

NOTE: θ_{JA}, Thermal impedance D package 90°C/W
DK package 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

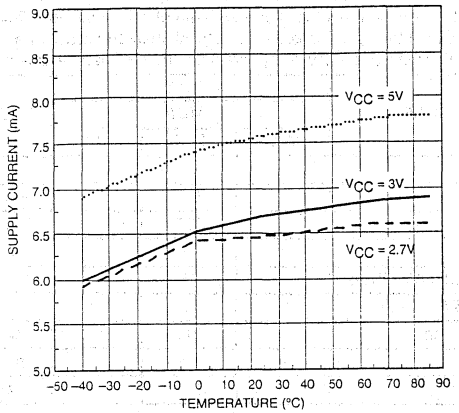
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA636			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7	3.0	5.5	V
I_{CC}	DC current drain	Pin 8 = HIGH	5.5	6.5	7.5	mA
	Input current	Pin 8 LOW	−10		10	µA
		Pin 8 HIGH	−10		10	
	Input level	Pin 8 LOW	0		0.3V_{CC}	V
		Pin 8 HIGH	0.7V_{CC}		V_{CC}	
I_{CC}	Standby	Pin 8 = LOW		0.2	0.5	mA
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

AC ELECTRICAL CHARACTERISTICS

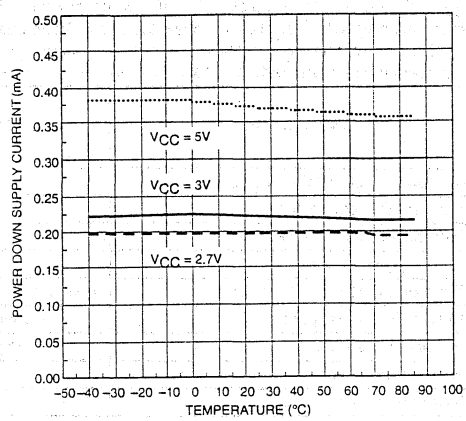
T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 240.05MHz + 14.5dBV RF input step-up; IF frequency = 10.7MHz; RF level = -45dBm; FM modulation = 1kHz with ±125kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA636 MIN	LIMITS SA636 TYP	LIMITS SA636 MAX	UNITS
Mixer/Osc section (ext LO = 160mV$_{RMS}$)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	External oscillator (buffer)			500		MHz
	Noise figure at 240MHz			12		dB
	Third-order input intercept point	Matched f1=240.05; f2=240.35MHz		-16		dBm
	Conversion power gain	Matched 14.5dBV step-up	8	11	14	dB
	RF input resistance	Single-ended input		700		Ω
	RF input capacitance			3.5		pF
	Mixer output resistance	(Pin 20)		330		Ω
IF section						
	IF amp gain	330Ω load		38		dB
	Limiter gain	330Ω load		54		dB
	Input limiting -3dB	Test at Pin 18		−105		dBm
	AM rejection	80% AM 1kHz		50		dB
	Data level	R_{LOAD} = 100kΩ	100	130		mV$_{RMS}$
	3dB data bandwidth		600	700		kHz
	SINAD sensitivity	RF level = -111dBm		16		dB
THD	Total harmonic distortion			-43	-38	dB
S/N	Signal-to-noise ratio	No modulation for noise		60		dB
	IF RSSI output with buffer	IF level = -118dBm		0.2	0.5	V
		IF level = -68dBm	0.3	0.6	1.0	V
		IF level = -10dBm	0.9	1.3	1.8	V
	IF RSSI output rise time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		1.2		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		1.1		us
	IF RSSI output fall time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		2.0		us
	(no RSSI bypass capacitor)	RF level = -28dBm		7.3		us
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance			330		Ω
	IF output impedance			330		Ω
	Limiter input impedance			330		Ω
	Limiter output impedance			300		Ω
	Limiter output level with no load			130		mV$_{RMS}$
RF/IF section (int LO)						
	System RSSI output	RF level = -10dBm		1.4		V
	System SINAD	RF level = -106dBm		12		dB

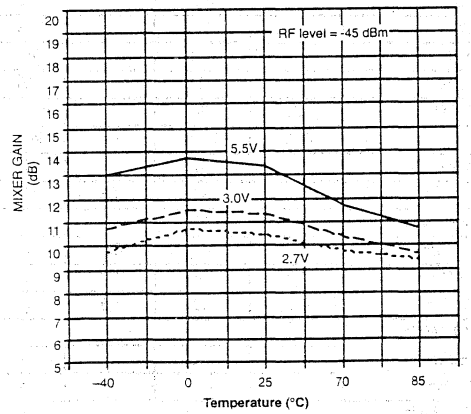
PERFORMANCE CHARACTERISTICS



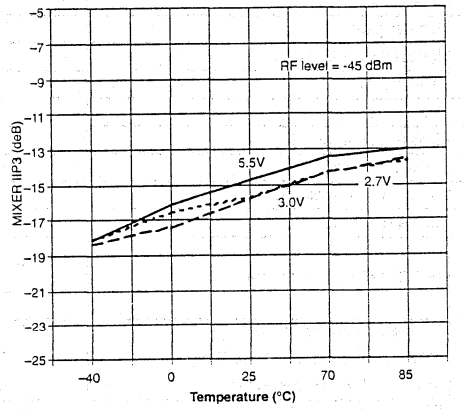
Supply Current vs Temperature and Supply Voltage



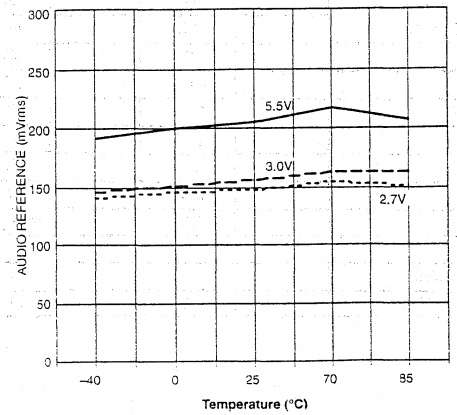
Power Down Supply Current vs Temperature and Supply Voltage



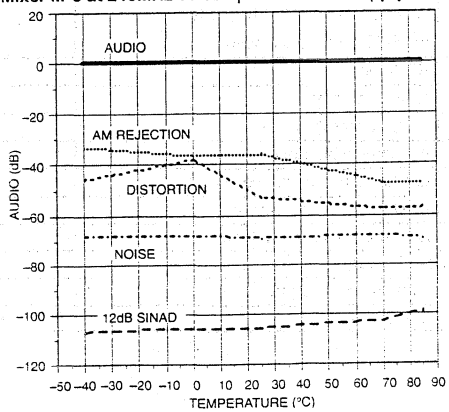
Mixer Power Gain vs Temperature and Supply Voltage



Mixer IIP3 at 240MHz vs Temperature and Supply Voltage

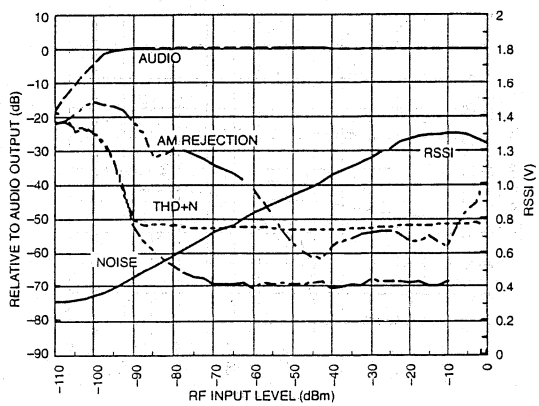


Audio Reference Level vs Temperature and Supply Voltage

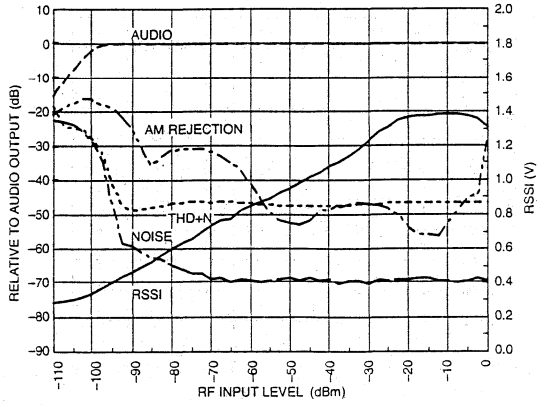


12dB SINAD and Relative Audio, THD, Noise and AM Rejection for VCC = 3V vs Temperature RF = 240MHz, Level = –68dBm, Deviation = 125kHz

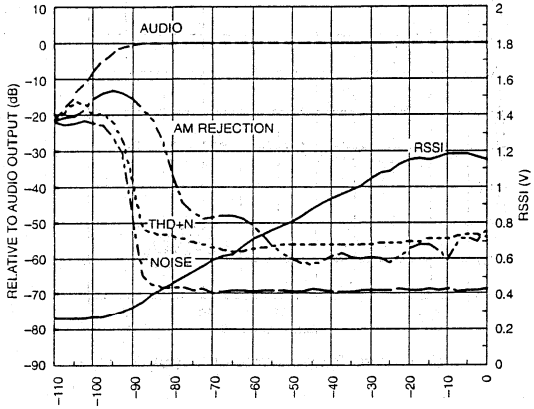
PERFORMANCE CHARACTERISTICS (continued)



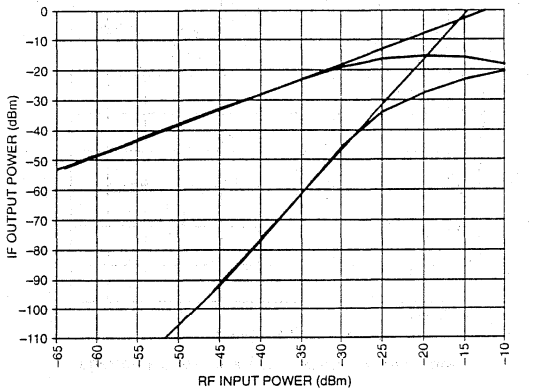
Receiver RF Performance — T = 25°C, Audio Level = 129mV$_{RMS}$



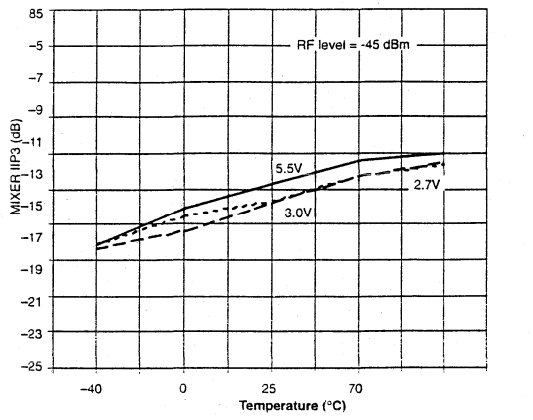
Receiver RF Performance — T = –40°C, Audio Level = 118mV$_{RMS}$



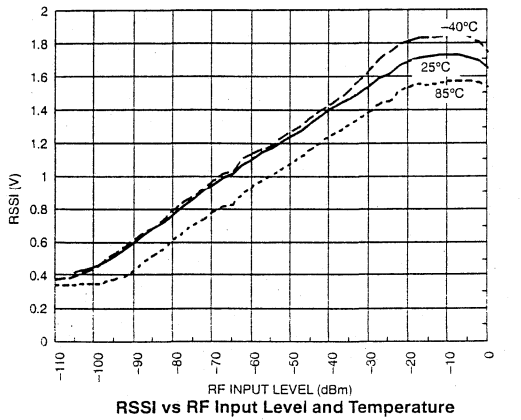
Receiver RF Performance – T = 85°C, Audio Level = 131mV$_{RMS}$



Mixer Third Order Intercept and Compression

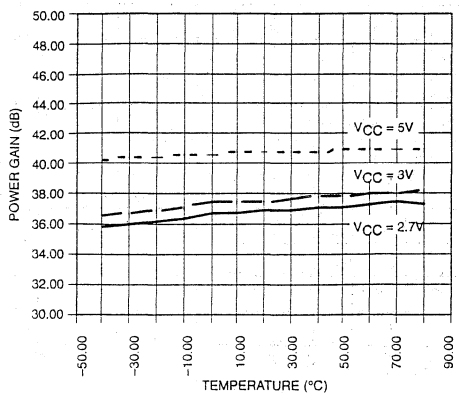


Mixer IIP3 at 240MHz vs Temperature and Supply Voltage

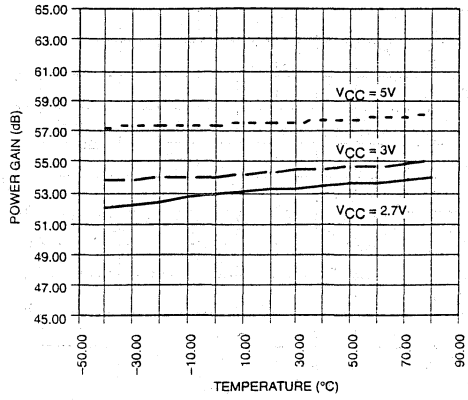


RSSI vs RF Input Level and Temperature

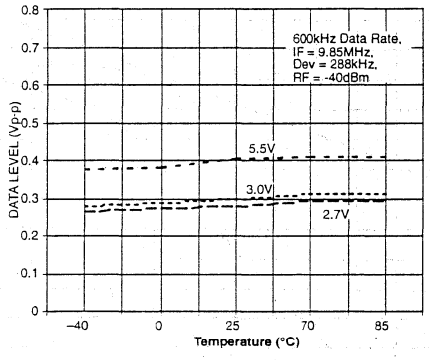
PERFORMANCE CHARACTERISTICS (continued)



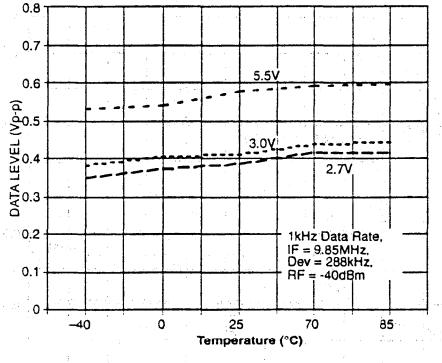
SA626 IF Amplifier Gain vs Temperature vs Supply Voltage



SA626 Limiting Amplifier Gain vs Temperature vs Supply Voltage

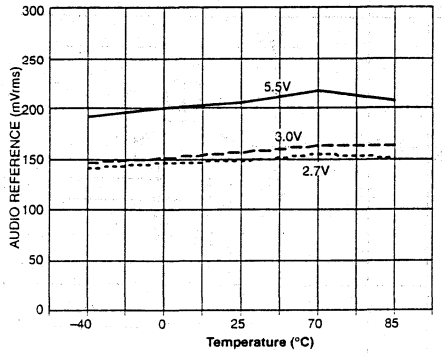


Data Level vs Temperature and Supply Voltage

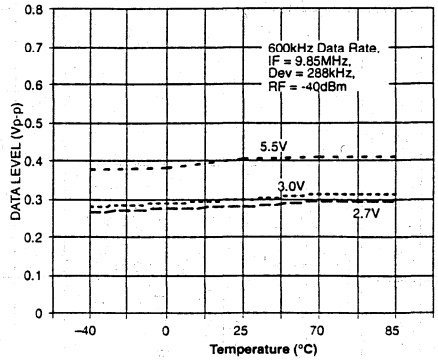


Data Level vs Temperature and Supply Voltage

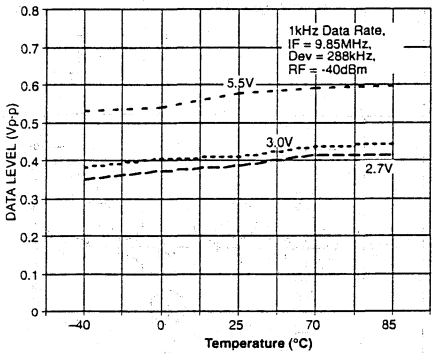
PERFORMANCE CHARACTERISTICS (continued)



Audio Reference Level vs Temperature and Supply Voltage

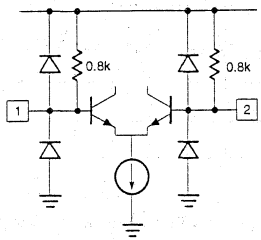
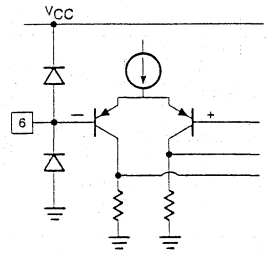
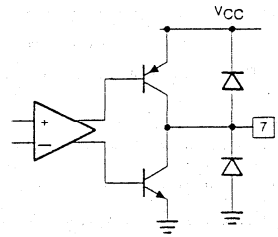
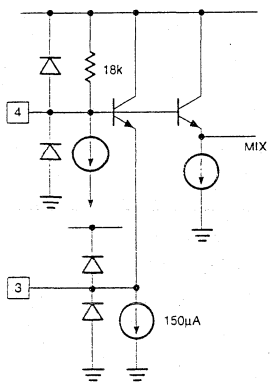
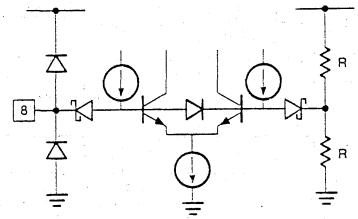
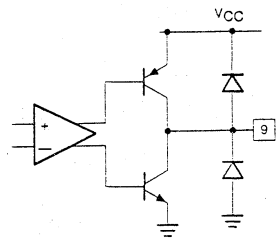
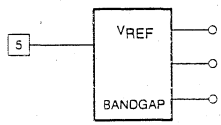
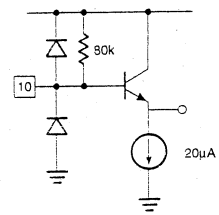


Data Level vs Temperature and Supply Voltage

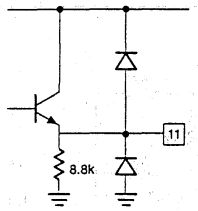
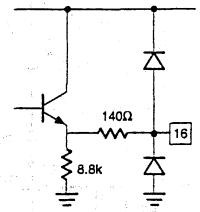
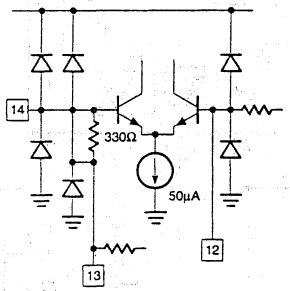
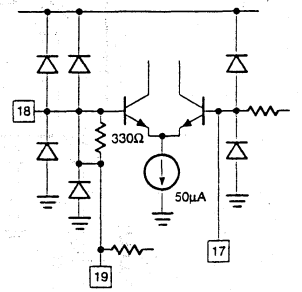
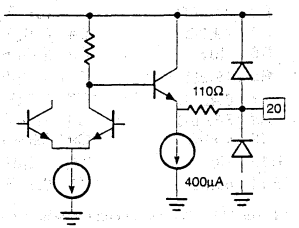


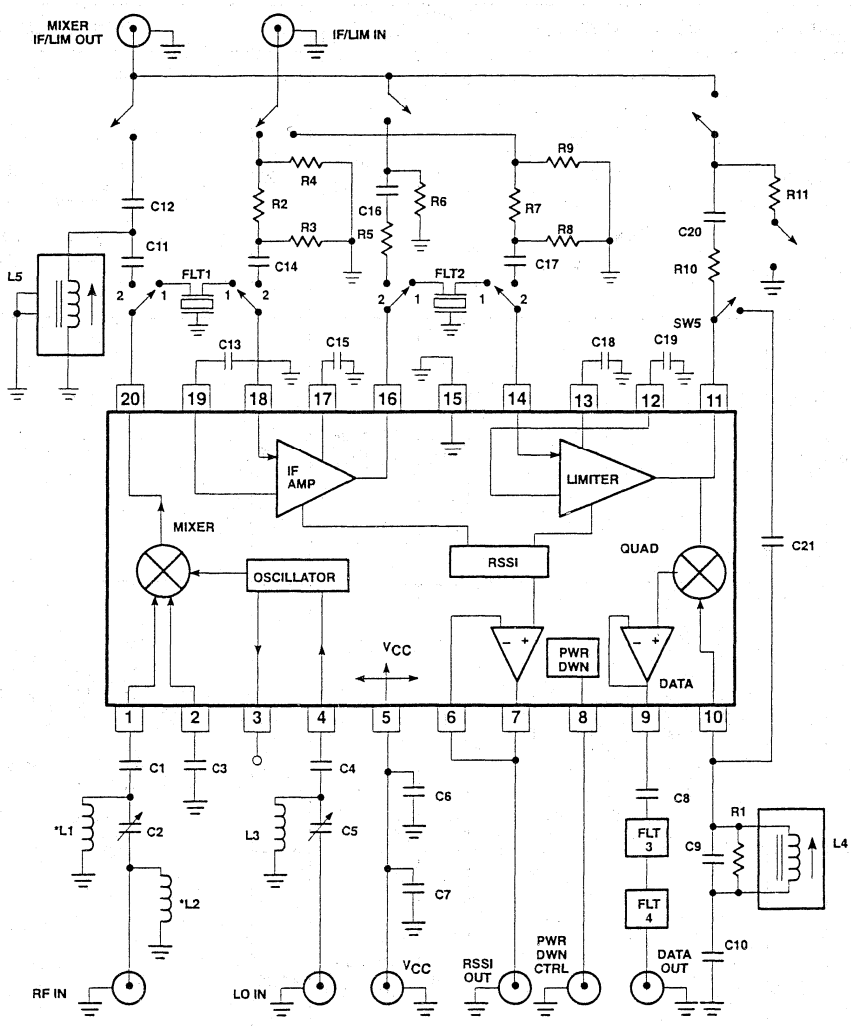
Data Level vs Temperature and Supply Voltage

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	+2.75	
4	XTAL OSC	+2.32		9	DATA OUT	+1.09	
5	VCC	+3.00		10	QUAD. IN	+3.00	

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	LIMITER OUT	+1.35		16	IF AMP OUT	+1.22	
12	LIMITER DECOUP	+1.23		17	IF AMP DECOUP	+1.22	
13	LIMITER COUPLING	+1.23		18	IF AMP IN	+1.22	
14	LIMITER IN	+1.23		19	IF AMP DECOUP	+1.22	
15	GND	0		20	MIXER OUT	+1.03	



Automatic Test Circuit Component List

R1	8.2kΩ select	C1	0.1µF	C12	160pF select	L1	150nH select for input match
R2	6.42kΩ	C2	1–5pF select for input match	C13	1000pF	L2	22nH select for input match
R3	347.8Ω	C3	0.1µF	C14	0.1µF	L3	47nH select for input match
R4	49.9Ω	C4	0.1µF	C15	1000pF	L4	5.6µH select for input match
R5	1kΩ	C5	1–5pF select for input match	C16	0.1µF	L5	1.27–2.25µH select for mixer output match
R6	49.9Ω	C6	100pF	C17	0.1µF		
R7	6.42kΩ	*C7	6.8µF 10V	C18	1000pF	FLT1	10.7MHz (Murata SFE10.7MA5-A)
R8	347.8Ω	C8	1µF	C19	1000pF	FLT2	10.7MHz (Murata SFE10.7MA5-A)
R9	49.9Ω	C9	39pF select	C20	0.1µF	FLT3	"C" message weighted
R10	1kΩ	C10	0.1µF	C21	1pF	FLT4	Active de-emphasis
R11	49.9Ω	C11	0.1µF				

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA636 240.05MHz (RF) / 10.7MHz (IF) Test Circuit

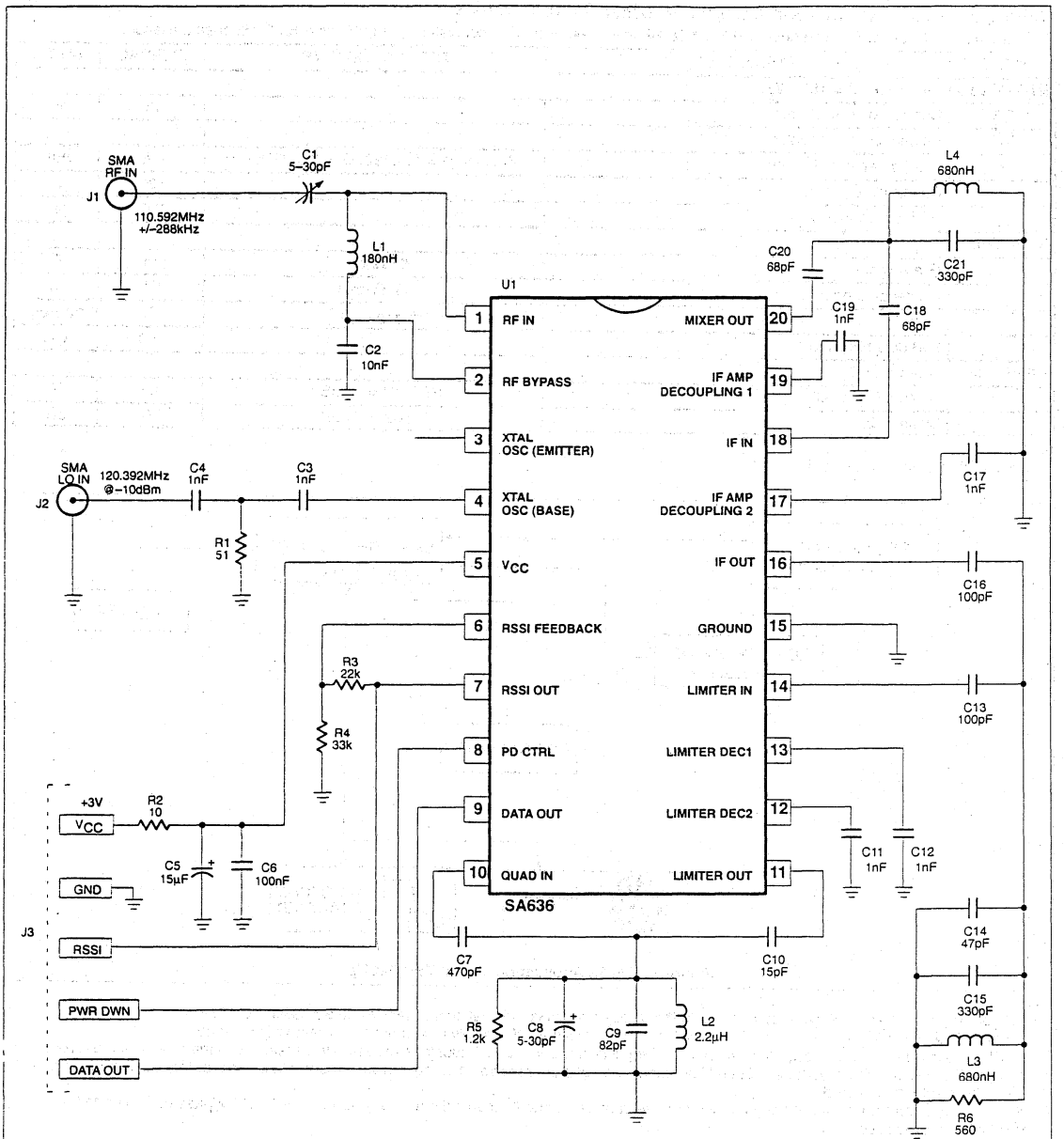


Figure 2. SA636 110.592MHz (RF) / 9.8MHz (IF) DECT Application Circuit

Table 1. DECT Application Circuit Electrical Characteristics

RF frequency = 110.592MHz; IF frequency = 9.8MHz; RF level = -45dBm; FM modulation = 100kHz with ±288kHz peak deviation.

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	UNITS
Mixer/Osc section (ext LO = 160mV$_{RMS}$)				
PG	Conversion power gain		13	dB
NF	Noise Figure at 110MHz		12	dB
IIP3	Third order input intercept	Matched f1 = 110.592; f2 = 110.892MHz	-15	dBm
R_{IN}	RF input resistance		690	Ω
C_{IN}	RF input capacitance		3.6	pF
IF section				
	IF amp gain	330Ω load	38	dB
	Limiter amp gain	330Ω load	54	dB
	Data level	R_{LOAD} = 3kΩ	130	mV$_{RMS}$
	3dB data bandwidth		700	kHz
RF/IF section (internal LO)				
	System RSSI output	RF level = -10dBm	1.4	V
	System S/N[1]	RF level = -83dBm	10	dB

NOTE:
1. 10dB S/N corresponds to BER = 10^{-3}.

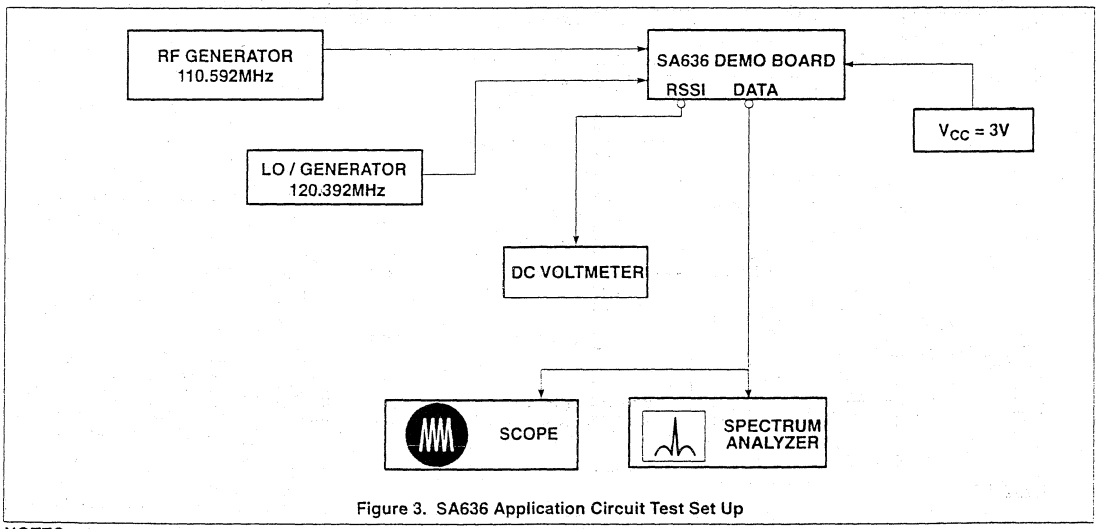
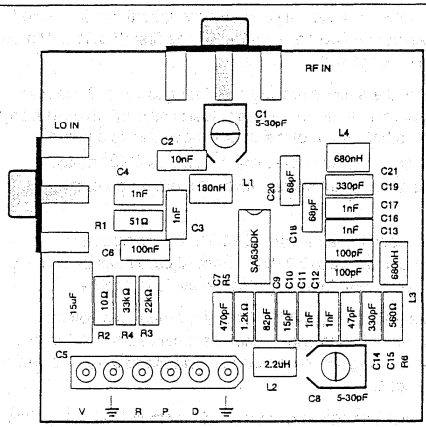
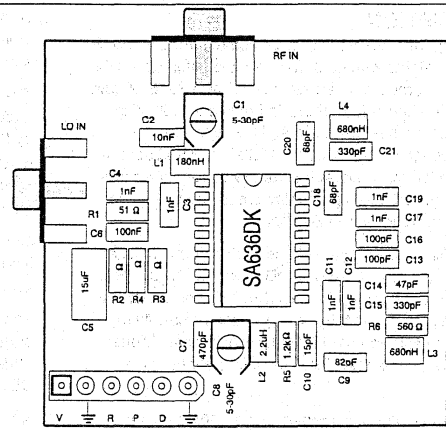


Figure 3. SA636 Application Circuit Test Set Up

NOTES:
1. RF generator: Set your RF generator at 110.592MHz. use a 100kHz modulation frequency and a ±288kHz deviation.
2. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
3. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
4. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1µF bypass capacitor on the supply pin improves sensitivity.

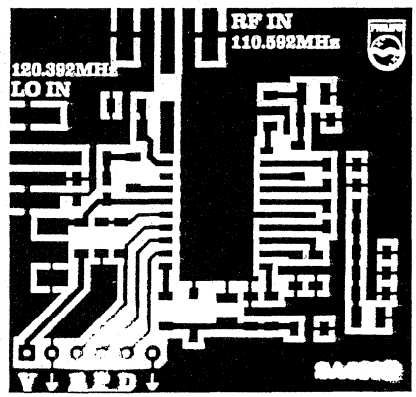


TOP SILK SCREEN (SSOP)

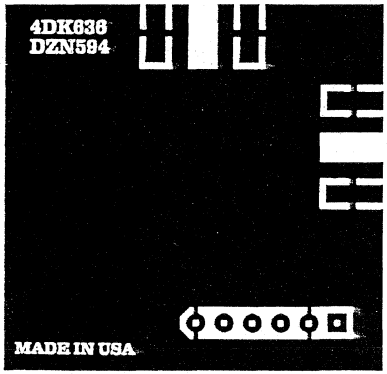


TOP SILK SCREEN (SOL)

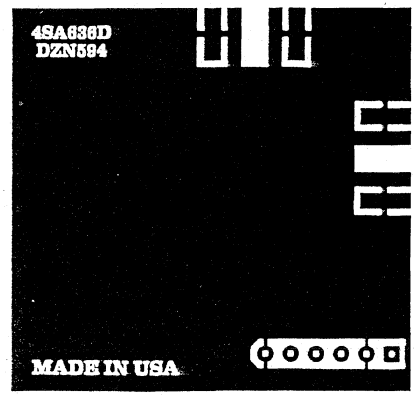
TOP VIEW (SSOP)



TOP VIEW (SOL)



BOTTOM VIEW (SSOP)



BOTTOM VIEW (SOL)

Figure 4. SA636 Demoboard Layout (Not Actual Size)

Low-voltage high performance mixer FM IF system with high-speed RSSI

SA636

CIRCUIT DESCRIPTION

The SA636 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 38dB of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 54dB of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 10.7MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as cordless and cellular hand-held phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 14dB, conversion gain of 11dB, and input third-order intercept of -16dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 10.7MHz ceramic filter for narrowband applications. The input resistance of the limiting IF amplifiers is also 330Ω. With most 10.7MHz ceramic filters and many crystal filters, no impedance matching network is necessary. For applications requiring wideband IF filtering, such as DECT, external LC filters are used (see Figure 2). To achieve optimum linearity of the log signal strength indicator, there must be a 6dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequency at 10.7MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output (DATA) of the quadrature is a voltage output. This output is designed to handle a minimum bandwidth of 600kHz. This is designed to demodulate wideband data, such as in DECT applications.

A Receive Signal Strength Indicator (RSSI) completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPS or TACS cellular telephone, DECT and RCR-28 cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

Low-voltage digital IF receiver SA637

DESCRIPTION

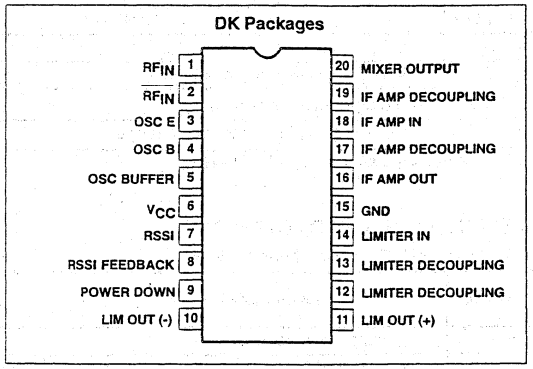
The SA637 is a low-voltage high performance monolithic digital system with high-speed RSSI incorporating a mixer, oscillator with buffered output, two limiting intermediate frequency amplifiers, fast logarithmic received signal strength indicator (RSSI), voltage regulator, RSSI op amp and power down pin. The SA637 is available in SSOP (shrink small outline package).

The SA637 was designed for portable digital communication applications and will function down to 2.7V. The limiter amplifier has differential outputs with 2MHz small signal bandwidth. The RSSI output has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

FEATURES

- V_{CC} = 2.7 to 5.5V
- Low power receiver (3.8mA @ 3V)
- Power down mode (I_{CC} = 110µA)
- Fast RSSI rise and fall times
- Extended RSSI range with temperature compensation
- RSSI op amp
- 2MHz limiter small signal bandwidth
- 455kHz filter matching (1.5kΩ)
- Differential limiter output

PIN CONFIGURATION



- Oscillator buffer
- SSOP-20 package

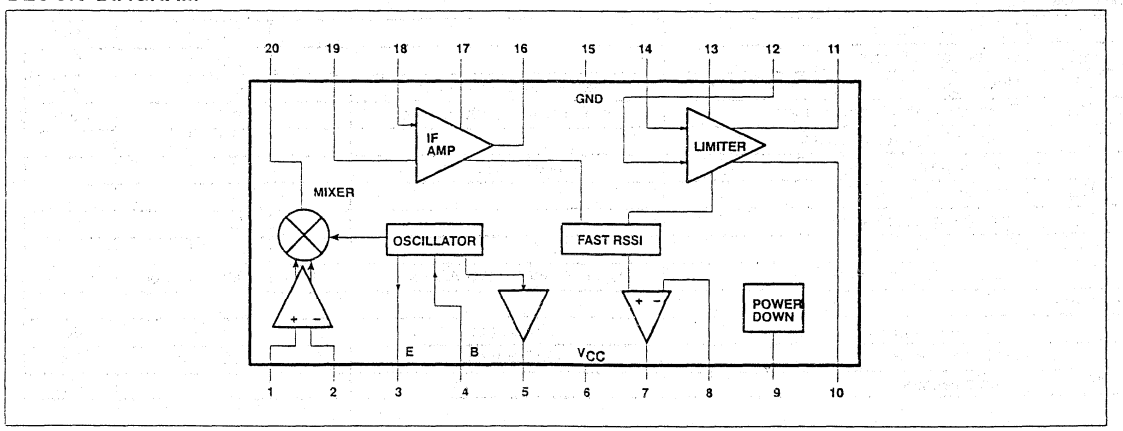
APPLICATIONS

- ADC (American Digital Cellular)
- Digital receiver systems
- Cellular radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA637DK	1563–

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		5.5	V
I_{CC}	DC current drain	Pin 9 = HIGH or OPEN		3.8	4.5	mA
		V_{CC} = 4.7V		4.4	5.5	mA
	Standby	Pin 9 = LOW		0.11	0.5	mA
	Input current	Pin 9 = LOW	-10		10	µA
		Pin 9 = HIGH	-10		10	
	Input level	Pin 9 = LOW	0		0.3V_{CC}	µA
		Pin 9 = HIGH	0.7V_{CC}		V_{CC}	
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 90MHz; RF input step-up = +14.5dBV; IF frequency = 455kHz; RF level = -68dBm. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section						
f_{IN}	Input signal frequency			200		MHz
f_{OSC}	Crystal oscillator frequency			200		MHz
NF	Noise figure at 90MHz	Matched input and output		6.2		dB
TOI	Third-order input intercept point	Input matched to 50Ω source		-17		dBm
P1dB	Input 1dB compression point			-27		dBm
	Conversion power gain	Matched 50Ω		7		dB
R_{IN}	Mixer input resistance			2.5		kΩ
C_{IN}	Mixer input capacitance			2.2		pF
R_{OUT}	Mixer output resistance			1.87		kΩ
	Buffered LO output level	LO = 447mV_{P-P}, 1kΩ AC load	100	300	500	mV_{P-P}
IF section						
	IF amp power gain	50Ω source		36		dB
	Limiter power gain	50Ω source		60		dB
IF_{BW}	IF amp bandwidth			2.5		MHz

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
	RF RSSI output	RF level = -118dBm	.01	0.2	.65	V
		RF level = -68dBm	.4	0.9	1.7	V
		RF level = -28dBm	1.0	1.7	2.3	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	RSSI ripple			30		mV_{P-P}
	RSSI speed Rise time	No interstage filter		2.5		µs
		With interstage filter		22		µs
	RSSI speed Fall time	No interstage filter		10		µs
		With interstage filter		50		µs
	IF input impedance			1.5		kΩ
	IF output impedance			1.5		kΩ
	Limiter input impedance			1.5		kΩ
	Limiter output impedance	(Pin 10, Pin 11)		200		Ω
	Limiter output signal level	(Pin 10, Pin 11) 1.5kΩ AC load		280		mV_{P-P}
	Limiter output DC level			1.27		V
	Differential output matching			±6		mV
	Differential output offset			±30		mV

CIRCUIT DESCRIPTION

Mixer

The mixer has a balanced input and is capable of being driven single-ended. The input impedance is 2.5kΩ in parallel with a 2.2pF cap at 90MHz RF. The mixer output can drive a 1500Ω ceramic filter at 455kHz or 600kHz directly without any matching required. The mixer conversion power gain is 7dB when both input and output are matched and optimum LO level is used to drive the internal mixer core.

Oscillator and Buffer

The on-board oscillator supplies the signal for the mixer down-conversion. The internally biased transistor can be configured as a Colpitts or Butler overtone crystal oscillator. The transistor's bias current can be increased if desired by adding a shunt resistor from Pin 3 to ground. The oscillator's buffered output (Pin 5) can be used as a feedback signal to lock the oscillator to an appropriate reference.

IF Amplifier and IF Limiter

The IF strip provides more than 95dB of power gain for the down converted signal. Its overall bandwidth is limited to 2MHz. The input and output impedance of the IF amplifier and the input impedance of the IF limiter are set to 1500Ω (match to 455kHz filter). A second filter is connected between the IF amplifier and the limiter for improved channel selectivity and reduced instability. This ceramic filter provides 3dB interstage insertion loss which results in optimal RSSI linearity. The overall gain can be reduced if desired by adding an external attenuator after the IF amplifier. The differential limiter outputs (Pins 10 and 11) are available for demodulator circuits.

RSSI

The received signal strength indicator provides a linear voltage indication of the received signal strength in dB for a range in excess of 90dB. The response time to a change in input signal is less than a few microseconds and the delay is kept to a minimum because of the use of a minimum phase shift circuit. Because of the speed of the RSSI circuit, the RSSI rise and fall time may, in practice, be dominated by the bandwidth of the external bandpass filter that is placed between the mixer and the IF, and the external filter placed between the IF amplifier and limiter. Since the RSSI function requires the signal to propagate through the whole IF strip, and the rise and fall time of the filters are inversely proportional to their bandwidth, there is a trade-off between channel selectivity and RSSI response. A possible solution is to use a second SA637 with wider band external filters for faster RSSI response.

The RSSI curve is temperature compensated and in addition is designed for improved consistency from unit to unit.

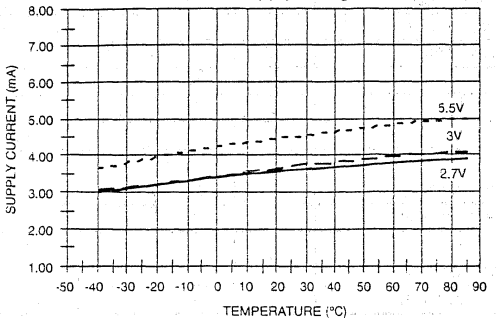
The RSSI circuit drives an on-chip low power op amp with rail-to-rail output which can be connected as a unity gain RSSI buffer or a gain stage or even a comparator.

DC Power Supply

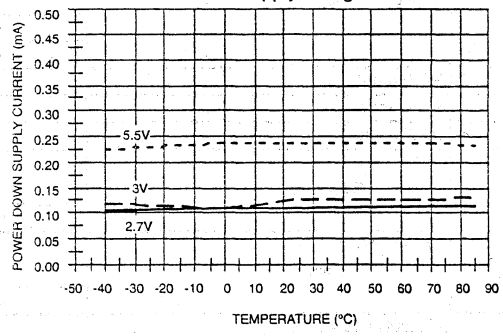
The IC is designed for operation between 2.7 and 5.5V. A power supply dependent biasing scheme is used in the mixers to benefit from the large headroom available at higher V_{CC}s.

PERFORMANCE CHARACTERISTICS

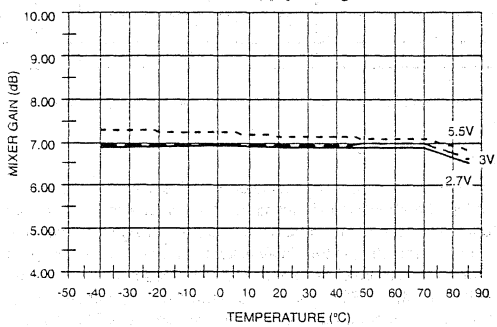
Supply Current vs Temperature and Supply Voltage



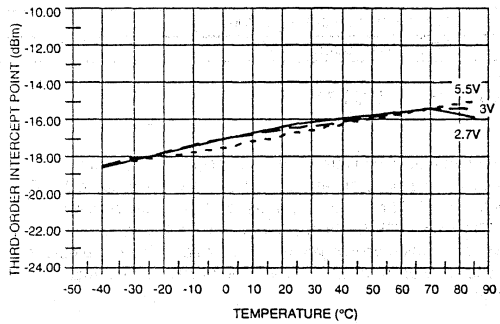
Power Down Supply Current vs Temperature and Supply Voltage



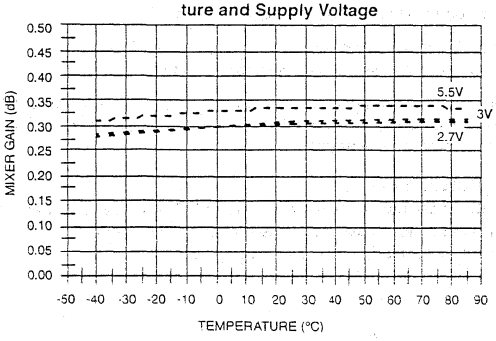
Mixer Power Gain vs Temperature and Supply Voltage



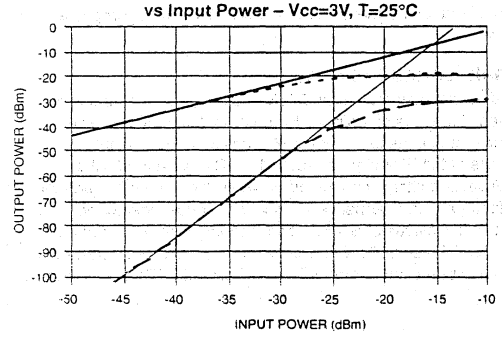
Mixer Third Order Input Intercept Point vs Temperature and Supply Voltage



Oscillator Buffer Output Level vs Temperature and Supply Voltage

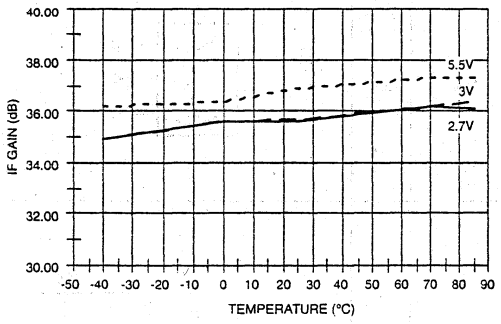


Mixer Third Order Intercept and Compression vs Input Power – Vcc=3V, T=25°C

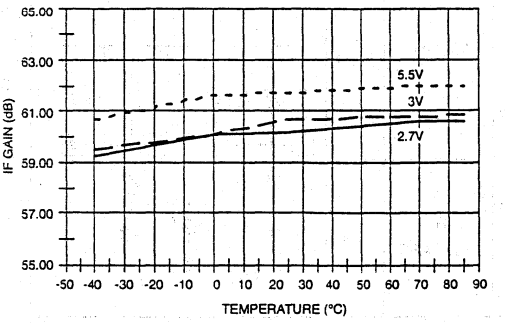


PERFORMANCE CHARACTERISTICS (cont.)

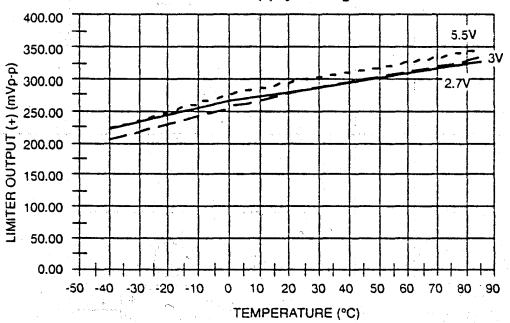
IF Power Gain vs Temperature and Supply Voltage



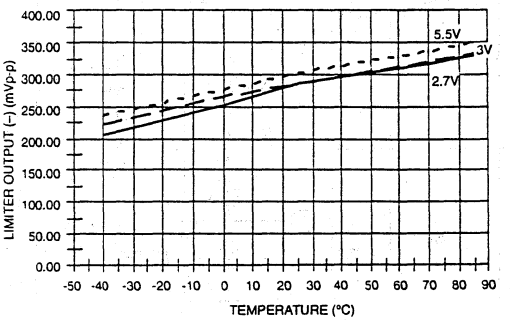
Limiter Power Gain vs Temperature and Supply Voltage



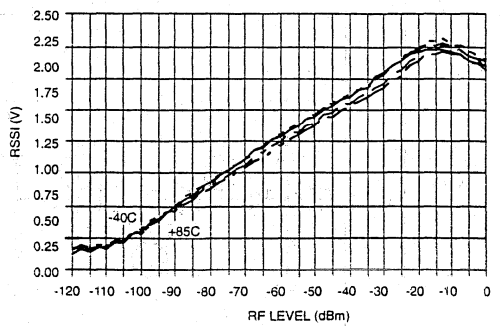
Limiter Output (+) Level vs Temperature and Supply Voltage



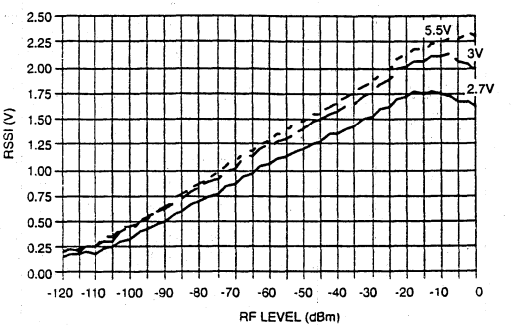
Limiter Output (–) Level vs Temperature and Supply Voltage



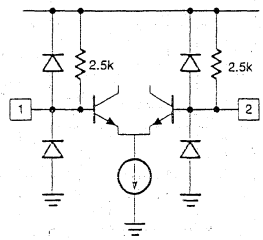
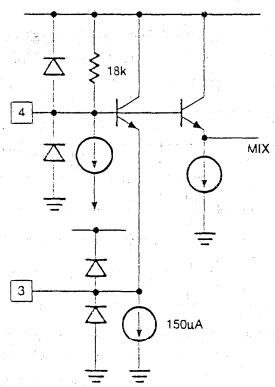
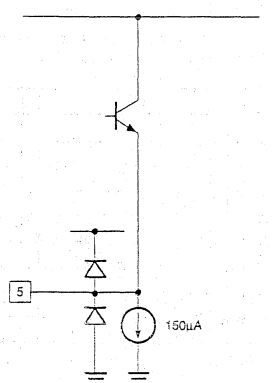
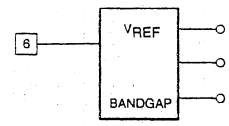
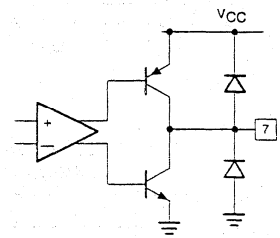
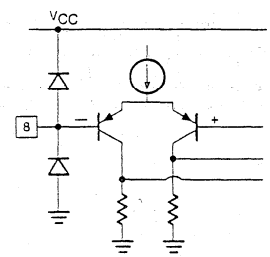
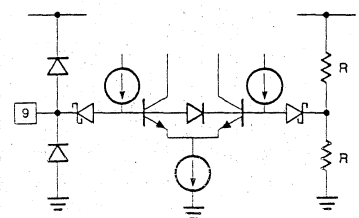
RSSI vs RF Level and Temperature – V_{CC} = 3V



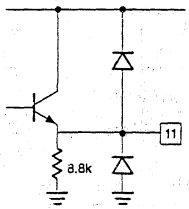
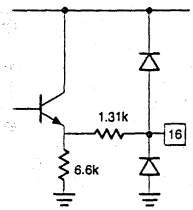
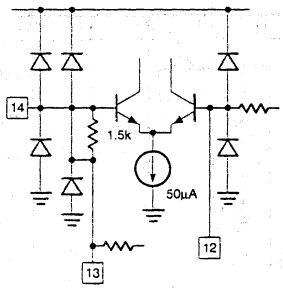
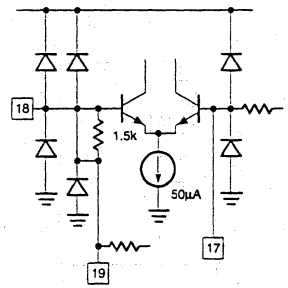
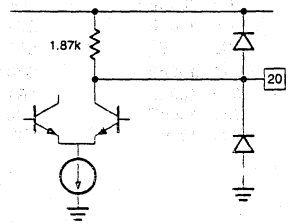
RSSI vs RF Level and Supply Voltage – Temperature = 25°C

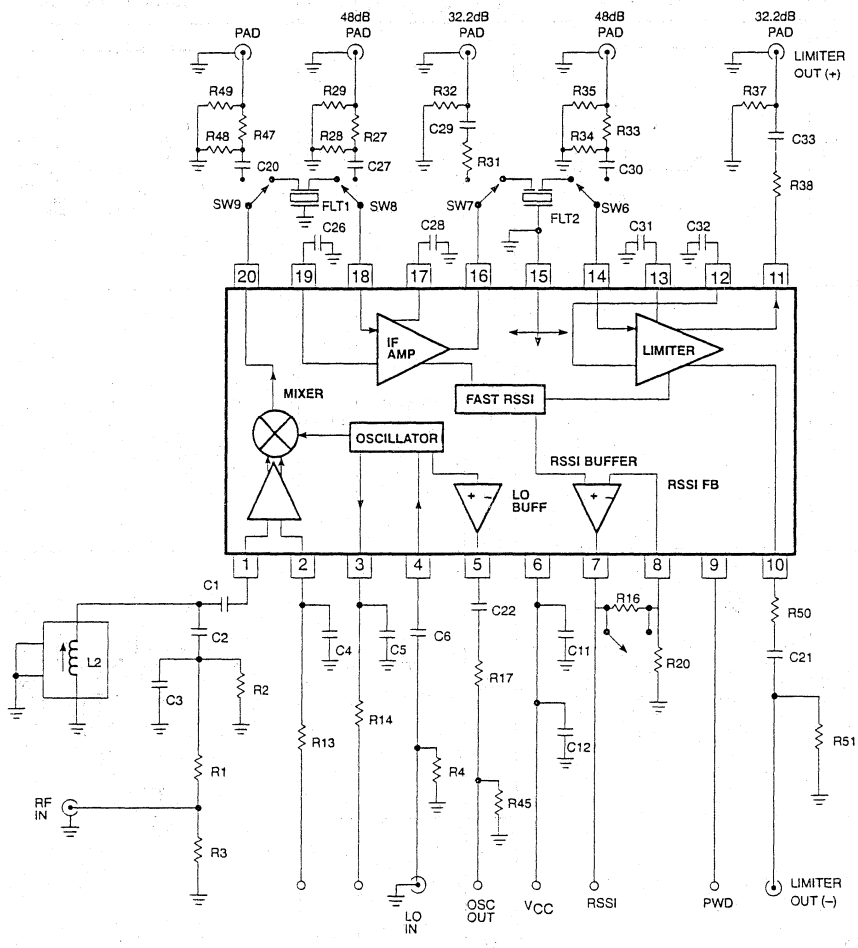


PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.40	
2	RF BYPASS	+1.40	
3	OSC E	+1.79	
4	OSC B	+2.56	
5	OSC BUFFER	+1.79	
6	V_{CC}	+3.00	
7	RSSI OUT	+0.20	
8	RSSI FEEDBACK	+0.20	
9	POWER DOWN	+2.00	

PIN FUNCTIONS (continued)

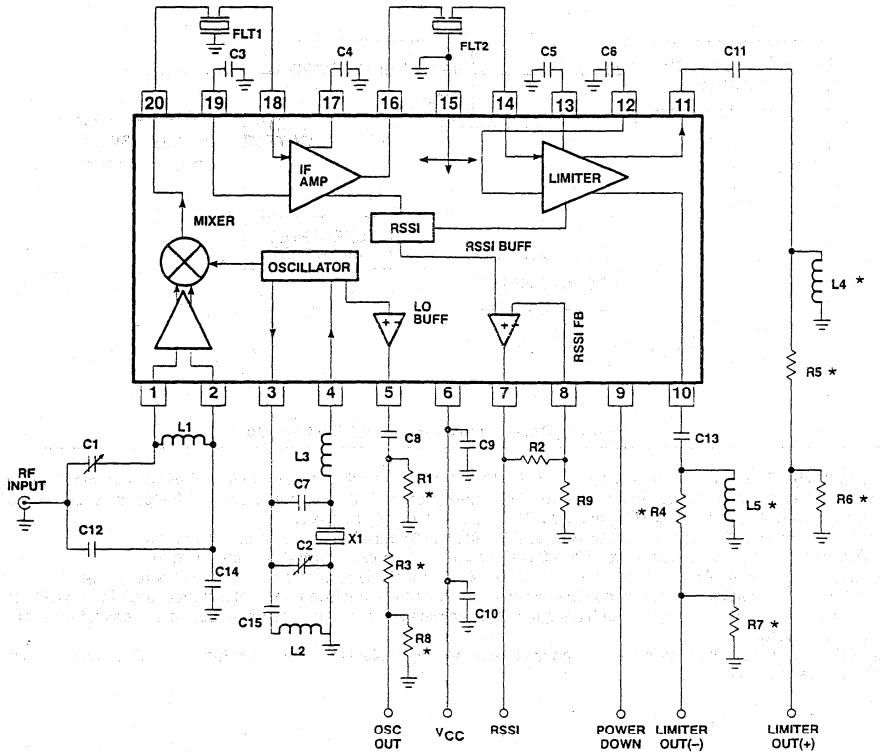
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
10 11	LIMITER OUT	+1.25		16	IF AMP OUT	+1.28	
12	LIMITER DECOUP	+1.28		17	IF AMP DECOUP	+1.28	
13	LIMITER COUPLING	+1.28		18	IF AMP IN	+1.28	
14	LIMITER IN	+1.28		19	IF AMP DECOUP	+1.28	
15	GND	0		20	MIXER OUT	+2.03	



Automatic Test Circuit Component List

C1	10nF	C27	100nF	R4	49.9Ω	R32	49.9Ω	R32	49.9Ω
C2	91pF	C28	100nF	R13	10kΩ	R33	13.7kΩ	R50	1kΩ
C3	620pF	C29	100nF	R14	10kΩ	R34	1.68kΩ	R51	49.9Ω
C4	100nF	C30	100nF	R16	10kΩ	R35	49.9Ω	L2	62nH
C5	100nF	C31	100nF	R17	1kΩ	R38	1kΩ		
C6	10nF	C32	100nF	R20	10kΩ	R39	49.9Ω		
C11	100nF	C33	100nF	R27	13.7kΩ	R45	49.9Ω		
C20	100nF	R1	249Ω	R28	1.68kΩ	R47	2.43kΩ		
C21	100nF	R2	60.4Ω	R29	49.9Ω	R48	39.2kΩ		
C26	100nF	R3	60.4Ω	R31	1kΩ	R49	49.9Ω		

Figure 1. SA637 Automatic Test Circuit



Component List

C1	5-30pF	C9	0.1µF	R1	OPEN	L1	0.15µH PM20-R15M
C2	5-30pF	C10	1.0µF	R2	0Ω (short)	L2	0.15µH PM20-R15M
C3	0.1µF	C11	0.1µF	R3	1kΩ	L3	0.47µH PM20-R47M
C4	0.1µF	C12	68pF	R4	1.0kΩ	L4	OPEN
C5	0.1µF	C13	0.1µF	R5	2.0kΩ	L5	OPEN
C6	0.1µF	C14	0.1µF	R6	51Ω	FLT1	455kHz SFGCC 455BX-TC
C7	10pF	C15	1000pF	R7	100Ω	FLT2	455kHz SFGCC 455BX-TC
C8	0.1µF			R8	100Ω	X1	82.705MHz CTS XTAL 020-3249-042
				R9	OPEN		

* NOTE: These components are optional and depend on user matching requirements. Pads are provided on the demo board. R2 and R9 set the RSSI buffer gain. For unity gain short R2 (Pin 7 to Pin 8) and leave R9 open.

Figure 2. SA637 Application Circuit

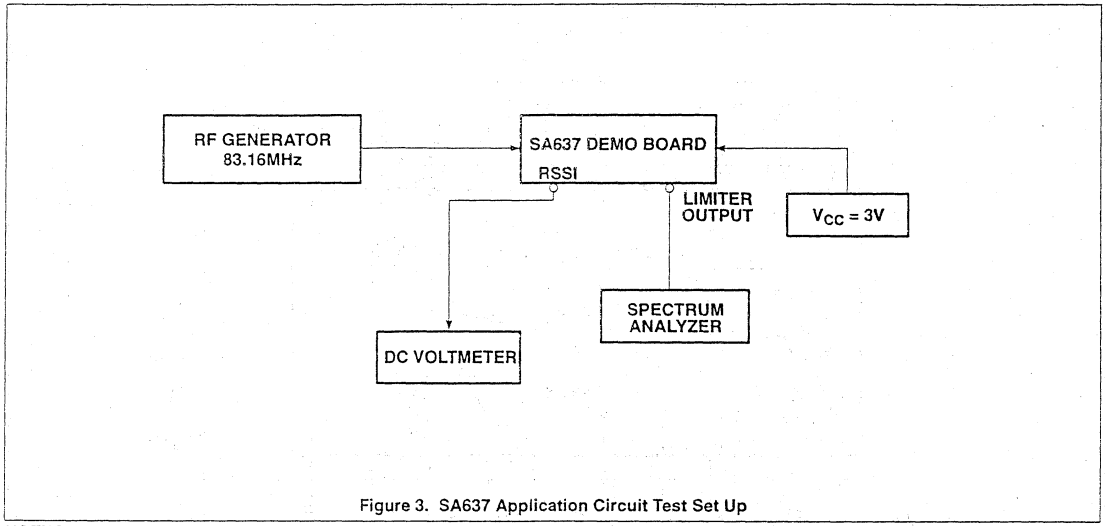
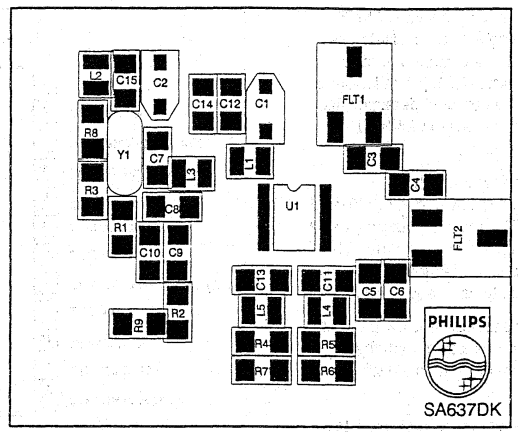
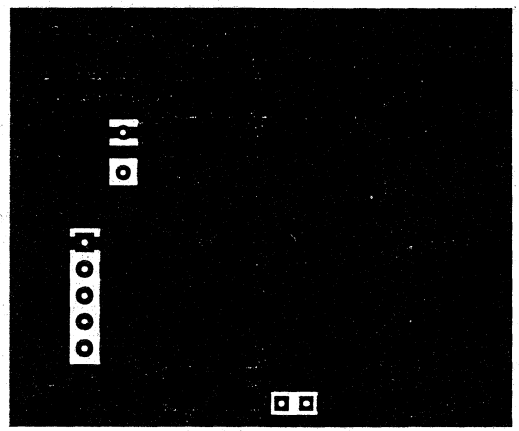


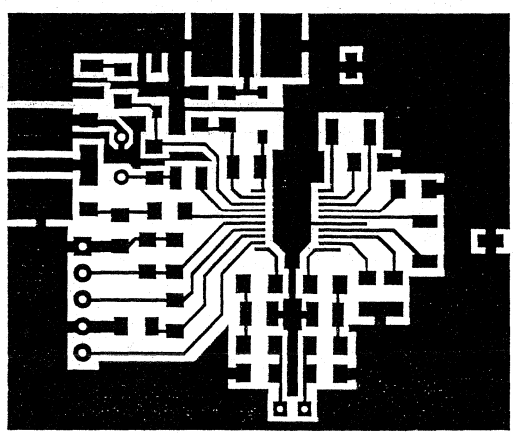
Figure 3. SA637 Application Circuit Test Set Up

NOTES:

1. Carrier-to-Noise (C/N): Connect a spectrum analyzer to Pin 10 or 11; set your RF generator to 83.16MHz or 455kHz above your LO frequency, modulation off; set the spectrum analyzer resolution bandwidth to 300Hz; and adjust your RF input level until the C/N = 26dB. Use video averaging. Assure that LIMOUT(+) and LIMOUT(–) are matched symetrically.
2. Ceramic filters: The ceramic filter can be SFGCC455BX-TC made by Murata which has 30kHz IF bandwidth.
3. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.45µV or -114dBm at the RF input.
4. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
5. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
6. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1µF bypass capacitor on the supply pin improves sensitivity.


L2
C15
C2
C14
C12
C1
FLT1
R8
Y1
C7
L3
L1
C3
C4
R3
C8
U1
R1
FLT2
C10
C9
C13
C11
C5
C6
L5
L4
R9
R2
R4
R5
R7
R6
PHILIPS
SA637DK





Low-voltage mixer FM IF system with filter amplifier and data switch

SA639

DESCRIPTION

The SA639 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), fast RSSI op amps, voltage regulator, wideband data output, post detection filter amplifier and data switch. The SA639 is available in 24-lead TSSOP (Thin shrink small outline package).

The SA639 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The data output provides a minimum bandwidth of 1MHz to demodulate wideband data. The RSSI output is amplified and has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

The post-detection amplifier may be used to realize a low pass filter function. A programmable data switch routes a portion of the data signal to an external integration circuit that generates a data comparator reference voltage.

SA639 incorporates a power down mode which powers down the device when Pin 8 is low. Power down logic levels are CMOS and TTL compatible with high input impedance.

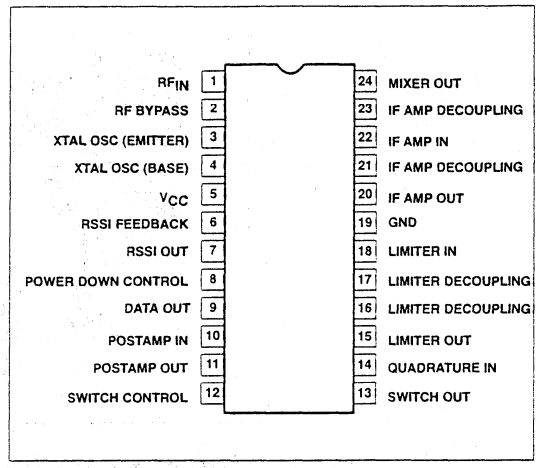
APPLICATIONS

- DECT (Digital European Cordless Telephone)
- FSK and ASK data receivers

FEATURES

- V_{CC} = 2.7 to 5.5V
- Low power consumption: 8.3mA typ at 3V
- Wideband data output (1MHz min.)
- Fast RSSI rise and fall times
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB and noise figure of 11dB at 110MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)

PIN CONFIGURATION



- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- 10.7MHz filter matching (330Ω)
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- RSSI output internal op amp
- Post detection amplifier for filtering
- Programmable data switch
- Excellent sensitivity: 1.25μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) with RF at 110MHz and IF at 10.7MHz
- ESD hardened
- Power down mode

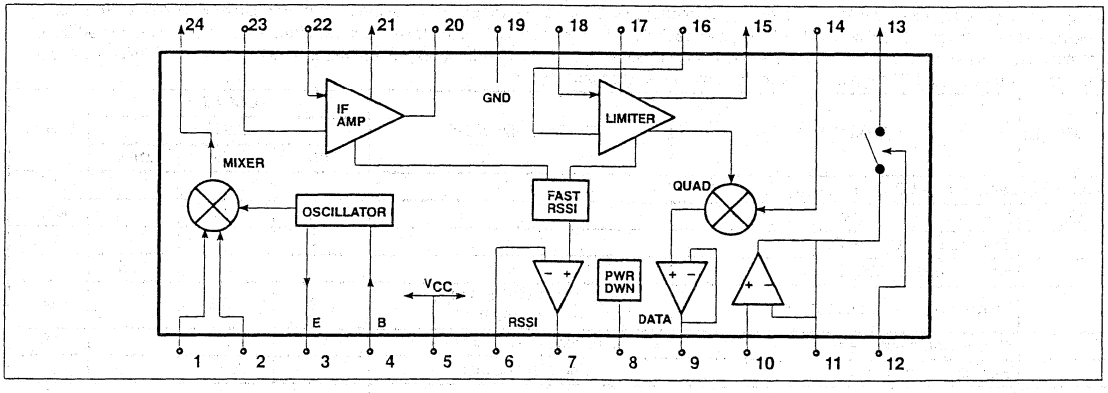
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic TSSOP (Thin Shrink Small Outline Package)	-40 to +85°C	SA639	

Low-voltage mixer FM IF system with filter amplifier and data switch

SA639

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA639	-40 to +85	°C

NOTE: θ_{JA} Thermal impedance (DH package) 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA639 MIN	LIMITS SA639 TYP	LIMITS SA639 MAX	UNITS
V_{CC}	Power supply voltage range		2.7	3.0	5.5	V
I_{CC}	DC current drain	Pin 8 = LOW		8.3		mA
I_{CC}	Standby	Pin 8 = HIGH			100	µA
	Input current	Pin 8 = LOW Pin 8 = HIGH		10		µA
	Input level	Pin 8 = LOW Pin 8 = HIGH[1]	0 0.7V_{CC}		0.3V_{CC} 6	V V
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs
	Power up settling time	Data output valid		100	200	µs
Data Switch Control Input						
	Switch closed	Pin 12 = LOW, PIN 8 = LOW	0		0.3 V_{CC}	V
	Switch open (output tri-state)	Pin 12 = HIGH	0.7 V_{CC}		6	V
	Input current low	Pin 12 = LOW		10	15	µA
	Input current high	Pin 12 = HIGH			4	µA
	Switch activation time			0.5	1	µs

NOTE:
1. When the device is forced in power down mode via Pin 8, the Data Switch will output a voltage close to 1.6V and the state of the switch control input will have no effect.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 110MHz + 14.5dBV RF input step-up; IF frequency = 10.7MHz; RF level = -45dBm; FM modulation = 576kHz with ±288kHz peak deviation, discriminator tank circuit Q=4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA639 MIN	LIMITS SA639 TYP	LIMITS SA639 MAX	UNITS
Mixer/Osc section (ext LO = 160mV$_{RMS}$)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	External oscillator (buffer)		0.2	500		MHz
	Noise figure at 110MHz			11	14.5	dB
	Third-order input intercept point	Matched f1=110.592MHz; f2=110.852MHz	-18	-15.5		dBm
	Conversion power gain	Matched 14.5dBV step-up	11	12.5		dB
	RF input resistance	Single-ended input		800		Ω
	RF input capacitance			3.5		pF
	Mixer output resistance	(Pin 24)		330		Ω
IF section						
	IF amp gain		34	38		dB
	Limiter gain		50	54		dB
	Input limiting -3dB	Test at Pin 22		–105		dBm
	AM rejection	80% AM 1kHz	30	34		dB
	Data level	R_L = 10kΩ, C_L = 30pF (see application circuit)	300	400		mV$_{P-P}$
	Data bandwidth		1	2		MHz
	SINAD sensitivity	RF level = -111dBm		16		dB
THD	Total harmonic distortion			-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		60		dB
	IF RSSI output with buffer	IF level = -118dBm	0	0.2	0.5	V
		IF level = -68dBm	0.3	0.6	1.0	
		IF level = -18dBm	0.9	1.3	1.8	
	IF RSSI output rise time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		1.2		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		1.1		
	IF RSSI output fall time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		2.0		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		7.3		
	RSSI range		85	90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance			330		Ω
	IF output impedance			330		Ω
	Limiter input impedance			330		Ω
	Limiter output impedance			300		Ω
	Limiter output level with no load			130		mV$_{RMS}$
RF/IF section (int LO)						
	System RSSI output	RF level = -27dBm	1.0	1.2	1.5	V
	System SINAD	RF level = -110dBm		12		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA639 MIN	LIMITS SA639 TYP	LIMITS SA639 MAX	UNITS
Post detection filter amplifier						
	Amplifier 3dB bandwidth	AC coupled: R_L = 10kΩ, C_L = 30pF	4			MHz
	Amplifier gain	AC coupled: R_L = 10kΩ, $V_{OUT\ DC}$ = 1.6V	-1	-0.2	0	dB
	Slew rate	AC coupled: R_L = 10kΩ, C_L = 30pF	1			V/µs
	Input resistance		300			kΩ
	Input capacitance				3	pF
	Output impedance			250	500	Ω
	Output load resistance	AC coupled	5			kΩ
	Output load capacitance[1]	AC coupled		30		pF
	DC output level[2]		1.5	1.6	1.7	V
Data switch						
	DC input voltage range[3]		1.2	1.6	2.0	V
	AC input swing			400		mV_{P-P}
	Input impedance		100			kΩ
	Input capacitance				5	pF
	Output load resistance			500		Ω
Through Mode (Pin 12 = LOW)						
	AC voltage gain[4]		-2	-1.5		dB
	Output drive capability	Sink/source, $V_{OUT\ DC}$ = 1.6V	3			mA
	Slew rate	$V_{OUT\ DC}$ = 1.6V	1			V/µs
	Input offset voltage[5]	$V_{IN\ DC}$ = 1.2 to 2.0V			±5	mV
Tri-State Mode (Pin 12 or Pin 8 = HIGH)						
	Output leakage current	$V_{OUT\ DC}$ = 1.2 to 2.0V			100	nA

NOTES:
1. Includes filter feedback capacitance, comparator input capacitance. PCB stray capacitances and switch input capacitance.
2. Demodulator output DC coupled with Post Detection Filter Amplifier input and the demodulator tank exactly tuned to center frequency.
3. Includes DC offsets due to frequency offsets between Rx and Tx carrier and demodulator tank offset due to mis-tuning.
4. With a 400mV_{P-P} sinusoid at 600kHz driving Pin 10. Output load resistance 500Ω in series with 10nF.
5. With a DC input and capacitor in the RC load fully charged.

Low-voltage mixer FM IF system with filter amplifier and data switch

SA639

CIRCUIT DESCRIPTION

The SA639 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 44dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 58dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 10.7MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as digital cordless phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 11dB, conversion gain of 12.5dB, and input third-order intercept of -15.5dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 10.7MHz ceramic filter. The input resistance of the limiting IF amplifiers is also 330Ω. With most 10.7MHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 6dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequency at 10.7MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output (DATA) of the quadrature is a low impedance voltage output. This output is designed to handle a minimum bandwidth of 1MHz. This is designed to demodulate wideband data, such as in DECT applications.

Post Detection Filter Amplifier

The filter amplifier may be used to realize a group delay optimized low pass filter for post detection. The filter amplifier can be configured for Sallen & Key low pass with Bessel characteristic and a 3dB cut frequency of about 800kHz.

The filter amplifier provides a gain of 0dB. The output impedance is less than 500Ω in order to reduce frequency response changes as a result of amplifier load variations. The filter amplifier has a 3dB bandwidth of at least 4 MHz in order to keep the amplifier's frequency response influence on the filter group delay characteristic at a minimum. At the center of the carrier it is mandatory to provide a filter output DC bias voltage of 1.6V in order to be within the input common mode range of the external data comparator. The filter output DC bias voltage specification holds for an exactly center tuned demodulator tank and for the demodulator output connected to the filter amplifier input.

Data Switch

The SA639 incorporates an active data switch used to derive the data comparator reference voltage by means of an external integration circuit. The data switch is typically closed for 10µs before and during reception of the synchronization word pattern, and is otherwise open. The external integration circuit is formed by an R/C low pass with a time constant of 5 to 10µs.

The active data switch provides excellent tracking behavior over a DC input range of 1.2 to 2.0V. For this range with an RC load (no static current drawn), the DC output voltage will not differ more than ±5mV from the input voltage. Since the active data switch is designed to behave like a non-linear charge pump (to allow fast tracking of the input signal without slew rate limitations under dynamic conditions of a 600kHz input signal with 400mV$_{P-P}$ and the RC load), the output signal will have a 340mV$_{P-P}$ output with a DC average that will not vary from the input DC average by more than ±15mV.

The data switch is able to sink/source 3mA from/to the external integration circuit in order to minimize the settling time after long power-down periods (DECT paging mode). In addition, during power-down conditions a reference voltage of approximately 1.6V will be used as the input to the switch. The switch will be in a low current mode to maintain the voltage on the external RC load. This will further reduce the settling time of the capacitor after power-up. It should be noted that during power-down the switch can only source and sink a trickle current (10µA). Thus, the user should make sure that other circuits (like the data comparator inputs) are not drawing current from the RC circuit.

The data switch provides a slew rate better than 1V/µs in order to track with system DC offset from receive slot to receive slot (DECT idle lock or active mode). When the data switch is opened the output is in a tri-state mode with a leakage current of less than 100nA. This reduces discharge of the external integration circuit. When powered-down, the data switch will output a reference of approximately 1.6V to maintain a charge on the external RC circuit.

A Receive Signal Strength Indicator (RSSI) completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for DECT cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}

Divide by: 128/129-64/65 dual modulus low-power ECL prescaler

SA701

DESCRIPTION

The SA701 is an advanced dual modulus (Divide By 128/129 or 64/65) low power ECL prescaler. The minimum supply voltage is 2.7V and is compatible with the CMOS UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package, and is pin compatible with Fujitsu MB501, Plessey SP8704 and Motorola MC12022.

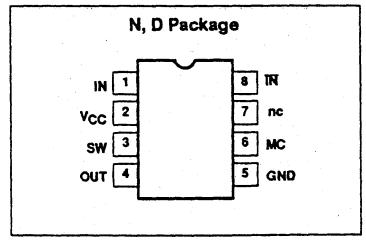
FEATURES

- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line (DIP)	-40 to +85°C	SA701N	0404B
8-Pin Plastic Small Outline (SO) (Surface-mount)	-40 to +85°C	SA701D	0174C

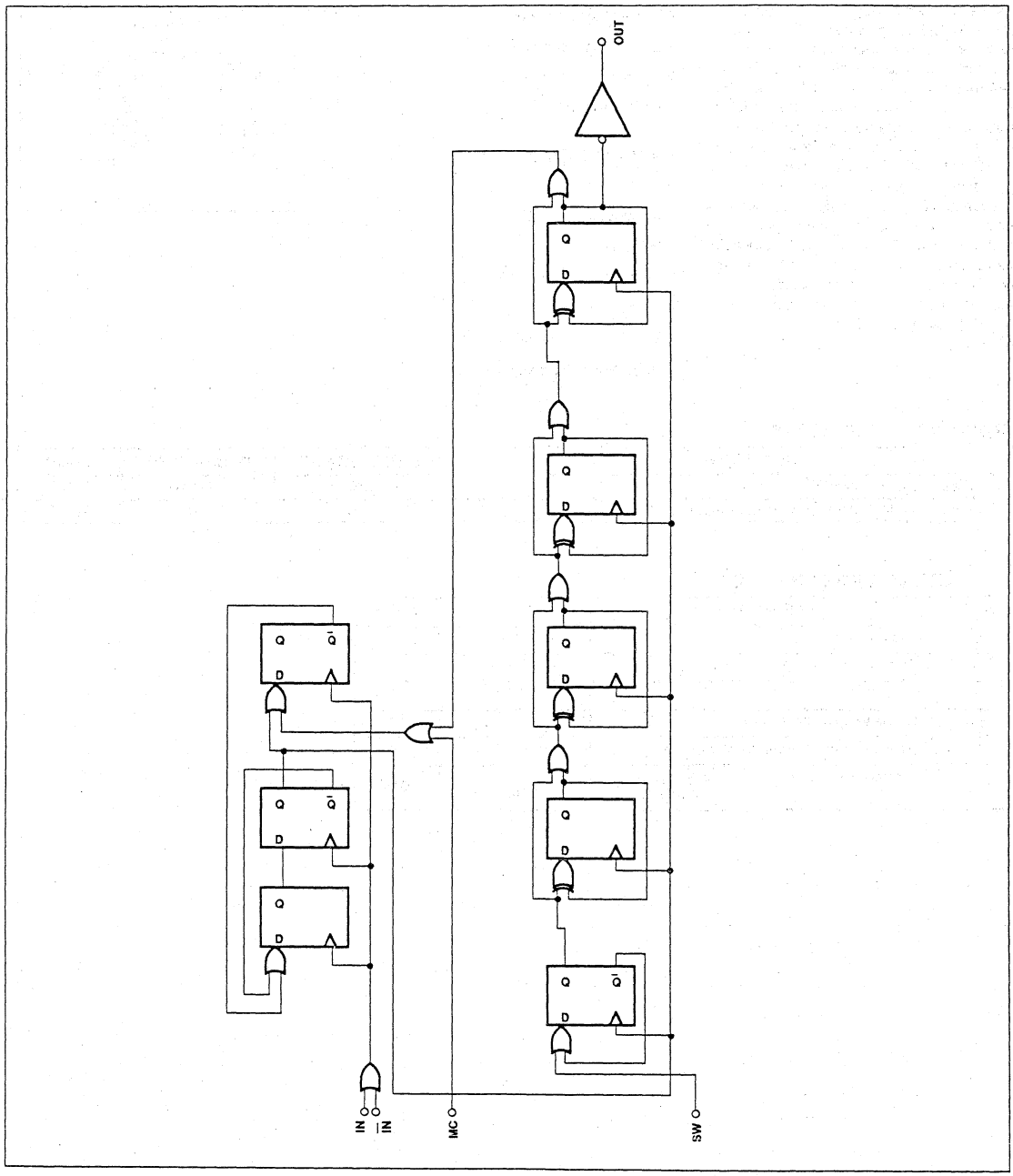
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

Divide by: 128/129-64/65 dual modulus low-power ECL prescaler

SA701

BLOCK DIAGRAM



Divide by: 128/129-64/65 dual modulus low-power ECL prescaler

SA701

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for T_A = 25°C and V_{CC} = 3.0V; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC input high threshold		2.0		V_{CC}	V
V_{IL}	MC input low threshold		–0.3		0.8	V
V_{IH}	SW input high threshold		2.0		V_{CC}	V
V_{IL}	SW input low threshold		–0.3		0.8	V
I_{IH}	MC input high current	V_{MC} = V_{CC} = 6V		0.1	50	µA
I_{IL}	MC input low current	V_{MC} = 0V, V_{CC} = 6V	–100	–30		µA
I_{IH}	SW input high current	V_{SW} = V_{CC} = 6V		35	100	µA
I_{IL}	SW input low current	V_{SW} = 0V, V_{CC} = 6V	–50	–0.1		µA

AC ELECTRICAL CHARACTERISTICS

The following AC specifications are valid for V_{CC} = 3.0V, f_{IN} = 1GHz, input level = 0dBm, T_A = 25°C; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	V_{CC} = 5.0V		1.6		V_{P-P}
		V_{CC} = 3.0V		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA701 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for SW (Modulus Set Switch) input to be set low and MC (Modulus Control) input to be set high in which case the circuit comprises a divide by 128. For divide by 129 the MC signal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. Similarly, for divide by 64 and 65 the SA701 will generate those respective moduli with the SW signal forced high, in which the fourth stage of the synchronous divider is bypassed.

A truth table for the modulus values is given below:

Table 1.

Modulus	MC	SW
128	1	0
129	0	0
64	1	1
65	0	1

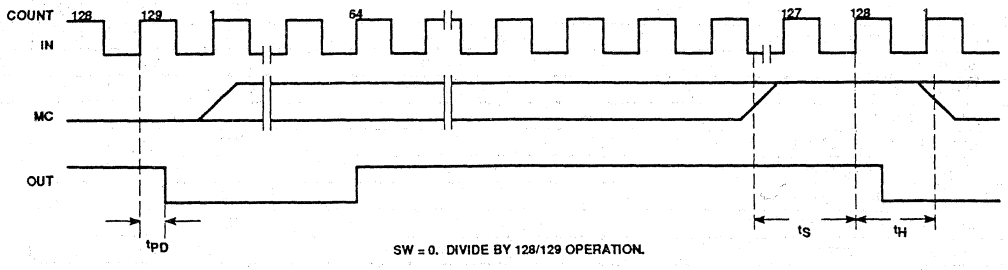
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 for modulus 128/129 or count 32 for modulus 64/65 with delay t_{PD}. The SW input is not designed for synchronous switching.

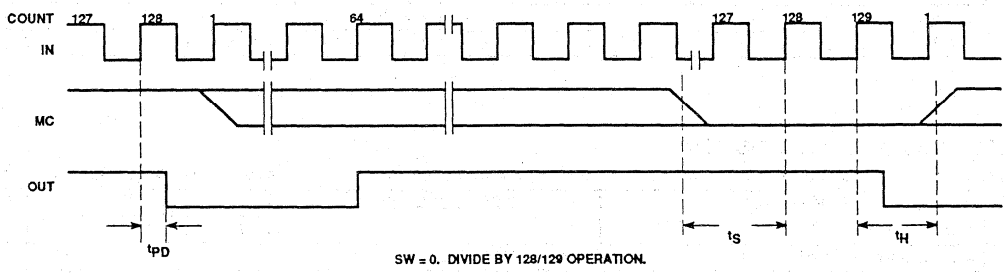
The MC and SW inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed. The SW input has an internal pull-down simplifying modulus group selection. With SW open the divide by 128/129 mode is selected and with SW connected to V_{CC} divide by 64/65 is selected.

The prescaler input is differential and ECL compatible. The output is single-ended ECL compatible.

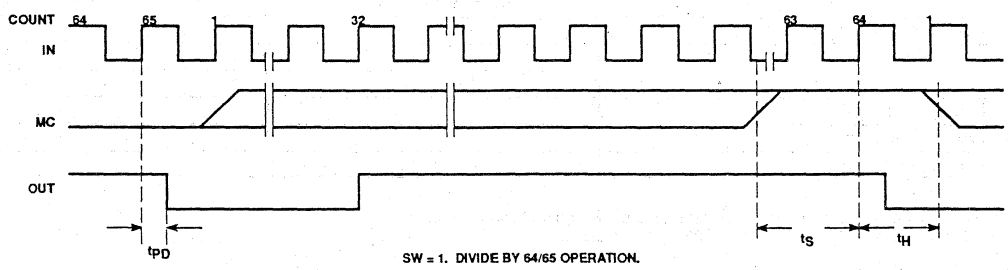
AC TIMING CHARACTERISTICS



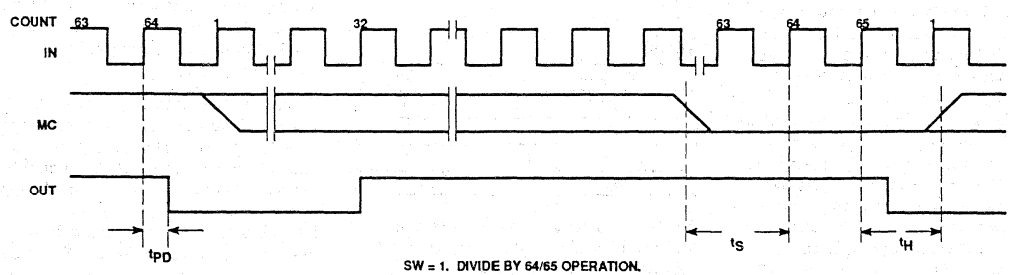
SW = 0. DIVIDE BY 128/129 OPERATION.



SW = 0. DIVIDE BY 128/129 OPERATION.



SW = 1. DIVIDE BY 64/65 OPERATION.



SW = 1. DIVIDE BY 64/65 OPERATION.

Divide by: 128/129-64/65 dual modulus low-power ECL prescaler

SA701

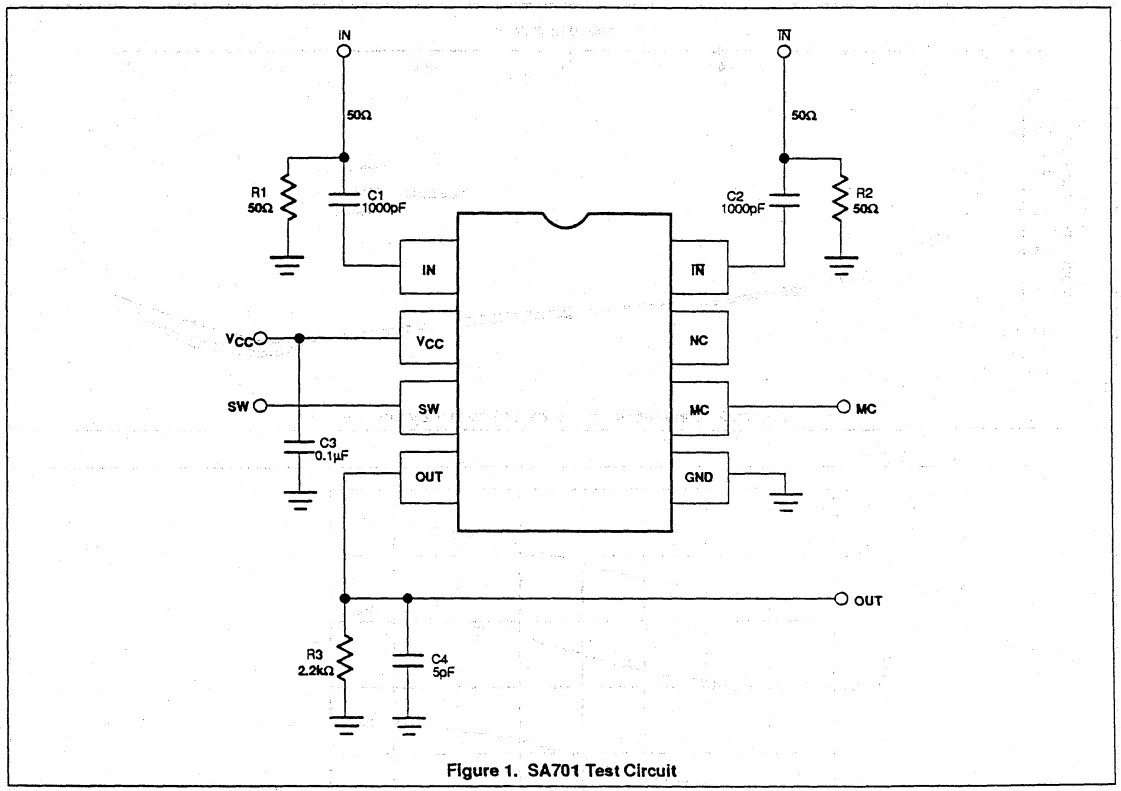


Figure 1. SA701 Test Circuit

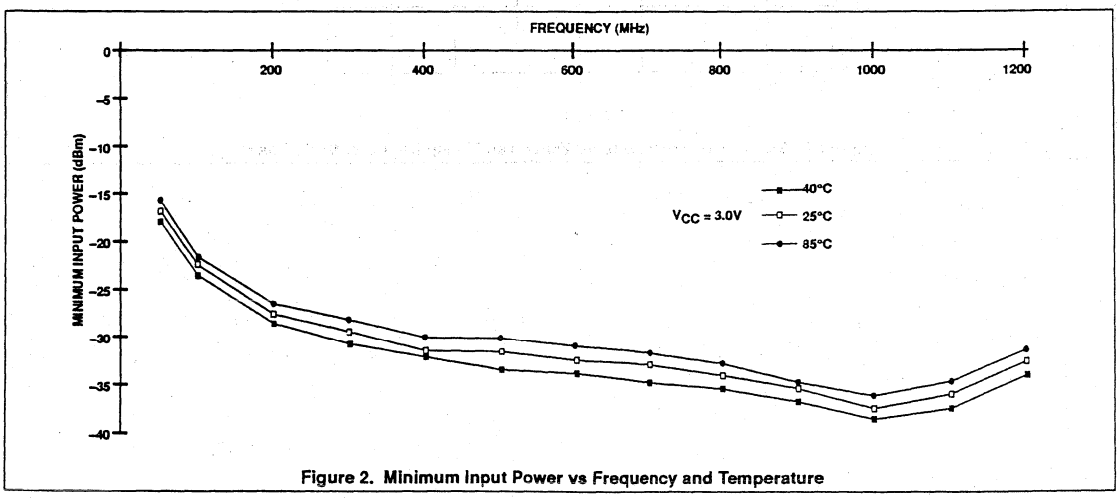


Figure 2. Minimum Input Power vs Frequency and Temperature

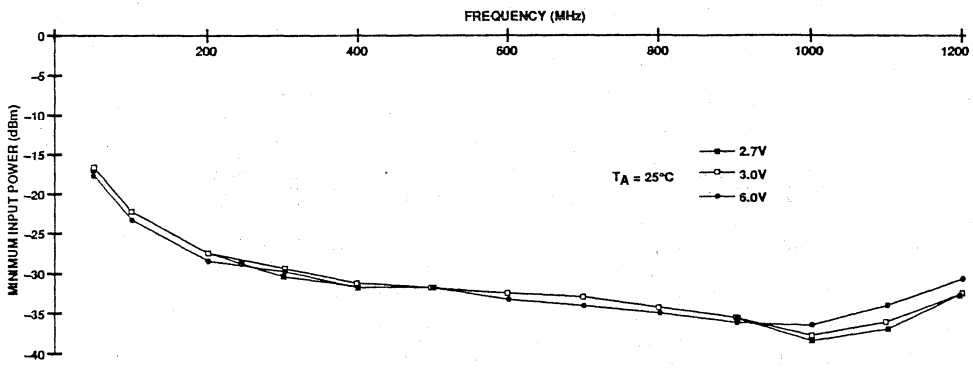


Figure 3. Minimum Input Power vs Frequency and V_{CC}

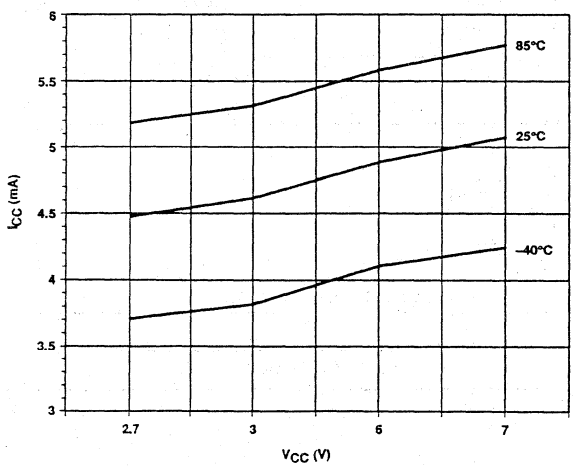
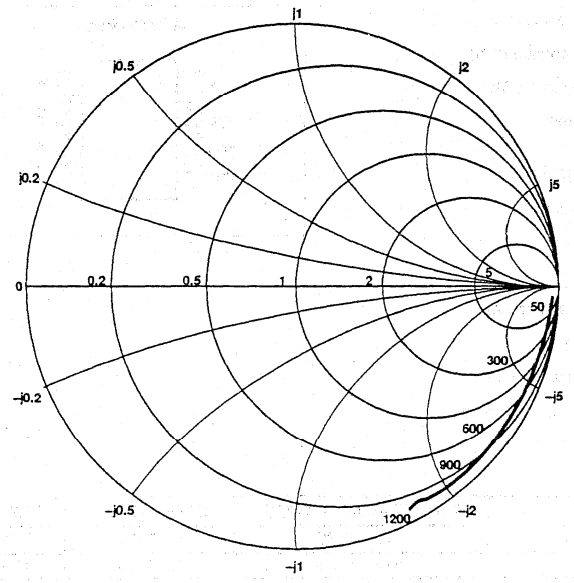


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load



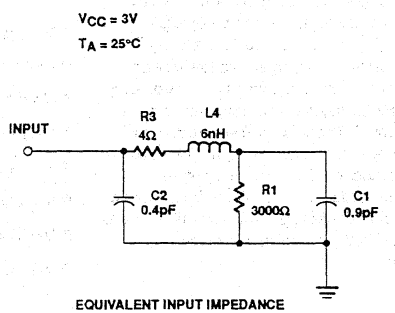
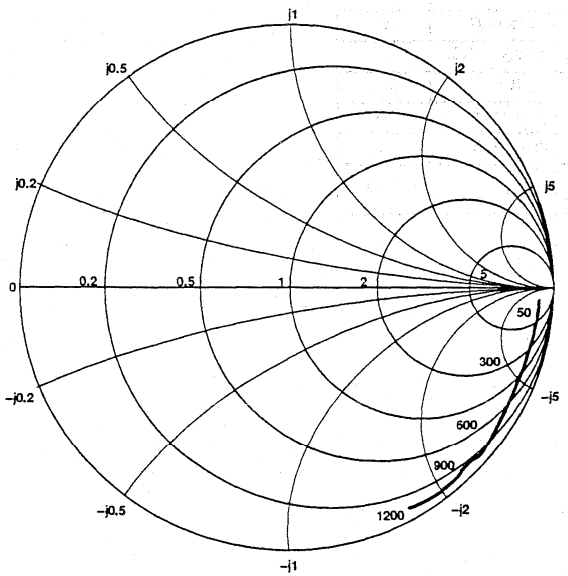


Figure 5. Typical N Package Input Impedance



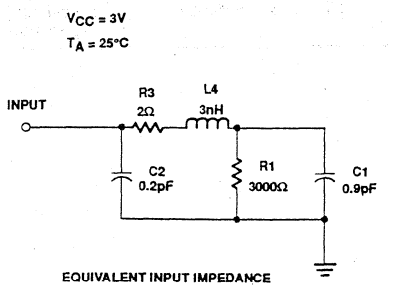


Figure 6. Typical D Package Input Impedance

Divide by: 64/65/72 triple modulus low-power ECL prescaler

SA702

DESCRIPTION

The SA702 triple modulus (Divide By 64/65/72) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.7V and is compatible with the CMOS UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package.

FEATURES

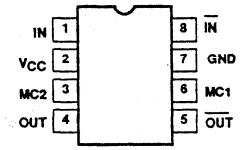
- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

N, D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line (DIP)	-40 to +85°C	SA702N	0404B
8-Pin Plastic Small Outline (SO) (Surface-mount)	-40 to +85°C	SA702D	0174C

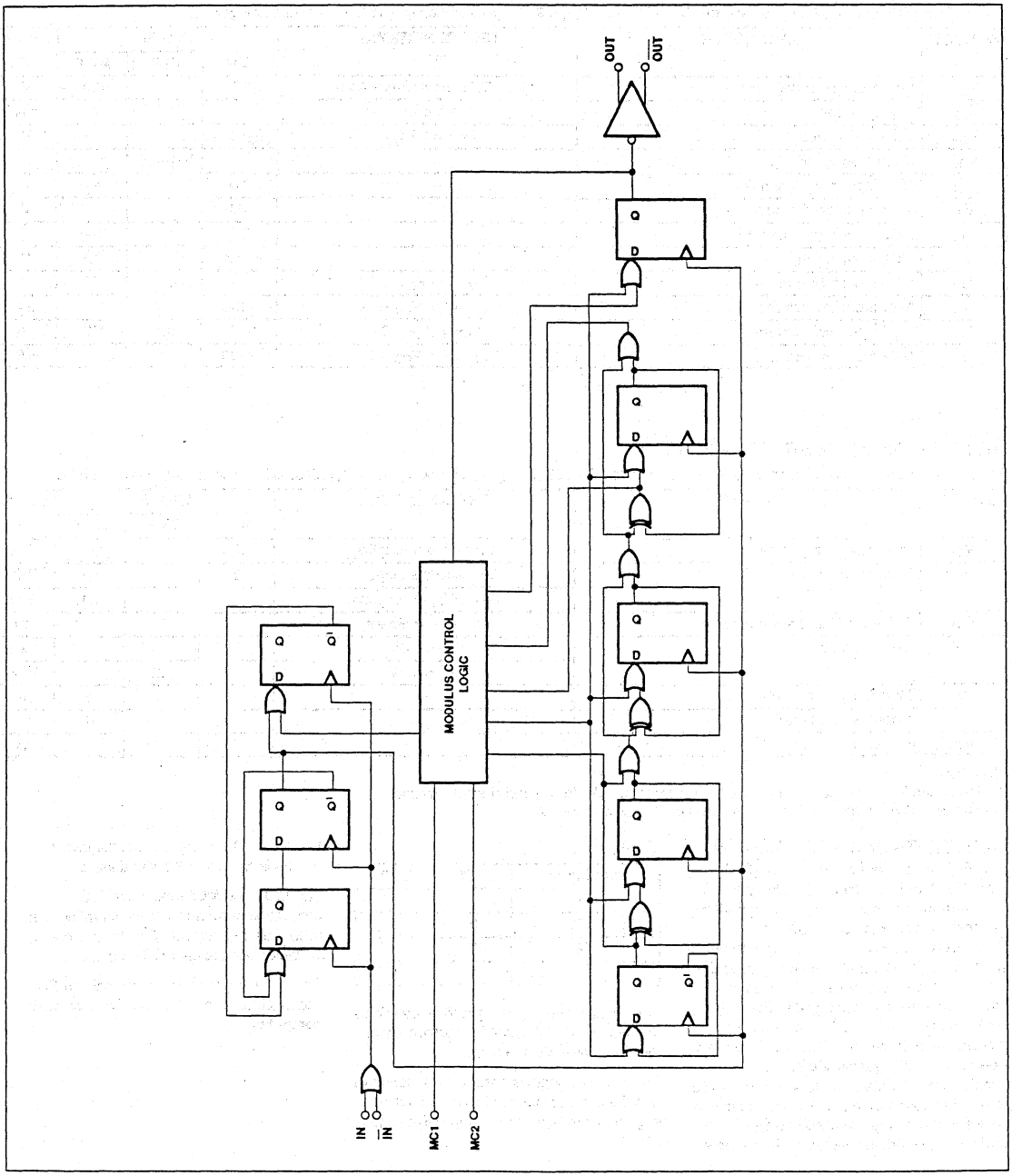
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

Divide by: 64/65/72 triple modulus low-power ECL prescaler

SA702

BLOCK DIAGRAM



Divide by: 64/65/72 triple modulus low-power ECL prescaler

SA702

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for T_A = 25°C and V_{CC} = 3.0V; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC1 input high threshold		2.0		V_{CC}	V
V_{IL}	MC1 input low threshold		–0.3		0.8	V
V_{IH}	MC2 input high threshold		2.0		V_{CC}	V
V_{IL}	MC2 input low threshold		–0.3		0.8	V
I_{IH}	MC1 input high current	V_{MC1} = V_{CC} = 6V		0.1	50	µA
I_{IL}	MC1 input low current	V_{MC1} = 0V, V_{CC} = 6V	–100	–30		µA
I_{IH}	MC2 input high current	V_{MC2} = V_{CC} = 6V		0.1	50	µA
I_{IL}	MC2 input low current	V_{MC2} = 0V, V_{CC} = 6V	–100	–30		µA

AC ELECTRICAL CHARACTERISTICS

These AC specifications are valid for f_{IN} = 1GHz, input level = 0dBm, V_{CC} = 3.0V and T_A = 25°C; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	V_{CC} = 5.0V		1.6		V_{P-P}
		V_{CC} = 3.0V		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA702 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 64. For divide by 65 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. For divide by 72, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 18. A truth table for the modulus values is given below:

Table 1.

Modulus	MC1	MC2
64	1	0
65	0	0
72	0	1
72	1	1

For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

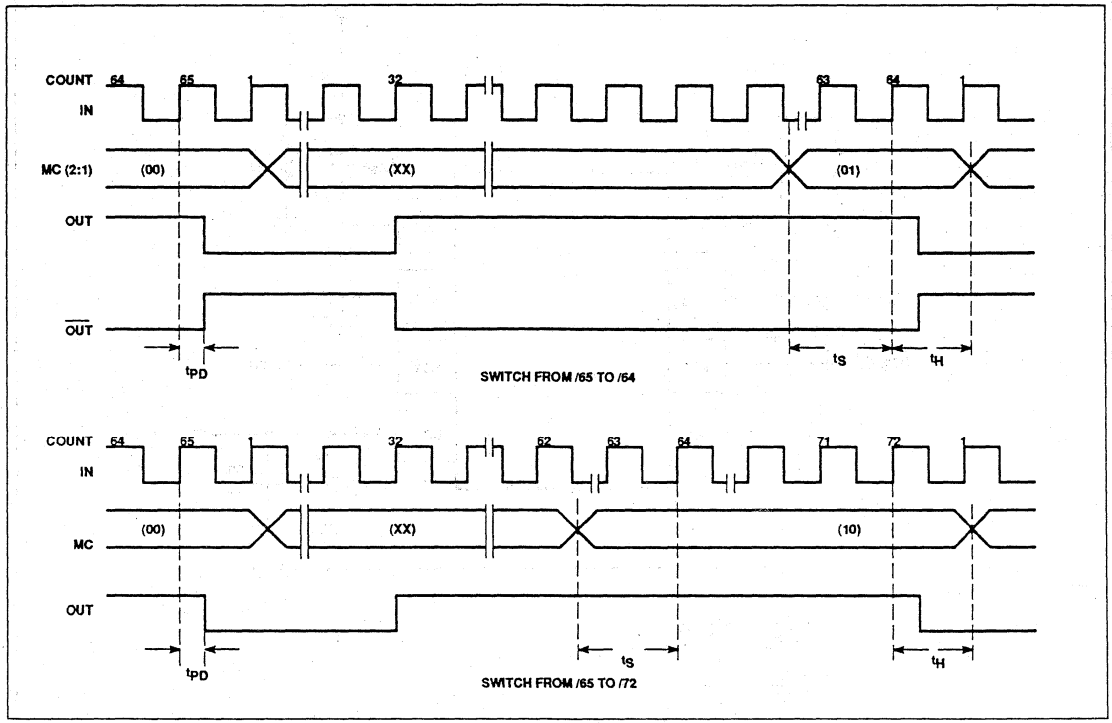
The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 32 with delay t_{PD}.

The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

Divide by: 64/65/72 triple modulus low-power ECL prescaler

AC TIMING CHARACTERISTICS



Divide by: 64/65/72 triple modulus low-power ECL prescaler

SA702

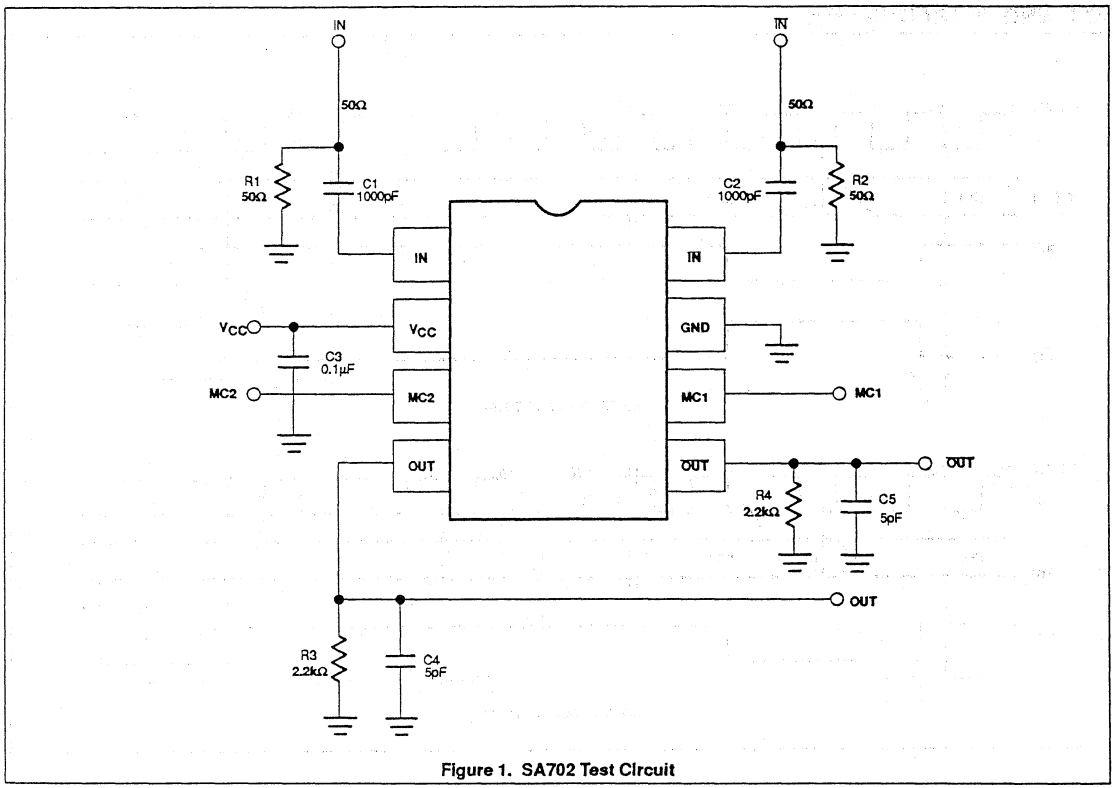


Figure 1. SA702 Test Circuit

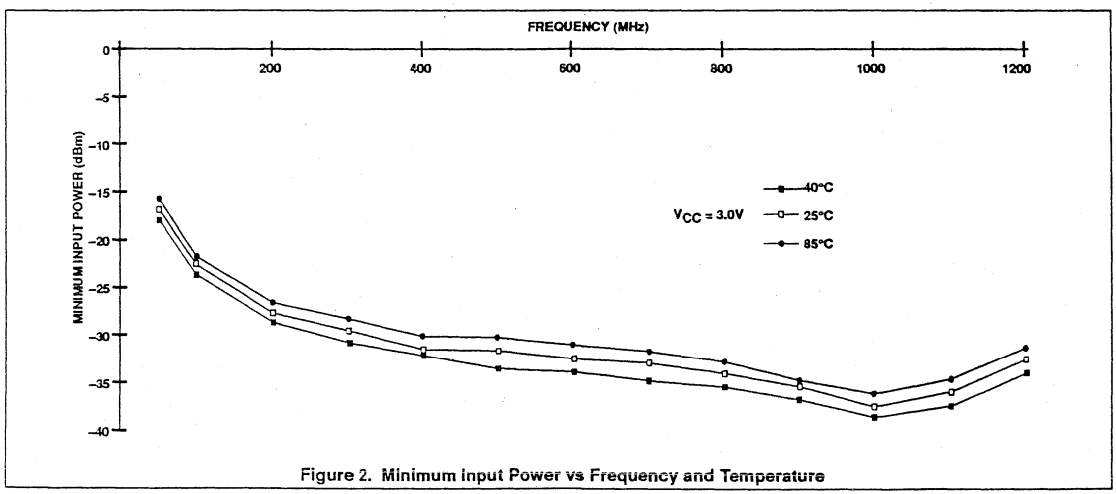


Figure 2. Minimum Input Power vs Frequency and Temperature

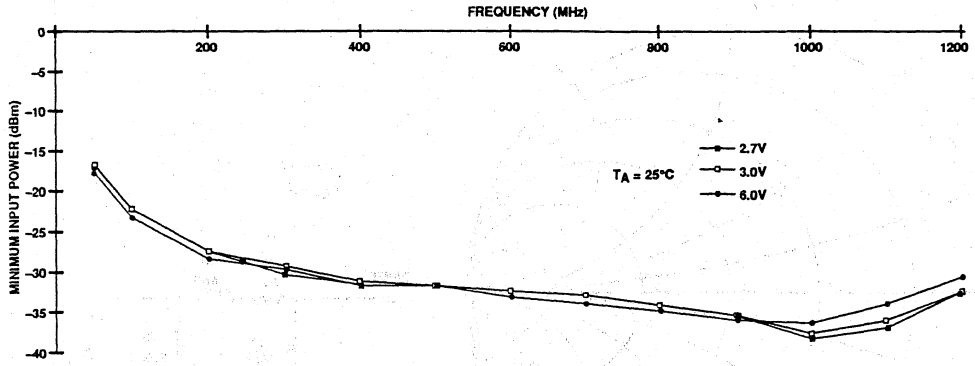


Figure 3. Minimum Input Power vs Frequency and V_{CC}

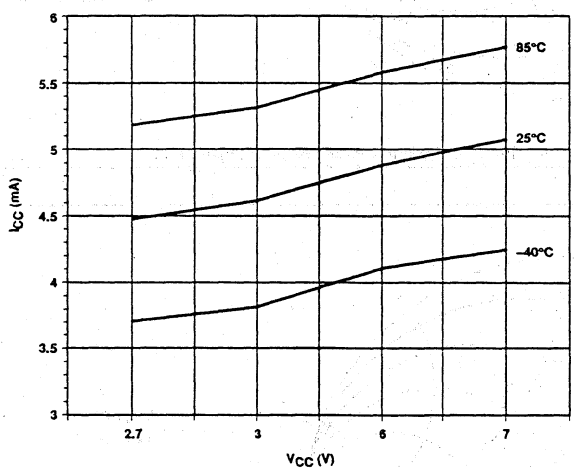
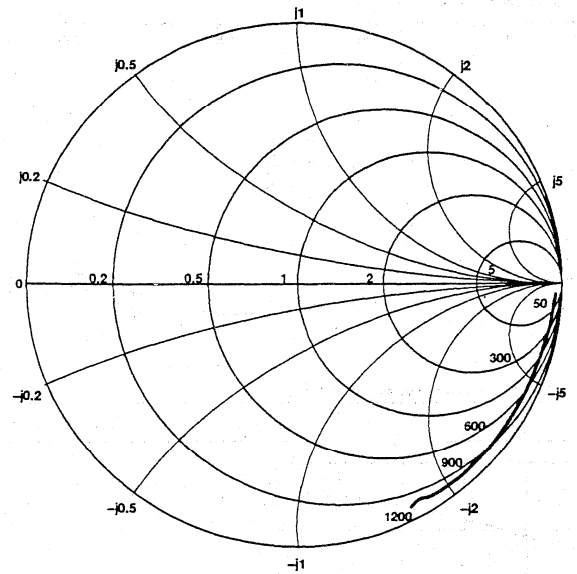


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load



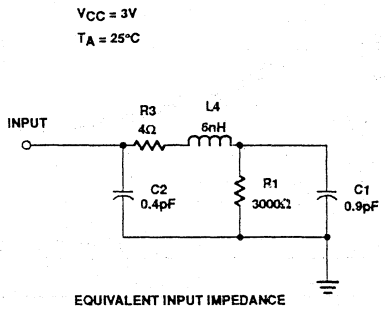
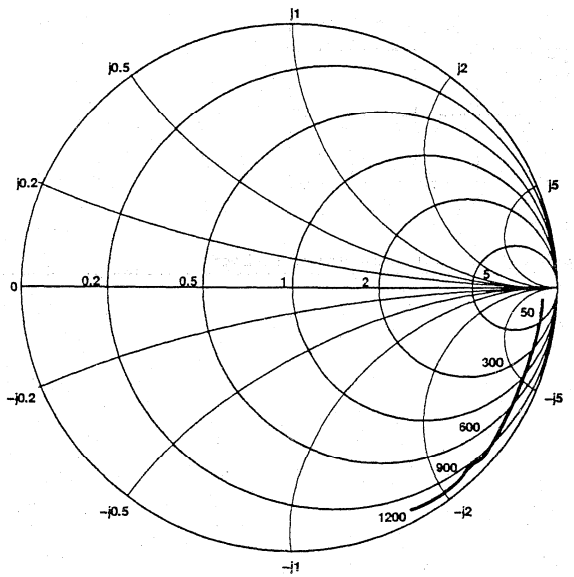


Figure 5. Typical N Package Input Impedance



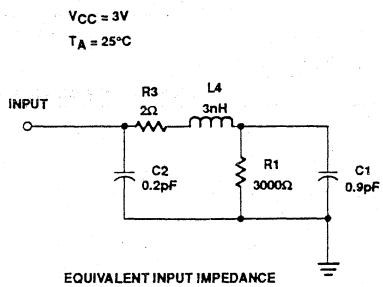


Figure 6. Typical D Package Input Impedance

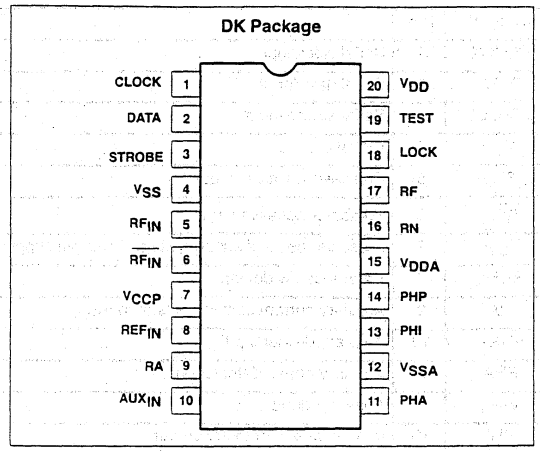
Low-voltage 1GHz fractional-N synthesizer

SA7025

DESCRIPTION

The SA7025 is a monolithic low power, high performance dual frequency synthesizer fabricated in QUBiC BiCMOS technology. Featuring Fractional-N division with selectable modulo 5 or 8 implemented in the Main synthesizer to allow the phase detector comparison frequency to be five or eight times the channel spacing. This feature reduces the overall division ratio yielding a lower noise floor and faster channel switching. The phase detectors and charge pumps are designed to achieve phase detector comparison frequencies up to 5MHz. A triple modulus prescaler (divide by 64/65/72) is integrated on chip with a maximum input frequency of 1.0GHz. Programming and channel selection are realized by a high speed 3-wire serial interface.

PIN CONFIGURATION



FEATURES

- Operation up to 1.0GHz
- Fast locking by "Fractional-N" divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High speed serial input
- Low power consumption
- Programmable charge pump currents
- Supply voltage range 2.7 to 5.5V
- Excellent input sensitivity:
  V_{RF_IN} = –20dBm

APPLICATIONS

- ADC (American Digital Cellular)
- Cellular radio
- Spread-spectrum receivers
- Portable communication systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA7025DK	1563

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V	Supply voltage, V_{DD}, V_{DDA}, V_{CCP}	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{DD} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W.

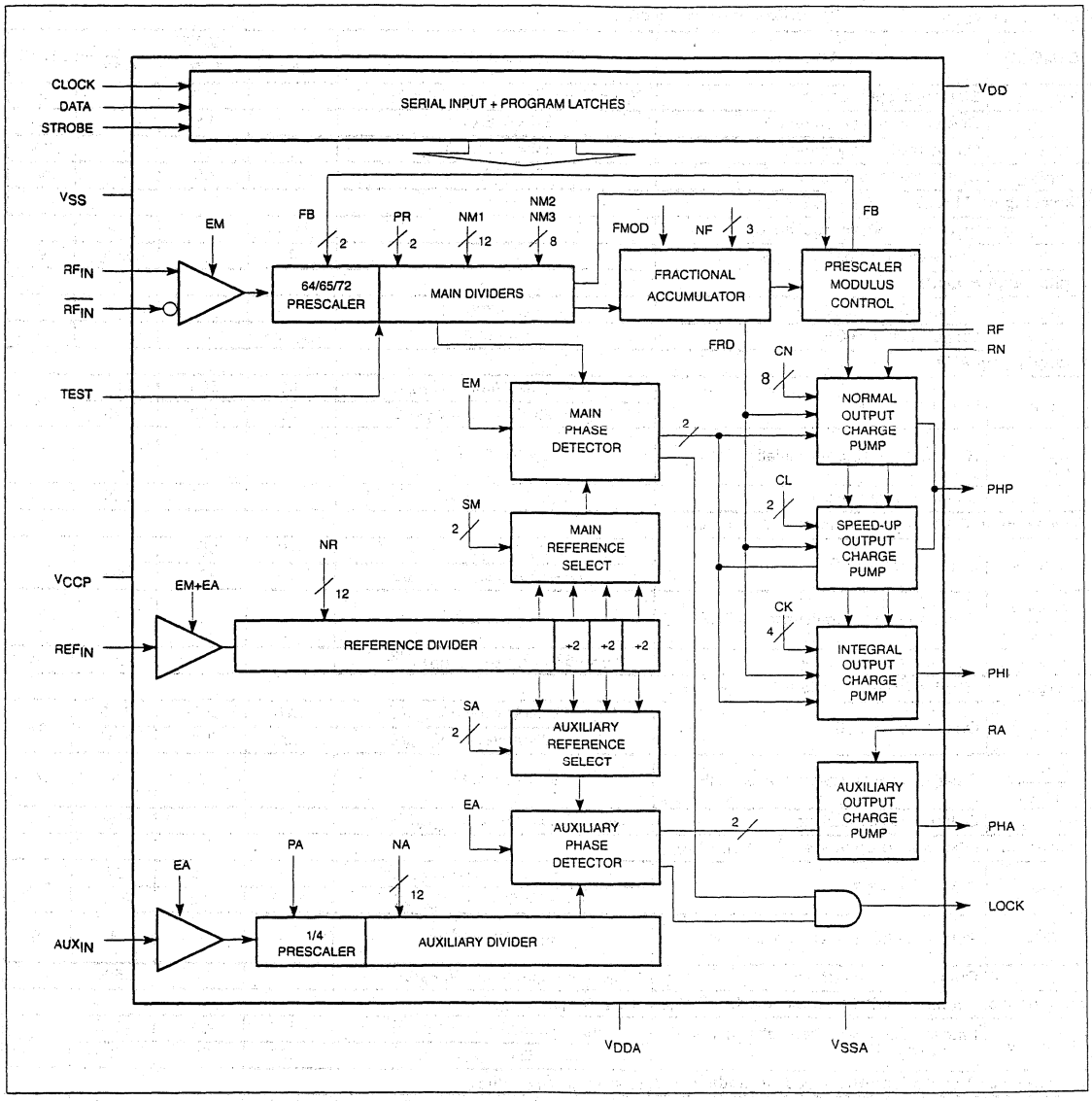
PIN DESCRIPTIONS

Symbol	Pin	Description
CLOCK	1	Serial clock input
DATA	2	Serial data input
STROBE	3	Serial strobe input
V_{SS}	4	Digital ground
RF_{IN}	5	Prescaler positive input
$\overline{RF_{IN}}$	6	Prescaler negative input
V_{CCP}	7	Prescaler positive supply voltage. This pin supplies power to the prescaler and RF input buffer
REF_{IN}	8	Reference divider input
RA	9	Auxiliary current setting; resistor to V_{SSA}
AUX_{IN}	10	Auxiliary divider input
PHA	11	Auxiliary phase detector output
V_{SSA}	12	Analog ground
PHI	13	Integral phase detector output
PHP	14	Proportional phase detector output
V_{DDA}	15	Analog supply voltage. This pin supplies power to the charge pumps, Auxiliary prescaler, Auxiliary and Reference buffers.
RN	16	Main current setting; resistor to V_{SSA}
RF	17	Fractional compensation current setting; resistor to V_{SSA}
LOCK	18	Lock detector output
TEST	19	Test pin; connect to V_{DD}
V_{DD}	20	Digital supply voltage. This pin supplies power to the CMOS digital part of the device

Low-voltage 1GHz fractional-N synthesizer

SA7025

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
$I_{STANDBY}$	Standby supply currents	$V_{RA} = V_{RF} = V_{RN} = V_{DDA}$. EM = EA = 0		100		µA
I_{AUX}	Operational supply currents[5]	EM = 0, EA = 1		3.5		mA
I_{MAIN}	Operational supply currents[5]	EM = 1, EA = 0		5.5		mA
I_{TOTAL}	Operational supply currents[5]	EM = EA = 1		7.5		mA
Digital inputs CLK, DATA, STROBE						
V_{IH}	High level input voltage range		0.7xV_{DD}		V_{DD}	V
V_{IL}	Low level input voltage range		0		0.3xV_{DD}	V
Digital outputs LOCK						
V_{OL}	Output voltage LOW	I_O = 2mA			0.4	V
V_{OH}	Output voltage HIGH	I_O = −2mA	V_{DD}−0.4			V
Charge pump PHA						
$\lvert I_{PHA}\rvert$	Output current PHA	$I_{RA} = -62.5µA$; $V_{PHA} = V_{DDA}/2^{13}$	400	500	600	µA
		$I_{RA} = -25µA$; $V_{PHA} = V_{DDA}/2$	160	200	240	
$\frac{\Delta I_{PHP\_A}}{\lvert I_{PHP\_A}\rvert}$	Relative output current variation PHA	$I_{RA} = -62.5µA$[2, 13]		2	6	%
ΔI_{PHA_M}	Output current matching	$I_{RA} = -62.5µA$; $V_{PHA} = V_{DDA}/2^{12, 13}$			±50	µA
Charge pump PHP, normal mode[1, 4, 6] $V_{RF} = V_{DDA}$						
$\lvert I_{PHP\_N}\rvert$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2^{13}$	440	550	660	µA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	175	220	265	
$\frac{\Delta I_{PHP\_N}}{I_{PHP\_N}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$[2, 13]		2	6	%
$\Delta I_{PHP\_N\_M}$	Output current matching	$I_{RN} = -62.5µA$;$V_{PHP} = V_{DDA}/2^{12, 13}$			±50	µA
Charge pump PHP, speed-up mode [1, 4, 7] $V_{RF} = V_{DDA}$						
$\lvert I_{PHP\_S}\rvert$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2^{13}$	2.20	2.75	3.30	mA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	0.85	1.1	1.35	
$\frac{\Delta I_{PHP\_S}}{I_{PHP\_S}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$[2, 13]		2	6	%
$\Delta I_{PHP\_S\_M}$	Output current matching	$I_{RM} = -62.5µA$;$V_{PHP} = V_{DDA}/2^{12, 13}$			±250	µA
Charge pump PHI, speed-up mode [1, 4, 8] $V_{RF} = V_{DDA}$						
$\lvert I_{PHI}\rvert$	Output current PHI	$I_{RN} = -62.5µA$; $V_{PHI} = V_{DDA}/2^{13}$	4.4	5.5	6.6	mA
		$I_{RN} = -25µA$; $V_{PHI} = V_{DDA}/2$	1.75	2.2	2.65	
$\frac{\Delta I_{PHI}}{I_{PHI}}$	Relative output current variation PHI	$I_{RN} = -62.5µA$[2, 13]		2	8	%
ΔI_{PHI_M}	Output current matching	$I_{RN} = -62.5µA$; $V_{PHI} = V_{DDA}/2^{12, 13}$			±500	µA
Fractional compensation PHP, normal mode [1, 9] $V_{RN} = V_{DDA}$, $V_{PHP} = V_{DDA}/2$						
$I_{PHP\_F\_N}$	Fractional compensation output current PHP vs F_{RD}[3]	$I_{RF} = -62.5µA$;F_{RD} = 1 to 7^{13}	−675	−500	−325	nA
		$I_{RF} = -25µA$;F_{RD} = 1 to 7	−270	−200	−130	
Fractional compensation PHP, speed up mode [1, 10] $V_{PHP} = V_{DDA}$, $V_{RN} = V_{DDA}$						
$I_{PHP\_F\_S}$	Fractional compensation output current PHP vs F_{RD}[3]	$I_{RF} = -62.5µA$;F_{RD} = 1 to 7^{13}	−3.35	−2.5	−1.65	µA
		$I_{RF} = -25µA$;F_{RD} = 1 to 7	−1.35	−1.0	−0.65	
Fractional compensation PHI, speed up mode [1, 11] $V_{PHP} = V_{DDA}/2$, $V_{RN} = V_{DDA}$						
I_{PHI_F}	Fractional compensation output current PHI vs F_{RD}[3]	$I_{RF} = -62.5µA$;F_{RD} = 1 to 7^{13}	−5.4	−4.0	−2.6	µA
		$I_{RF} = -25µA$;F_{RD} = 1 to 7	−2.15	−1.6	−1.05	

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Charge pump leakage currents, charge pump not active						
I_{PHP_L}	Output leakage current PHP; normal mode[1]	V_{PHP} = 0.7 to V_{DDA} – 0.8		0.1	10	nA
I_{PHI_L}	Output leakage current PHI; normal mode[1]	V_{PHI} = 0.7 to V_{DDA} – 0.8		0.1	10	nA
I_{PHA_L}	Output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} – 0.8		0.1	10	nA

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP}$ = 3V; T_A = 25°C; f_{RF_IN} = 1GHz, input level = –10dBm; unless otherwise specified. Test Circuit, Figure 2. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Main divider						
f_{RF_IN}	Input signal frequency	Direct coupled input[14]	0		1.0	GHz
		1000pF input coupling			1.0	
V_{RF_IN}	Input sensitivity		–20		0	dBm
Reference divider						
f_{REF_IN}	Input signal frequency		0		20	MHz
		4.5V ≤ V_{DDA} ≤ 5.5V	0		30	
V_{REF_IN}	Input signal range, AC coupled		300			mV_{P-P}
Z_{REF_IN}	Reference divider input impedance			100		kΩ
					3	pF
Auxiliary divider						
f_{AUX_IN}	Input signal frequency		0		50	MHz
	PA = "0", prescaler enabled	4.5V ≤ V_{DDA} ≤ 5.5V	0		150	
	Input signal frequency		0		30	
	PA = "1", prescaler disabled	4.5V ≤ V_{DDA} ≤ 5.5V	0		40	
V_{AUX_IN}	Input signal range, AC coupled		200			mV_{P-P}
Z_{AUX_IN}	Auxiliary divider input impedance			100		kΩ
					3	pF
Serial interface[15]						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time; CLOCK to DATA		30			ns
t_W	Pulse width; CLOCK		30			ns
	Pulse width; STROBE	B, C, D, E words	30			
t_{SW}	Pulse width; STROBE	A word, PR = '01'	$\frac{1}{f_{VCO}} \cdot (NM2 \cdot 65) + t_W$			ns
		A word, PR = '10'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM3 + 1) \cdot 72] + t_W$			

NOTES:

1. When a serial input "A" word is programmed, the main charge pumps on PHP and PHI are in the "speed up mode" as long as STROBE = H. When this is not the case, the main charge pumps are in the "normal mode".
2. The relative output current variation is defined thus:
$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|}$$ with $V_1 = 0.7V$, $V_2 = V_{DDA} - 0.8V$ (see Figure 1).
3. F_{RD} is the value of the 3 bit fractional accumulator.
4. Monotonicity is guaranteed with $C_N = 0$ to 255.
5. Power supply current measured with $f_{REF\ IN}$ = 953.19MHz, NM1 = 48, NM2 = 3, NM3 = 7, NF = 5, FMOD = 8, N = 3971+5/8, main phase detector frequency = 240kHz, $f_{REF\ IN}$ = 21.36MHz, NR = 89, SM = 1, $f_{AUX\ IN}$ = 82.56MHz, NA = 86, SA = 2, PA = 0, auxiliary phase detector frequency = 120kHz, IRN = IRA = IRF = 25µA, CN = 160, CL = 0, CK = 0, lock condition, normal mode, V_{DDA} = 5V, $V_{DD} = V_{CCP}$ = 3V. Operational supply current = $I_{DDA} + I_{DD} + I_{CCP}$.
6. Specification condition: CN = 255
7. Specification conditions:
   1) CN = 255; CL = 1, or
   2) CN = 75; CL = 3
8. Typical output current $|I_{PHI}| = -I_{RN} \times CN \times 2^{(CL+1)} \times CK/32$:
   1) CN = 160; CL = 3; CK = 1, or
   2) CN = 160; CL = 2; CK = 2, or
   3) CN = 160; CL = 1; CK = 4, or
   4) CN = 160; CL = 0; CK = 8
9. Specification condition: F_{RD} = 1 to 7.
10. Specification conditions: F_{RD} = 1 to 7; CL = 1.
11. Specification conditions:
    1) F_{RD} = 1 to 7; CL = 1; CK = 2, or
    2) F_{RD} = 1 to 7; CL = 2; CK = 1.
12. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on.
13. Limited analog supply voltage range 4.5 to 5.5V.
14. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.
15. Guaranteed by design.

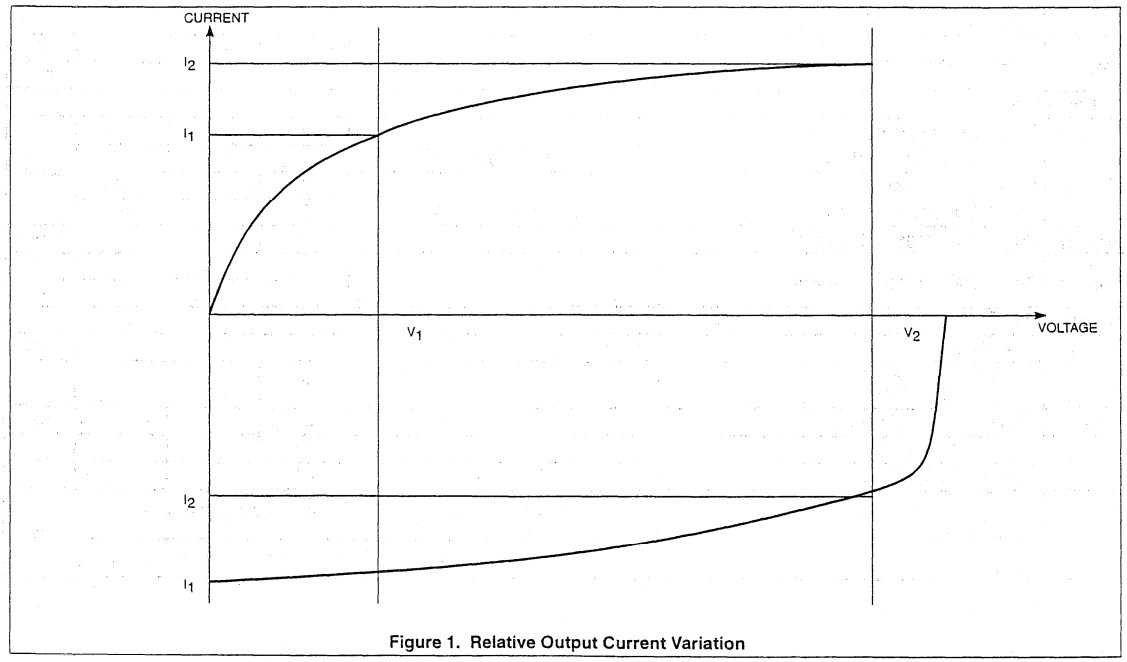


Figure 1. Relative Output Current Variation

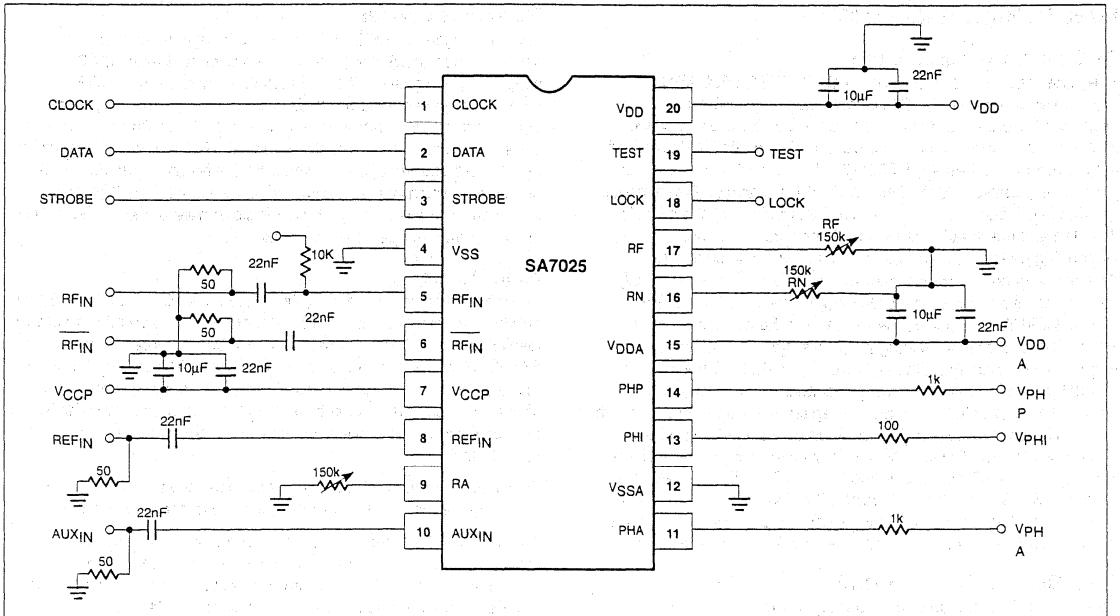


Figure 2. Test Circuit

AC TIMING CHARACTERISTICS

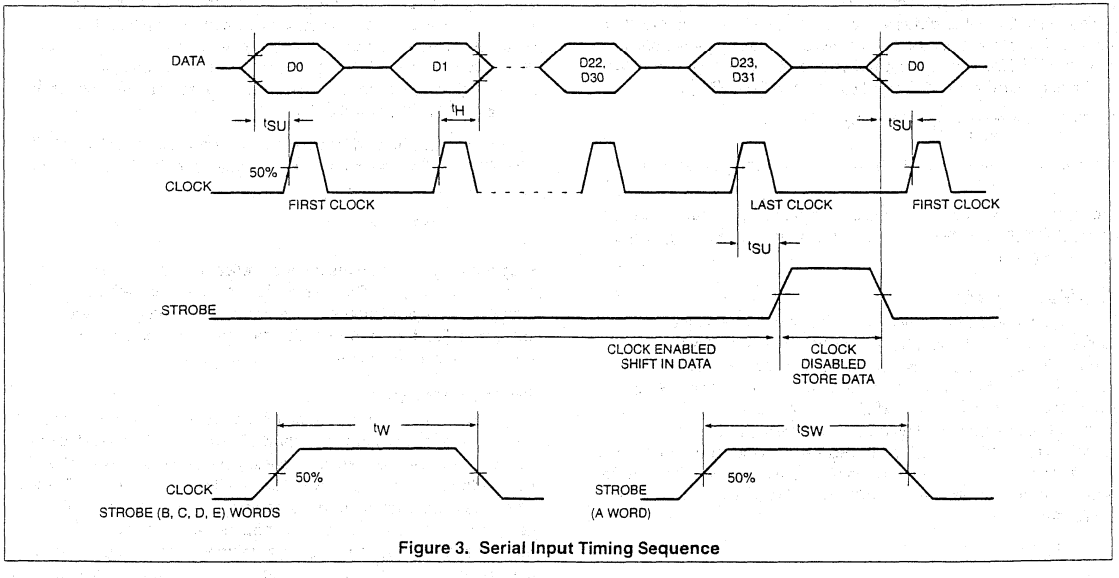


Figure 3. Serial Input Timing Sequence

FUNCTIONAL DESCRIPTION

Serial Input Programming

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32 bit words; each word includes 1 or 4 address bits. Figure 3 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent: D, C, B and A. Figure 4 and Table 1 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for CN and PR is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24 bit A0 word is used. CN will be directly loaded by programming a long 32 bit A1 word. The flag LONG in the D word determines whether A0 (LONG = "0") or A1 (LONG = "1") format is applicable. The A word contains new data for the main divider.

Main Divider Synchronization

The A word is loaded only when a main divider synchronization signal is also active in order to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. The signal is active while the NM1 divider is counting down from the programmed value. The new A word will be loaded after the NM1 divider has reached its terminal count; also, at this time a main divider output pulse will be sent to the main phase detector. The loading of the A word is disabled while the NM2 or NM3 dividers are counting up to their programmed values. Therefore, the new A word will be correctly loaded provided that the STROBE signal has been at an active high value for at least a minimum number of VCO input cycles at RF_{IN} or $\overline{RF_{IN}}$.

$$t\_strobe\_min = \frac{1}{f_{VCO}}(NM_2 \cdot 65) + t_W \text{ for } PR = '01'$$

$$t\_strobe\_min = \frac{1}{f_{VCO}}[NM_2 \cdot 65 + (NM_3 + 1) \cdot 72] + t_W \text{ for } PR = '10'$$

Programming the A word means also that the main charge pumps on output PHP and PHI are set into the speed-up mode as long as the STROBE is H.

Auxiliary Divider

The input signal on AUX_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled if the serial control bit EA = "1". Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = "0". This divider has been optimized to accept a high frequency input signal. If PA = "1", this divider is disabled and the input signal is fed directly to the second stage, which is a 12-bit programmable divider with standard input frequency (40MHz). The division ratio can be expressed as:

if PA = "0": N = 4 x NA

if PA = "1": N = NA; with NA = 4 to 4095

Reference Divider

The input signal on REF_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 4095) followed by a three bit binary counter. The 2 bit SM register (see Figure 5) determines which of the 4 output pulses is selected as the main phase detector input. The 2 bit SA register determines the selection of the auxiliary phase detector signal.

Main Divider

The differential inputs are amplified (to internal ECL logic levels) and provide excellent sensitivity (–20dBm at 1GHz) making the prescaler ideally suited to directly interface to a VCO as integrated on the SA620 RF gain stage, VCO and mixer device. The internal triple modulus prescaler feedback loop FB controls the selection of the divide by ratios 64/65/72, and reduces the minimum system division ratio below the typical value required by standard dual modulus (64/65) devices.

This input stage is enabled when serial control bit EM = "1". Disabling means that all currents in the prescaler are switched off.

The main divider is built up by a 12 bit counter plus a sign bit. Depending on the serial input values NM1, NM2, NM3, and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles according to Table 2 and Table 3.

The loading of the work registers NM1, NM2, NM3 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as explained in the Serial Input Programming section.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = "1". Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider will then be

$$NQ = N + \frac{NF}{Q}$$

Programming a fraction means the prescaler with main divider will divide by N or N + 1. The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

Phase Detectors

The auxiliary and main phase detectors are a two D-type flip-flop phase and frequency detector shown in Figure 6. The flip-flops are set by the negative edges of output signals of the dividers. The rising edge of the signal, L, will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

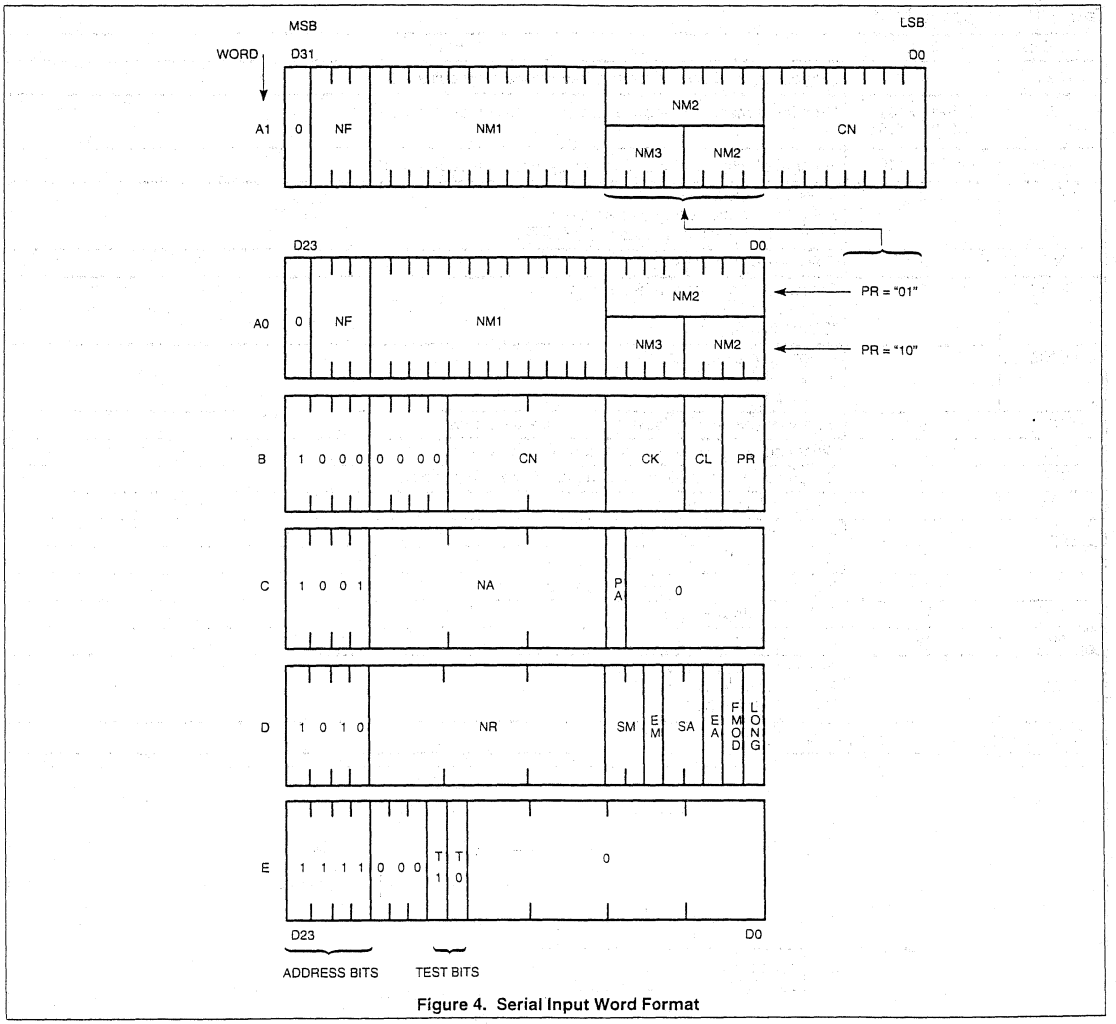


Figure 4. Serial Input Word Format

Current Settings

The SA7025 has 3 current setting pins: RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current connected between the current setting pin and V_{SS}. The typical value R (current setting resistor) can be calculated with the formula:

$$R = \frac{V_{DDA} - 0.9 - 150\sqrt{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary Output Charge Pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor RA at pin RA. The active charge pump current is typically:

$$|I_{PHA}| = 8 \cdot I_{RA}$$

Main Output Charge Pumps and Fractional Compensation Currents

The main charge pumps on pin PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 7 shows the waveforms for a typical case.

Table 1. Function Table

Symbol	Bits	Function
NM1	12	Number of main divider cycles when prescaler modulus = 64*
NM2	8 if PR = "01" 4 if PR = "10"	Number of main divider cycles when prescaler modulus = 65*
NM3	4 if PR = "10"	Number of main divider cycles when prescaler modulus = 72*
PR	2	Prescaler type in use PR = "01": modulus 2 prescaler (64/65) PR = "10": modulus 3 prescaler (64/65/72)
NF	3	Fractional-N increment
FMOD	1	Fractional-N modulus selection flag "1": modulo 8 "0": modulo 5
LONG	1	A word format selection flag "0": 24 bit A0 format "1": 32 bit A1 format
CN	8	Binary current setting factor for main charge pumps
CL	2	Binary acceleration factor for proportional charge pump current
CK	4	Binary acceleration factor for integral charge pump current
EM	1	Main divider enable flag
EA	1	Auxiliary divider enable flag
SM	2	Reference select for main phase detector
SA	2	Reference select for auxiliary phase detector
NR	12	Reference divider ratio
NA	12	Auxiliary divider ratio
PA	1	Auxiliary prescaler mode: PA = "0": divide by 4 PA = "1": divide by 1

*Not including reset cycles and Fractional-N effects.

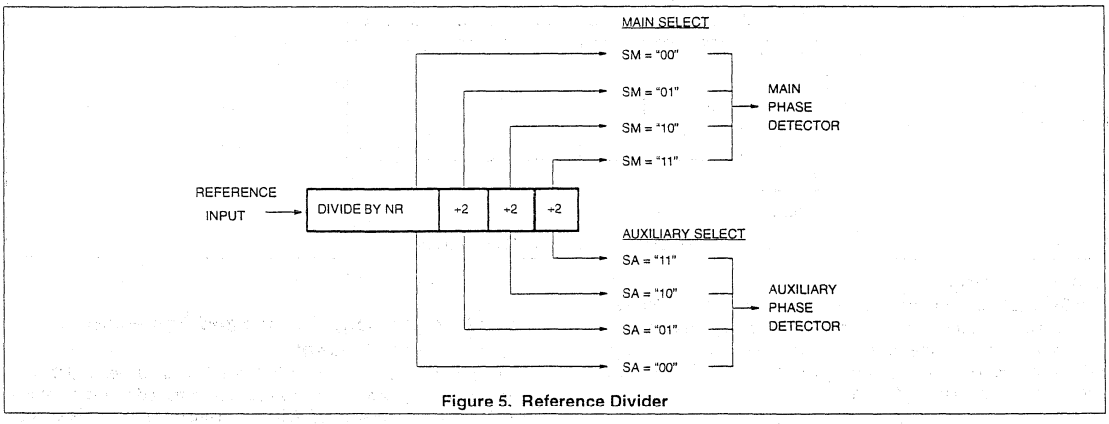


Figure 5. Reference Divider

Table 2. Prescaler Ratio

The total division ratio from prescaler to the phase detector may be expressed as:	
if PR = "01"	N = (NM1 + 2) x 64 + NM2 x 65 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 (*)
if PR = "10"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 72 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 72 (*)
(*) When the fractional accumulator overflows the prescaler ratio = 65 (64 + 1) and the total division ratio N' = N + 1	

Table 3. PR Modulus

PR	Modulus Prescaler	Bit Capacity		
		NM1	NM2	NM3
01	2	12	8	–
10	3	12	4	4

When the serial input A word is loaded, the output circuits are in the "speed-up mode" as long as the STROBE is H, else the "normal mode" is active. In the "normal mode" the current output PHP is:

$$I_{PHP\_N} = I_{PHP} + I_{PHP\_comp}$$

where:

$$|I_{PHP}| = \frac{CN \cdot I_{RN}}{32} \quad \text{:charge pump current}$$

$$|I_{PHP\_comp}| = FRD \cdot \frac{I_{RF}}{128} \quad \text{:fractional comp. current}$$

The current in PHI is zero in "normal mode".

In "speed-up mode" the current in output PHP is:

$$I_{PHP\_S} = I_{PHP} + I_{PHP\_comp}$$

$$|I_{PHP}| = \left(\frac{CN \cdot I_{RN}}{32}\right)(2^{CL+1} + 1)$$

$$|I_{PHP\_comp}| = \left(\frac{F_{RD} \cdot I_{RF}}{128}\right)(2^{CL+1} + 1)$$

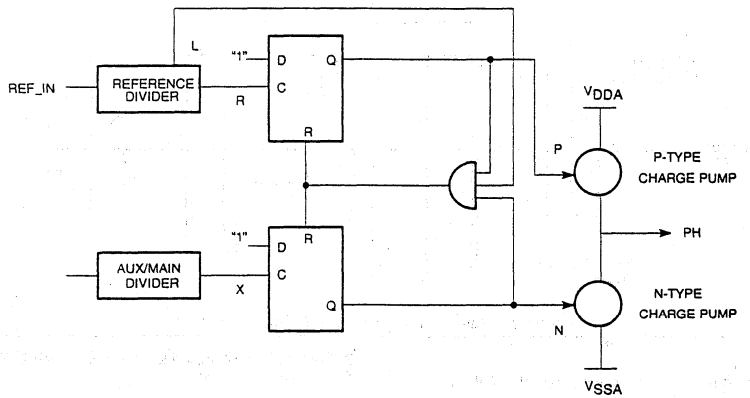
In "speed-up mode" the current in output PHI is:

$$I_{PHI\_S} = I_{PHI} + I_{PHI\_comp}$$

where:

$$|I_{PHI}| = \left(\frac{I_{RN}CN}{32}\right)(2^{CL+1})\ CK$$

$$|I_{PHI\_comp}| = \left(\frac{I_{RF}F_{RD}}{128}\right)(2^{CL+1})\ CK$$



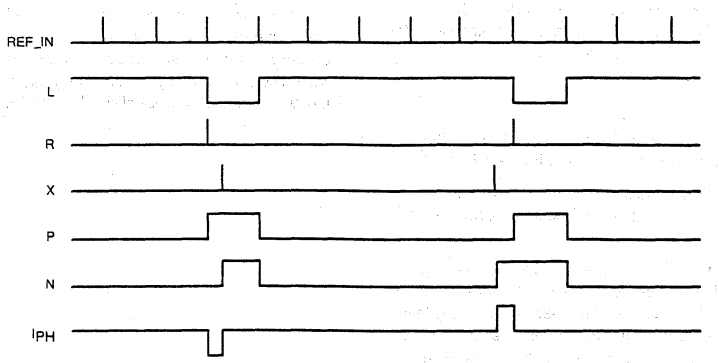


Figure 6. Phase Detector Structure with Timing

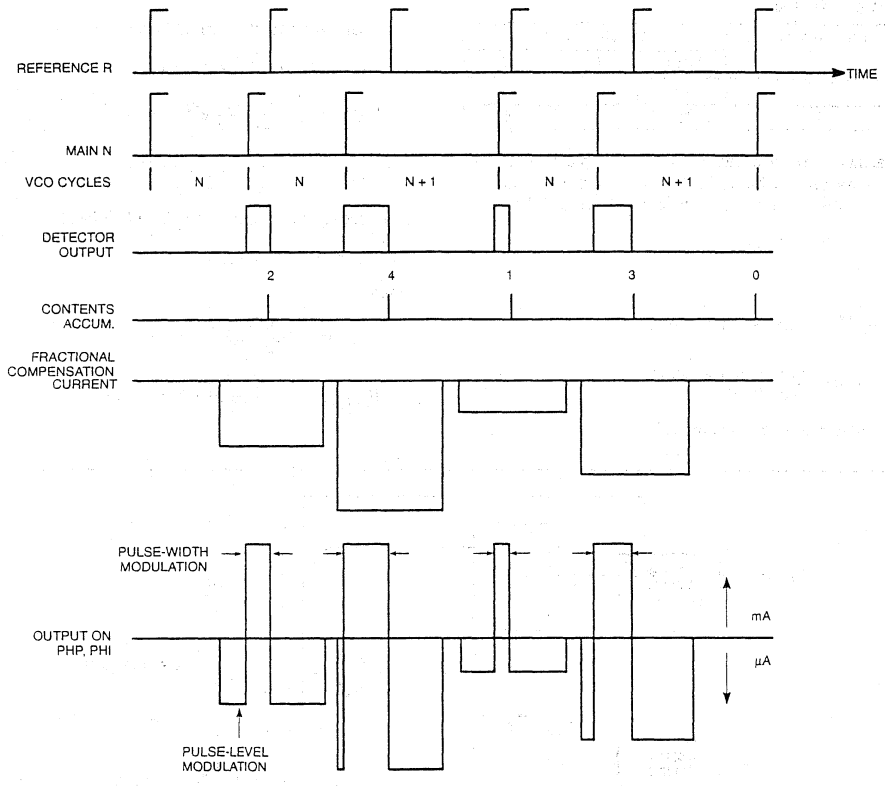


Figure 7. Waveforms for NF = 2, Fraction = 0.4

Lock Detect

The output LOCK is H when the auxiliary phase detector AND the main phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than +1 cycle on the reference input REF_IN. The lock condition is also fulfilled when the relative counter is disabled (EM = "0" or respectively EA = "0") for the main, respectively auxiliary counter.

Test Modes

The lock output is selectable as f_{REF}, f_{AUX}, f_{MAIN} and lock. Bits T1 and T0 of the E word control the selection (see Figures 4 and 8).

If T1 = T0 = Low, or if the E-word is not sent, the lock output is configured as the normal lock output described in the Lock Detect section.

If T1 = Low and T0 = High, the lock output is configured as f_{REF}. The signal is the buffered output of the reference divider NR and the 3-bit binary counter SM. The f_{REF} signal appears as normally low and pulses high whenever the divider reaches terminal count from the value programmed into the NR and SM registers. The f_{REF} signal can be used to verify the divide ratio of the Reference divider.

If T1 = High and T0 = Low, the lock output is configured as f_{AUX}. The signal is normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NA and PA registers. The f_{AUX} signal can be used to verify the divide ratio of the Auxiliary divider.

If T1 = High and T0 = High, the lock output is configured as f_{MAIN}. The signal is the buffered output of the MAIN divider. The f_{MAIN} signal appears as normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NM1, NM2 or NM3 registers. The f_{MAIN} signal can be used to verify the divide ratio of the MAIN divider and the prescaler.

Test Pin

The Test pin, Pin 19, is a buffered logic input which is exclusively ORed with the output of the prescaler. The output of the XOR gate is the input to the MAIN divider. The Test pin must be connected to V_{DD} during normal operation as a synthesizer. This pin can be used as an input for verifying the divide ratio of the MAIN divider; while in this condition the input to the prescaler, RF_{IN}, may be connected to V_{CCP} through a 10kΩ resistor in order to place prescaler output into a known state.

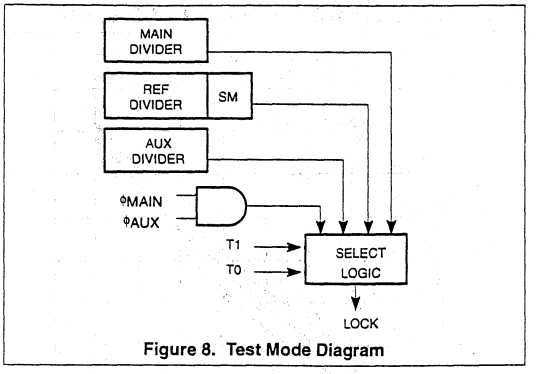
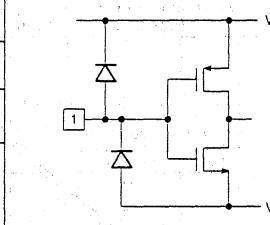
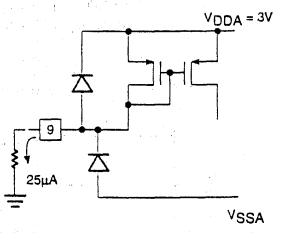
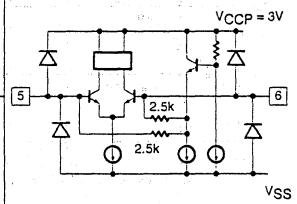
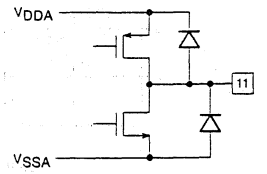
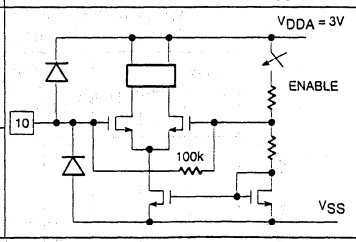
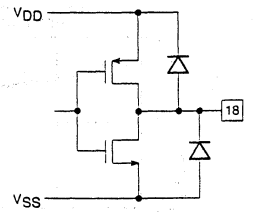


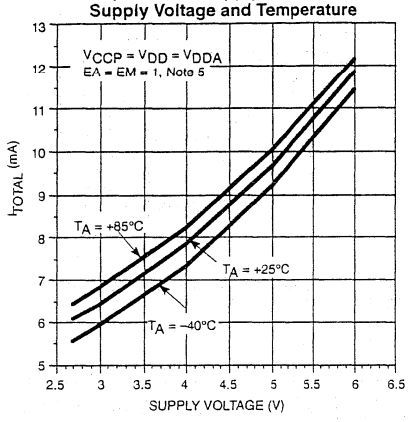
Figure 8. Test Mode Diagram

PIN FUNCTIONS

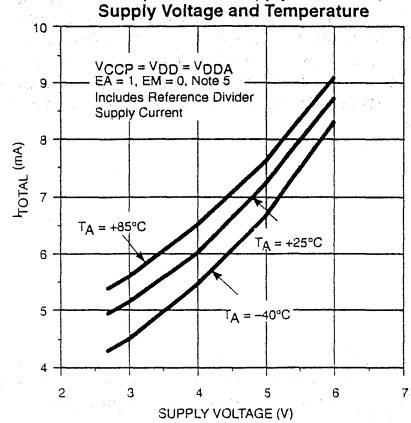
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	CLOCK	—		9	RA	1.35	
2	DATA	—		16	RN	1.35	
3	STROBE	—					
19	TEST	—		17	RF	1.35	
5	RF_{IN}	2.1		11	PHA	—	
6	$\overline{RF_{IN}}$	2.1		13	PHI	—	
				14	PHP	—	
8	REF_{IN}	1.8		18	LOCK	—	
10	AUX_{IN}	1.8					

TYPICAL PERFORMANCE CHARACTERISTICS

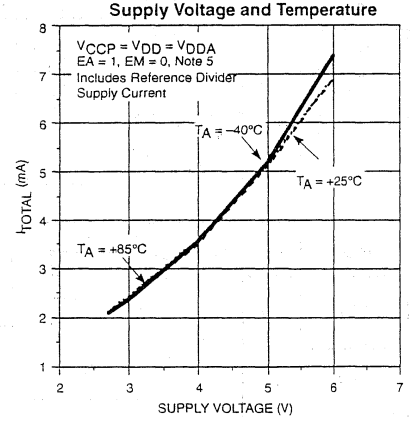
Operational Supply Current vs Supply Voltage and Temperature



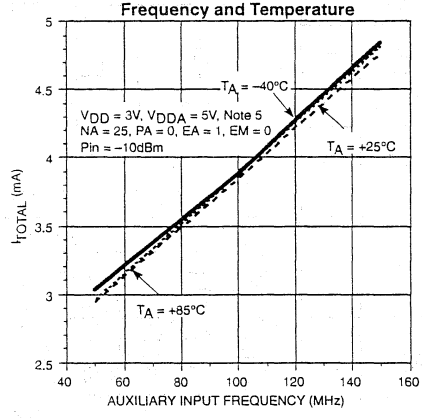
Main Operational Supply Current vs Supply Voltage and Temperature



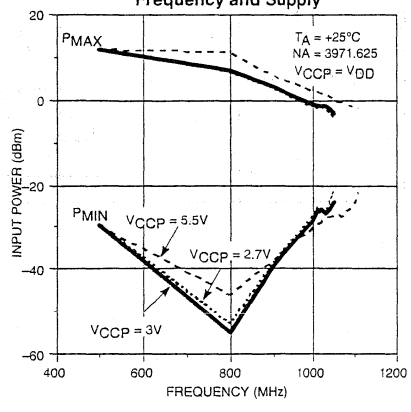
Auxiliary Operational Supply Current vs Supply Voltage and Temperature



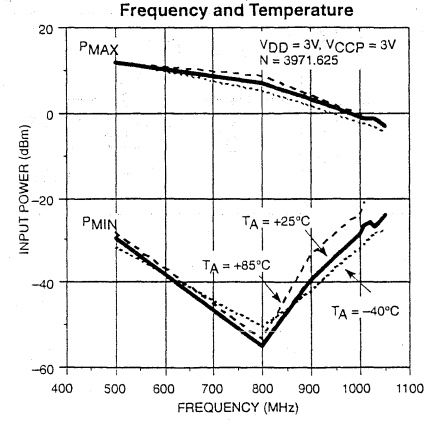
Auxiliary Operational Supply Current vs Frequency and Temperature



Main Divider Input Power vs Frequency and Supply

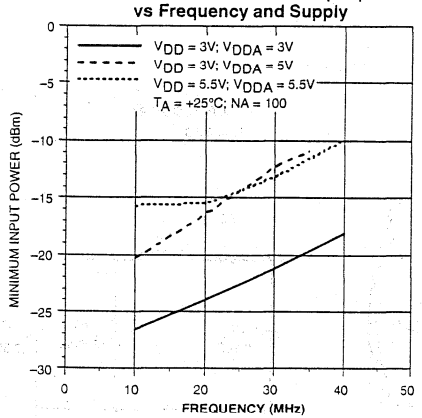


Main Divider Input Power vs Frequency and Temperature

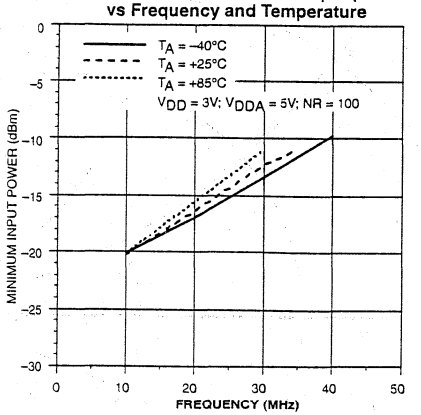


TYPICAL PERFORMANCE CHARACTERISTICS

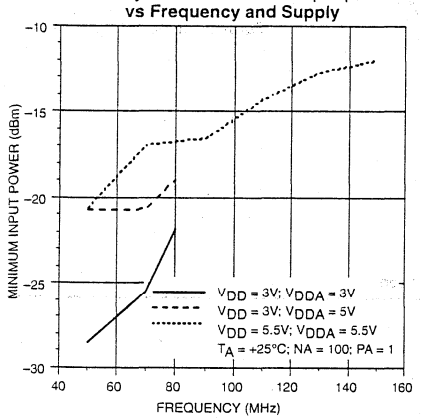
Reference Divider Minimum Input power vs Frequency and Supply



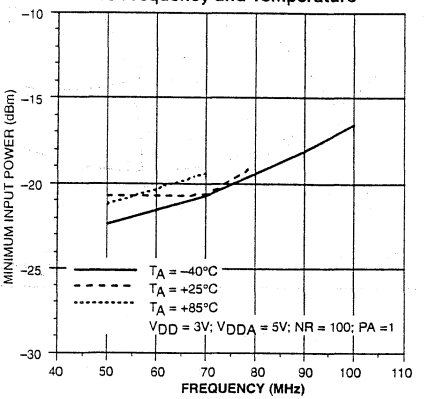
Reference Divider Minimum Input power vs Frequency and Temperature



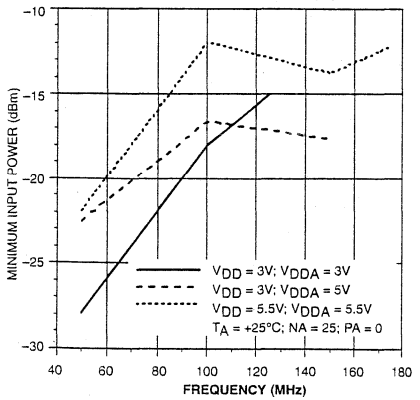
Auxiliary Divider Minimum Input power vs Frequency and Supply



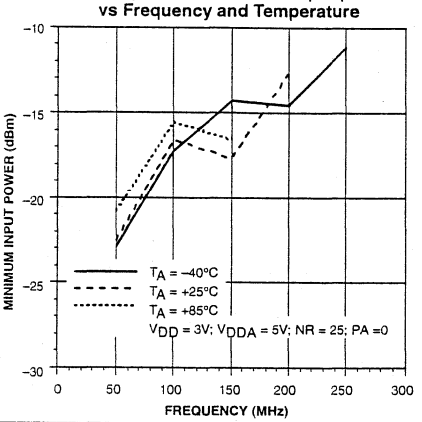
Auxiliary Divider Minimum Input power vs Frequency and Temperature

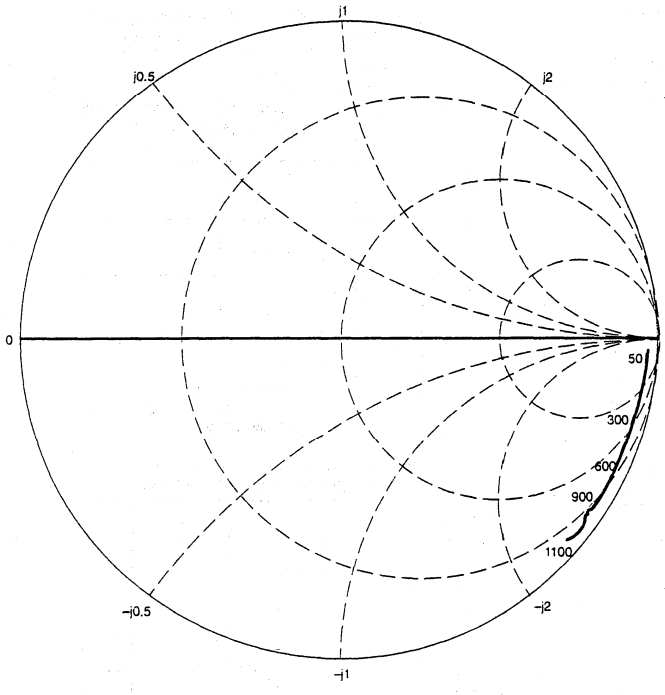


Auxiliary Divider Minimum Input power vs Frequency and Supply

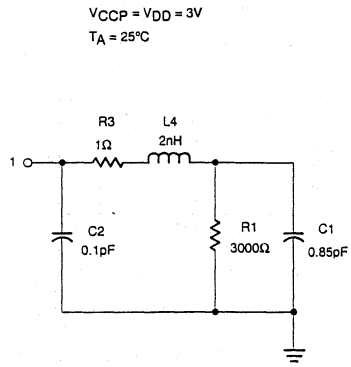


Auxiliary Divider Minimum Input power vs Frequency and Temperature

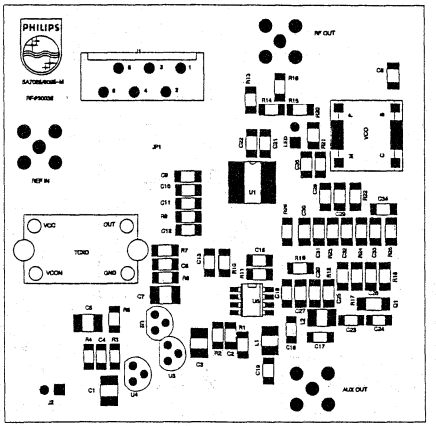




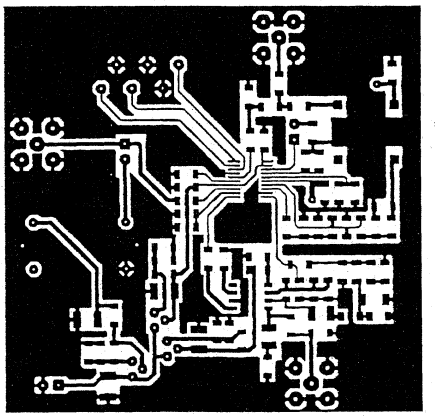
Typical RF_{IN} Input Impedance



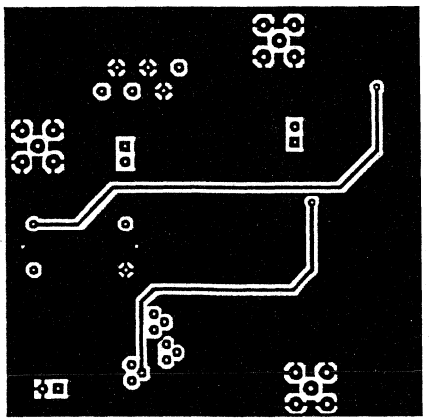
Equivalent Input Impedance



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

Figure 9. SA7025DK Demoboard Layout (NOT ACTUAL SIZE)

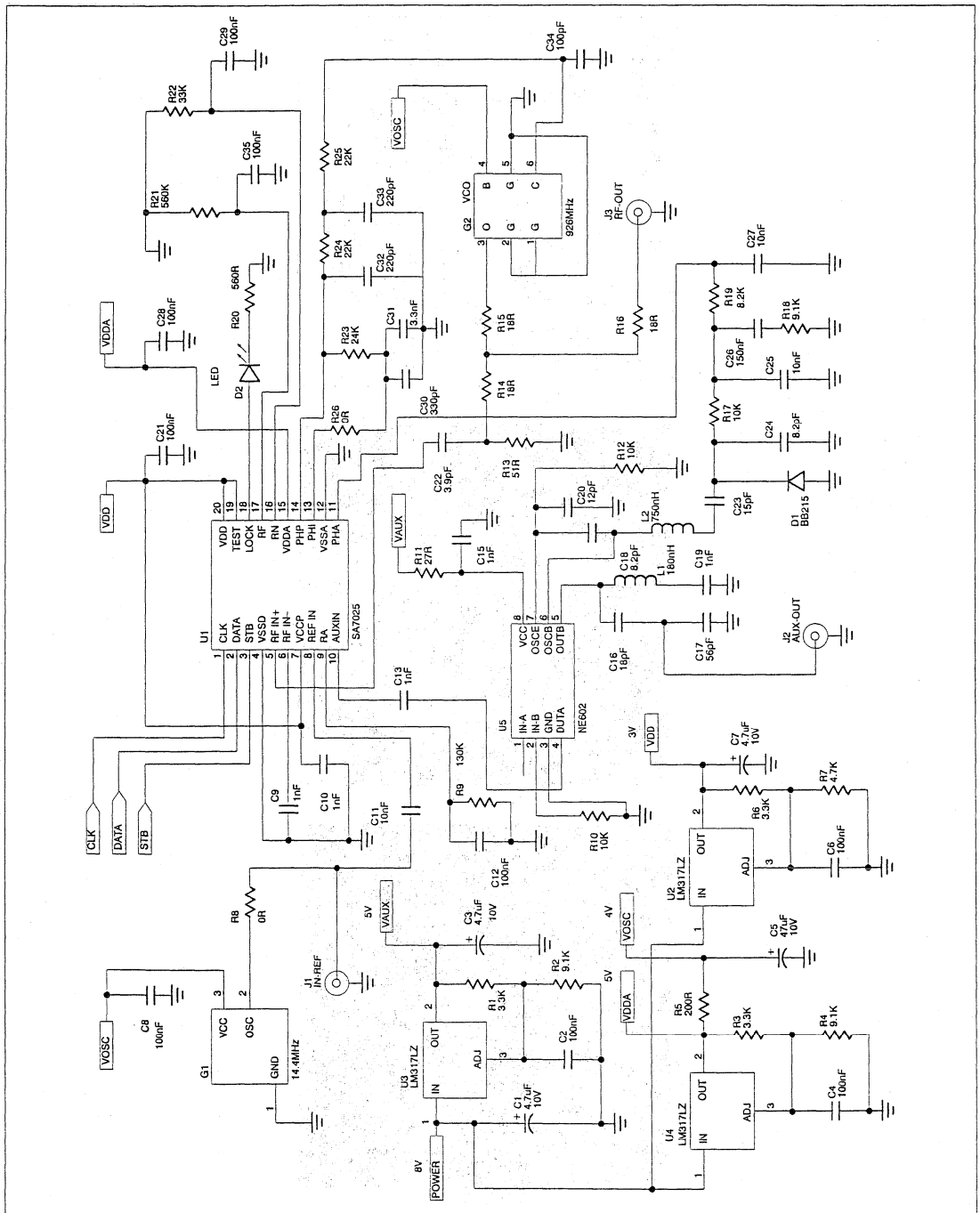


Figure 10. SA7025DK Application Circuit

Divide by: 128/129/144 triple modulus low-power ECL prescaler

SA703

DESCRIPTION

The SA703 triple modulus (Divide By 128/129/144) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.7V and is compatible with the UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package.

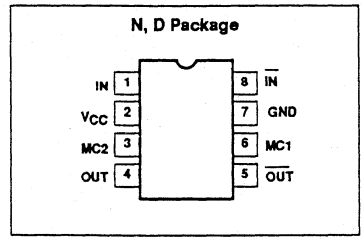
FEATURES

- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line (DIP)	-40 to +85°C	SA703N	0404B
8-Pin Plastic Small Outline (SO) (Surface-mount)	-40 to +85°C	SA703D	0174C

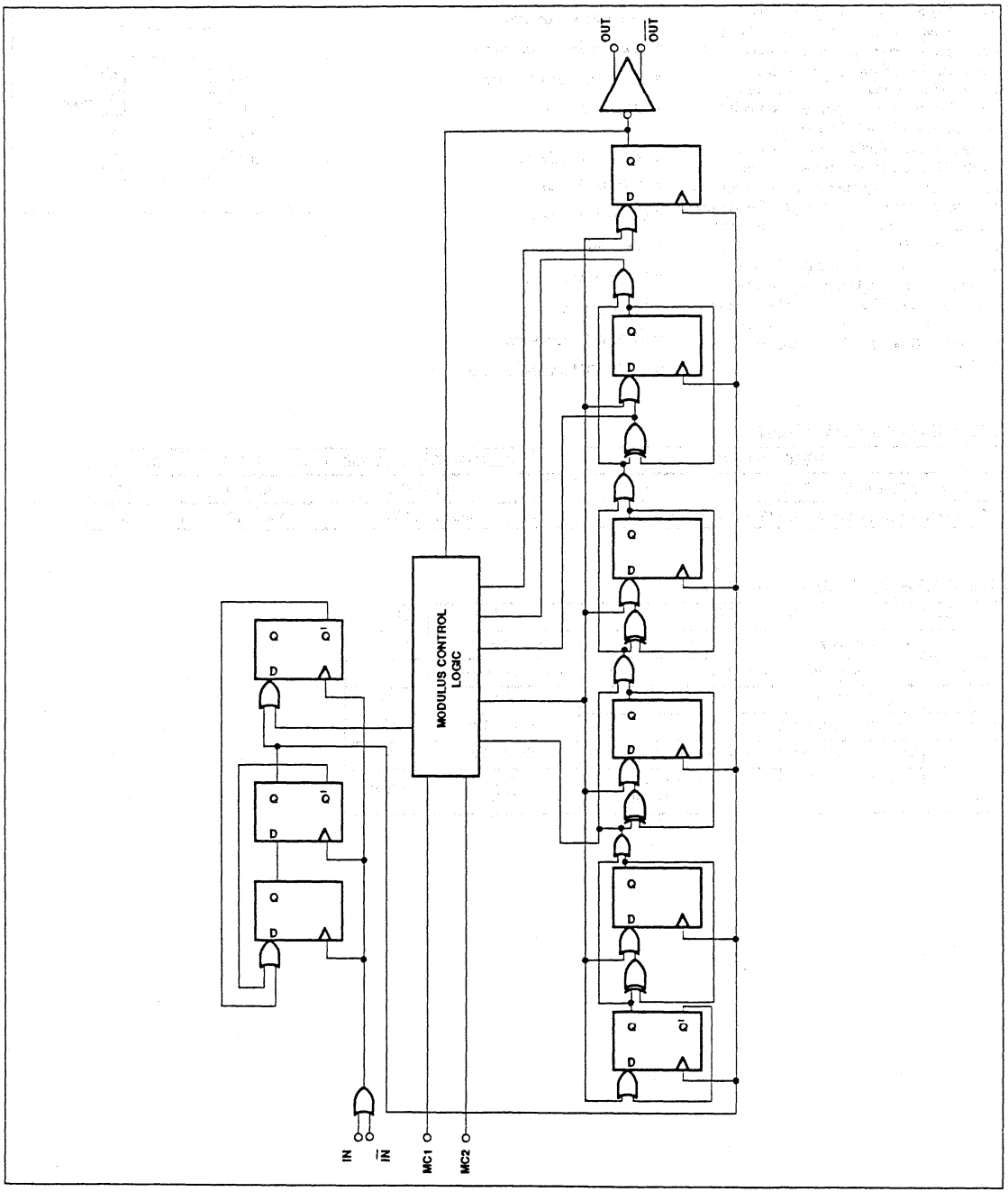
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

Divide by: 128/129/144 triple modulus low-power ECL prescaler

SA703

BLOCK DIAGRAM



Divide by: 128/129/144 triple modulus low-power ECL prescaler

SA703

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for T_A = 25°C and V_{CC} = 3.0V; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC1 input high threshold		2.0		V_{CC}	V
V_{IL}	MC1 input low threshold		–0.3		0.8	V
V_{IH}	MC2 input high threshold		2.0		V_{CC}	V
V_{IL}	MC2 input low threshold		–0.3		0.8	V
I_{IH}	MC1 input high current	V_{MC1} = V_{CC} = 6V		0.1	50	µA
I_{IL}	MC1 input low current	V_{MC1} = 0V, V_{CC} = 6V	–100	–30		µA
I_{IH}	MC2 input high current	V_{MC2} = V_{CC} = 6V		0.1	50	µA
I_{IL}	MC2 input low current	V_{MC2} = 0V, V_{CC} = 6V	–100	–30		µA

AC ELECTRICAL CHARACTERISTICS

These AC specifications are valid for V_{CC} = 3.0V, f_{IN} = 1GHz, input level = 0dBm, T_A = 25°C; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	V_{CC} = 5.0V		1.6		V_{P-P}
		V_{CC} = 3.0V		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA703 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 128. For divide by 129 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. For divide by 144, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 36. A truth table for the modulus values is given below:

Table 1.

Modulus	MC1	MC2
128	1	0
129	0	0
144	0	1
144	1	1

For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 with delay t_{PD}.

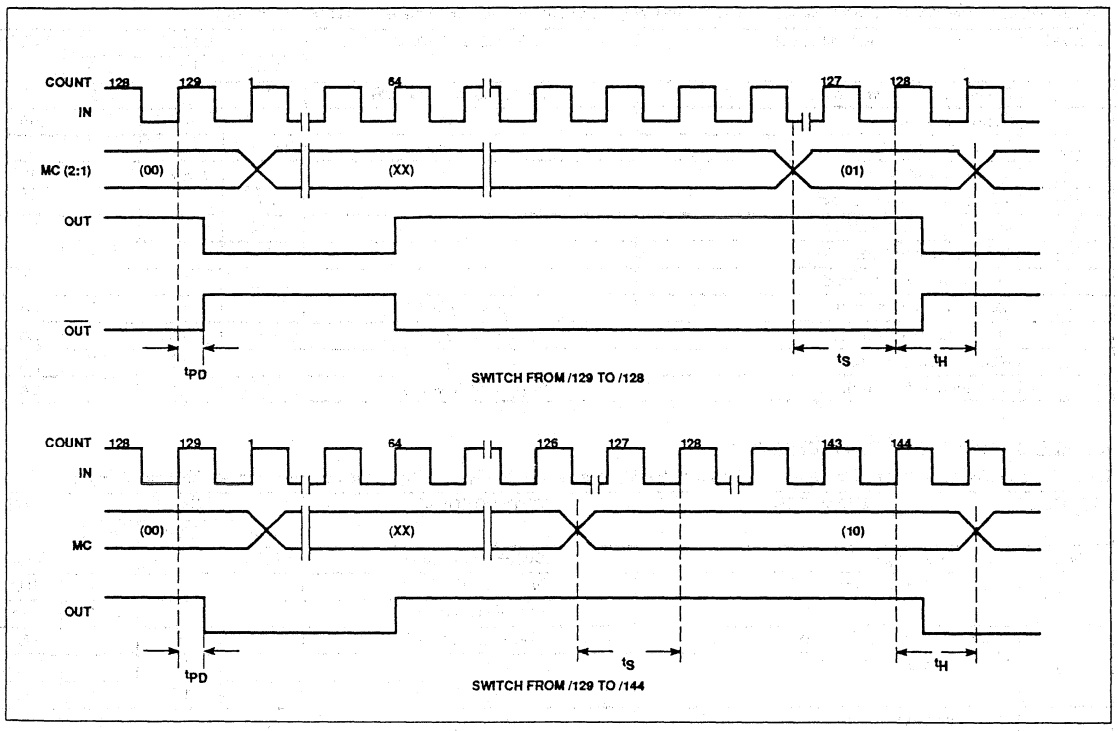
The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

Divide by: 128/129/144 triple modulus low-power ECL prescaler

SA703

AC TIMING CHARACTERISTICS



Divide by: 128/129/144 triple modulus low-power ECL prescaler

SA703

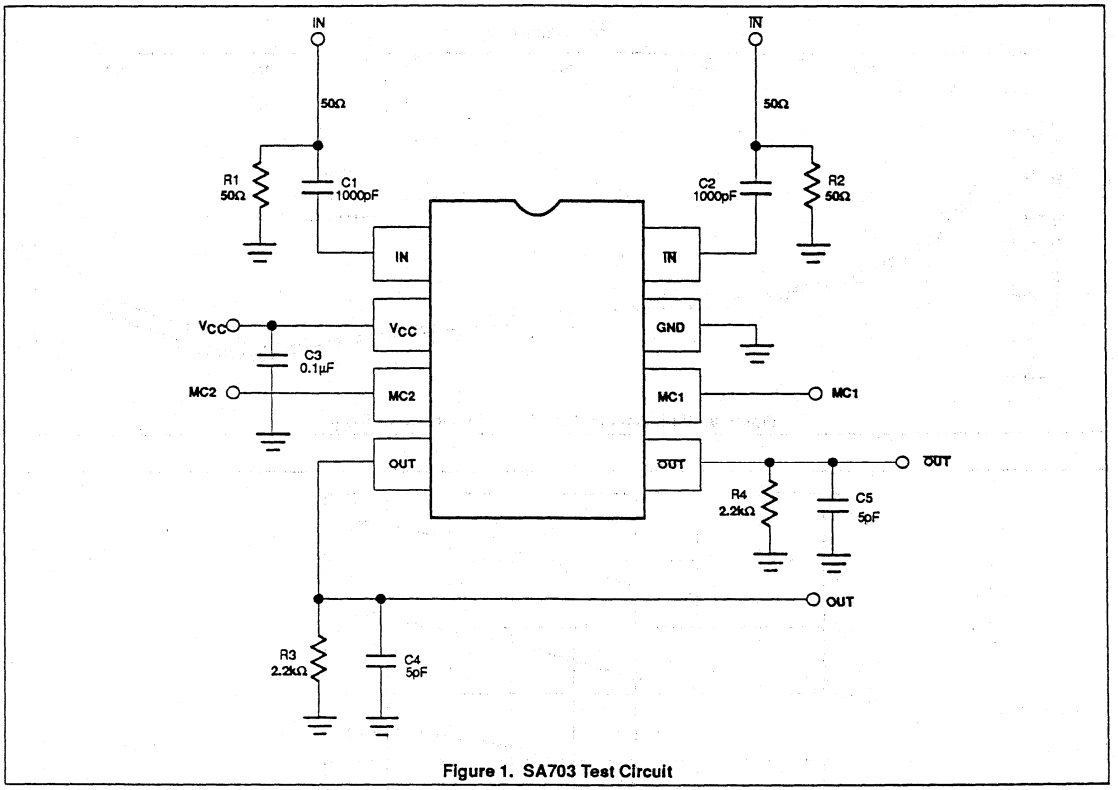


Figure 1. SA703 Test Circuit

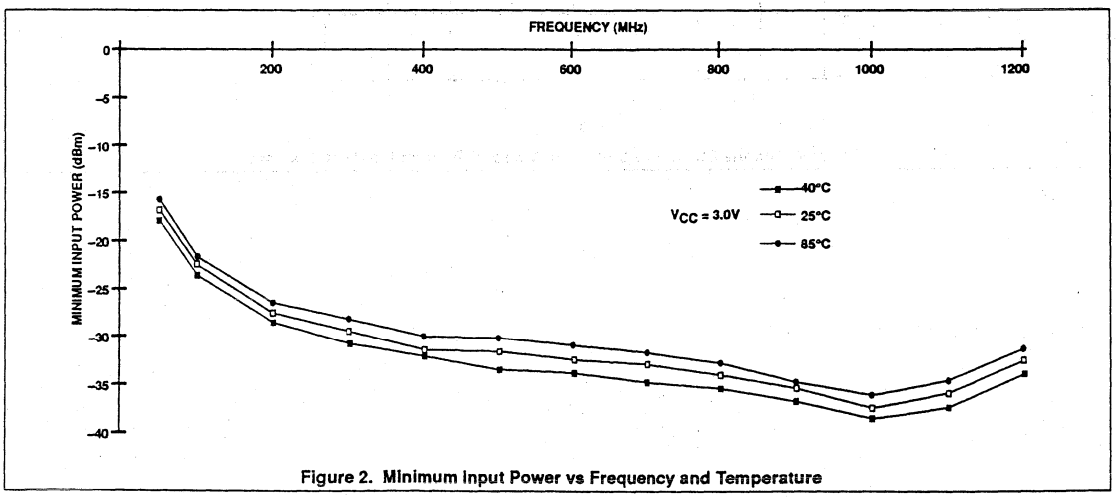


Figure 2. Minimum Input Power vs Frequency and Temperature

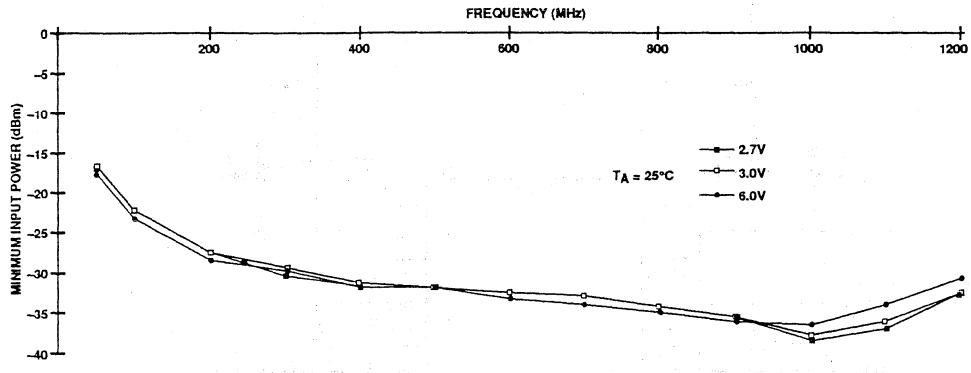


Figure 3. Minimum Input Power vs Frequency and V_{CC}

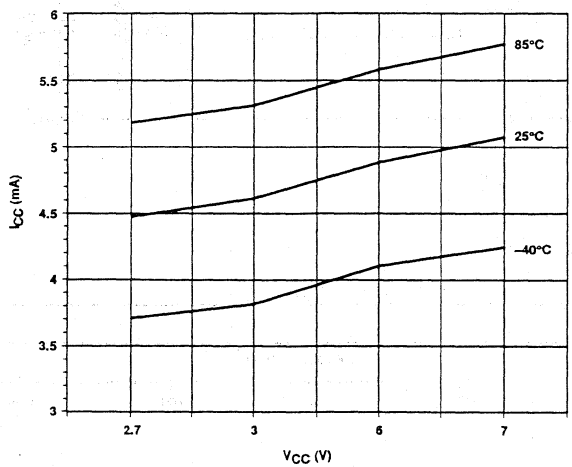
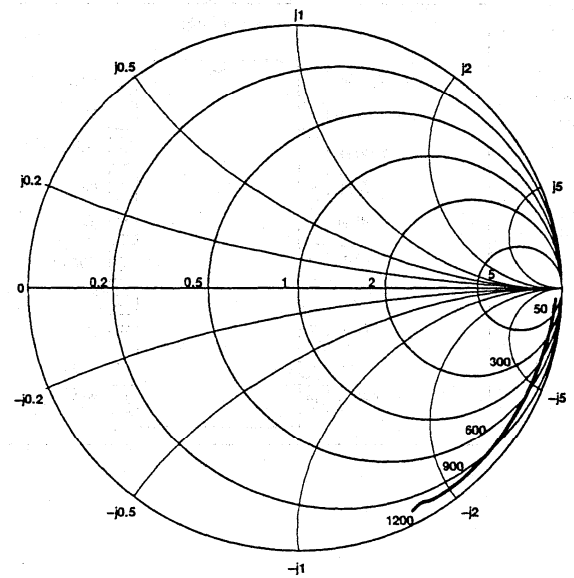


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load

Divide by: 128/129/144 triple modulus low-power ECL prescaler

SA703



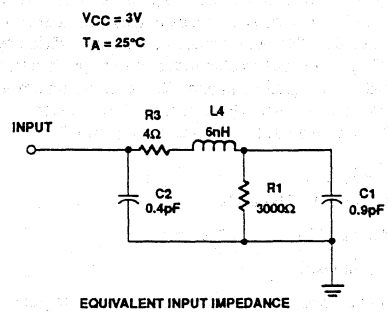
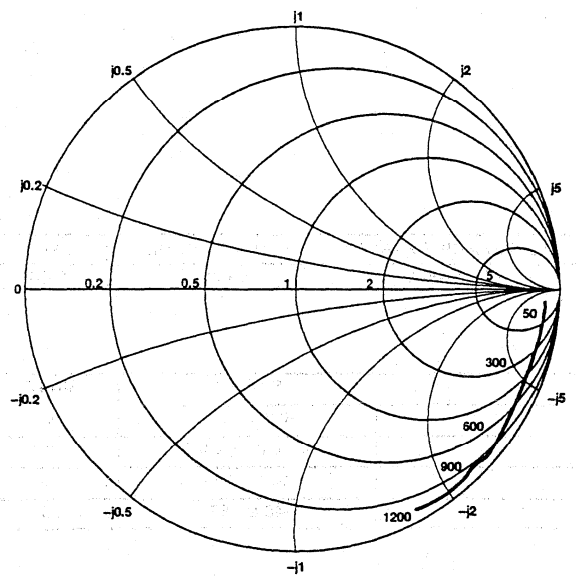


Figure 5. Typical N Package Input Impedance



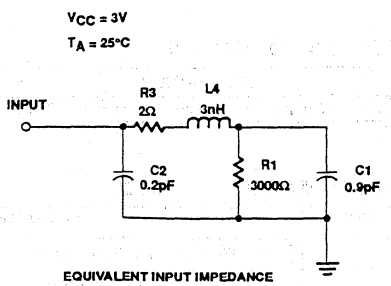


Figure 6. Typical D Package Input Impedance

Low-voltage 2GHz fractional-N synthesizer

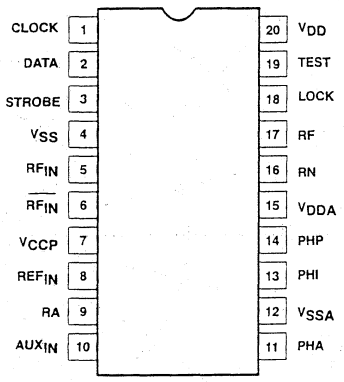
SA8025

DESCRIPTION

The SA8025 is a monolithic low power, high performance dual frequency synthesizer fabricated in QUBiC BiCMOS technology. Featuring Fractional-N division with selectable modulo 5 or 8 implemented in the Main synthesizer to allow the phase detector comparison frequency to be five or eight times the channel spacing. This feature reduces the overall division ratio yielding a lower noise floor and faster channel switching. The phase detectors and charge pumps are designed to achieve phase detector comparison frequencies up to 5MHz. A four modulus prescaler (divide by 64/65/68/73) is integrated on chip with a maximum input frequency of 1.8GHz at 3V. Programming and channel selection are realized by a high speed 3-wire serial interface. A 1GHz version (SA7025DK) is also available with the same pinout.

PIN CONFIGURATION

DK Package



FEATURES

- Operation up to 1.8GHz at 3V
- Fast locking by "Fractional-N" divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High speed serial input
- Low power consumption
- Programmable charge pump currents
- Supply voltage range 2.7 to 5.5V
- Excellent input sensitivity: V_{RF_IN} = –20dBm

APPLICATIONS

- PHP (Personal Handy Phone)
- PDC (Personal Digital Cellular)
- PCS (Personal Communication Service)
- Portable communication systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA8025DK	1563–

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V	Supply voltage, V_{DD}, V_{DDA}, V_{CCP}	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{DD} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W.

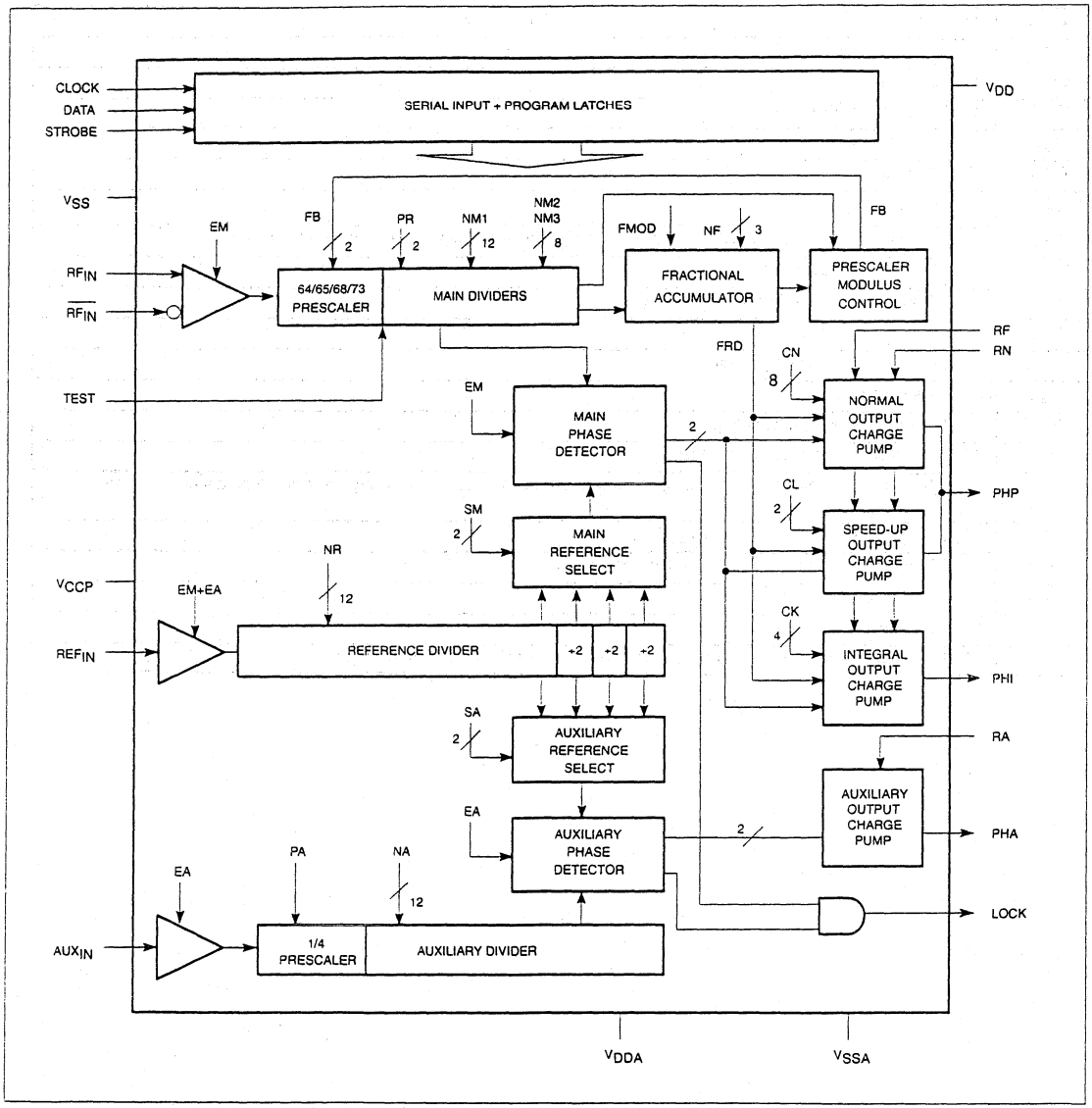
PIN DESCRIPTIONS

Symbol	Pin	Description
CLOCK	1	Serial clock input
DATA	2	Serial data input
STROBE	3	Serial strobe input
V_{SS}	4	Digital ground
RF_{IN}	5	Prescaler positive input
$\overline{RF_{IN}}$	6	Prescaler negative input
V_{CCP}	7	Prescaler positive supply voltage. This pin supplies power to the prescaler and RF input buffer
REF_{IN}	8	Reference divider input
RA	9	Auxiliary current setting; resistor to V_{SSA}
AUX_{IN}	10	Auxiliary divider input
PHA	11	Auxiliary phase detector output
V_{SSA}	12	Analog ground
PHI	13	Integral phase detector output
PHP	14	Proportional phase detector output
V_{DDA}	15	Analog supply voltage. This pin supplies power to the charge pumps, Auxiliary prescaler, Auxiliary and Reference buffers.
RN	16	Main current setting; resistor to V_{SSA}
RF	17	Fractional compensation current setting; resistor to V_{SSA}
LOCK	18	Lock detector output
TEST	19	Test pin; connect to V_{DD}
V_{DD}	20	Digital supply voltage. This pin supplies power to the CMOS digital part of the device

Low-voltage 2GHz fractional-N synthesizer

SA8025

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
$I_{STANDBY}$	Standby supply currents	$V_{RA} = V_{RF} = V_{RN} = V_{DDA}$, EM = EA = 0		100		µA
I_{AUX}	Operational supply currents[5]	EM = 0, EA = 1		2.7		mA
I_{MAIN}	Operational supply currents[5]	EM = 1, EA = 0		9.6		mA
I_{TOTAL}	Operational supply currents[5]	EM = EA = 1		11		mA
Digital inputs CLK, DATA, STROBE						
V_{IH}	High level input voltage range		0.7xV_{DD}		V_{DD}	V
V_{IL}	Low level input voltage range		0		0.3xV_{DD}	V
Digital outputs LOCK						
V_{OL}	Output voltage LOW	I_O = 2mA			0.4	V
V_{OH}	Output voltage HIGH	I_O = −2mA	V_{DD}−0.4			V
Charge pump PHA						
$\lvert I_{PHA} \rvert$	Output current PHA	$I_{RA} = -62.5µA$; $V_{PHA} = V_{DDA}/2^{13}$	400	500	600	µA
		$I_{RA} = -25µA$; $V_{PHA} = V_{DDA}/2$	160	200	240	
$\frac{\Delta I_{PHP\_A}}{\lvert I_{PHP\_A} \rvert}$	Relative output current variation PHA	$I_{RA} = -62.5µA$[2, 13]		2	6	%
ΔI_{PHA_M}	Output current matching	$I_{RA} = -62.5µA$; $V_{PHA} = V_{DDA}/2^{12, 13}$			±50	µA
Charge pump PHP, normal mode[1, 4, 6] $V_{RF} = V_{DDA}$						
$\lvert I_{PHP\_N} \rvert$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2^{13}$	440	550	660	µA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	175	220	265	
$\frac{\Delta I_{PHP\_N}}{I_{PHP\_N}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$[2, 13]		2	6	%
$\Delta I_{PHP\_N\_M}$	Output current matching	$I_{RN} = -62.5µA$;$V_{PHP} = V_{DDA}/2^{12, 13}$			±50	µA
Charge pump PHP, speed-up mode [1, 4, 7] $V_{RF} = V_{DDA}$						
$\lvert I_{PHP\_S} \rvert$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2^{13}$	2.20	2.75	3.30	mA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	0.85	1.1	1.35	
$\frac{\Delta I_{PHP\_S}}{I_{PHP\_S}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$[2, 13]		2	6	%
$\Delta I_{PHP\_S\_M}$	Output current matching	$I_{RM} = -62.5µA$;$V_{PHP} = V_{DDA}/2^{12, 13}$			±250	µA
Charge pump PHI, speed-up mode [1, 4, 8] $V_{RF} = V_{DDA}$						
$\lvert I_{PHI} \rvert$	Output current PHI	$I_{RN} = -62.5µA$; $V_{PHI} = V_{DDA}/2^{13}$	4.4	5.5	6.6	mA
		$I_{RN} = -25µA$; $V_{PHI} = V_{DDA}/2$	1.75	2.2	2.65	
$\frac{\Delta I_{PHI}}{I_{PHI}}$	Relative output current variation PHI	$I_{RN} = -62.5µA$[2, 13]		2	8	%
ΔI_{PHI_M}	Output current matching	$I_{RN} = -62.5µA$; $V_{PHI} = V_{DDA}/2^{12, 13}$			±500	µA
Fractional compensation PHP, normal mode [1, 9] $V_{RN} = V_{DDA}$, $V_{PHP} = V_{DDA}/2$						
$I_{PHP\_F\_N}$	Fractional compensation output current PHP vs F_{RD}[3]	$I_{RF} = -62.5µA$;F_{RD} = 1 to 7[13]	−675	−500	−325	nA
		$I_{RF} = -25µA$;F_{RD} = 1 to 7	−270	−200	−130	
Fractional compensation PHP, speed up mode [1, 10] $V_{PHP} = V_{DDA}$, $V_{RN} = V_{DDA}$						
$I_{PHP\_F\_S}$	Fractional compensation output current PHP vs F_{RD}[3]	$I_{RF} = -62.5µA$;F_{RD} = 1 to 7[13]	−3.35	−2.5	−1.65	µA
		$I_{RF} = -25µA$;F_{RD} = 1 to 7	−1.35	−1.0	−0.65	
Fractional compensation PHI, speed up mode [1, 11] $V_{PHP} = V_{DDA}/2$, $V_{RN} = V_{DDA}$						
I_{PHI_F}	Fractional compensation output current PHI vs F_{RD}[3]	$I_{RF} = -62.5µA$;F_{RD} = 1 to 7[13]	−5.4	−4.0	−2.6	µA
		$I_{RF} = -25µA$;F_{RD} = 1 to 7	−2.15	−1.6	−1.05	

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Charge pump leakage currents, charge pump not active						
I_{PHP_L}	Output leakage current PHP; normal mode[1]	V_{PHP} = 0.7 to V_{DDA} – 0.8		0.1	10	nA
I_{PHI_L}	Output leakage current PHI; normal mode[1]	V_{PHI} = 0.7 to V_{DDA} – 0.8		0.1	10	nA
I_{PHA_L}	Output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} – 0.8		0.1	10	nA

AC ELECTRICAL CHARACTERISTICS

V_{DD} = V_{DDA} = V_{CCP} = 3V; T_A = 25°C; unless otherwise specified. Test Circuit, Figure 2. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Main divider						
f_{RF_IN}	Input signal frequency	Pin = -10dBm, Direct coupled input[14]	0	1.8		GHz
		Pin = -10dBm, 1000pF input coupling		1.8		
V_{RF_IN}	Input sensitivity	f_{IN} = 1700MHz	–20		0	dBm
Reference divider						
f_{REF_IN}	Input signal frequency		0		20	MHz
		4.5V ≤ V_{DDA} ≤ 5.5V	0		30	
V_{REF_IN}	Input signal range, AC coupled		300			mV_{P-P}
Z_{REF_IN}	Reference divider input impedance[15]			100		kΩ
					3	pF
Auxiliary divider						
f_{AUX_IN}	Input signal frequency		0		50	MHz
	PA = "0", prescaler enabled	4.5V ≤ V_{DDA} ≤ 5.5V	0		150	
	Input signal frequency		0		30	
	PA = "1", prescaler disabled	4.5V ≤ V_{DDA} ≤ 5.5V	0		40	
V_{AUX_IN}	Input signal range, AC coupled		200			mV_{P-P}
Z_{AUX_IN}	Auxiliary divider input impedance[15]			100		kΩ
					3	pF
Serial interface[15]						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time; CLOCK to DATA		30			ns
t_W	Pulse width; CLOCK		30			ns
	Pulse width; STROBE	B, C, D, E words	30			
t_{SW}	Pulse width; STROBE	A word, PR = '01'	$\frac{1}{f_{VCO}} \cdot (NM2 \cdot 65) + t_W$			ns
		A word, PR = '10'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM3 + 1) \cdot 68] + t_W$			
		A word, PR = '11'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65 + (NM3 + 1) \cdot 68 - (NM4 + 1) \cdot 73)] + t_W$			
		A word, PR = '00'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM4 + 1) \cdot 73] + t_W$			

NOTES:

1. When a serial input "A" word is programmed, the main charge pumps on PHP and PHI are in the "speed up mode" as long as STROBE = H. When this is not the case, the main charge pumps are in the "normal mode".
2. The relative output current variation is defined thus:
$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|}$$ with $V_1 = 0.7V$, $V_2 = V_{DDA} - 0.8V$ (see Figure 1).
3. F_{RD} is the value of the 3 bit fractional accumulator.
4. Monotonicity is guaranteed with $C_N = 0$ to 255.
5. Power supply current measured with f_{RF_IN} = 1667.4MHz, NM1 = 0, NM2 = 1, NM3 = 1, NM4 = 4, FMOD = 8, N = 694 6/8, main phase detector frequency = 2.4MHz, $f_{REF\ IN}$ = 19.2MHz, NR = 8, SM = 1, f_{AUX_IN} = 150MHz, NA = 125, SA = 1, PA = 0, auxiliary phase detector frequency = 300kHz, IRN = IRA = IRF = 25µA, CN = 160, CL = 0, CK = 0, lock condition, normal mode, $V_{CCP} = V_{DD} = V_{DDA} = 3V$. Operational supply current = $I_{DDA} + I_{DD} + I_{CCP}$
6. Specification condition: CN = 255
7. Specification conditions:
   1) CN = 255; CL = 1, or
   2) CN = 75; CL = 3
8. Typical output current $|I_{PHI}| = -I_{RN} \times CN \times 2^{(CL+1)} \times CK/32$:
   1) CN = 160; CL = 3; CK = 1, or
   2) CN = 160; CL = 2; CK = 2, or
   3) CN = 160; CL = 1; CK = 4, or
   4) CN = 160; CL = 0; CK = 8
9. Specification condition: F_{RD} = 1 to 7.
10. Specification conditions: F_{RD} = 1 to 7; CL = 1.
11. Specification conditions:
    1) F_{RD} = 1 to 7; CL = 1; CK = 2, or
    2) F_{RD} = 1 to 7; CL = 2; CK = 1.
12. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on.
13. Limited analog supply voltage range 4.5 to 5.5V.
14. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.
15. Guaranteed by design.

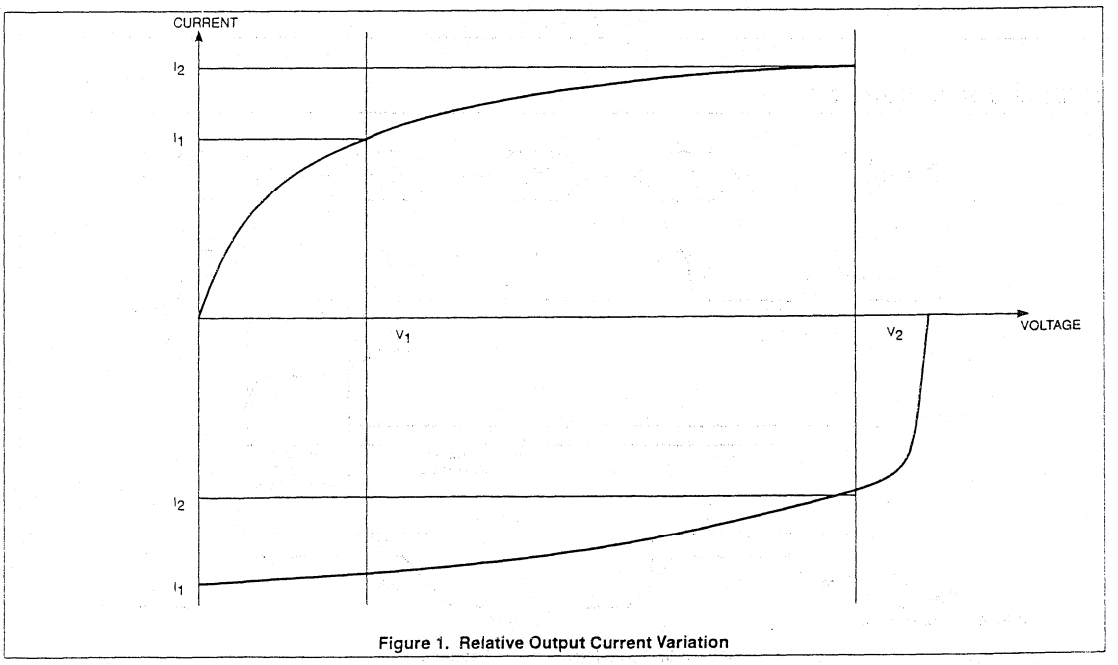


Figure 1. Relative Output Current Variation

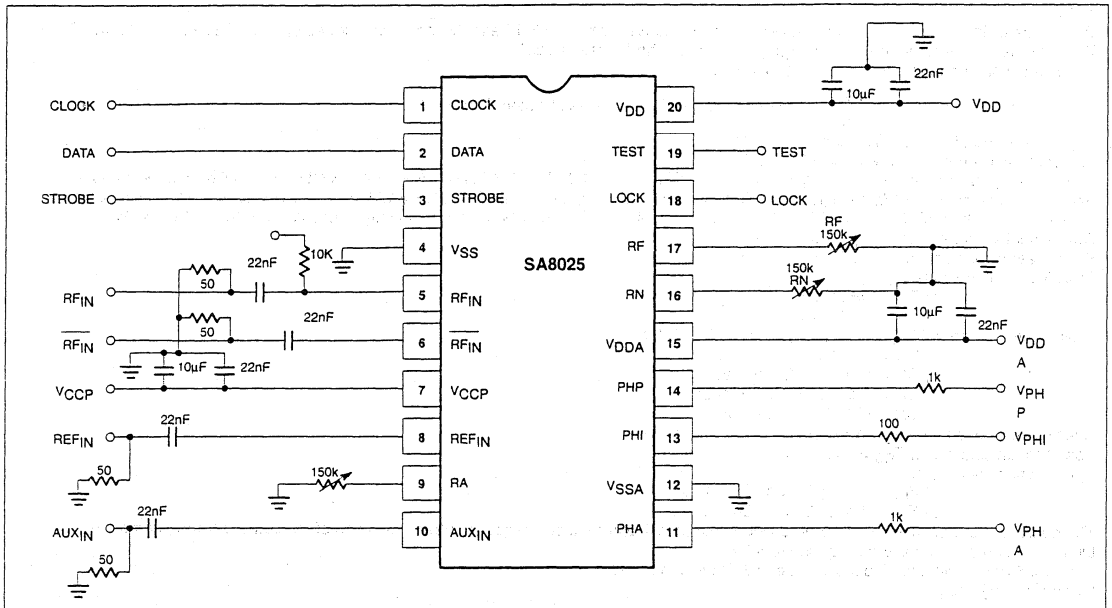


Figure 2. Test Circuit

AC TIMING CHARACTERISTICS

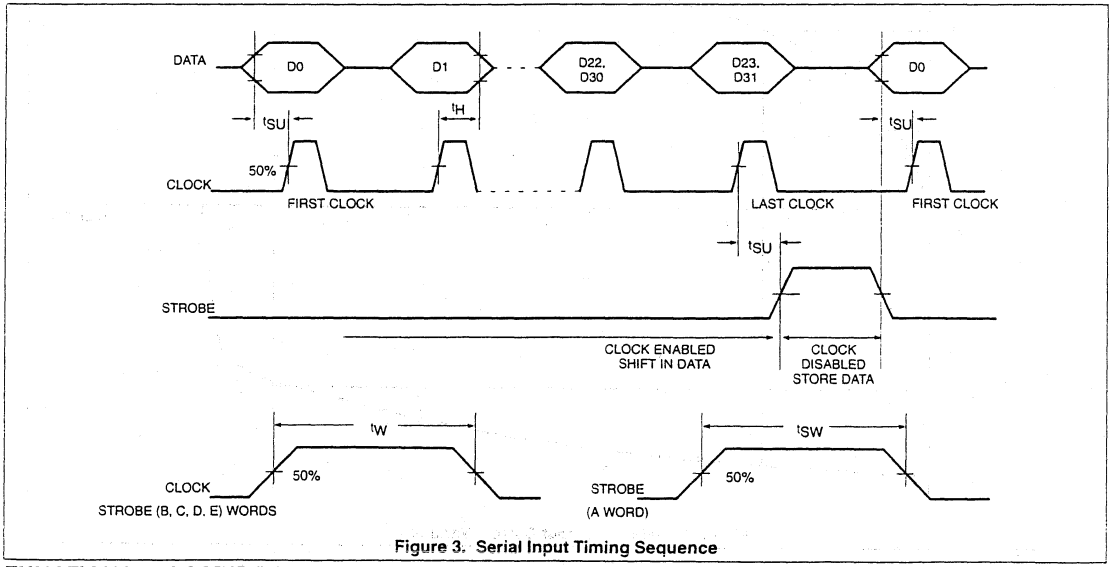


Figure 3. Serial Input Timing Sequence

FUNCTIONAL DESCRIPTION

Serial Input Programming

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32 bit words; each word includes 1 or 4 address bits. Figure 3 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is

clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent: D, C, B and A. Figure 4 and Table 1 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for CN and PR is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24 bit A0 word is used. CN will be directly loaded by programming a long 32 bit A1 word. The flag LONG in the D word determines whether A0 (LONG = "0") or A1 (LONG = "1") format is applicable. The A word contains new data for the main divider.

Main Divider Synchronization

The A word is loaded only when a main divider synchronization signal is also active in order to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. The signal is active while the NM1 divider is counting down from the programmed value. The new A word will be loaded after the NM1 divider has reached its terminal count; also, at this time a main divider output pulse will be sent to the main phase detector. The loading of the A word is disabled while the other dividers are counting up to their programmed values. Therefore, the new A word will be correctly loaded provided that the STROBE signal has been at an active high value for at least a minimum number of VCO input cycles at RF_{IN} or $\overline{RF_{IN}}$.

For PR = '01'

$$t\_strobe\_min = \frac{1}{f_{VCO}}(NM2 \cdot 65) + t_W$$

For PR = '10'

$$t\_strobe\_min = \frac{1}{f_{VCO}}[NM2 \cdot 65 + (NM3 + 1) \cdot 68] + t_W$$

For PR = '11'

$$t\_strobe\_min = \frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65 + (NM3 + 1) \cdot 68 + (NM4 + 1) \cdot 73)] + t_W$$

For PR = '00'

$$t\_strobe\_min = \frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM4 + 1) \cdot 73] + t_W$$

Programming the A word means also that the main charge pumps on output PHP and PHI are set into the speed-up mode as long as the STROBE is H.

Auxiliary Divider

The input signal on AUX_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled if the serial control bit EA = "1". Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = "0". This divider has been optimized to accept a high frequency input signal. If PA = "1", this divider is disabled and the input signal is fed directly to the second stage, which is a 12-bit programmable divider with standard input frequency (40MHz). The division ratio can be expressed as:

if PA = "0": N = 4 x NA
if PA = "1": N = NA; with NA = 4 to 4095

Reference Divider

The input signal on REF_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 4095) followed by a three bit binary counter. The 2 bit SM register (see Figure 5) determines which of the 4 output pulses is selected as the main phase detector input. The 2 bit SA register determines the selection of the auxiliary phase detector signal.

Main Divider

The differential inputs are amplified (to internal ECL logic levels) and provide excellent sensitivity (–20dBm at 1.7GHz) making the prescaler ideally suited to directly interface to a VCO as integrated on the Philips front-end devices including RF gain stage, VCO and mixer. The internal four modulus prescaler feedback loop FB controls the selection of the divide by ratios 64/65/68/73, and reduces the minimum system division ratio below the typical value required by standard dual modulus (64/65) devices.

This input stage is enabled when serial control bit EM = "1". Disabling means that all currents in the prescaler are switched off.

The main divider is built up by a 12 bit counter plus a sign bit. Depending on the serial input values NM1, NM2, NM3, NM4 and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles according to Table 2 and Table 3.

The loading of the work registers NM1, NM2, NM3, NM4 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as explained in the Serial Input Programming section.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = "1". Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider will then be

$$NQ = N + \frac{NF}{Q}$$

Programming a fraction means the prescaler with main divider will divide by N or N + 1. The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

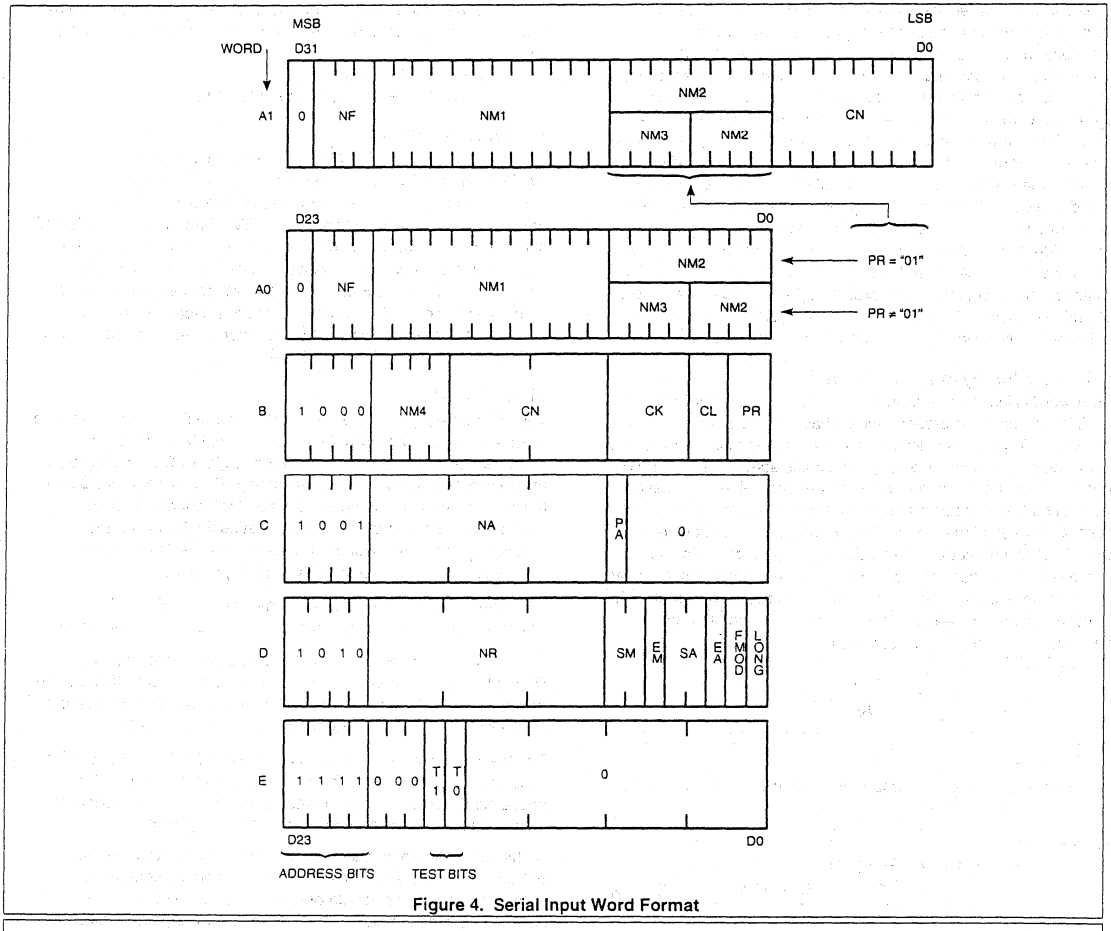


Figure 4. Serial Input Word Format

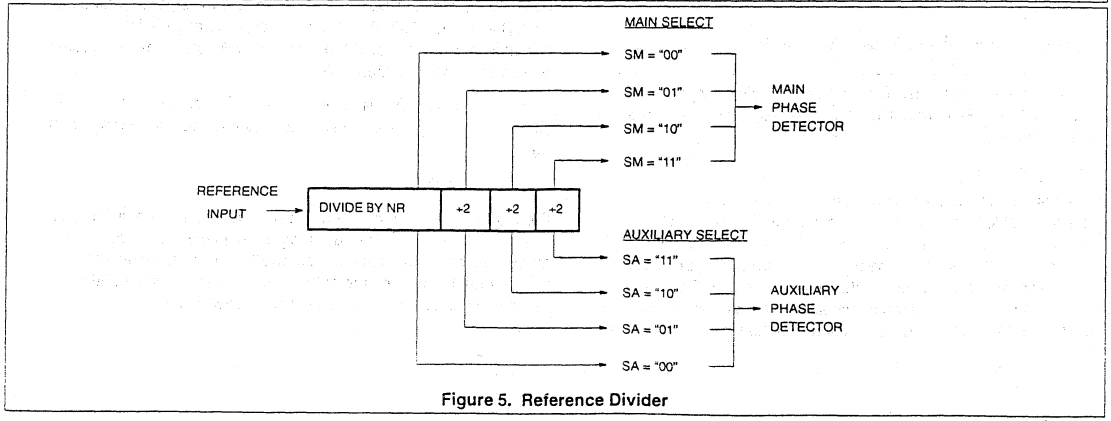


Figure 5. Reference Divider

Table 1. Function Table

Symbol	Bits	Function
NM1	12	Number of main divider cycles when prescaler modulus = 64*
NM2	8 if PR = "01" 4 if PR = "10"	Number of main divider cycles when prescaler modulus = 65*
NM3	4 if PR = "10"	Number of main divider cycles when prescaler modulus = 68*
NM4	4 if PR = "11" or "00"	Number of main divider cycles when prescaler modulus = 73*
PR	2	Prescaler type in use PR = "01": modulus 2 prescaler (64/65) PR = "10": modulus 3 prescaler (64/65/68) PR = "11": modulus 4 prescaler (64/65/68/73) PR = "00": modulus 3 prescaler (64/65/73)
NF	3	Fractional-N increment
FMOD	1	Fractional-N modulus selection flag "1": modulo 8 "0": modulo 5
LONG	1	A word format selection flag "0": 24 bit A0 format "1": 32 bit A1 format
CN	8	Binary current setting factor for main charge pumps
CL	2	Binary acceleration factor for proportional charge pump current
CK	4	Binary acceleration factor for integral charge pump current
EM	1	Main divider enable flag
EA	1	Auxiliary divider enable flag
SM	2	Reference select for main phase detector
SA	2	Reference select for auxiliary phase detector
NR	12	Reference divider ratio
NA	12	Auxiliary divider ratio
PA	1	Auxiliary prescaler mode: PA = "0": divide by 4 PA = "1": divide by 1

*Not including reset cycles and Fractional-N effects.

Table 2. Prescaler Ratio

The total division ratio from prescaler to the phase detector may be expressed as:	
if PR = "01"	N = (NM1 + 2) x 64 + NM2 x 65 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 (*)
if PR = "10"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 68 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 68 (*)
if PR = "11"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 68 + (NM4 + 1) x 73 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 68 + (NM4 + 1) x 73 (*)
if PR = "00"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM4 + 1) x 73 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM4 + 1) x 73 (*)
(*) When the fractional accumulator overflows the prescaler ratio = 65 (64 + 1) and the total division ratio N' = N + 1	

Table 3. PR Modulus

PR	Modulus Prescaler	Bit Capacity			
		NM1	NM2	NM3	NM4
01	2	12	8	–	–
10	3	12	4	4	–
11	4	12	4	4	4
00	3	12	4	–	4

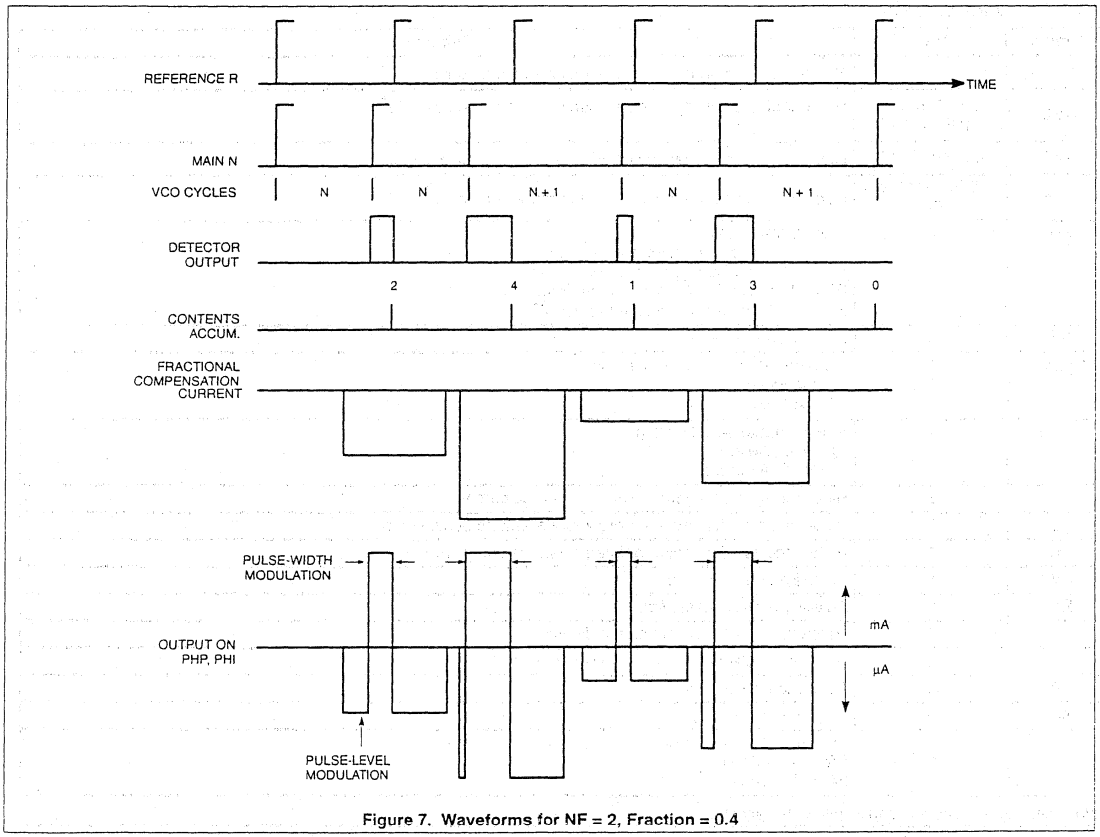


Figure 7. Waveforms for NF = 2, Fraction = 0.4

Main Output Charge Pumps and Fractional Compensation Currents

The main charge pumps on pin PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 7 shows the waveforms for a typical case.

When the serial input A word is loaded, the output circuits are in the "speed-up mode" as long as the STROBE is H, else the "normal mode" is active. In the "normal mode" the current output PHP is:

$$I_{PHP\_N} = I_{PHP} + I_{PHP\_comp}$$

where:

$$|I_{PHP}| = \frac{CN \cdot I_{RN}}{32} \quad \text{:charge pump current}$$

$$|I_{PHP\_comp}| = FRD \cdot \frac{I_{RF}}{128} \quad \text{:fractional comp. current}$$

The current in PHI is zero in "normal mode".

In "speed-up mode" the current in output PHP is:

$$I_{PHP\_S} = I_{PHP} + I_{PHP\_comp}$$

$$|I_{PHP}| = \left(\frac{CN \cdot I_{RN}}{32}\right)(2^{CL+1} + 1)$$

$$|I_{PHP\_comp}| = \left(\frac{FRD \cdot I_{RF}}{128}\right)(2^{CL+1} + 1)$$

In "speed-up mode" the current in output PHI is:

$$I_{PHI\_S} = I_{PHI} + I_{PHI\_comp}$$

where:

$$|I_{PHI}| = \left(\frac{CN \cdot I_{RN}}{32}\right)(2^{CL+1})\ CK$$

$$|I_{PHI\_comp}| = \left(\frac{FRD \cdot I_{RN}}{128}\right)(2^{CL+1})\ CK$$

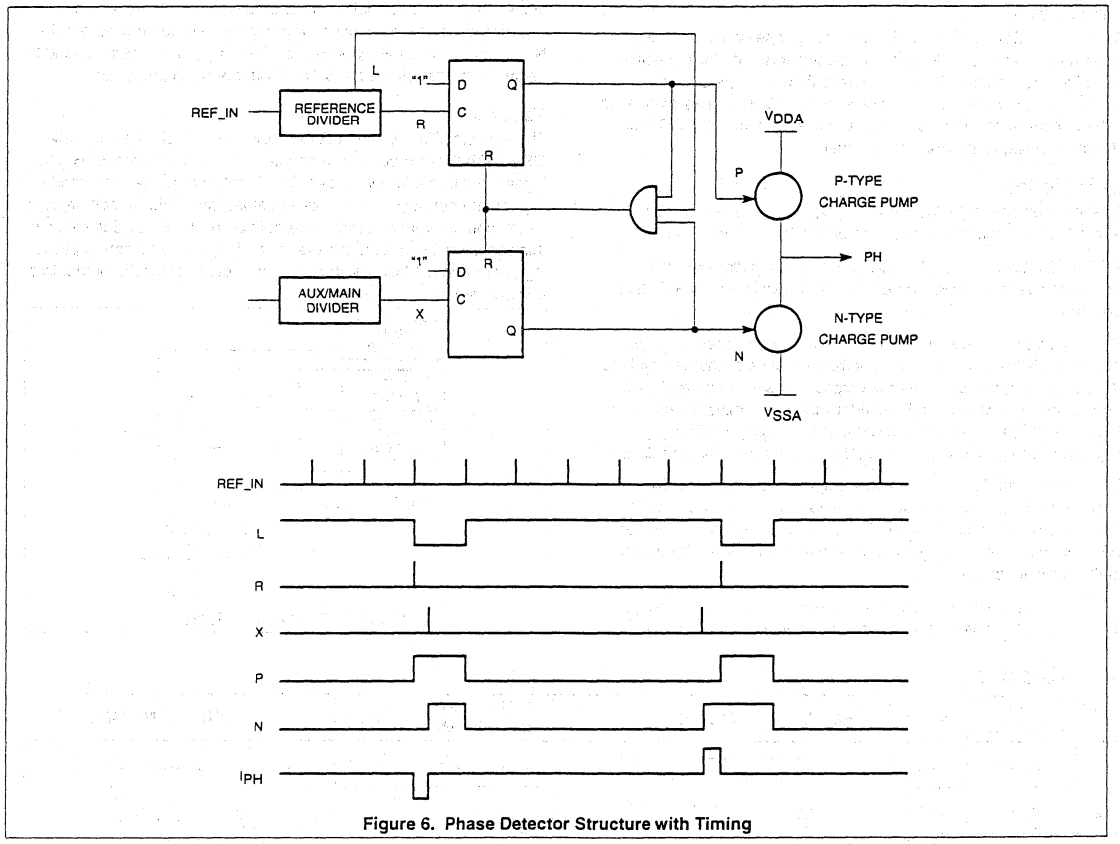


Figure 6. Phase Detector Structure with Timing

Phase Detectors

The auxiliary and main phase detectors are a two D-type flip-flop phase and frequency detector shown in Figure 6. The flip-flops are set by the negative edges of output signals of the dividers. The rising edge of the signal, L, will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

Current Settings

The SA8025 has 3 current setting pins: RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current connected between the current setting pin and V_{SS}. The typical value R (current setting resistor) can be calculated with the formula:

$$R = \frac{V_{DDA} - 0.9 - 150\sqrt{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary Output Charge Pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor RA at pin RA. The active charge pump current is typically:

$$|I_{PHA}| = 8 \cdot I_{RA}$$

Lock Detect

The output LOCK is H when the auxiliary phase detector AND the main phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than +1 cycle on the reference input REF_IN. The lock condition is also fulfilled when the relative counter is disabled (EM = "0" or respectively EA = "0") for the main, respectively auxiliary counter.

Test Modes

The lock output is selectable as f_{REF}, f_{AUX}, f_{MAIN} and lock. Bits T1 and T0 of the E word control the selection (see Figures 4 and 8).

If T1 = T0 = Low, or if the E-word is not sent, the lock output is configured as the normal lock output described in the Lock Detect section.

If T1 = Low and T0 = High, the lock output is configured as f_{REF}. The signal is the buffered output of the reference divider NR and the 3-bit binary counter SM. The f_{REF} signal appears as normally low and pulses high whenever the divider reaches terminal count from the value programmed into the NR and SM registers. The f_{REF} signal can be used to verify the divide ratio of the Reference divider.

If T1 = High and T0 = Low, the lock output is configured as f_{AUX}. The signal is normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NA and PA registers. The f_{AUX} signal can be used to verify the divide ratio of the Auxiliary divider.

If T1 = High and T0 = High, the lock output is configured as f_{MAIN}. The signal is the buffered output of the MAIN divider. The f_{MAIN} signal appears as normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NM1, NM2, NM3 or NM4 registers. The f_{MAIN} signal can be used to verify the divide ratio of the MAIN divider and the prescaler.

Test Pin

The Test pin, Pin 19, is a buffered logic input which is exclusively ORed with the output of the prescaler. The output of the XOR gate is the input to the MAIN divider. The Test pin must be connected to V_{DD} during normal operation as a synthesizer. This pin can be used as an input for verifying the divide ratio of the MAIN divider; while in this condition the input to the prescaler, RF_{IN}, may be connected to V_{CCP} through a 10kΩ resistor in order to place prescaler output into a known state.

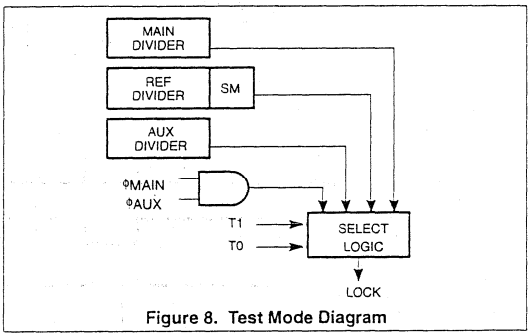
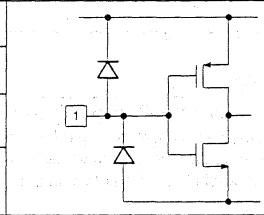
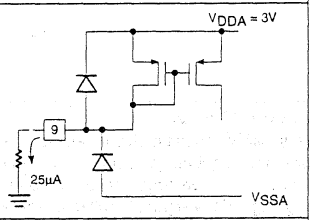
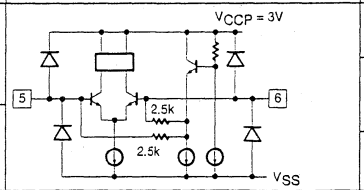
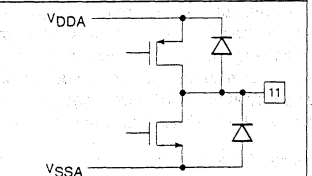
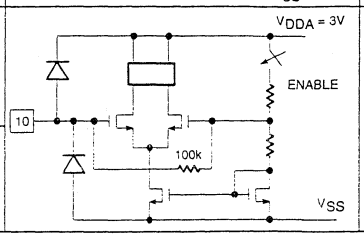
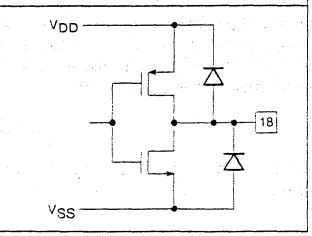


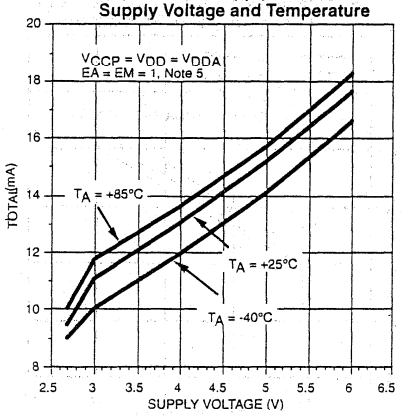
Figure 8. Test Mode Diagram

PIN FUNCTIONS

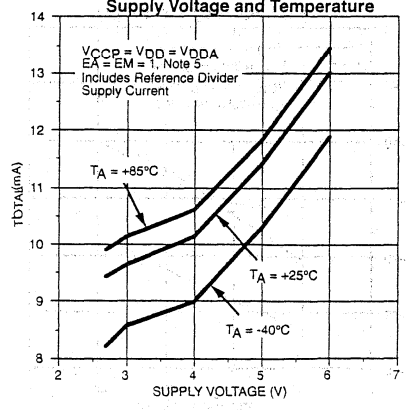
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	CLOCK	—		9	RA	1.35	
2	DATA	—		16	RN	1.35	
3	STROBE	—					
19	TEST	—		17	RF	1.35	
5	RF_{IN}	2.1		11	PHA	—	
6	$\overline{RF_{IN}}$	2.1		13	PHI	—	
				14	PHP	—	
8	REF_{IN}	1.8		18	LOCK	—	
10	AUX_{IN}	1.8					

TYPICAL PERFORMANCE CHARACTERISTICS

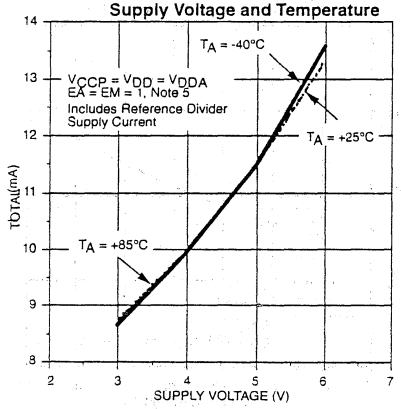
Operational Supply Current vs Supply Voltage and Temperature



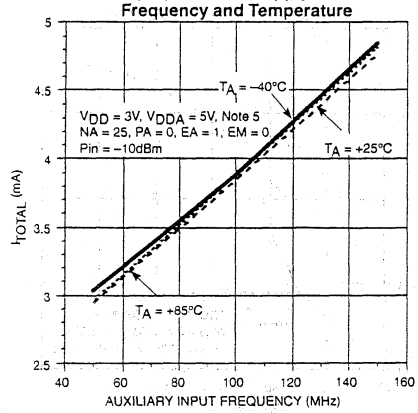
Main Operational Supply Current vs Supply Voltage and Temperature



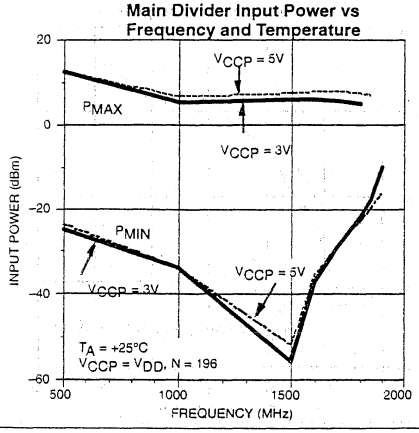
Auxiliary Operational Supply Current vs Supply Voltage and Temperature



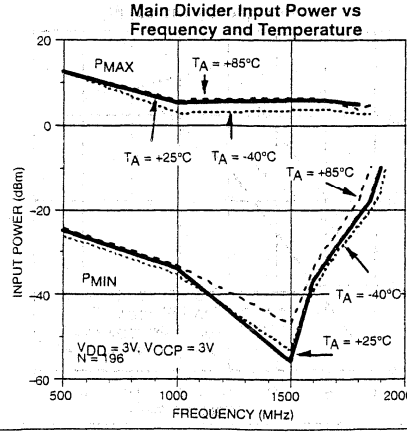
Auxiliary Operational Supply Current vs Frequency and Temperature



Main Divider Input Power vs Frequency and Temperature

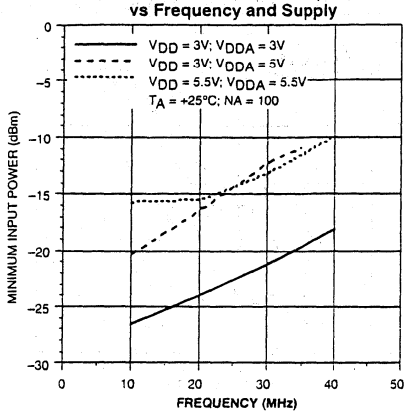


Main Divider Input Power vs Frequency and Temperature

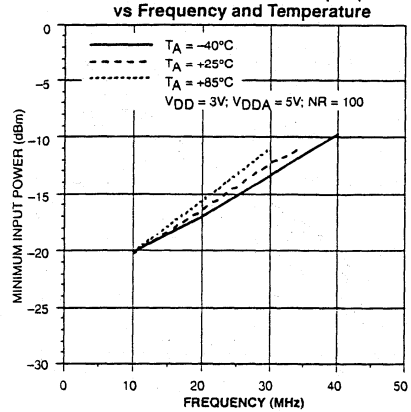


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

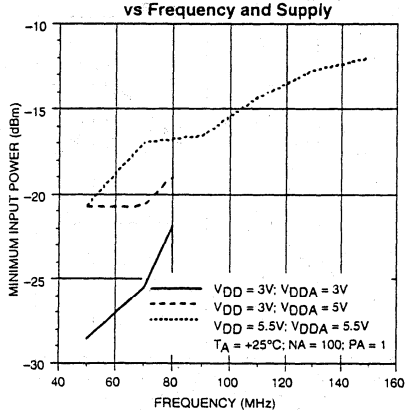
Reference Divider Minimum Input power vs Frequency and Supply



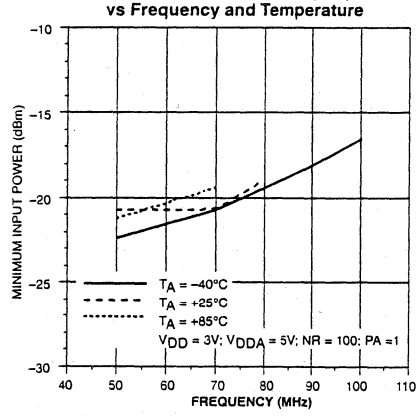
Reference Divider Minimum Input power vs Frequency and Temperature



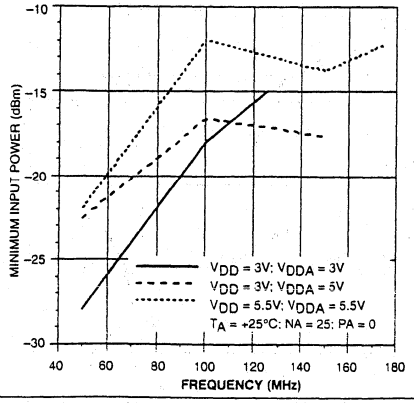
Auxiliary Divider Minimum Input power vs Frequency and Supply



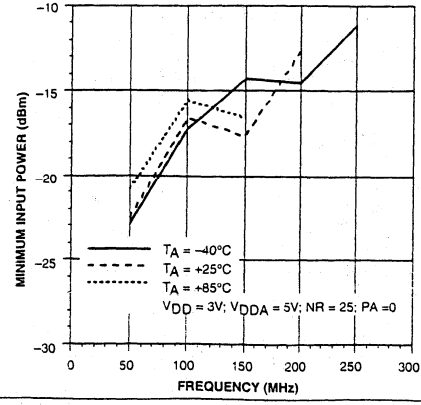
Auxiliary Divider Minimum Input power vs Frequency and Temperature

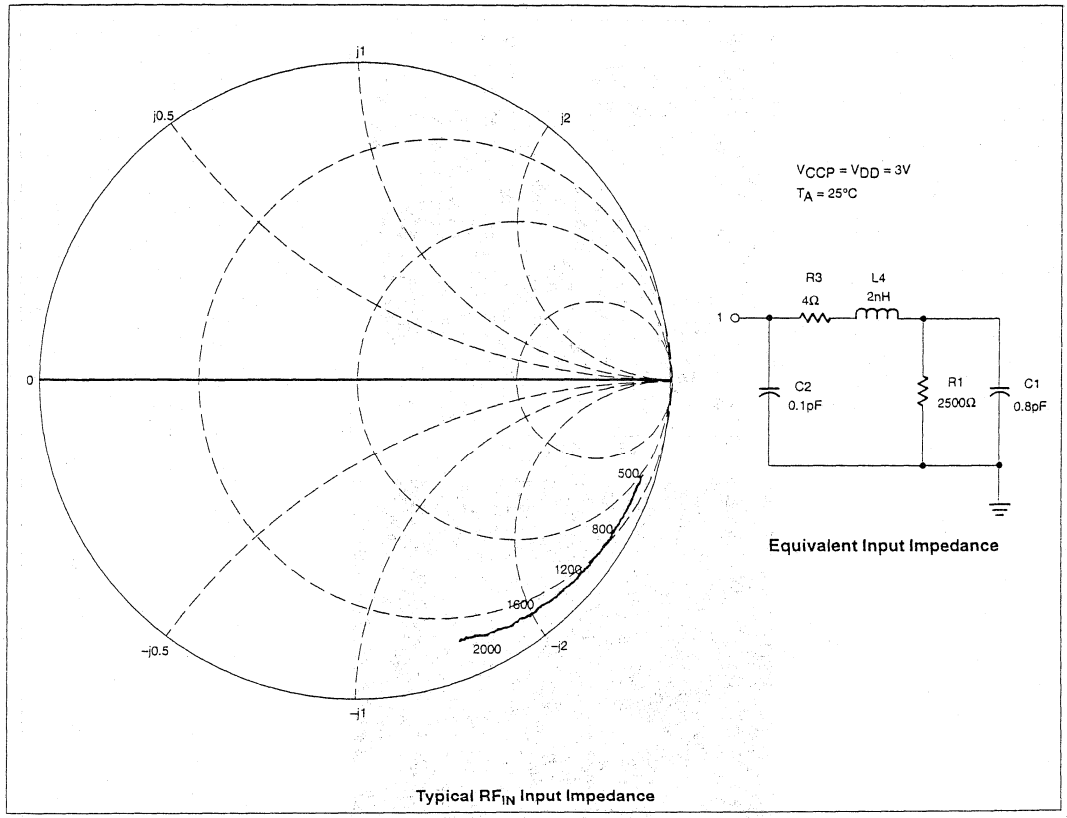


Auxiliary Divider Minimum Input power vs Frequency and Supply



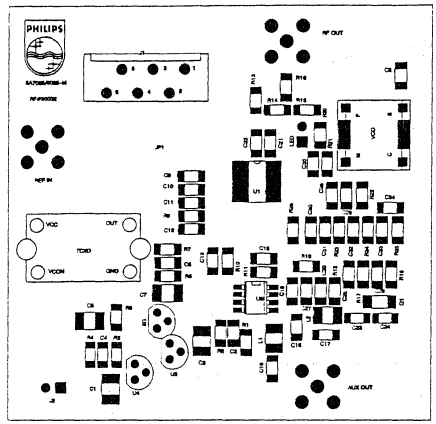
Auxiliary Divider Minimum Input power vs Frequency and Temperature



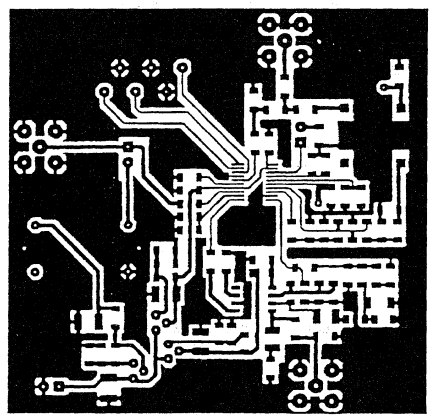


Typical RF_{IN} Input Impedance

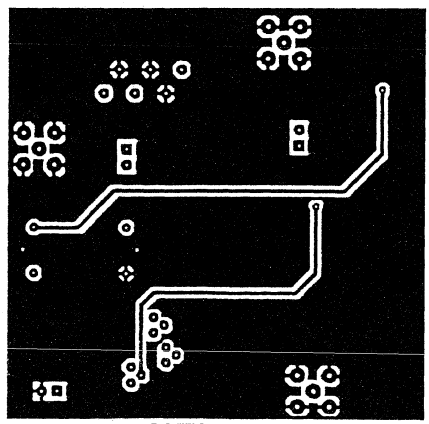
Equivalent Input Impedance



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

Figure 9. SA8025DK Demoboard Layout (NOT ACTUAL SIZE)

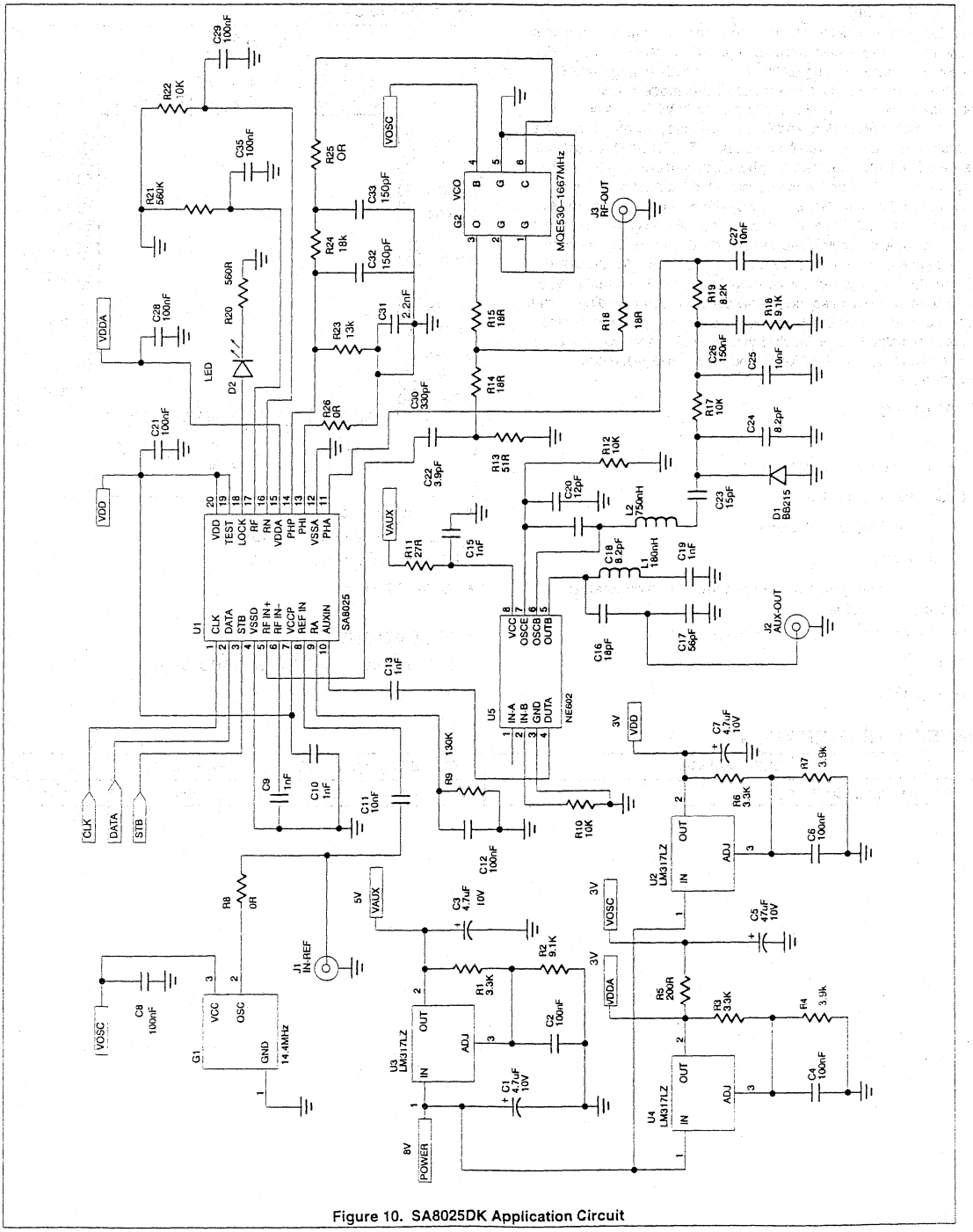


Figure 10. SA8025DK Application Circuit

I/Q transmit modulator SA900

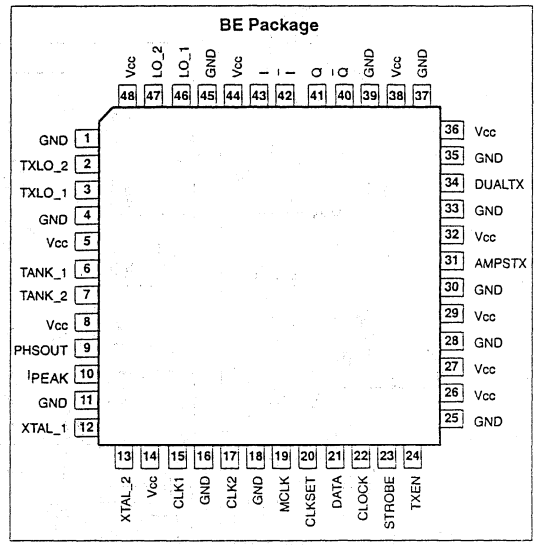
DESCRIPTION

The SA900 is a monolithic high performance, multi-function transmit modulator for use in cellular radio applications, fabricated in QUBiC BiCMOS technology. The SA900 features both analog (AMPS) mode and complex, I/Q digital (NADC IS54) mode quadrature modulation functions, a PLL synthesizer with VCO, crystal oscillator, programmable prescalers and Gilbert cell multiplier phase detector with programmable charge pump output. The DUALTX output can be used in DUAL mode cellular phone applications with the AMPS and NADC modulation being applied to the I/Q baseband inputs. The DUALTX output also provides 6-bit power control with 40dB of gain control in 0.63dB steps. In addition, buffered crystal oscillator programmable prescaler outputs are provided to support system clock reference needs. Programming of the SA900 functions are realized by a high speed 3-wire serial interface. The SA900 can be programmed into a sleep mode (low current mode providing crystal oscillator and Master Clock functions), a standby mode (providing crystal oscillator, Master Clock, System Clock 1 and Transmit LO buffer functions), and the AMPS mode and the DUAL mode configurations.

FEATURES

- V_{CC} = 4.8V
- Tx output frequency = 900MHz
- Direct modulation of RF
- DUAL mode, on-chip PA control
- I/Q modulator
- Single sideband quadrature LO generation with no external adjustments required
- On-chip crystal oscillator with 3 buffered outputs
- AMPS/TACS
- On-chip VCO

PIN CONFIGURATION



- Selective power-down
  - Low power AMPS/TACS mode
  - Low power dual mode NADC
- 48-Pin TQFP package

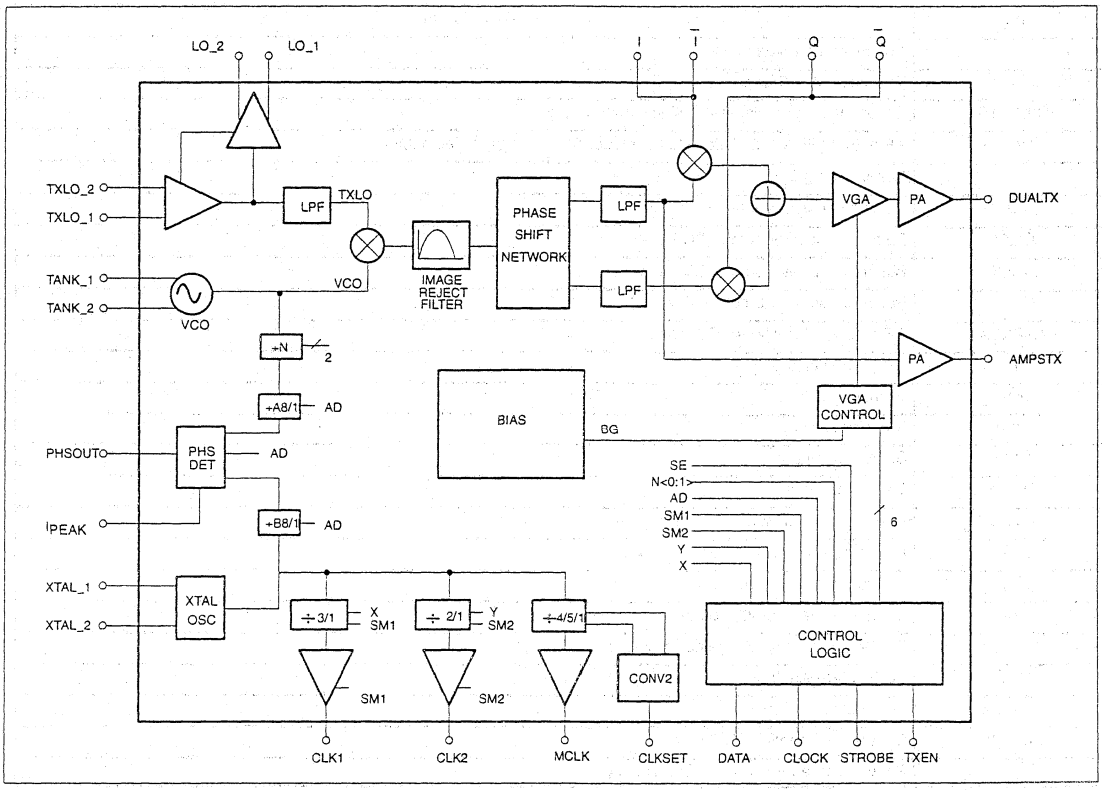
APPLICATIONS

- North American Digital Cellular (NADC IS-54)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (TQFP)	-40 to +85°C	SA900BE	1706A

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Description
I	Non-inverting I Mod Signal
$\overline{I}$	Inverting I Mod Signal
TXLO_1/2	Second LO Input (differential/single-ended input)
DUALTX	RF output (850MHz) digital (DUAL) mode, complex modulated output
Q	Non-inverting Q Mod Signal
$\overline{Q}$	Inverting Q Mod Signal
CLK1	Buffered oscillator output (XO ÷3/÷1)
MCLK	Buffered oscillator output (XO ÷4/÷5/÷1)
CLK2	Buffered oscillator output (XO ÷2/÷1)
AMPSTX	RF output (850MHz) AMPS mode
V_{CC}	+5V_{DC} power supply
GND	Ground
Data	Serial data input
Clock	Serial clock input
Strobe	Data strobe input
TXEN	AMPS and Dual Mode transmit enable
CLKSET	Program control pin for MCLK prescaler
XTAL1	Crystal oscillator base input
XTAL2	Crystal oscillator emitter output
PHSOUT	Phase comparator charge pump output
TANK_1	VCO differential tank
TANK_2	VCO differential tank
LO_1/2	Buffered differential TXLO output
I_{PEAK}	Phase comparator current programming

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)	600	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+10	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}.
   48-pin TQFP: θ_{JA} = 67°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.5 to 5.1	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.8V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply range		4.5		5.1	V
I_{CC}	Supply current	Sleep mode		3.4		mA
		Standby mode		8.7		
		AMPS mode		42		
		DUAL mode		68		
I / $\overline{I}$	In-phase differential baseband input	DC		$0.5V_{CC}$		V
Q / $\overline{Q}$	Quadraphase differential baseband input	DC		$0.5V_{CC}$		V
CLKSET	Divide by 4/5/1	÷ 4		V_{CC}		V
		÷ 5		$0.5V_{CC}$		
		÷ 1		0		
V_{IL}	Clock, data, strobe, TXEN	Input low	–0.3		$0.3V_{CC}$	V
V_{IH}	Clock, data, strobe, TXEN	Input high	$0.7V_{CC}$		V_{CC}+0.3	V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.8V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
TXLO_1/2	Transmit LO input (AC couple) (50Ω)	Input power	-13		-10	dBm
		VSWR (50Ω)		2:1		
		Frequency range	900		1040	MHz
TANK_1/2	VCO tank differential inputs	Frequency range	90		140	MHz
PHSOUT	Phase detector charge pump output	Output level	0.5		V_{CC}–0.5	V
I_{PEAK}	PHSOUT programming	R_{SET} = 75kΩ, AD=0		100		µA
		R_{SET} = 4.7kΩ, AD=1		6.4		mA
XTAL_1	XO transistor base	XO frequency	10		45	MHz
		External drive	150		500	mV_{P-P}
CLK1	XO divide 3/1, power down SM1=0, 50% duty cycle	Frequency range	3.33		45	MHz
	÷3, X=1, ÷1, X=0	Output level, 5kΩ ll 7pF		1		V_{P-P}
CLK2	XO divide 2/1, power down SM2=0	Frequency range	5		45	MHz
	÷2, Y=1, ÷1, Y=0	Output level, 5kΩ ll 7pF		1		V_{P-P}
MCLK	XO divide 4/5/1, 50% duty cycle	Frequency range	2		45	MHz
	÷4, CLKSET = V_{CC}, ÷5, CLKSET = 0.5V_{CC}, ÷1, CLKSET = 0V	Output level, 5kΩ ll 7pF		1		V_{P-P}
CLOCK	Serial data clock input, 33% duty cycle	Max clock rate			10	MHz
	Serial interface (CMOS levels)	Logic LOW			0.3V_{CC}	V
	DATA, CLOCK, STROBE, TXEN	Logic HIGH	0.7V_{CC}			V
AMPSTX	AMPS output, SE=1, AD=0, TXEN=1 (AC couple)	Frequency range	820		860	MHz
		VSWR		2:1		
		Output level	0	+2		dBm
	Spurious output	869 to 894MHz		-104		dBm
		824 to 849MHz		-47		dBc
		2 to 824MHz		-41		dBc
		849 to 869MHz		-41		dBc
		894MHz to 8.49GHz		-41		dBc
	TXLO and harmonics			-21		dBc
	Adjacent channel noise power	@30kHz		-95		dBc/Hz
	Alternate channel noise power	@60kHz		-101		dBc/Hz
	Broadband noise power	869 to 894MHz		-136		dBm/Hz
DUALTX	DUAL output, SE=1, AD=1, TXEN=1 (with external matching Figure 5)	Frequency range	820		920	MHz
		VSWR		2:1		
		Output level (avg min) (I and Q quad, 0dB VGA)	0	+2		dBm
		Gain flatness		1		dB

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DUALTX (cont.)	Linearity (0dB VGA, I and Q inphase)	3rd order		-42		dBc
		5th order		-55		dBc
		7th order		-65		dBc
	Carrier suppression (I and Q quadrature)	VGA = 0dB	-35	-45		dBc
	Carrier suppression (I and Q quadrature)	VGA = –40dB		-33		dBc
	Sideband suppression	I and Q quadrature	-35	-45		dBc
	Spurious output	869 to 894MHz		–104		dBm
		824 to 849MHz		–47		dBc
		2 to 824MHz		–41		dBc
		849 to 869MHz		–41		dBc
		894MHz to 8.49GHz		–41		dBc
	TXLO and harmonics			–21		dBc
	Broadband noise (0dB VGA)	869 to 894MHz		–136		dBm/Hz
		935 to 960MHz		–136		dBm/Hz
	Adjacent channel noise power	@30kHz		–95		dBc/Hz
	Alternate channel noise power	@60kHz		–101		dBc/Hz
Q/$\overline{Q}$	Baseband quadrature differential input	Max frequency			2	MHz
		Differential modulation level	0.6	0.8	1.0	V_{P-P}
		Differential input impedance	10			kΩ
I/$\overline{I}$	Baseband inphase differential input	Max frequency			2	MHz
		Differential modulation level	0.6	0.8	1.0	V_{P-P}
		Differential input impedance	10			kΩ
LO_1/2	Buffered TXLO differential outputs (AC coupled)	Frequency range	900		1040	MHz
		VSWR (single-ended)		2:1		
	Output impedance	single-ended		50		Ω
		differential		100		Ω
	Output level	single-ended, 50Ω		90		mV_{P-P}
		differential, 100Ω		180		mV_{P-P}

FUNCTIONAL DESCRIPTION

Dual Mode Operation

The SA900 transmit modulator provides direct single sideband quadrature modulation of the difference of the TXLO and VCO frequencies, while providing quadrature LO signals for the I/Q modulator. The quadrature LO signals are modulated with high linearity by the baseband inphase (I) and quadrature (Q) signals. The summed modulator output produces the lower sideband, while rejecting the upper sideband. The I and Q inputs also provide DC biasing for the modulator inputs. The summed output of the modulator goes to a variable gain amplifier (VGA) to control the output level, it has 40.0dB of attenuation control range, with 0.63dB steps. The power control function is programmed by means of a 6-bit word (see Table 3). The VGA output drives the power amp output stage to provide +2dBm average minimum power level (at 0dB power control) into 50Ω, in conjunction with external matching components on DUALTX. The AD (AMPS/DUAL) and the SE (synthesizer enable) bit control the power up/down of the DUAL mode function. The transition of the TXEN, from low to high turns on the modulator. The falling edge of the TXEN signal disables the synthesizer and modulator. The TXLO is a system supplied LO signal. The SA900 buffers the TXLO signal (LO_1/2) for use with the system synthesizer (such as the SA7025) to form the system LO synthesizer loop. The DUAL mode can also be used for AMPS operation. The AMPS and DUAL mode modulation is generated by the system DSP IC to provide the required I/Q baseband modulation for the SA900. The DUAL output provides low broadband noise output power (so that the receiver sensitivity is not degraded) and high linearity to meet cellular phone system needs. Table 1 provides the VGA power control limits.

The SA900 DUALTX output is externally matched with either a shunt inductor to V_{CC} and a series capacitor or a shunt inductor to V_{CC} and a series inductor. This matches the DUALTX output to 50Ω. Values of the matching components are dependent on PCB layout, typical values are shown in Figure 5.

Table 1. VGA Power Control Limits

Attenuation (dB)	Tolerance[1]
0.0 to 21.4	±0.4dB
22.0 to 27.7	±1.0dB
28.4 to 40.0	±2.0dB

1. Guaranteed to be monotonic.

AMPS Mode Operation

The SA900 can be configured to operate in the AMPS mode, where FM modulation is applied to the SA900's VCO. For the AMPS mode, the VCO is configured with the proper synthesizer bandwidth to allow the application of the AMPS modulation to the VCO varactor tuned tank circuit. The modulated VCO signal is input into an image reject mixer along with the TXLO signal, where the upper sideband is rejected. This single sideband modulated signal then drives the AMPS output power amplifier. The PA provides +2dBm power level into 50Ω, with no external matching components required. The AD (AMPS/DUAL) and the SE (synthesizer enable) bit control the power up/down of the AMPS mode function. The transition of the TXEN signal from low to high turns on the modulator. The falling edge of TXEN signal disables the synthesizer and the modulator.

Synthesizer Operation

The SA900 synthesizer is comprised of the differential VCO circuit, with external tank components, the Gilbert cell multiplier phase detector with programmable charge pump current, crystal oscillator and programmable prescalers. The charge pump output drives an external second order loop filter. The output of the loop filter is used to provide the control voltage to the VCO tuning varactor to complete the PLL synthesizer. The synthesized VCO output frequency is mixed with the TXLO signal to generate the transmit LO from the lower sideband (the difference of the VCO and TXLO frequencies). The output of VCO is fed to a programmable /N prescaler with user selectable divides of 6, 7, 8 and 9 (all divides configured to provide 50% duty cycle). The output of the /N divider drives the A8/1 prescaler. The A8/1 divide is selected by the AD control bit (AD=1 for /1, and AD=0 for /8). The output of the divide A8/1 is fed into one input of the phase detector. The reference input for the phase comparator is generated from the crystal oscillator (XO) output from the B8/1 prescaler. The B8/1 divide is selected by the AD control bit (AD=0 for /8, and AD=1 for /1). The phase detector compares the prescaled XO reference phase to the VCO prescaled phase, to generate a charge pump output current proportional to the phase error. The phase detector, a Gilbert cell multiplier type, having a linear output from 0 to π ($\pi/2 \pm \pi/2$). The charge pump peak output current is programmable from 100µA for the AMPS mode (AD=0) to a maximum of 6.4mA for the DUAL mode (AD=1) by way of an external current setting resistor placed from I_{PEAK} to circuit ground. The typical loop filter network

Table 2. Data Word Format

Mnemonics	Bits	Function
A0	1 (MSB)	Address bit 0 (1)
A1	2	Address bit 1 (0)
A2	3	Address bit 2 (1)
A3	4	Address bit 4 (1)
PC0	5	Power control bit 0
PC1	6	Power control bit 1
PC2	7	Power control bit 2
PC3	8	Power control bit 3
PC4	9	Power control bit 4
PC5	10	Power control bit 5
N0	11	Divide N bit 0
N1	12	Divide N bit 1
AD	13	AMPS/DUAL mode select bit
SE	14	Synthesizer enable bit
NA	15	NA
SM1	16	Sleep mode 1 control bit
SM2	17	Sleep mode 2 control bit
X	18	Divide 3/1 control bit
Y	19	Divide 2/1 control bit
NA	20	NA
NA	21	NA
NA	22	NA
NA	23	NA
NA	24 (LSB)	NA

is shown in Figure 1. The charge pump current output is programmed by

$$AD = 0 \qquad I_{OUT} = 6 \cdot \left(\frac{1.25V}{R_{SET}}\right)$$

$$AD = 1 \qquad I_{OUT} = 24 \cdot \left(\frac{1.25V}{R_{SET}}\right)$$

where R_{SET} is placed between I_{PEAK} and GROUND.

The PLL frequency is determined by

$$VCO = XO \cdot N \cdot \frac{\left(\frac{A8}{1}\right)}{\left(\frac{B8}{1}\right)}$$

where N=6, 7, 8, 9 and A8/1 and B8/1 are controlled by the AD bit (AD=1 A8/1 and B8/1 are divide by 1, AD=0 A8/1 and B8/1 are divide 8).

VCO Operation

The VCO is designed to operate from 90MHz to 140MHz. The VCO tank is configured using a parallel inductor and a dual common cathode tuning varactor diodes. DC blocking capacitors are used to isolate the varactor
control voltage from the VCO tank DC bias voltages. The VCO tuning voltage is generated from the output of the PLL loop filter. The VCO tank configuration is shown in Figure 2.

Crystal Oscillator (XO) Operation

For cellular radio applications, the SA900 will most likely utilize an external reference TCXO in order to provide the frequency stability necessary to operate to system requirements. The output of the system TCXO can be AC coupled to the XTAL_1 input. However, for applications that do not require such accuracy the XO circuit can be configured as a Colpitts type oscillator with the addition of two external capacitors along with the reference crystal and a trim capacitor as shown in Figure 3.

Programmable Clock Outputs

The SA900 generates three buffered XO outputs used for external reference signals. The XO feeds three sets of programmable prescalers, the prescaler outputs are buffered to provide the CLK1, CLK2 and MCLK signals. The CLK1 signal is a selectable divide 3/1 (X=1 divide 3, X=0 divide 1), 50% duty cycle, of the XO reference signal. The CLK2 signal is a selectable divide 2/1 (Y=1 divide 2, Y=0 divide 1), 50% duty cycle, of the XO reference signal. The MCLK signal is a selectable divide 4/5/1 (CLKSET = V_{CC} divide 4, CLKSET = $V_{CC}/2$ divide 5, and CLKSET = 0V divide 1), 50% duty cycle, of the XO reference signal. MCLK is externally set by means of the tri-level CLKSET input to provide a default master system clock prior to programming the SA900.

Programming Operation

The SA900 is configured by means of a 3-wire input (CLOCK, STROBE, DATA) to program the AMPS and DUAL modes, in addition there are two power saving modes of operation, SLEEP and STANDBY. The control logic section of the SA900 is designed using low power CMOS logic. During SLEEP mode only the circuitry required to provide a master clock (MCLK) to the digital portion of the system is enabled. During the STANDBY mode of operation MCLK, CLK1 and the TXLO and buffered LO outputs are powered on, which may be the case when the system is in the receive only mode. In the AMPS or DUAL operational modes all functions of the SA900 are powered on to support receive, transmit and system clock functions. The programming of the SA900 is identical to the programming format of the SA7025 low-voltage 1GHz fractional-N synthesizer, that can be used in conjunction with the SA900 to provide the cellular radio channel selection.

The programming data is structured as a 24 bit long serial data word; the word includes 4 address bits (dedicated 1 0 1 1) for chip select. Data bits are shifted in on the leading edge of the clock, with the least significant bit (LSB) first and the most significant bit (MSB) last. Table 2 shows data word format, the 15th and last 5 bits are not used. Figure 4 shows the chip timing diagram.

Address

A0	A1	A2	A3
1	0	1	1

Divide By N

N0	N1	Divide
0	0	6
1	0	7
0	1	8
1	1	9

AMPS/DUAL Mode

The A/D mode select enables or disables that portion of the circuitry used for either the AMPS or DUAL mode of operation.

AD	Mode
0	AMPS
1	DUAL

Synthesizer Enable

The SE bit turns on and off the synthesizer circuitry.

SE	Operation
0	Disabled
1	Enabled

Sleep Mode 1

The SM1 bit is used to power down the TXLO buffer, the divide 3/1 prescaler and the CLK1 output buffer.

SM1	Operation
0	Power down
1	Power up (STANDBY)

Sleep Mode 2

The SM2 bit is used to power down the divide 2/1 prescaler and the CLK2.

SM2	Operation
0	Power down
1	Power up (with SM1=1 normal operation)

Divide 3

X	Operation
0	Divide 1
1	Divide 3

Divide 2

Y	Operation
0	Divide 1
1	Divide 2

Table 3. Power Control

Atten (dB)	PC0 (0.6dB)	PC1 (1.3dB)	PC2 (2.5dB)	PC3 (5.0dB)	PC4 (10.0dB)	PC5 (20.0dB)
0	0	0	0	0	0	0
0.6	1	0	0	0	0	0
1.3	0	1	0	0	0	0
1.9	1	1	0	0	0	0
2.5	0	0	1	0	0	0
3.2	1	0	1	0	0	0
3.8	0	1	1	0	0	0
4.4	1	1	1	0	0	0
5.0	0	0	0	1	0	0
5.7	1	0	0	1	0	0
6.3	0	1	0	1	0	0
⋮						
23.3	1	0	1	0	0	1
⋮						
39.7	1	1	1	1	1	1

Component Designator	Value	
	DUAL Mode	AMPS Mode
R1	560Ω	560Ω
R2	1kΩ	5.6kΩ
C1	2.2nF	2.7μF
C2	No Load	.27μF
C3	33pF	6.8nF
R_{SET}	15kΩ	75kΩ

Typical Filter Network

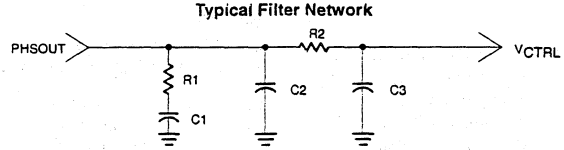


Figure 1. PLL Loop Filter

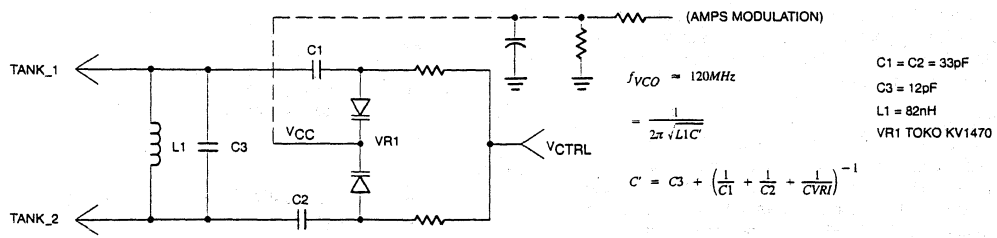


Figure 2. VCO Tank Configuration

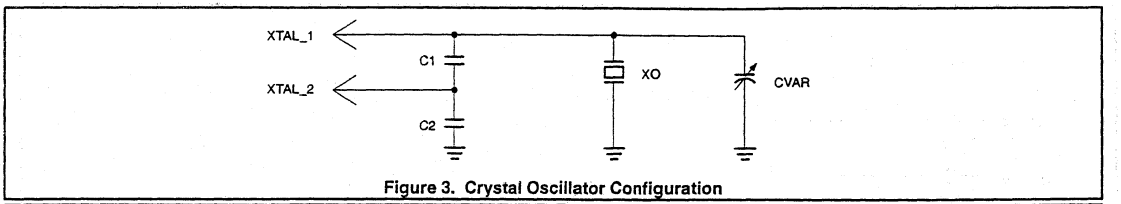


Figure 3. Crystal Oscillator Configuration

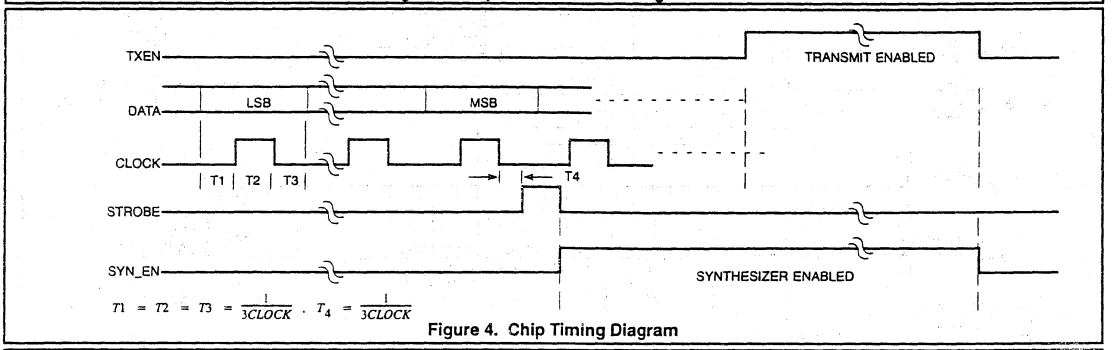


Figure 4. Chip Timing Diagram

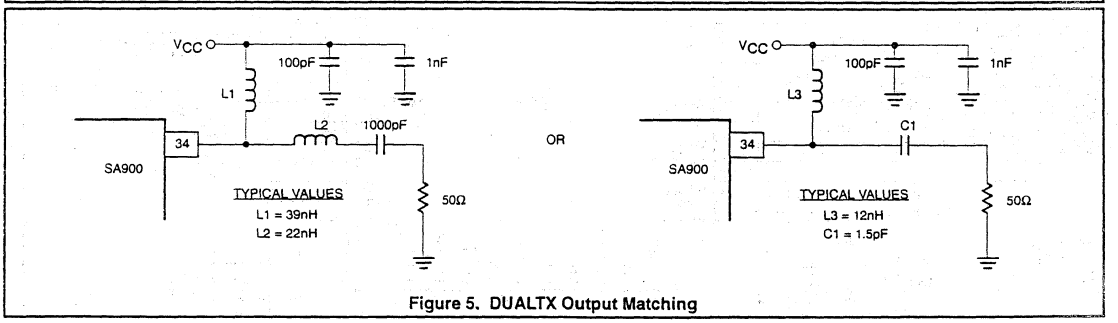


Figure 5. DUALTX Output Matching

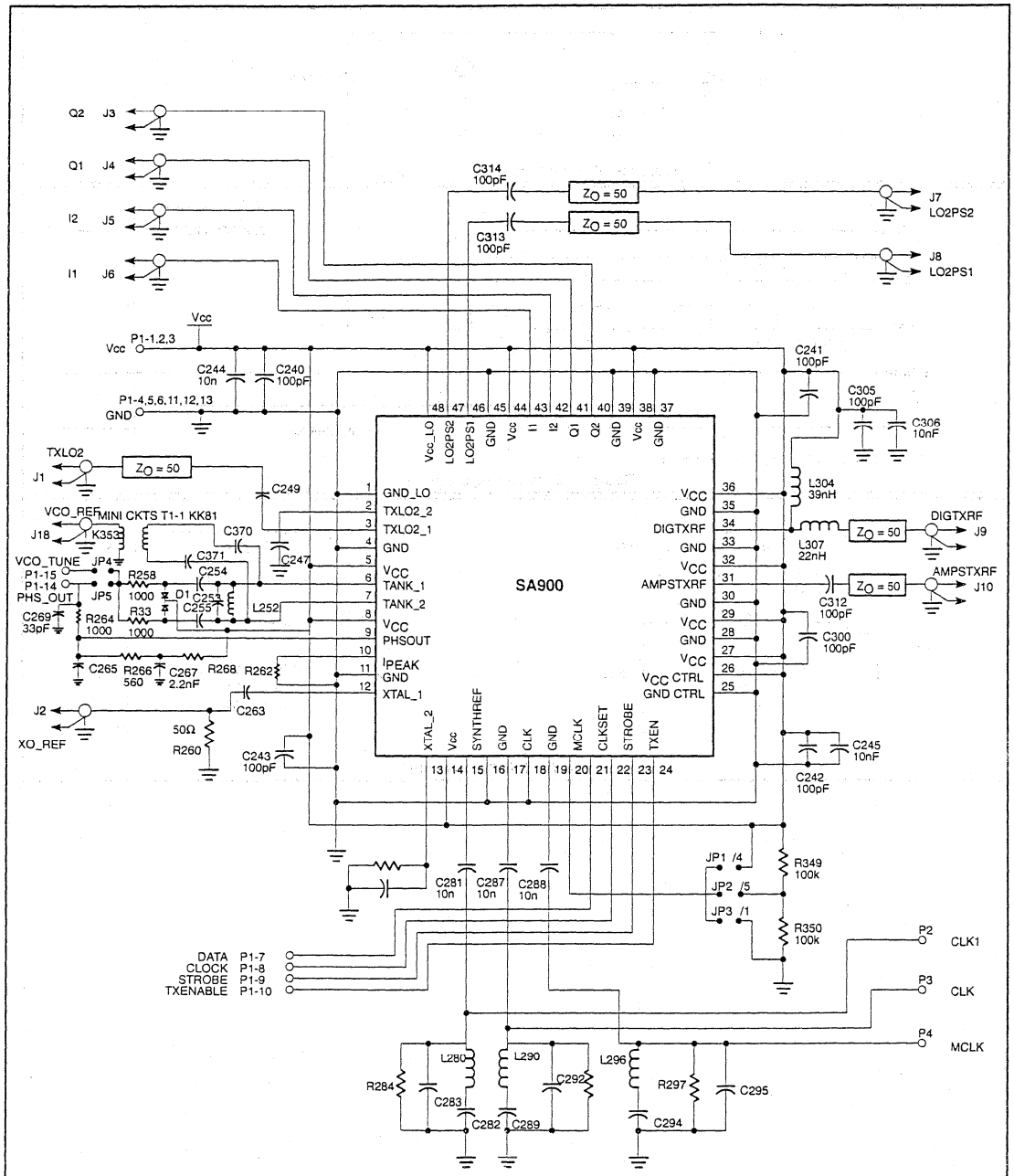
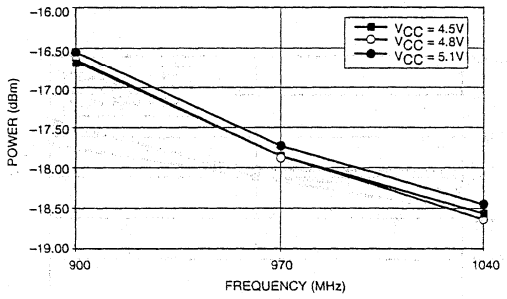
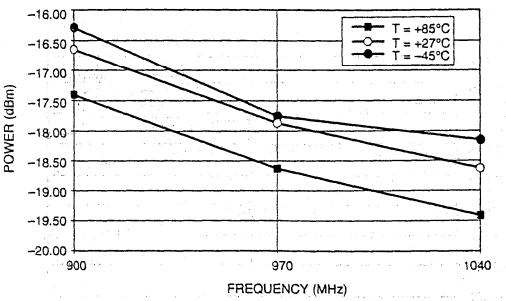


Figure 6. SA900 Application Circuit

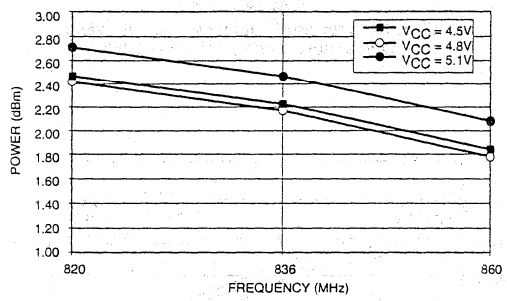
PERFORMANCE CHARACTERISTICS



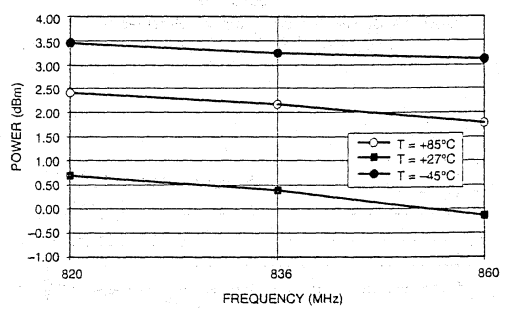
LO Buffer vs. Frequency (27°C, TXLO = –10dBm)



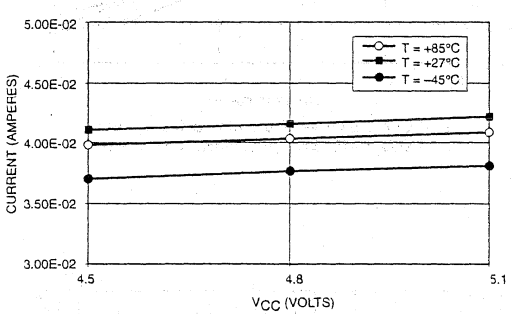
LO Buffer vs. Frequency (V_{CC} = 4.8V, TXLO = –10dBm)



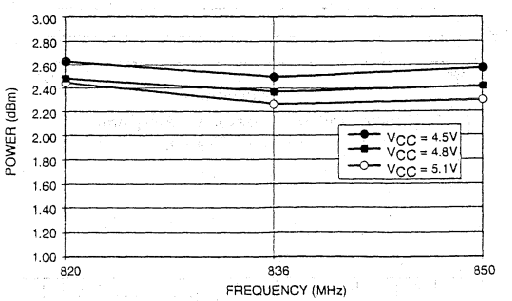
AMPTX vs. Frequency (27°C, TXLO = –10dBm)



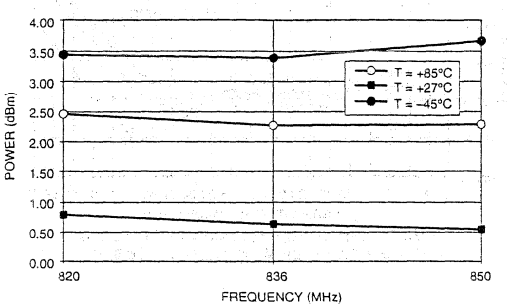
AMPTX vs. Frequency (V_{CC} = 4.8V, TXLO = –10dBm)



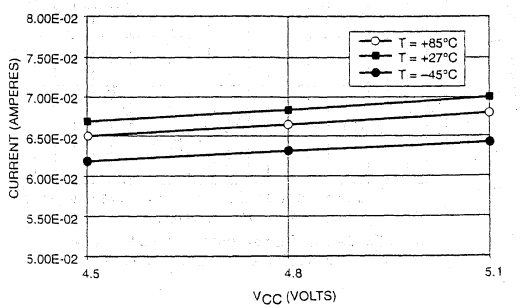
AMP I_{CC} vs. V_{CC}



DUALTX vs. Frequency (27°C, TXLO = –10dBm)

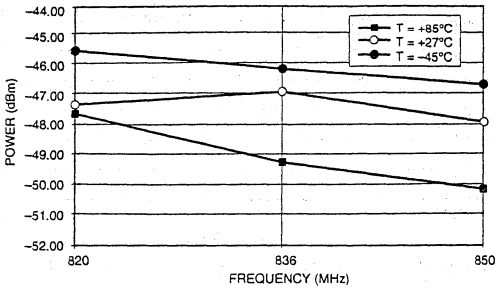


DUALTX vs. Frequency (V_{CC} = 4.8V, TXLO = –10dBm)

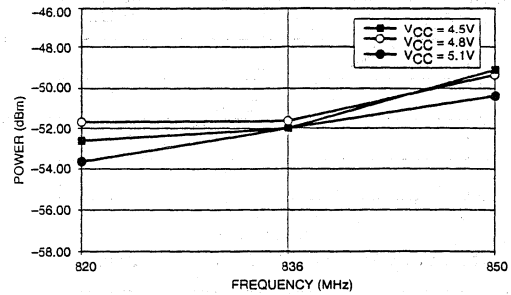


DUAL I_{CC} vs. V_{CC}

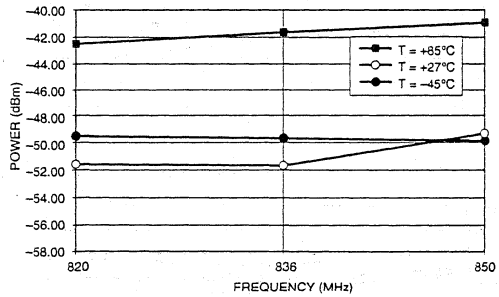
PERFORMANCE CHARACTERISTICS



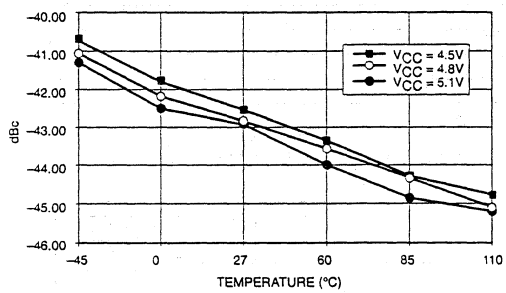
DUALTX Carrier Suppression vs. Frequency
(V_{CC} = 4.8, TXLO = –10dBm)



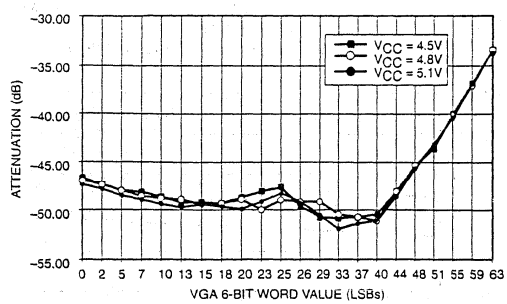
DUALTX Sideband Suppression vs. Frequency
(Temperature = 27°C, TXLO = –10dBm)



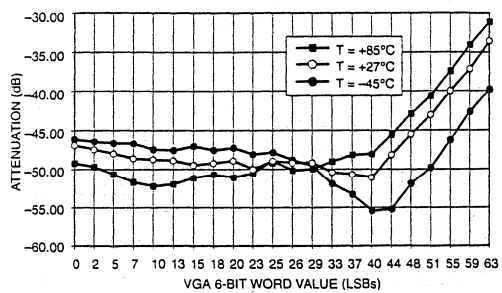
DUALTX Sideband Suppression vs. Frequency
(V_{CC} = 4.8, TXLO = –10dBm)



DUALTX 3rd Order Products vs Temperature
(TXLO = –10dBm, f = 836MHz, 0dB VGA)

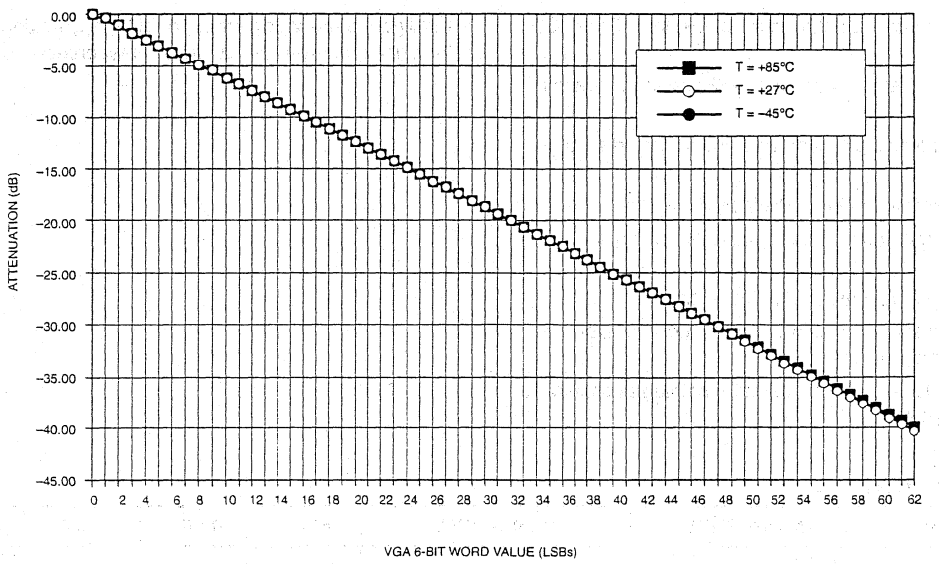


DUALTX Carrier Suppression vs VGA Range
(27°C, f = 836MHz, TXLO = –10dBm)

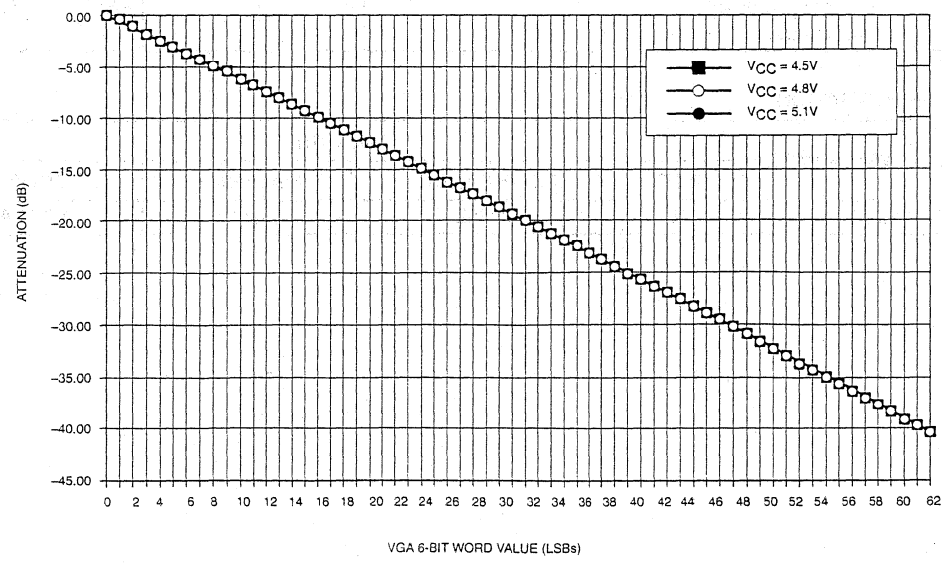


DUALTX Carrier Suppression vs VGA Range
(V_{CC} = 4.8V, f = 836MHz, TXLO = –10dBm)

PERFORMANCE CHARACTERISTICS



DUALTX VGA Attenuation Profile vs. Temperature (V_{CC} = 4.8V, f = 836MHz, TXLO = –10dBm)



DUALTX VGA Attenuation Profile vs. V_{CC} (27°C, f = 836MHz, TXLO = –10dBm)

State-of-charge indicator for NiMH and NiCd powered applications

SAA1500T

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

FEATURES

- 5-segment state-of-charge indication for LED or LCD displays
- Numerous display facilities to indicate the operational modes
- Designed for constant charge and varying discharge currents
- Large dynamic range of discharge currents
- Independent setting for charge and discharge efficiency
- Battery self-discharge compensation
- Automatic switch-over from fast to trickle charge (to prevent overcharging)
- Low standby current for permanent integration into a battery pack.

APPLICATIONS

- Intelligent battery powered, portable, applications with 'remaining energy' indication and fast charge control.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		1.8	–	7.0	V
I_{CC}	supply current	V_{CC} = 2.6 V; V_{CI} = 0 V	–	–	90	µA
f_{OSC}	fixed frequency	charging	–	4.2	–	kHz
V_{CI}	input sense voltage	discharging	20	–	200	mV
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1500T	20	SO20L	plastic	SOT163AH

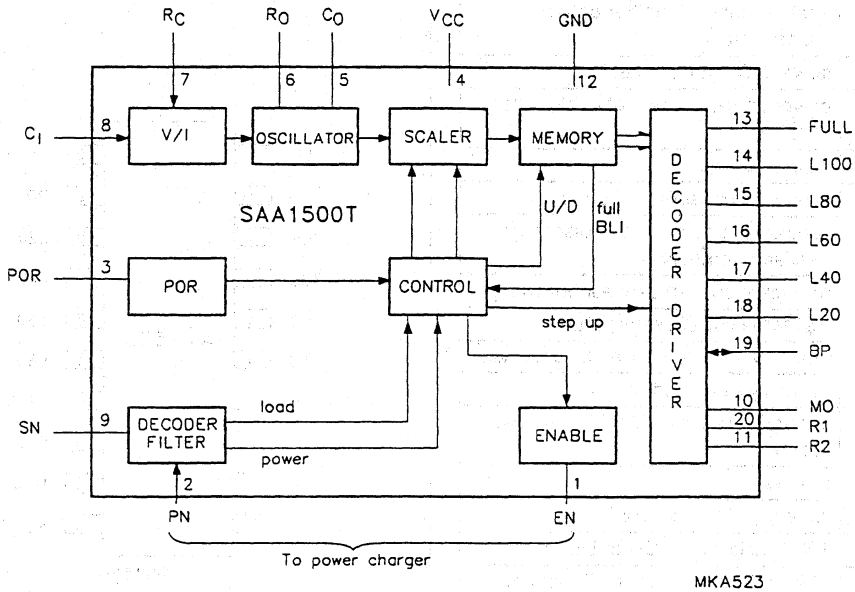


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
EN	1	enable control signal for battery charge unit
PN	2	power NOT mode detection
POR	3	power-on-reset, reset at LOW battery voltage
V_{CC}	4	supply voltage
C_O	5	capacitor for oscillator frequency
R_O	6	resistor for charge or self-discharge oscillator frequency
R_C	7	resistor to convert sense input voltage
C_I	8	discharge current sense input
SN	9	switch NOT, load switch ON detection
MO	10	mains ON state indication
R2	11	battery LOW drive signal for external buzzer
GND	12	ground
FULL	13	battery FULL indication, only LCD
L100	14	100% indication, LCD or LED driven
L80	15	80% indication, LCD or LED driven
L60	16	60% indication, LCD or LED driven
L40	17	40% indication, LCD or LED driven
L20	18	20% indication, LCD or LED driven
BP	19	backplane, (LCD), LCD/LED mode detection input
R1	20	battery LOW indicator, LOW drive

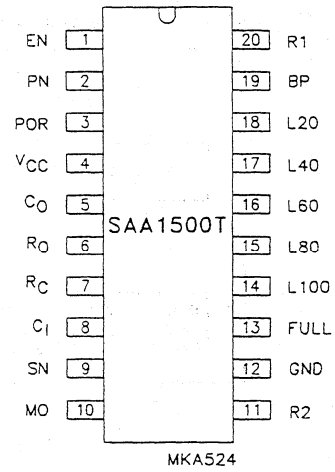


Fig.4 Pin configuration.

Battery level indicator SAA1501T

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

FEATURES

- High level of integration to allow assembly in intelligent battery packs
- Accurate charge and discharge account
- Large dynamic range of charge and discharge currents
- Independent settings of charge and discharge efficiency
- 2 V minimum supply voltage (2 cell operation)
- Temperature adjustment via adjustable absolute temperature detection
- Temperature controlled self-discharge register
- Accurate charge current regulation
- Two charge amount display modes, LCD and LED.

GENERAL DESCRIPTION

The SAA1501T is intended to be used as a battery monitor and control circuit in rechargeable battery systems.

The SAA1501T is processed in BiCMOS technology where the benefits of mixed bipolar and CMOS technology is fully utilized to achieve a high accuracy. The general function of the integrated circuit is a Coulomb counter. During battery charging, the charge current and charge time are registered in a Coulomb counter. During discharge, the discharge current and time are recorded. The momentary charge amount of the batteries can be displayed either on an LCD screen or on an LED bargraph. Using the SAA1501T, intelligent batteries or intelligent battery powered systems can be easily designed with only a few external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.0	3.0	4.3	V
I_{CC}	supply current	V_{CC} = 3 V; $I_c = I_d$ = 60 µA	–	1.2	1.7	mA
I_{CCstb}	supply current in standby mode	V_{CC} = 3 V; $V_{CSI} = V_{DSI}$ = 0 V	–	–	100	µA
f_{osc}	fixed oscillator frequency	C_{osc} = 820 pF; R_{ref} = 51.5 kΩ	–	4.2	–	kHz
$V_{i(s)}$	input sense voltage (pins 9 and 10)		0	–	V_{CC} – 1.6	V
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA1501T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

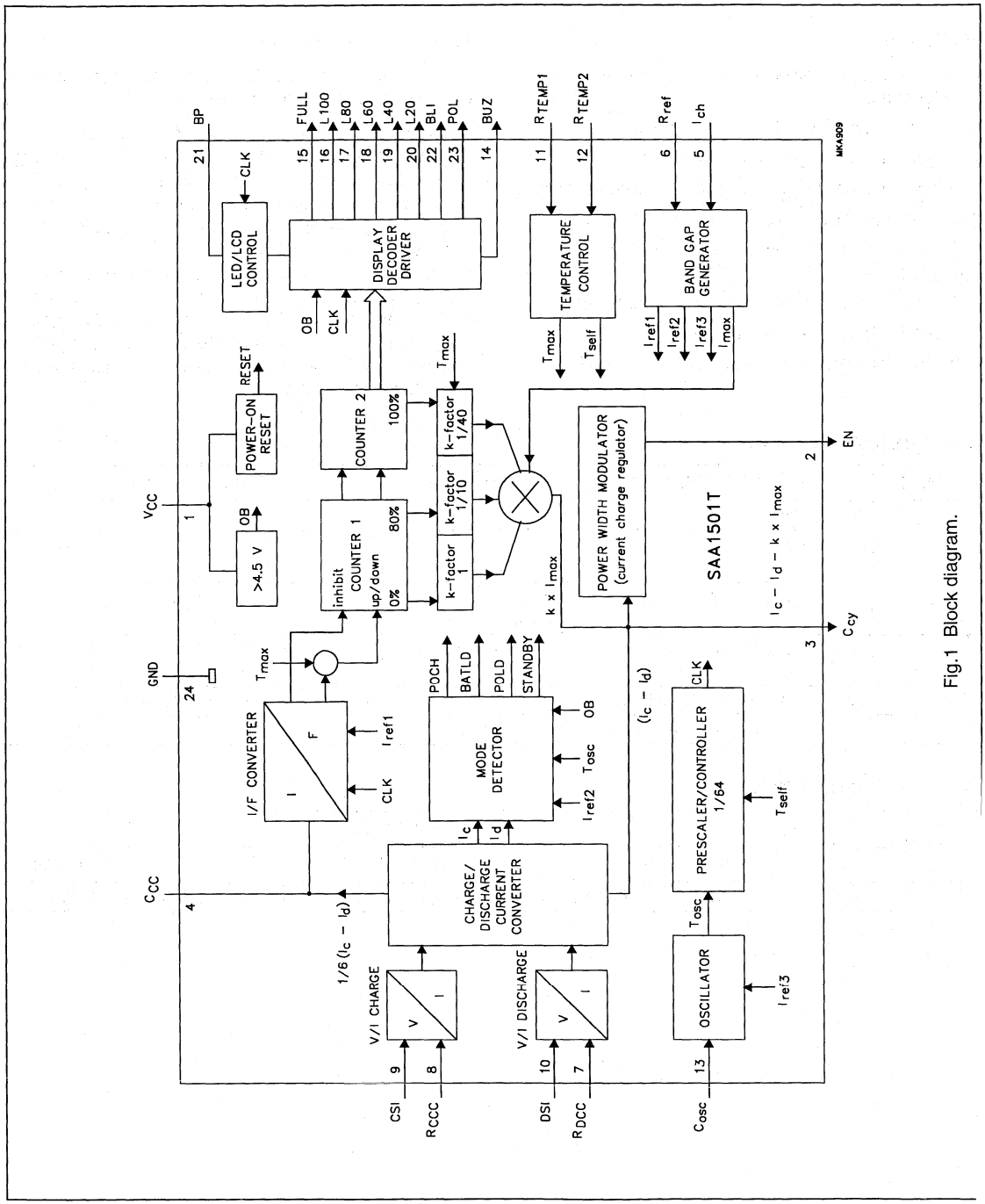


Fig.1 Block diagram.

6 W audio power amplifier in car applications
10 W audio power amplifier in mains-fed applications

TDA1010A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 24	V
Repetitive peak output current	I_{ORM}	max.	3	A
Output power at pin 2; d_{tot} = 10%				
V_P = 14,4 V; R_L = 2 Ω	P_O	typ.	6,4	W
V_P = 14,4 V; R_L = 4 Ω	P_O	typ.	6,2	W
V_P = 14,4 V; R_L = 8 Ω	P_O	typ.	3,4	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_O	typ.	9	W
Total harmonic distortion at P_O = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	typ.	30	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31	mA
Sensitivity for P_O = 5,8 W; R_L = 4 Ω	V_i	typ.	10	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

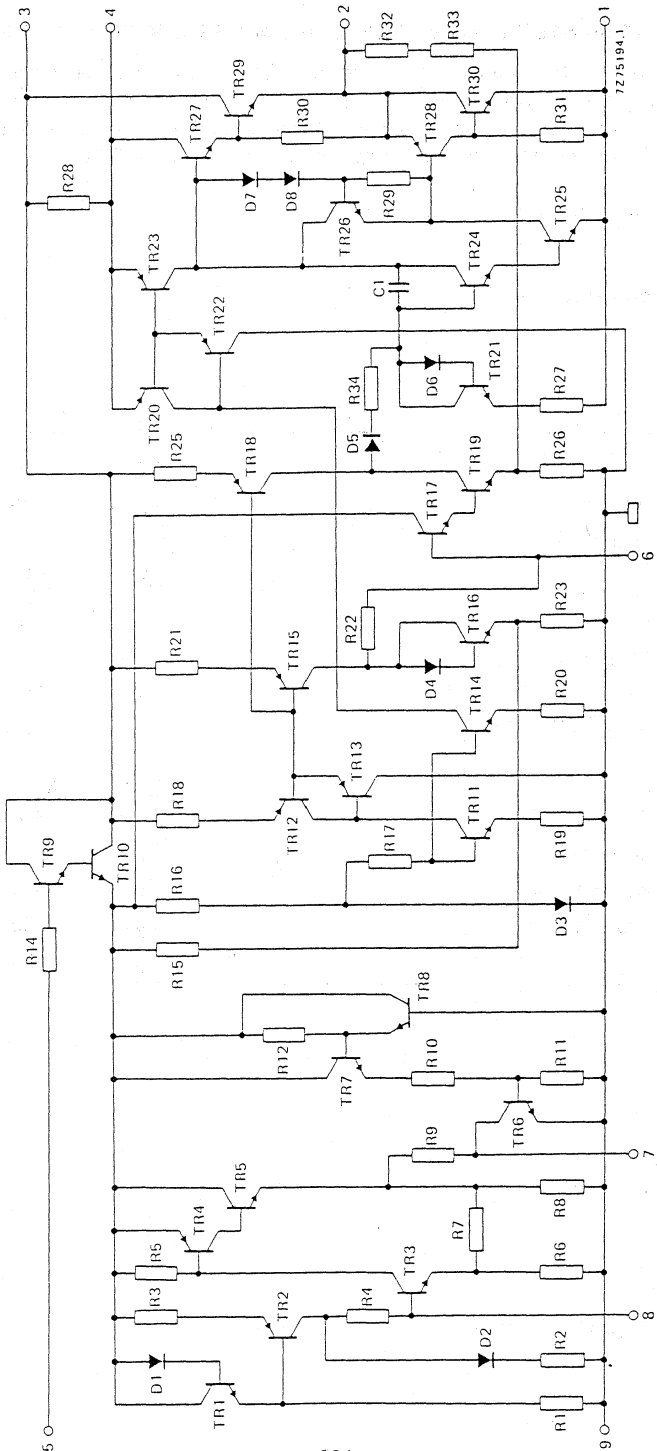


Fig. 1 Circuit diagram.

2 to 6 W audio power amplifier TDA1011

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 20	V
Peak output current	I_{OM}	max. 3	A
Output power at d_{tot} = 10%			
V_P = 16 V; R_L = 4 Ω	P_o	typ. 6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ. 0,2	%
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	> 100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ. 20	kΩ
Total quiescent current	I_{tot}	typ. 14	mA
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

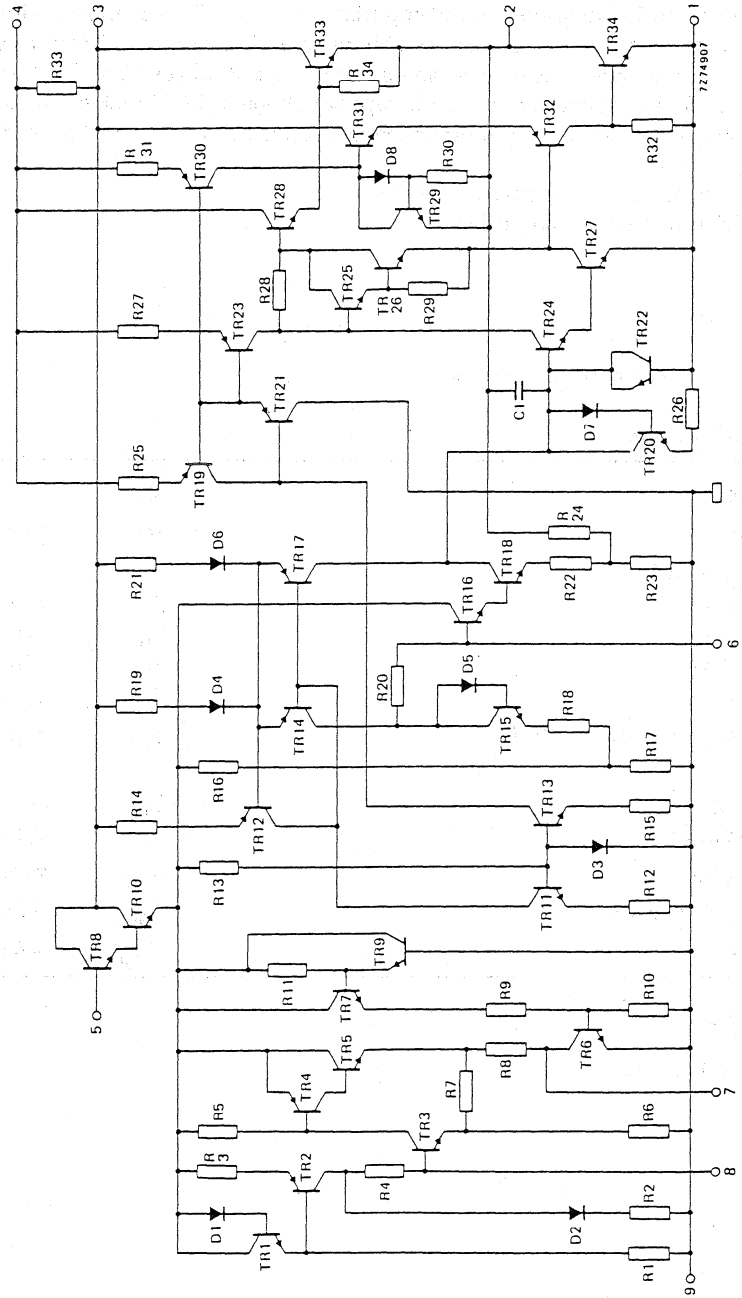


Fig. 1 Circuit diagram.

0.5 W audio power amplifier — TDA1015T

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 12	V
Peak output current	I_{OM}	max.	1	A
Output power	P_o	typ.	0,5	W
Voltage gain power amplifier	G_{v1}	typ.	29	dB
Voltage gain preamplifier	G_{v2}	typ.	23	dB
Total quiescent current	I_{tot}	max.	22	mA
Operating ambient temperature range	T_{amb}		−25 to +150	°C
Storage temperature range	T_{stg}		−55 to +150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

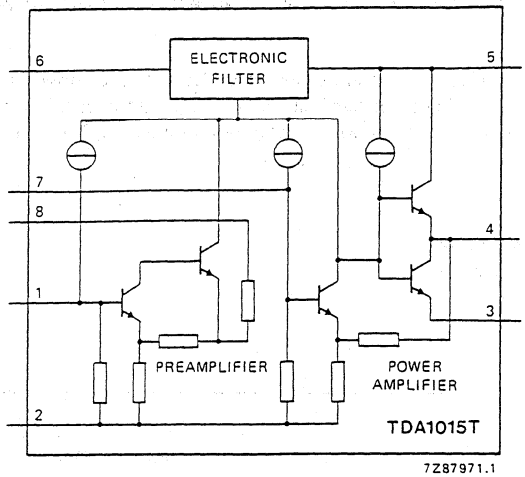


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	12 V
Peak output current	I_{OM}	max.	1 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range			−55 to +150 °C
A.C. short-circuit duration of load during sine-wave drive at V_P = 9 V	t_{sc}	max.	1 hour

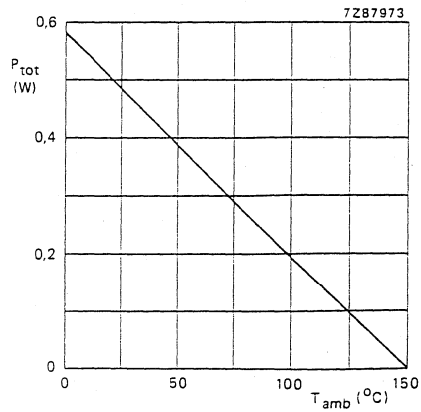


Fig. 2 Power derating curve.

FM-IF amplifier/demodulator circuit — TDA1576T

FEATURES

- Fully balanced 4-stage limiting IF amplifier
- Symmetrical quadrature demodulator
- Field-strengh indication output for 1 mA ammeter
- Detune detector for side response and noise attenuation
- Detune voltage output
- Internal muting circuit
- 0° and 180° AF output signals
- Reference voltage output
- Electronic smoothing of the supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)	7.5	8.5	15	V
I_P	supply current	10	16	23	mA
V_{iIF}	input sensivity (RMS value)				
	–3 dB before limiting	14	22	35	μV
	S/N = 26 dB	-	10	-	μV
	S/N = 46 dB	-	55	-	μV
V_{oAF}	AF output signal (RMS value)	-	67	-	mV
THD	total harmonic distortion with double resonant circuits	-	0.02	-	%
S/N	signal-to-noise ratio (V_i > 1 mV)	-	72	-	dB
α_{AM}	AM suppression	-	50	-	dB
RR	ripple rejection (f = 100 Hz)	43	48	-	dB
I_{15}	maximum indicator output current	-	-	2	mA
T_{amb}	operating ambient temperature	–30	-	+80	°C

GENERAL DESCRIPTION

The TDA1576T is a monolithic integrated FM-IF amplifier circuit for use in mono and stereo FM-receivers of car radios or home sets.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1576T	20	mini-pack	plastic	SOT163A

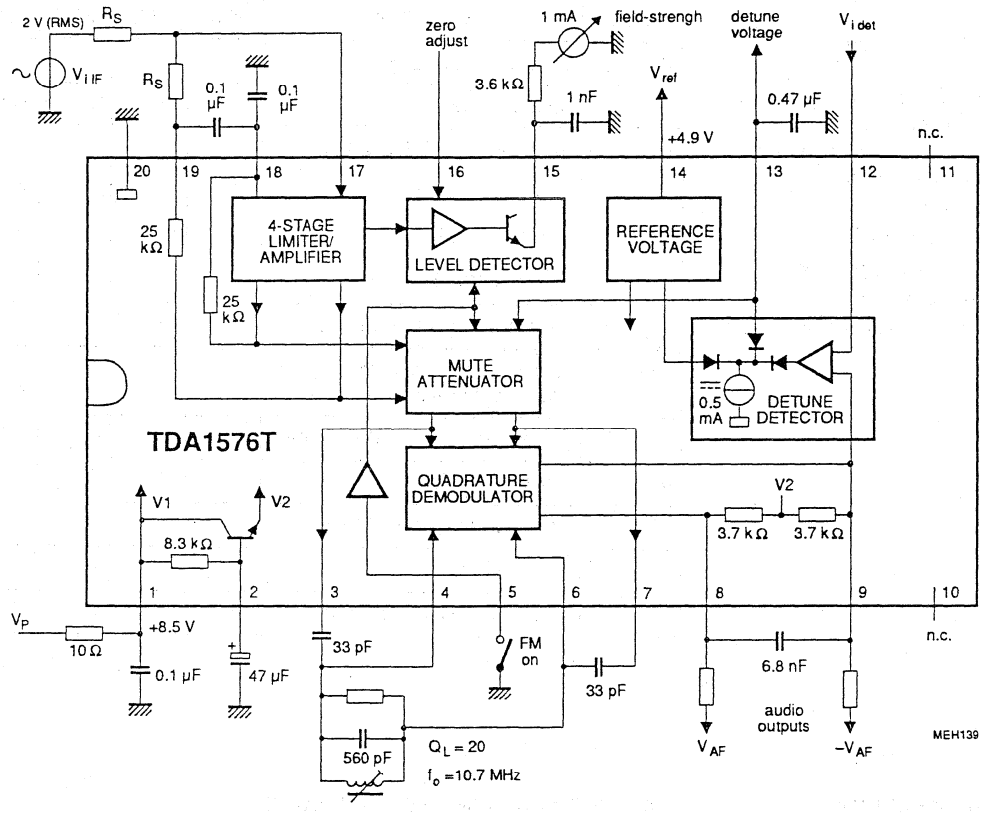


Fig.1 Block diagram and application circuit.

FM-IF amplifier/demodulator circuit TDA1576T

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
C_{PS}	2	smoothing capacitor of power supply
IF1	3	IF signal to resonant circuit
RES1	4	resonant circuit
FMON	5	FM-ON, standby switch
RES2	6	resonant circuit
IF2	7	IF signal to resonant circuit
$V_{o\ AF1}$	8	AF output voltage (0° phase)
$V_{o\ AF2}$	9	AF output voltage (180° phase)
n.c.	10	not connected
n.c.	11	not connected
$V_{i\ det}$	12	detune detector input for external audio reference
$V_{o\ det}$	13	detune detector output voltage
V_{ref}	14	reference voltage output
V_F	15	level output for field-strengh
$V_{F\ o}$	16	zero adjust for field-strengh
$V_{i\ IF}$	17	FM-IF input signal
IN2	18	input 2 of differential IF amplifier
IFLV	19	IF input level
GND	20	ground (0 V)

PIN CONFIGURATION

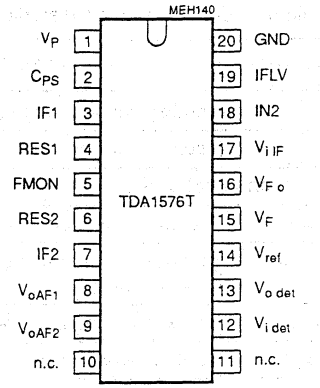


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	15	V
$V_{2, 5, 16}$	voltage on pins 2, 5 and 16	0	V_P	V
P_{tot}	total power dissipation	0	450	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	−30	+85	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air		85	K/W

CHARACTERISTICS

V_P = 8.5 V; $f_{i\,ZF}$ = 10.7 MHz; R_S = 60 Ω; f_m = 400 Hz with Δf = ±22.5 kHz; 50 μs de-emphasis (C8-9 = 6.8 nF); T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified. The demodulator circuit is adjusted at minimum second harmonic distortion for $V_{i\,ZF}$ = 1 mV and a deviation Δf = ±75 kHz.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		7.5	8.5	15	V
I_P	supply current	$V_5 = V_9 = V_{13} = 0$	10	16	23	mA
Reference voltage						
V_{ref}	reference voltage (pin 14)	I_{14} = −1 mA	-	4.9	-	V
ΔV_{ref}	reference voltage dependence on temperature	$\Delta V_{14} / V_{14} * \Delta T$	-	0.3	-	%/K
I_{14}	maximum output current	short-circuit current	4	6	7.5	mA
R_{14}	output resistor ($\Delta V_{14} / \Delta I_{14}$)	I_{14} < 1.2 mA	-	60	150	Ω
IF amplifier						
$V_{i\,IF}$	input sensivity (RMS value, pin 17)	−3 dB before limiting	14	22	35	μV
R_{17-18}	input resistance	$V_{i\,IF}$ = 200 mV (RMS)	10	-	-	kΩ
C_{17-18}	input capacitance	$V_{i\,IF}$ = 200 mV (RMS)	-	5	-	pF
$V_{o\,IF}$	output signal at pins 3 and 7 (peak-to-peak value)	$Z_{3,7}$ = 10 pF // 1MΩ	610	680	750	mV
R_{3-7}	output impedance		200	250	300	Ω
Demodulator						
R_{4-6}	input resistance		20	30	40	kΩ
C_{4-6}	input capacitance		-	1	2.5	pF
$R_{8,9}$	output impedance		2.9	3.7	4.5	kΩ
$V_{8,9}$	DC offset voltage on output pins at V_{4-6} = 0	V_5 > 3 V or V_{3-7} = 0 or V_{13} < 0.3 V	-	0	±100	mV
$\Delta V/\Delta\varphi$	demodulator efficiency	$\Delta V_{8-9}/\Delta\varphi$	-	40	-	mV/°
	demodulator efficiency dependent on supply voltage (note 1)	K	-	6.2	-	mV/°
V/V	DC voltage ratio	$V_{8+}V_9 / 2*V_2$	0.653	0.667	0.680	V/V
$\Delta V/\Delta T$	dependence on temperature	$\Delta(V_8+V_9 / 2*V_2)/\Delta T$	-	10^{-5}	-	1/K
Field-strengh output						
V_{15}	output voltage (Fig.4)	$V_{i\,IF}$ = 0	0	0.1	0.25	V
		$V_{i\,IF}$ = 1 mV (RMS)	1.1	1.5	1.9	V
		$V_{i\,IF}$ = 250 mV (RMS)	3.2	3.6	4.1	V
S	control steepness	Fig.4	-	0.85	-	V/dec
R_{15}	output resistance		-	150	200	Ω
$\Delta V/\Delta T$	dependence on temperature	$V_{i\,IF} = \Delta V_{15} / (\Delta T * V_{15})$	-	0.3	-	%/K
I_{15}	stand-by operational cut-off current	$V_5 \geq 3$ V; V_{15} = 0 to 5 V	-	-	10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero level adjustment						
V_{16}	internal bias voltage		-	260	-	mV
R_{16}	input resistance		-	19	-	kΩ
S	control steepness	$V_{i\ IF}$ = 100 mV; $A = \Delta V_{15} / \Delta V_{16}$	0.87	1.0	1.2	V/V
Detuning detector						
I_{12}	input bias current		-	20	100	nA
R_{12}	input resistance (Fig.5)	5 V/ΔI_{12}	6	30	-	MΩ
V_{13}/V_{14}	output voltage ratio for $\Delta\varphi = \varphi$ (pins 3-7) – φ (pins 4-6) –90°; (Fig.6)	$V_1 = V_2$ = 7.5 V; $R_{13\text{-}14}$ = 10 kΩ; pins 9 and 12 short-circuit				
	$\Delta\varphi$ = 9.2° (43 kHz), Q = 20	$V_{9,\ 12}$ = 334 mV	0.45	0.5	0.55	V/V
	$\Delta\varphi$ = 3.5° (16 kHz), Q = 20	$V_{9,\ 12}$ = 138 mV	0.75	0.8	0.85	V/V
	$\Delta\varphi$ = 14° (65 kHz), Q = 20	$V_{9,\ 12}$ = 501 mV	0.335	0.345	0.355	V/V
I_{13}	maximum output current (Fig.7)	V_{13} = 6 V	0.4	0.5	0.6	mA
	cut-off current	V_{13} = 2.5 V; $V_{9,\ 12}$ = 0	-	-	–100	nA
Internal audio attenuation						
V_{13}/V_{14}	output voltage ratio (Fig.8)	α = attenuation factor				
	for α = 1 dB		0.11	0.12	0.13	
	for α = 7.2 dB		0.095	0.1	0.105	
	for $\alpha \geq$ 40 dB		-	0.06	-	
I_{13}	input current	$V_{13} / V_{13} \leq 0.1$	-	-	–225	nA
Stand-by switch						
V_5	input voltage for FM-on	$V_{3,\ 7} / V_{3,\ 7(max)}$ = 0.9	2.4	2.5	-	V
	input voltage for FM-off	V_{19} = 0.3 V	-	2.9	3	V
	linear range (Fig 9)		-	350	-	mV
I_5	input current	V_5 = 0 to 2 V	-	-	–100	µA
		V_5 = 3.5 to 15 V	-	-	1	µA
$V_5/\Delta T$	temperature dependence	FM-on ($3.5V_{BE}$)	-	7	-	mV/K
		FM-off ($5V_{BE}$)	-	10	-	mV/K
Supply voltage smoothing						
$V_{1\text{-}2}$	internal voltage drop	proportional to $V_1 - 3V_{BE}$	80	210	400	mV
$R_{1\text{-}2}$	internal resistor		5.8	8.3	10.8	kΩ

OPERATING CHARACTERISTICS

V_P = 8.5 V; $f_{i\,ZF}$ = 10.7 MHz; R_S = 60 Ω; f_m = 400 Hz with Δf = ±22.5 kHz; 50 μs de-emphasis (C_{8-9} = 6.8 nF); T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified. The demodulator circuit is adjusted at minimum second harmonic distortion with $V_{i\,ZF}$ = 1 mV.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator						
$V_{i\,IF}$	input sensivity (RMS value, pin 17)	−3 dB before AF limiting	14	22	35	μV
	input signal for S/N = 26 dB	f = 250 to 15000 Hz	-	10	-	μV
	input signal for S/N = 46 dB	f = 250 to 15000 Hz	-	55	-	μV
$V_{o\,AF}$	output signal at (RMS value, pins 8 and 9)		60	67	75	mV
$V_{o\,N}$	noise voltage for $V_{i\,IF}$ = 0 (RMS value, pins 8 and 9)	R_S = 300 Ω f = 250 to 15000 Hz	-	900	-	μV
	weighted noise voltage according to	DIN 45405	-	2	-	mV
S/N	signal-to-noise ratio Fig.3 (pin 8 and 9)	$V_{i\,IF}$ = 1 mV (RMS)	-	72	-	dB
α_{AM}	AM suppression	$V_{i\,IF}$ = 0.5 to 200 mV FM: 70 Hz, ±15 kHz AM: 1 kHz, m = 30%	-	50	-	dB
α_{FM}	FM rejection for FM-off	$V_{i\,IF}$ = 500 mV; V_5 = 3V	80	-	-	dB
$\Delta V_{8,9}$	AFC shift in relation to minimum second harmonic distortion α_{2H}	$V_{i\,IF}$ = 0.03 to 500 mV	-	25	-	mV
	DC offset at second harmonic distortion	operating	-	0	±100	mV
		mute or FM-off	-	0	±50	mV
α_{3H}	distortion for third harmonic		-	0.65	-	%
RR	ripple rejection V_{ripple} = 200 mV on V_P	f = 100 Hz	43	48	-	dB

Note to the characteristics

1. $V_{8-9} / \Delta\varphi = K(V_P - 3\,V_{BE})$

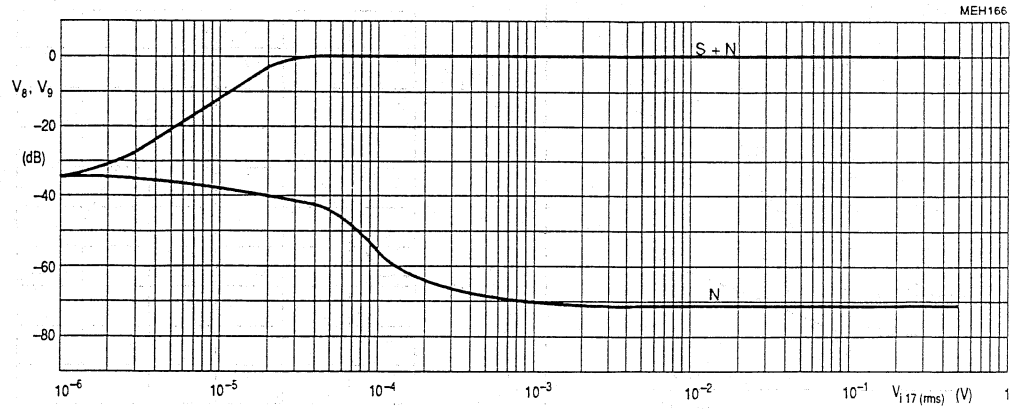


Fig.3 AF output voltage level on pins 8 and 9 as a function of $V_{i\,IF}$ at V_P = 8.5 V; f_m = 1 kHz; Q_L = 20 and with de-emphasis. S = signal; N = noise.

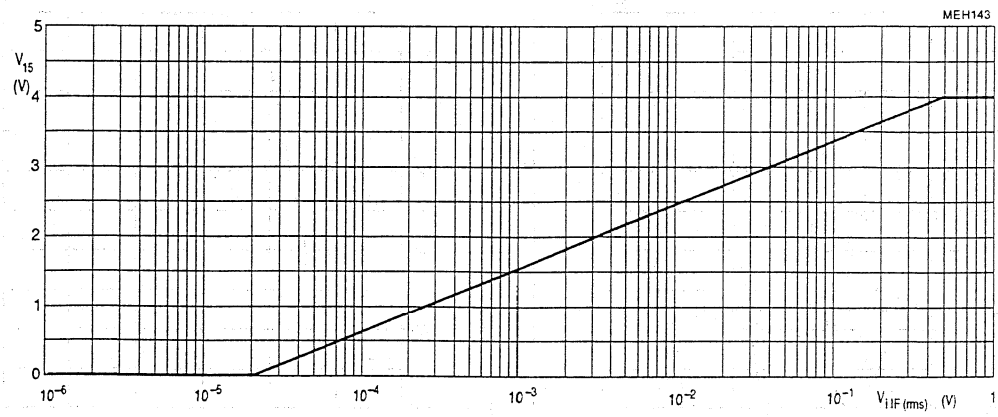


Fig.4 Field-strengh output (I_{16} = 0)

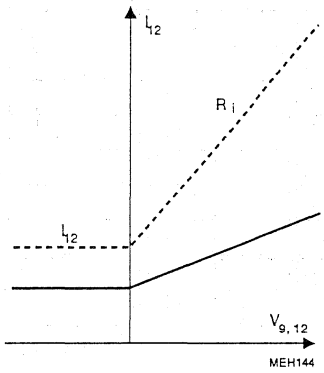


Fig.5 Detuning input impedance.

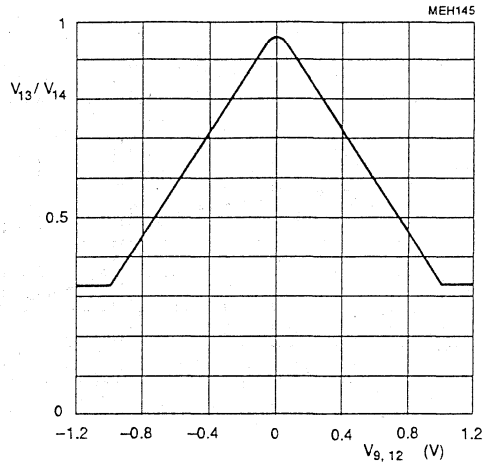


Fig.6 Detuning curve.

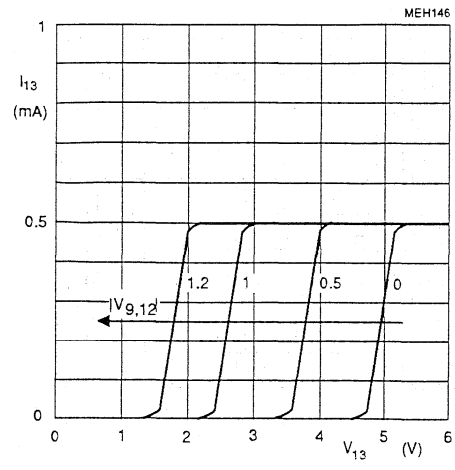


Fig.7 Detuning output.

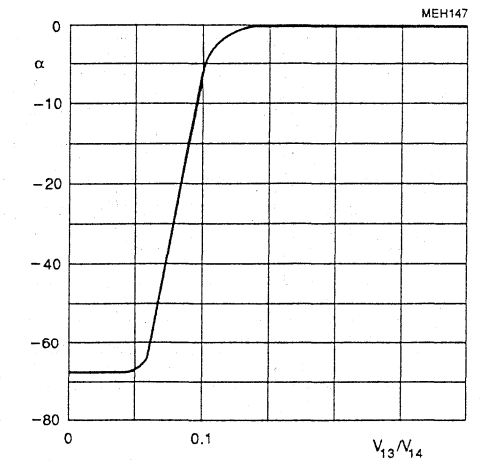


Fig.8 Internal audio attenuation.

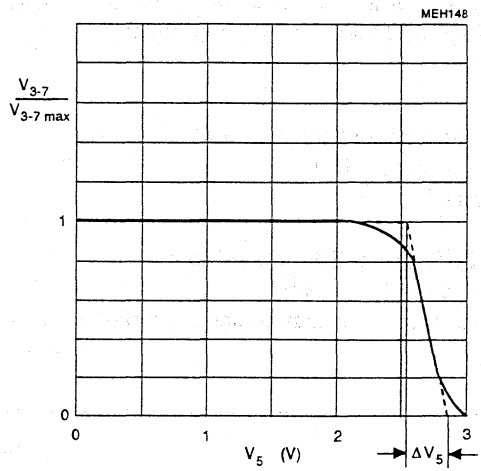


Fig.9 Stand-by switch.

Low voltage mono/stereo power amplifier TDA7050

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use — mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

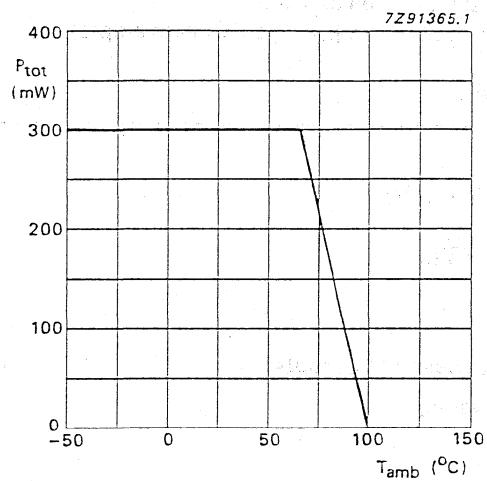


Fig. 1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient R_{thj-a} = 110 K/W

Low voltage mono/stereo power amplifier TDA7050T

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use — mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

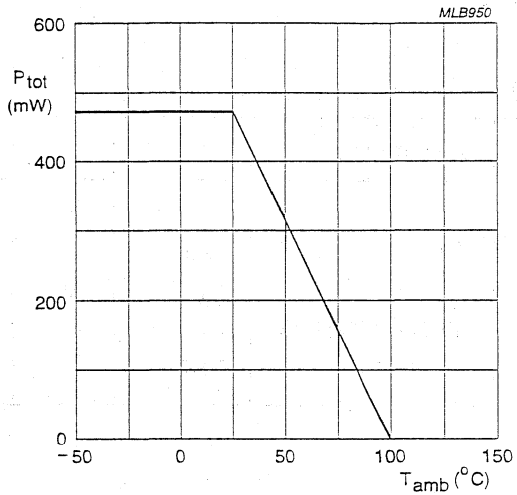


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\ max} - T_{amb}}{R_{th\ j\text{-}a}} = \frac{100-60}{160} = 0.25\ W$$

1 W BTL mono audio amplifier TDA7052

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	18	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

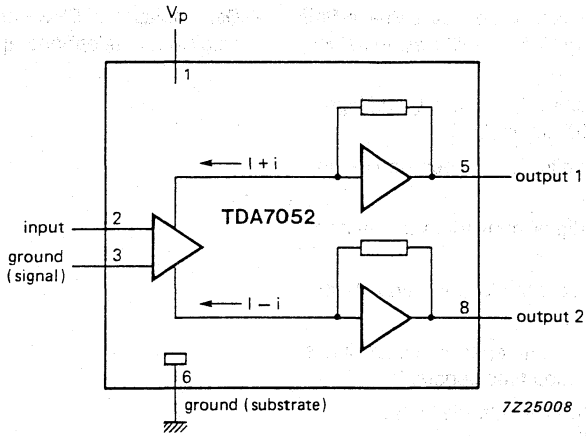


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

Quadrature demodulator controller TDA8041H

FEATURES

- Generates all control signals for Quadrature Phase-Shift Keying (QPSK) and Binary Phase-Shift Keying (BPSK) demodulation
- Can be used in applications with low E_b/N_o and high symbol rate (up to 30×10^6 symbols/s)
- Digital I and Q outputs (3 bits) for soft decision within error correction
- Two matched analog-to-digital converters to quantize the I and Q signals
- A digital detector for each control loop to generate the required control signals
- Digital-to-analog converters and operational amplifiers to allow high flexibility for loop time constants
- Special input stage to interface with the voltage controlled crystal oscillator
- Positive 5 V supply voltage.

APPLICATIONS

- Demodulation of BPSK and QPSK modulated signals in satellite and telephone applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DD(A)}$	supply voltage for operational amplifiers (pin 5)		4.75	5.0	5.25	V
$V_{DDA(C)}$	analog supply voltage for converters (pin 20)		4.75	5.0	5.25	V
$V_{DD(I/O)}$	supply voltage for digital inputs/outputs (pin 30)		4.75	5.0	5.25	V
V_{DDD}	supply voltage for digital section (pin 35)		4.75	5.0	5.25	V
$V_{DD(C)}$	supply voltage for digital part of ADC and DAC (pin 42)		4.75	5.0	5.25	V
$I_{DD(tot)}$	total supply current	$V_{DD} = 5$ V	–	30	–	mA
V_{IQ}	I and Q input voltage		–	1.0	–	V
R_{sym}	symbol rate		–	–	30×10^6	symbols/s
$I_{O(DAC)}$	DAC output current		−100	–	+100	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8041H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm; high stand-off height	SOT307-1

Note

1. When using reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

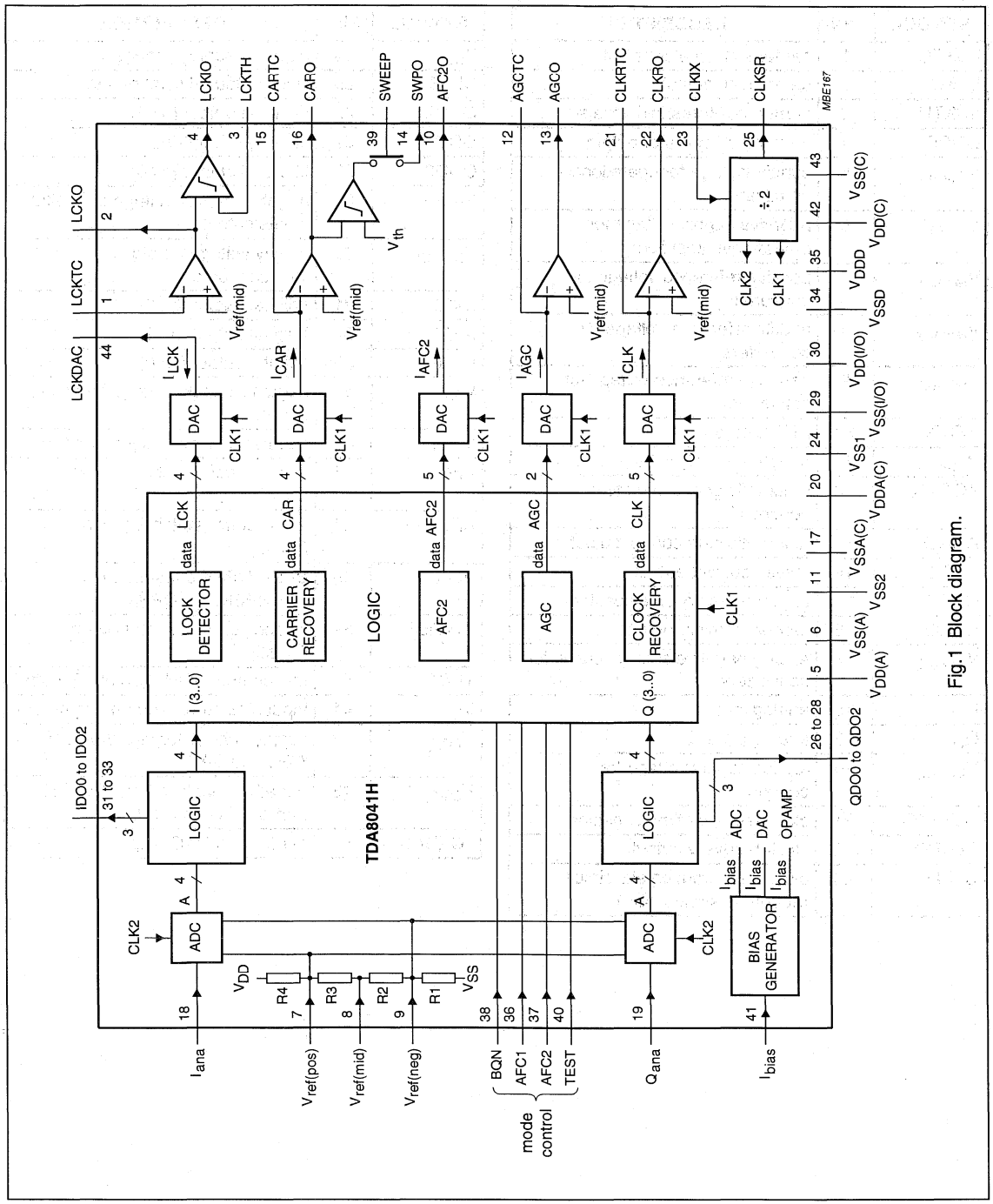


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LCKTC	1	carrier lock time constant
LCKO	2	carrier lock output
LCKTH	3	carrier lock threshold voltage
LCKIO	4	carrier lock indicator output
$V_{DD(A)}$	5	supply voltage for operational amplifiers
$V_{SS(A)}$	6	negative supply voltage for operational amplifiers
$V_{ref(pos)}$	7	positive reference voltage for converters
$V_{ref(mid)}$	8	middle reference voltage for converters
$V_{ref(neg)}$	9	negative reference voltage for converters
AFC2O	10	AFC 2 output
V_{SS2}	11	negative supply voltage 2
AGCTC	12	automatic gain control time constant
AGCO	13	automatic gain control output
SWPO	14	sweep current output
CARTC	15	carrier recovery time constant
CARO	16	carrier recovery output
$V_{SSA(C)}$	17	analog negative supply voltage for converters
I_{ana}	18	analog input I
Q_{ana}	19	analog input Q
$V_{DDA(C)}$	20	analog supply voltage for converters
CLKRTC	21	clock recovery time constant
CLKRO	22	clock recovery output
CLKIX	23	clock input from crystal circuit (at double symbol rate)

SYMBOL	PIN	DESCRIPTION
V_{SS1}	24	negative supply voltage 1
CLKSR	25	clock output at symbol rate
QDO2	26	Q digital output (bit 2)
QDO1	27	Q digital output (bit 1)
QDO0	28	Q digital output (bit 0)
$V_{SS(I/O)}$	29	negative supply voltage for digital inputs/outputs
$V_{DD(I/O)}$	30	supply voltage for digital inputs/outputs
IDO2	31	I digital output (bit 2)
IDO1	32	I digital output (bit 1)
IDO0	33	I digital output (bit 0)
V_{SSD}	34	negative supply voltage for digital section
V_{DDD}	35	supply voltage for digital section
AFC1	36	AFC control switch 1 (1 = on; 0 = off)
AFC2	37	AFC control switch 2 (1 = on; 0 = off)
BQN	38	BPSK/QPSK control switch (1 = BPSK; 0 = QPSK)
SWEEP	39	sweep control switch (1 = on; 0 = off)
TEST	40	test control switch (1 = on; 0 = off)
I_{bias}	41	input bias current for analog blocks
$V_{DD(C)}$	42	supply voltage for digital part of ADC and DAC
$V_{SS(C)}$	43	negative supply voltage for digital part of ADC and DAC
LCKDAC	44	carrier lock DAC output

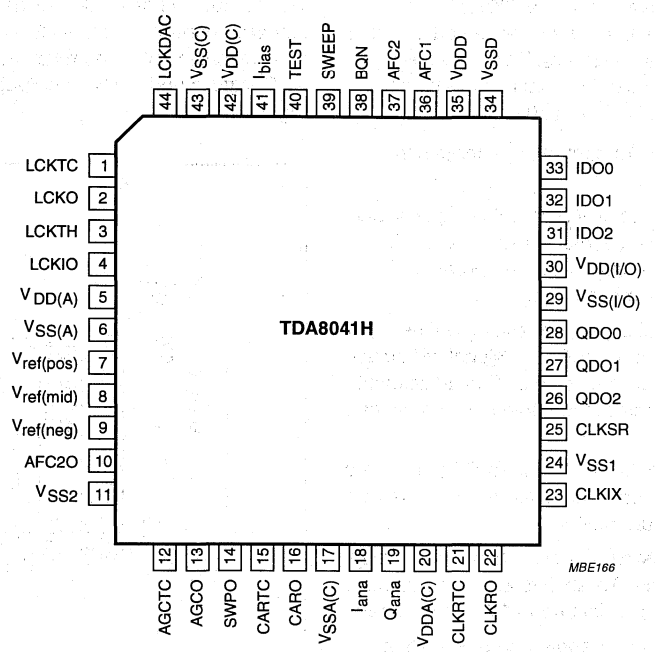


Fig.2 Pin configuration.

GENERAL DESCRIPTION

The quadrature demodulator controller TDA8041H, generates all control signals required for demodulation of BPSK and QPSK modulated signals. This device is specially designed to be used in conjunction with the quadrature demodulator IC, TDA8040T.

The quadrature demodulator controller generates the following signals:

- Symbol clock recovery control signal; this signal locks the VCXO to the received symbol clock. The clock recovery algorithm used in this device operates independently from the other loops.
- Carrier recovery control signal; depending on the selected mode (BPSK or QPSK), this signal will adjust the phase of the I and Q input signal. This adjustment will be such that the constellation points are as defined in Fig.4.
- Frequency control signals (AFC1 and AFC2); to serve a broad range of applications, two different AFC detectors and a sweep function are built-in:
  - AFC1: this is a robust detector which forces the offset frequency in the I and Q branch to zero. This detector can handle frequency offset up to 1/8 × symbol rate.
  - AFC2: this detector can handle frequency offsets greater than 1/8 × symbol frequency. However this AFC algorithm will bring the offset frequency only close to zero.
  - Sweep: this signal generates a triangular current output which can tune a VCO over its complete frequency range. Sweeping must be switched off as soon as the logical output of the lock detect function becomes positive. The value of the sweep current is set by an external resistor.
- Amplitude control signals (AGC); this signal adjusts a variable gain amplifier so that the amplitude of the I and Q signals is in accordance with the specified constellation points of Fig.4.
- Lock detect signal; this signal is related to the E_b/N_o of the incoming I and Q signals. This lock detect signal can be used for two purposes:
  - Lock detection by comparing the lock detect signal with an external set reference voltage, one can obtain a logical signal indicating lock detect.
  - The relationship between E_b/N_o can be used to display the E_b/N_o for antenna adjustment.

FUNCTIONAL DESCRIPTION

The TDA8041H has a 3-bit-wide digital I and Q output for soft error correction. These 3-bit outputs represent the main symbols only. The relationship between the 4-bits ADC signals and the 3-bit output signals is illustrated in Fig.3.

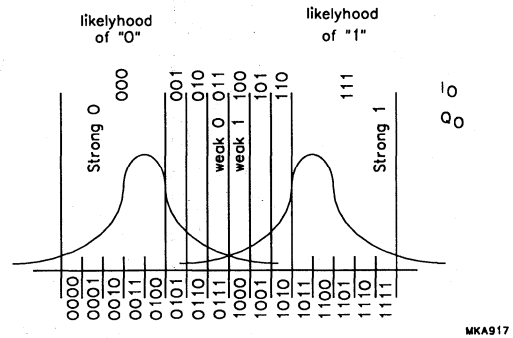


Fig.3 I and Q output levels for soft error decision FEC.

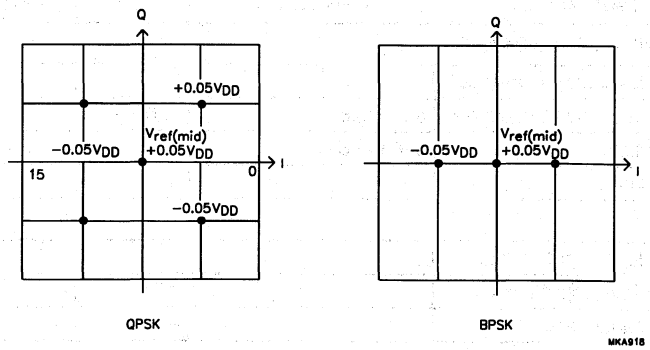


Fig.4 Constellation points.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD(A)}$	supply voltage for operational amplifiers (pin 5)		−0.5	+6.5	V
$V_{DDA(C)}$	analog supply voltage for converters (pin 20)		−0.5	+6.5	V
$V_{DD(I/O)}$	supply voltage for digital inputs/outputs (pin 30)		−0.5	+6.5	V
V_{DDD}	supply voltage for digital section (pin 35)		−0.5	+6.5	V
$V_{DD(C)}$	supply voltage for digital part of ADC and DAC (pin 42)		−0.5	+6.5	V
$V_{n(max)}$	maximum voltage on all pins		0	V_{DD}	V
P_{tot}	total power dissipation	T_{amb} = 70 °C	–	500	mW
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		–	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

V_{DD} = 4.75 to 5.25 V; $R_{sym} = 30 \times 10^6$ symbols/s; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs (pins 26 to 28 and 31 to 33)						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DD}$	V
V_{OH}	HIGH level output voltage	see Fig.6	$0.9V_{DD}$	–	V_{DD}	V
t_d	delay time	see Fig.6	t_h	–	22	ns
t_h	hold time		8	–	t_d	ns
Digital inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
C_I	input capacitance		–	–	10	pF
Clock output (pins 22 and 25); see Fig.5						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DD}$	V
V_{OH}	HIGH level output voltage		$0.9V_{DD}$	–	V_{DD}	V
T_{cy}	cycle time		33	–	–	ns
t_W	pulse width	duty cycle 40/60	13.2	–	–	ns
t_r	rise time	C_L = 30 pF	–	–	6	ns
t_f	fall time	C_L = 30 pF	–	–	6	ns
Clock input (pin 23)						
R_{source}	source resistance		–	–	50	Ω
f_s	sampling frequency		–	–	60	MHz
Analog inputs (pins 18 and 19)						
R_{sym}	symbol rate		–	–	30×10^6	symbols/s
$V_{ref(pos)}$	positive reference voltage	I_O = 0	–	$0.48V_{DD}$	–	V
$V_{ref(mid)}$	middle reference voltage	I_O = 0	–	$0.38V_{DD}$	–	V
$V_{ref(neg)}$	negative reference voltage	I_O = 0	–	$0.28V_{DD}$	–	V
I_L	load current at pin 8	note 1	–5	–	+5	mA
$V_{i(I,Q)}$	I and Q input voltage		0	–	V_{DD}	V
$V_{I,Q(op)}$	I and Q operating voltage		$0.28V_{DD}$	–	$0.48V_{DD}$	V
R_I	input resistance		50	–	–	kΩ
C_I	input capacitance		–	–	20	pF
I_{bias}	input bias current	R_L = 100 kΩ	–	–37	–	mA
DAC outputs (pins 10, 12, 15 and 21)						
$I_{o(av)}$	average output current	$V_{DAC} = V_{ref(mid)}$; note 2	–	100	–	mA
D_{Io}	matching of positive and negative output currents	$V_{DAC} = V_{ref(mid)}$; note 2	–7	–	+7	%
I_o	zero output current		–25	–	+25	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sweep current (pin 14)						
V_{OH}	HIGH level output voltage		–	$2V_{ref(mid)}$	–	V
V_{OL}	LOW level output voltage		–	0	–	V
Z_O	output impedance	SWEEP = 1	–	2	–	kΩ
		SWEEP = 0	10	–	–	MΩ
$V_{CARO(min)}$	LOW switching level		$0.1V_{DD}$	–	$0.2V_{DD}$	V
$V_{CARO(max)}$	HIGH switching level		$0.8V_{DD}$	–	$0.9V_{DD}$	V
Loop amplifiers						
V_o	output voltage		$0.1V_{DD}$	–	$0.9V_{DD}$	V
G_v	open loop gain		–.	60	–	dB
G_B	gain bandwidth		–	1	–	MHz
R_L	load resistance		5	–	–	kΩ

Notes

1. $V_{ref(mid)}$ is usually open-circuit. However, this pin may also be used as a reference output for an external buffer.

2. $I_{o(av)} = \frac{(I_{pos} - I_{neg})}{2}$; $D_{Io} = 100 \times \frac{(I_{pos} + I_{neg})}{(I_{pos} - I_{neg})}$

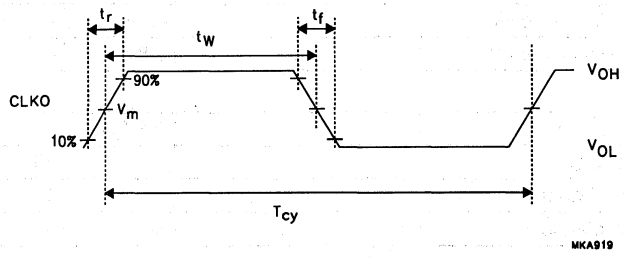


Fig.5 Timing of CLKO.

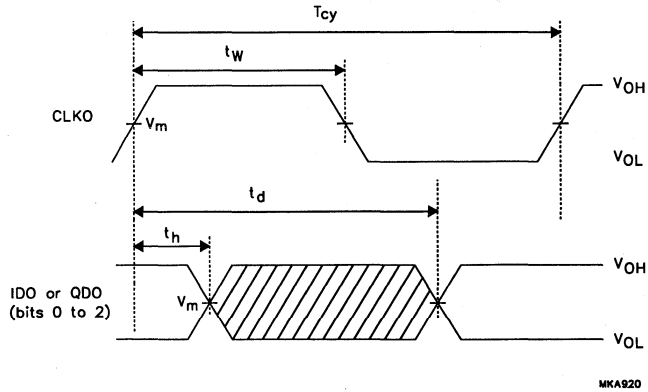


Fig.6 Timing definition of digital outputs.

APPLICATION INFORMATION

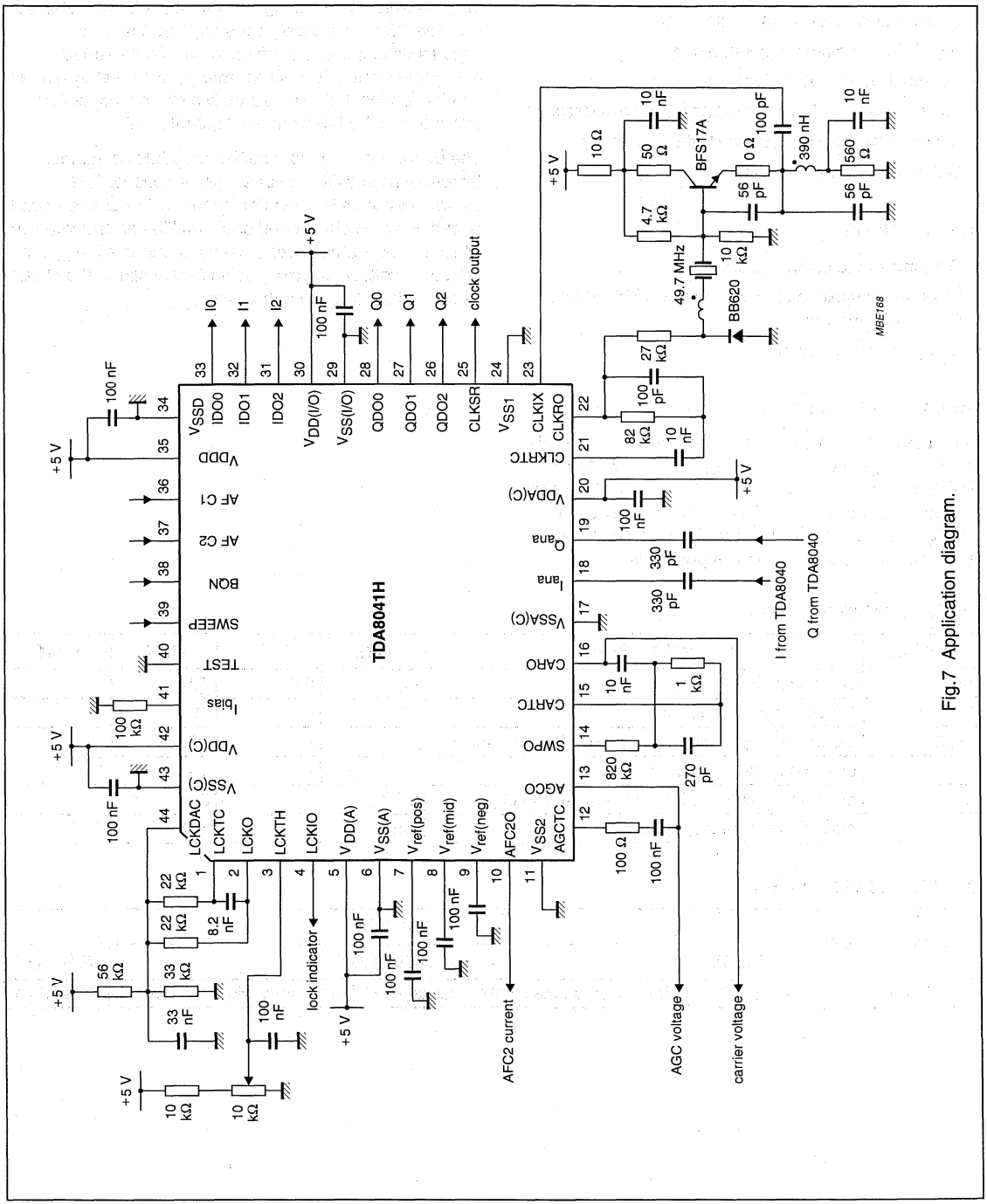


Fig.7 Application diagram.

True logarithmic amplifier TDA8780M

FEATURES

- 72 dB true logarithmic dynamic range
- Small-signal gain-adjustment facility
- Constant limiting output voltage
- Temperature and DC power supply voltage independent
- Easy interfacing to analog-to-digital converters
- Output DC level shift facility.

APPLICATIONS

- Dynamic range compression
- IF signal dynamic range reduction in GSM900 and DCS1800 receivers
- Compression receivers.

GENERAL DESCRIPTION

The TDA8780M is a true logarithmic amplifier intended for dynamic range reduction of IF signals at 10.7 MHz in GSM900 and DCS1800 receivers. It offers true logarithmic characteristics over a 72 dB input dynamic range, has a small-signal gain-adjustment facility and a constant limiting output voltage for large input levels.

The device is manufactured in an advanced BiCMOS process which enables high performance being obtained with low DC power supply consumption. The true logarithmic amplifier can be driven by single-ended or differential inputs. The DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors, which define the low-frequency cut-off point.

The performance of the amplifier is stabilized against temperature and DC power supply variations. The differential output is converted internally to a single-ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. A power-down facility allows the circuit to be disabled from a control input.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	DC power supply voltage	4.5	5.0	5.5	V
I_P	DC power supply current	–	–	10	mA
$I_{P(PD)}$	DC power supply current in power-down mode	–	–	250	µA
f_i	operating input frequency	–	–	15	MHz
$V_{i(M)}$	dynamic logarithmic input voltage (peak value)	0.06	–	300	mV
T_{amb}	operating ambient temperature	–20	–	+75	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8780M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

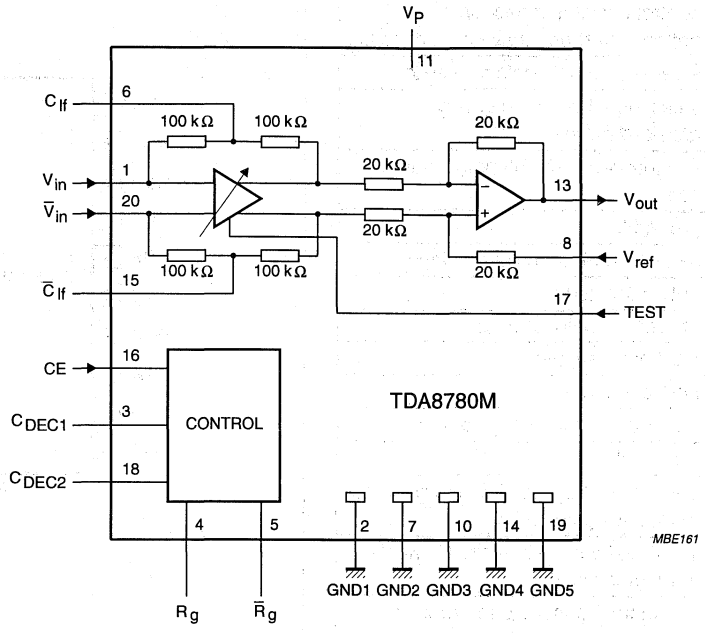


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{in}	1	signal voltage input
GND1	2	ground 1
C_{DEC1}	3	control circuit first decoupling and optional start-up capacitor connection
R_g	4	small-signal gain-setting resistor
$\overline{R}_g$	5	small-signal complementary gain-setting resistor
C_{lf}	6	low-frequency cut-off point setting capacitor
GND2	7	ground 2
V_{ref}	8	external reference voltage input
n.c.	9	not connected
GND3	10	ground 3 (main ground)
V_P	11	DC power supply
n.c.	12	not connected
V_{out}	13	true logarithmic voltage output
GND4	14	ground 4
$\overline{C}_{lf}$	15	complementary low-frequency cut-off point setting capacitor
CE	16	TTL-level-compatible circuit enable input (active HIGH)
TEST	17	test input; connected to ground in normal operation
C_{DEC2}	18	control circuit second decoupling and optional start-up capacitor
GND5	19	ground 5
$\overline{V}_{in}$	20	complementary signal voltage input

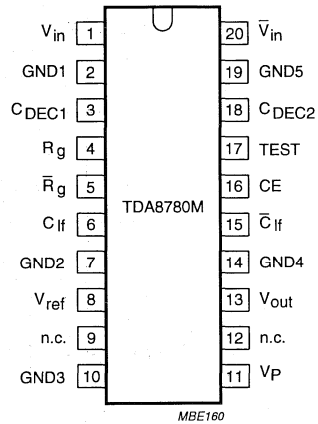


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

A true logarithmic amplifier can be realized from a cascade of similar stages each stage consisting of a pair of amplifiers whose inputs and outputs are connected in parallel. One of these amplifiers can be formed by an undegenerated long-tailed pair which provides high gain but limited linear input signal-handling capability. The other amplifier can be formed by a degenerated long-tailed pair which provides a gain of unity and a much larger linear input signal-handling capability.

The overall cascade amplifies very small input signals but, once these reach the level at which the undegenerated long-tailed pair in the last stage is at the limit of its linear signal-handling capability, the output voltage becomes logarithmically dependent on the input signal level. This behaviour continues until the input signal reaches the level at which undegenerated long-tailed pair in the first stage is at the limit of its linear input signal-handling capability. The transfer characteristic beyond this point then depends on the exact configuration of the degenerated long-tailed pair in the first stage.

Five stages are used in the TDA8780M to provide a 72 dB true logarithmic dynamic range. The DC bias current in the undegenerated long-tailed pair in the first stage is made externally adjustable, using an off-chip resistor, to provide a small-signal gain adjustment facility. A high-level limiter is inserted between the first and second stages to provide a constant limiting output voltage which is essentially independent of the value of the gain setting resistor. These stages can be driven by single-ended or differential inputs. The DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance is stabilized against temperature and DC power supply variations. The input to the true logarithmic amplifier is protected against damage due to excessive differential input signals by diodes.

The differential output from the true logarithmic amplifier is converted internally to a single-ended output by an on-chip operational amplifier arrangement in the which the DC output level is set by an externally-supplied reference voltage. The output is capable of driving loads down to 10 kΩ. The limiting output voltage and the output drive capability have been chosen to facilitate interfacing to analog-to-digital converters. A major part of the DC power supply current consumption of the device is associated with provision of this output drive capability. The DC power supply consumption is significantly less when the device is driving smaller loads.

A power-down facility allows the circuit to be disabled from a TTL-level compatible control input.

True logarithmic amplifier TDA8781T

FEATURES

- 55 dB true logarithmic dynamic range
- Small-signal gain-adjust facility
- Constant limiting output voltage
- Temperature and DC power supply voltage compensation
- Easy interfacing to TDA8703 analog-to-digital converter
- Output DC level shift facility
- Additional received signal-strength indication (RSSI) output.

APPLICATIONS

- Dynamic range compression
- IF signal dynamic range reduction in GSM900 and DCS1800 receivers
- Compressive receivers.

GENERAL DESCRIPTION

The TDA8781T is a true logarithmic amplifier intended for dynamic range reduction of IF signals at 10.7 MHz in GSM900 and DCS1800 receivers. It offers true logarithmic characteristics over a 55 dB input dynamic range and has a small-signal gain-adjust facility and a constant limiting output voltage for large input levels. It is manufactured in an advanced BICMOS process which enables high performance to be obtained with low DC power supply consumption. The true logarithmic amplifier can be driven by single-ended or differential inputs and the DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance of the true logarithmic amplifier is stabilized against temperature and DC power supply voltage variations. The differential output is converted internally to a single-ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. An additional received signal-strength indication (RSSI) output is available and a power-down facility allows the circuit to be disabled from a TTL-level compatible control input.

The device can be used to compress IF signals prior to being digitized in digital radio systems. It allows the usage of low-cost, low-power 8-bit DACs instead of the 10 or 12-bit types. In GSM systems decompression is performed by the digital signal processor such as the PCD5080. The TDA8781T interfaces directly with the ADC which is integrated on the Base Band Interface PCD5070.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC power supply voltage	4.5	5.0	5.5	V
I_{CC}	DC power supply current	–	–	10	mA
I_{OFF}	I_{CC} in power-down mode	–	250	400	µA
f_i	operating input frequency	0.1	10.7	15.0	MHz
T_{amb}	operating ambient temperature	−20	–	+75	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8781T	14	SO14	plastic	SOT108A

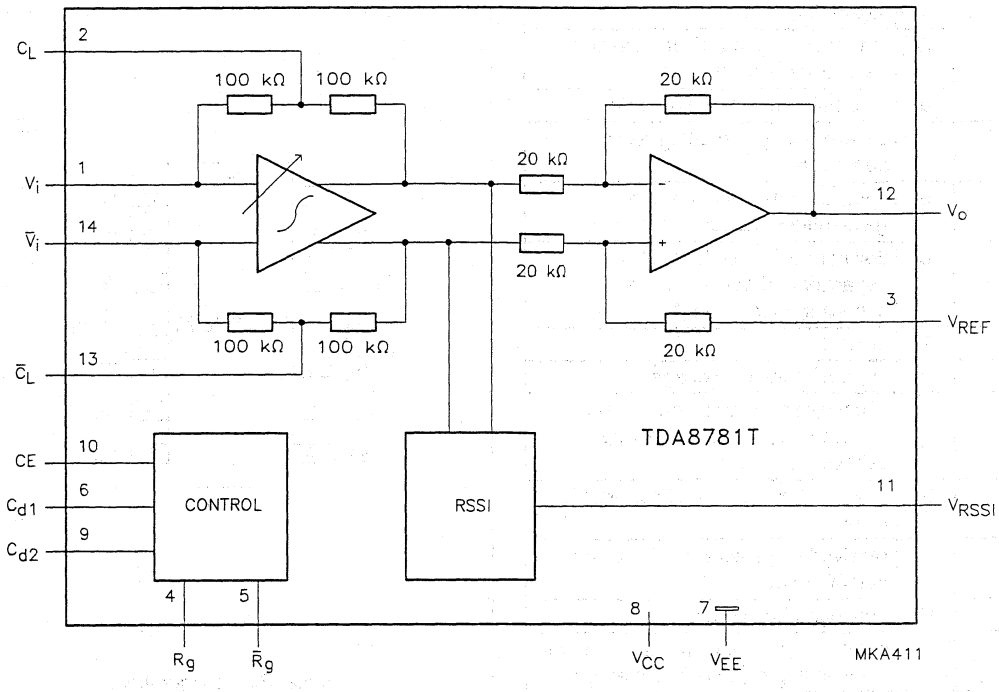


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_i	1	signal input
C_L	2	low-frequency cut-off point setting capacitor connection
V_{REF}	3	external reference voltage input
R_g	4	small-signal gain-setting resistor connection
$\overline{R}_g$	5	complementary small-signal gain-setting resistor connection
C_{d1}	6	first control circuit decoupling capacitor and optional start-up capacitor connection
V_{EE}	7	ground
V_{CC}	8	DC power supply voltage
C_{d2}	9	second control circuit decoupling capacitor and optional start-up capacitor connection
CE	10	TTL-level-compatible circuit enable input
V_{RSSI}	11	received signal-strength indication output (RSSI)
V_o	12	true logarithmic output
$\overline{C}_L$	13	complementary low-frequency cut-off point setting capacitor connection
$\overline{V}_i$	14	complementary signal input

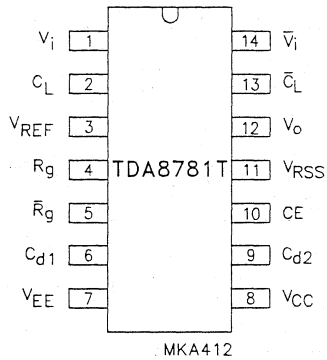


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

A true logarithmic amplifier can be realized from a cascade of similar stages each of which consists of a pair of amplifiers whose inputs and outputs are connected in parallel. One of these amplifiers can be formed by an undegenerated long-tailed pair which provides high gain but a limited linear input signal-handling capability. The other amplifier can be formed by a degenerated long-tailed pair which provides a gain of unity and a much larger linear input signal-handling capability. The overall cascade amplifies very small input signals linearly but, once these reach the level at which the undegenerated long-tailed pair in the last stage is at the limit of its linear input signal-handling capability, the output voltage becomes logarithmically dependent on the input signal level. This behavior continues until the input signal reaches the level at which the undegenerated long-tailed pair in the first stage is at the limit of its linear input signal-handling capability. The transfer characteristic beyond this point then depends on the exact configuration of the degenerated long-tailed pair in the first stage.

Three stages are used in the TDA8781T to provide a 55 dB true logarithmic dynamic range. The DC bias current in the undegenerated long-tailed pair in the first stage is made externally adjustable, by means of an off-chip resistor, to provide a small-signal gain-adjust facility. A high-level limiter is inserted between the first and second stages to provide a constant limiting output voltage which is essentially independent of the value of the gain-setting resistor. These stages can be driven by single-ended or differential inputs and the DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance of these stages is stabilized against temperature and DC power supply voltage variations. The input to the true logarithmic amplifier is protected against damage due to excessive differential input signals by diodes.

The differential output from the true logarithmic amplifier is converted internally to a single ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. The output is capable of driving loads down to 10 kΩ in parallel with 20 pF. The limiting output voltage and this output drive capability have been chosen to facilitate interfacing to a TDA8703 analog-to-digital converter. A major proportion of the DC power supply current consumption of the device is associated with provision of this output drive capability. The DC power supply consumption is significantly less when the device is driving less-highly capacitive loads.

An additional received signal-strength indication (RSSI) output is available from the true logarithmic amplifier. This output is protected against damage due to excessive current being drawn by means of a series resistor. A power-down facility allows the circuit to be disabled from a TTL-level-compatible control input.

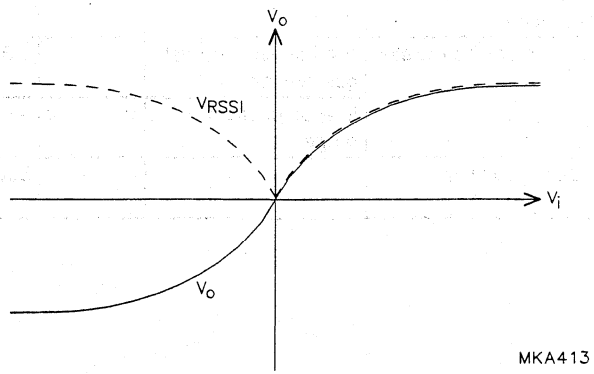


Fig.3 Transfer function.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC power supply voltage	−0.3	+5.5	V
V_I	DC voltage at all other pins with respect to ground	−0.3	V_{CC} + 0.3	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−20	+75	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

V_{CC} = 5.0 V; V_{REF} = 2.5 V; V_i at f_i = 10.7 MHz; T_{amb} = 25 °C; nominal small-signal gain setting resistor in use; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_{CC}	operating DC power supply voltage		4.5	5.0	5.5	V
I_{CC}	DC power supply current	V_{CC} = 5.5 V; V_i = 1 V (peak)	–	8	10	mA
I_{OFF}	DC power supply current in power-down mode	10 µs after V_{CE} changes from $V_{CE(ON)}$ to $V_{CE(OFF)}$	–	250	400	µA
Control: CE, R_g, $\overline{R}_g$, C_{d1}, C_{d2} (pins 10, 4, 5, 6 and 9)						
$V_{CE(ON)}$	circuit enable input voltage		2.0	–	V_{CC}	V
$V_{CE(OFF)}$	circuit enable input voltage in power-down mode		0	–	0.8	V
R_g	small-signal gain-setting resistor	nominal small-signal gain setting	–	3.3	–	kΩ
		total adjustment range	0	–	–	kΩ
C_{d1}, C_{d2}	control circuit decoupling capacitors		–	560	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs: V_I, V_{REF}, C_L, $\overline{C}_L$ (pins 1, 3, 2 and 13)						
f_i	operating input frequency		0.1	10.7	15	MHz
R_i	small-signal input resistance	differential input at f_i = 10.7 MHz; V_i = 10 mV (peak)	–	10	–	kΩ
C_i	input capacitance	differential input at f_i = 10.7 MHz	–	3	–	pF
$V_{i(min)}$	peak input voltage at start of true logarithmic characteristic		–	800	–	μV
$V_{i(max)}$	peak input at end of true logarithmic characteristic		–	450	–	mV
$V_{i(limit)}$	maximum peak input signal	input protection diodes not conducting	–	1	–	V
ΔV_i	spread in true logarithmic output amplitude transfer characteristic across true logarithmic range over whole temperature and DC power supply voltage range	input spread for fixed output	–	±2.5	–	dB
ΔG_v	small-signal gain-adjustment range		±6	–	–	dB
C_L, $\overline{C}_L$	low-frequency cut-off point setting capacitors	f = 100 kHz at 3 dB	–	560	–	pF
R_{REF}	external reference input resistance		–	40	–	kΩ
V_{REF}	external reference voltage		2.0	2.5	V_{CC} – 2.0	V
Outputs: V_o, V_{RSSI} (pins 12 and 13)						
$V_{o(min)}$	peak true logarithmic output voltage relative to V_{REF} at start of true logarithmic characteristic	V_i = 800 μV (peak)	–	90	–	mV
$V_{o(max)}$	peak true logarithmic output voltage relative to V_{REF} at end of true logarithmic characteristic	V_i = 450 mV (peak)	–	900	–	mV
V_o	true logarithmic peak output voltage across true logarithmic range	V_i = 1 mV (peak)	55	100	145	mV
		V_i = 10 mV (peak)	340	410	480	mV
		V_i = 100 mV (peak)	630	730	830	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(limit)}$	limiting peak output voltage	V_i = 1 V (peak)	800	950	1100	mV
$V_o - V_{REF}$	DC offset voltage	V_i = 0 V	−100	+35	+100	mV
ΔG_{vo}	change in small-signal true logarithmic gain referred to V_o at V_i = 10 mV (peak); R_g = 3.3 kΩ	V_i = 5 mV (peak); R_g = 0	0	–	+2	dB
		V_i = 20 mV (peak); R_g = ∞	−2	–	0	dB
ΔV_o	change in small-signal true logarithmic output voltage with frequency	V_i = 10 mV (peak); f_i = 100 kHz and 15 MHz referenced to 1 MHz	–	0.4	1.5	dB
$\Delta\phi$	spread in true logarithmic output phase transfer characteristic across true logarithmic range		–	15	–	deg
V_{RSSI}	RSSI output across true logarithmic range	V_i = 1 mV (peak)	1.85	2.0	2.15	V
		V_i = 10 mV (peak)	2.05	2.2	2.35	V
		V_i = 100 mV (peak)	2.25	2.4	2.55	V

APPLICATION INFORMATION

The circuit is connected as shown in the typical application circuit diagram (Fig.4). The single-ended 10.7 MHz input IF signal is applied (arbitrarily) to one of the two input pins via a ceramic filter. These inputs should not be DC coupled as this will disable the on-chip feedback which sets the DC operating point of the true logarithmic amplifier. The relatively high input impedance of these inputs facilitates correct termination of the ceramic filter by means of an off-chip resistor.

The low-frequency cut-off point is determined by the value of the capacitors which decouple the overall DC feedback as well as the value of the input coupling capacitors. The output is AC coupled to a TDA8703 analog-to-digital converter in order that the value of the voltage fed to the reference voltage input is not critical. It could be useful in other applications, where the output might be DC coupled to an alternative analog-to-digital converter, to derive this reference voltage from the centre of the input resistor chain of the analog-to-digital converter.

The additional RSSI output is required only in applications where this is not derived in subsequent digital signal processing stages. The capacitor connected to this output provides a simple peak-hold and averaging function. Excessively large values of capacitance may lead to distortion of the true logarithmic output.

It may be found advantageous to add two small capacitors to speed up the re-enabling of the circuit after it has been in power-down mode. These should be connected between the circuit enable input and the control circuit decoupling capacitors. The size of these capacitors will be related to the size of the control circuit decoupling capacitors which are required both for stability and to prevent degradation of the noise figure.

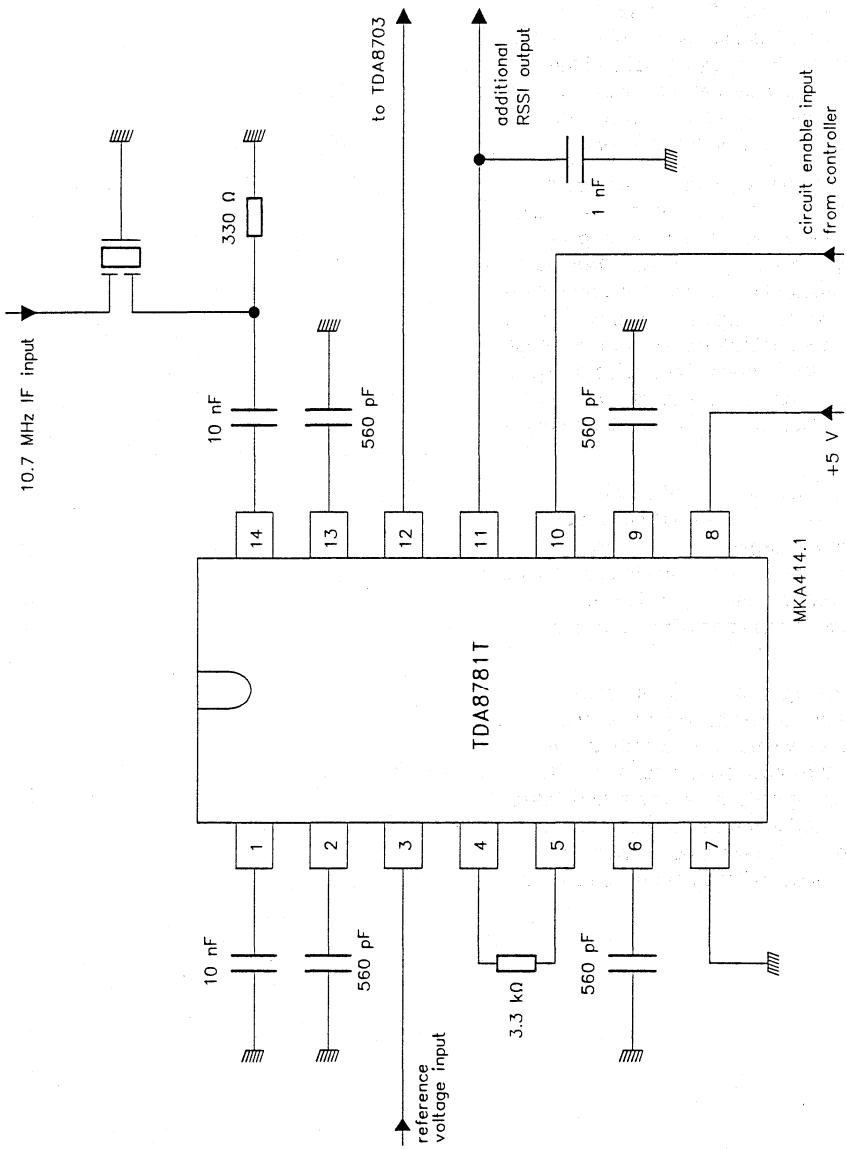


Fig.4 Typical application diagram.

Low power fequency synthesizer (LOPSY)

TDD1742T

GENERAL DESCRIPTION

The TDD1742T is a low power, high-performance frequency synthesizer in local oxidation CMOS (LOCMOS) technology. The device is designed for use in channelized VHF/UHF applications especially portable and mobile radios.

The circuit incorporates many of the features of the HEF4750V (frequency synthesizer) and HEF4751 (universal divider), including a high-gain phase comparator together with an on-chip sample-and-hold capacitor and phase modulator.

A multiplexed or bus-structured programming sequence allows interface to a microcontroller or external memory (ROM/PROM); power is applied to the memory only when it is required for programming via additional on-chip circuitry.

Operation is possible with a minimum supply voltage of 7 V and a maximum input frequency of 8,5 MHz.

Encapsulation in a 28-lead mini-pack enables the construction of small, low power consumption synthesizers with low noise performance and high side-band attenuation.

Features

- On-chip sample-and-hold capacitor
- Low power consumption
- High-gain phase comparator with low levels of noise and spurious outputs
- Auxiliary digital phase comparator for fast locking
- On-chip phase modulator
- Simple interfacing to external memory
- Microcontroller compatible
- Power-on reset circuitry

QUICK REFERENCE DATA

Supply voltage ranges			
pin 14	$V_{DD1} = V_{14-6}$	7 to 10	V
pin 8	$V_{DD2} = V_{8-6}$	4,5 to 5	V
pin 1	$V_{DD3} = V_{1-6}$	7 to 10	V
Supply current (at T_{amb} = 25 °C; $V_{DD1} = V_{DD3}$ = 7,4 V; V_{DD2} = 5 V)			
pin 14 (phase modulator OFF)	$I_{DD1} = I_{14}$	max. 1,5	mA
pin 8	$I_{DD2} = I_8$	max. 100	μA

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

Low power fequency synthesizer (LOPSY)

TDD1742T

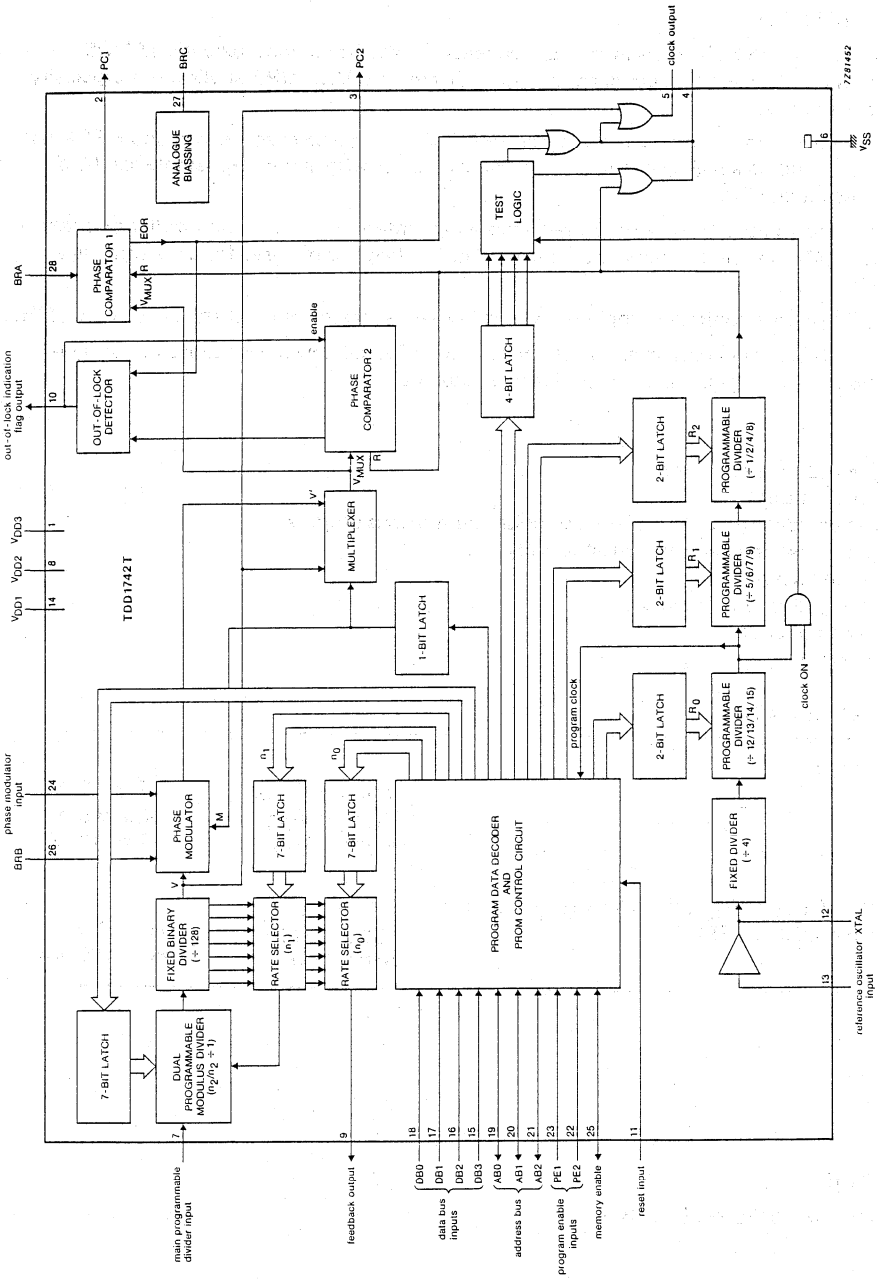


Fig. 1 Block diagram.

Low power fequency synthesizer (LOPSY) TDD1742T

PINNING

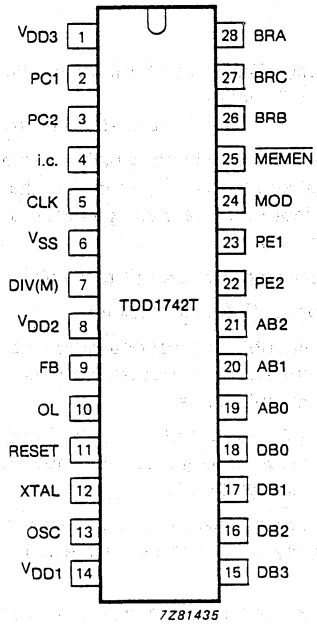


Fig. 2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	V_{DD3}	**Power Supply 3:** analogue supply voltage (7 to 10 V).
2	PC1	**Phase Comparator 1:** high-gain analogue phase comparator output which is used when the system is in-lock to give low levels of noise and spurious outputs.
3	PC2	**Phase Comparator 2:** low-gain digital phase comparator 3-state output which enables the achievement of fast lock times when the system is initially out-of-lock. Phase comparator 2 is inhibited when the phase is within the locking range of phase comparator 1.
4	i.c.	**internally connected** (must be left floating).
5	CLK	**Clock:** clock output.
6	V_{SS}	**Ground:** circuit earth potential.
7	DIV(M)	**Divider:** input to the main programmable divider (8,5 MHz max.), usually from prescaler.
8	V_{DD2}	**Power Supply 2:** supply voltage for TTL-compatible stages (+ 5 V ± 10%).
9	FB	**Feedback:** feedback output to control the modulus of the external prescaler.
10	OL	**Out-of-lock:** out-of-lock indication flag output. This output is HIGH when phase comparator 2 is in operation (when the system is out-of-lock).
11	RESET	**Power-on-Reset:** Following power up an initial pulse is applied to this input pin to set the internal counters.

Pin functions (continued)

pin no.	mnemonic	description
12	XTAL	**Crystal:** output to external crystal to form the oscillator circuit in combination with the OSC input. Alternatively this pin may be used as a buffer output.
13	OSC	**Oscillator:** input to reference oscillator which together with the XTAL output and an external crystal is used to generate the reference frequency. Alternatively to OSC input may be used as a buffer amplifier for an external reference oscillator.
14	V_{DD1}	**Power Supply 1:** digital supply voltage (7 to 10 V).
15-18	DB3-DB0	**Data Bus:** Data Bus inputs (TTL compatible).
19-21	AB0-AB2	**Address Bus:** TTL compatible bidirectional address bus. Provides address output to an external memory or input from microcontroller. The outputs are 3-state with internal pull-downs.
22	PE2	**Program Enable 2:** } TTL compatible inputs to initiate the programming cycle or strobe the internal data latches.
23	PE1	**Program Enable 1:** }
24	MOD	**Modulator:** high impedance linear phase modulator input, which applies a voltage controlled delay to the programmable divider output to the phase comparator.
25	$\overline{\text{MEMEN}}$	**Memory Enable:** mode control and memory enable bidirectional pin. If pin 25 is LOW at general reset the TDD1742T is set to the microcontroller mode; if pin 25 is HIGH at general reset the TDD1742T is set to the memory mode and the ROM/PROM is enabled.
26	BRB	**Bias Resistor B:** current mirror which acts as gain control for the phase modulator.
27	BRC	**Bias Resistor C:** current mirror pin which provides analogue biassing.
28	BRA	**Bias Resistor A:** current mirror pin which acts as gain control for phase comparator 1.

Low power fequency synthesizer (LOPSY) TDD1742T

FUNCTIONAL DESCRIPTION

Reference oscillator chain

The reference oscillator chain comprises a crystal oscillator and dividers to give the required frequency to drive the phase comparators.
The oscillator stage is a single inverter connected between pin 12 (XTAL) and pin 13 (OSC). Satisfactory operation is achieved with crystals up to 9 MHz. Alternatively, the OSC input may be used as a buffer amplifier for an external reference oscillator.
The reference divider chain comprises a fixed divide by 4-stage followed by three cascaded programmable dividers of ratios ÷ 12/13/14/15, ÷ 5/6/7/9 and ÷ 1/2/4/8. The output of the last stage is applied as one input (R) to the two phase comparators. Thus a number of division ratios between 240 and 4320 are possible which provides all the required VHF and UHF channel spacings with reference crystals in a 1 to 9 MHz range.

Main programmable divider

The main programmable divider is a rate feedback binary divider. As shown in figure 1 it comprises a fixed 7-bit binary divider (÷ 128) and two rate selectors (n_1 and n_0). One rate selector controls a 7-bit fully programmable dual modulus divider (÷ $n_2/n_2 + 1$) and the other controls the external dual modulus prescaler (÷ A/A + 1).

The overall division rate (N) is given by:

$$N = (128\, n_2 + n_1)\, A + n_0$$

Where:

$$0 \leqslant n_0 \leqslant 127$$
$$0 \leqslant n_1 \leqslant 127$$
$$1 \leqslant n_2 \leqslant 127.$$

The output from the programmable divider is fed to the phase comparators via the phase modulator and the multiplexer. The phase modulator is bypassed if not selected.

Phase comparison

The TDD1742T contains 2 phase comparators which act in close co-operation. Phase comparator 1 is the main comparator. It is designed to have a high-gain analogue output, 4500 volts/cycle at 10 kHz (typ.). This enables a low noise performance to be achieved. However, the output of phase comparator 1 will saturate at high or low levels for very small phase excursions.
Phase comparator 2 is an auxiliary comparator with a wide range, which enables faster lock times to be achieved than otherwise would be possible. This digital phase comparator has a linear $\pm 2\pi$ radians phase range, which corresponds to a gain of $\frac{V_{DD}}{2}$ volts/cycle.

To avoid degrading the noise performance of the system by the relatively low gain of phase comparator 2, once a small phase error has been achieved an internal switch disconnects phase comparator 2, leaving only phase comparator 1 connected. Thus the low noise properties of phase comparator 1 are obtained once phase-lock has been achieved.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 1 (see Fig. 3)

Phase comparator 1 is comprised of a linear ramp generator and a sample and hold circuit.

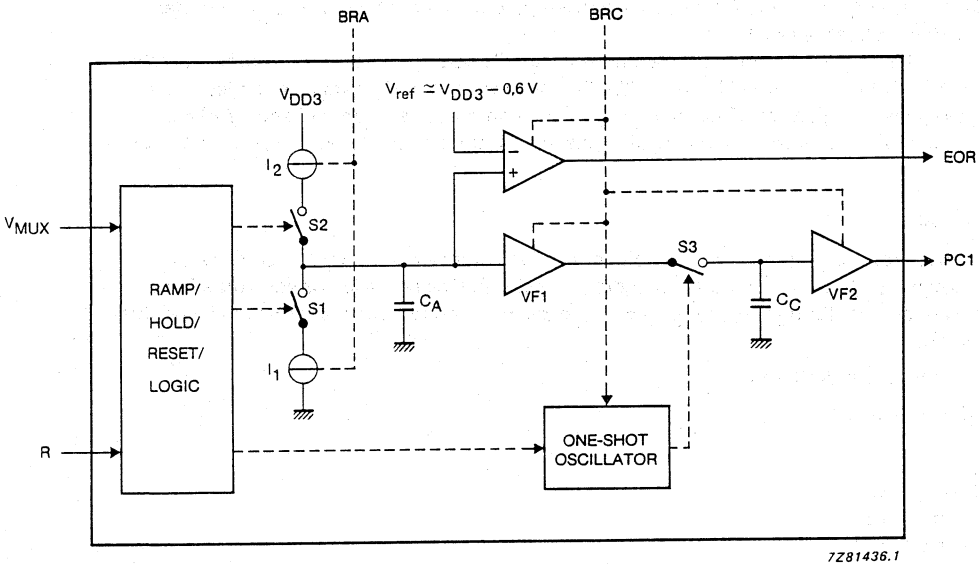


Fig. 3 Simplified block diagram of phase comparator 1.

A negative-going transition at the V_{MUX} input causes the hold capacitor C_A to be discharged via switch S1 and constant current source I_1.
A positive-going transition at the V_{MUX} input causes the hold capacitor C_A to be charged via switch S2 and constant current source I_2, which produces a linear ramp.
A negative-going transition at the R input terminates the linear ramp.
Capacitor C_A holds the voltage that the ramp has attained, and is buffered by the voltage follower VF1. After the output of VF1 is stable (2 μs), the sample switch S3 is closed for approximately 1 μs by the one-shot oscillator. This enables the capacitor C_C to charge to the voltage level of VF1 and in turn buffered by voltage follower VF2 made available at output PC1.
The construction and small duty cycle of the sample switch S3 provides a low hold step, resulting in a minimum side-band level.
If the linear ramp terminates before a negative-going transition at the R input is present, an end of ramp (EOR) signal is produced, generating in turn an out-of-lock (OL) signal. OL enables phase comparator 2 via the out-of-lock detector.

These actions are illustrated in the waveforms of Fig. 4 and Fig. 5.

The gain of phase comparator 1 as measured at PC1 is given by:

$$\text{PC gain} \simeq \frac{446\ I_{BRA}}{F_R}$$

Where:

I_{BRA} is in μA
F_R is the phase comparator reference frequency in kHz

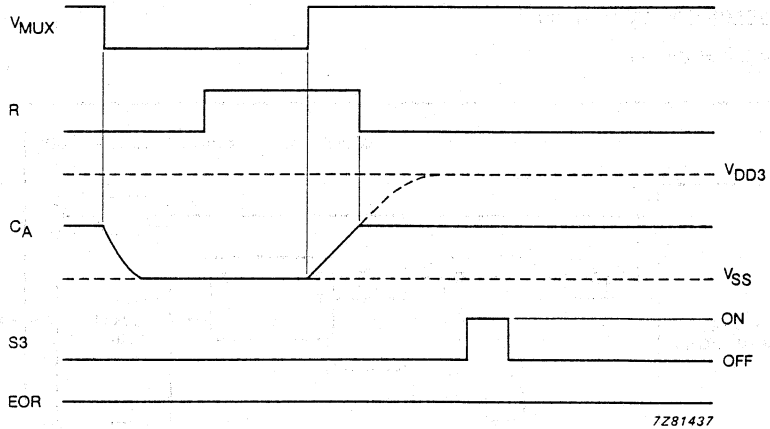


Fig. 4 Waveforms of phase comparator 1; in-lock condition.

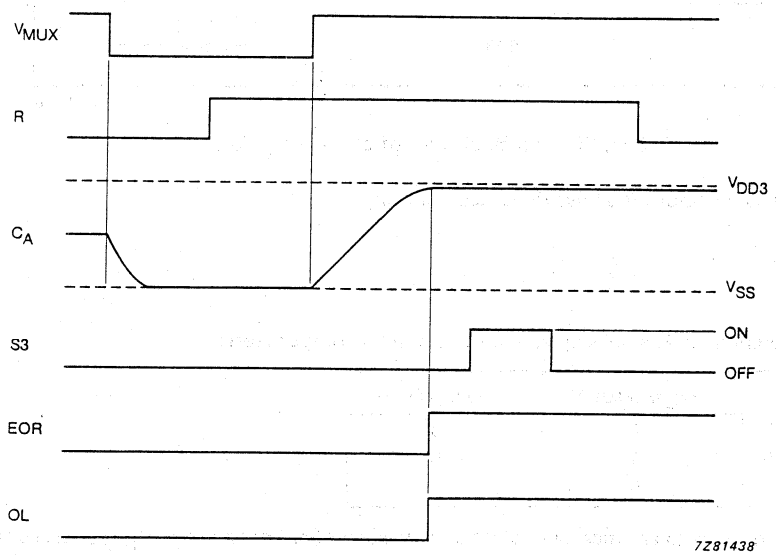


Fig. 5 Waveforms of phase comparator 1; out-of-lock condition.

When V_{MUX} leads R the output signal at pin 2 (PC1) is proportional to the phase difference (in-lock condition) or HIGH (out-of-lock condition).
When R leads V_{MUX} the output signal at pin 2 (PC1) remains LOW.

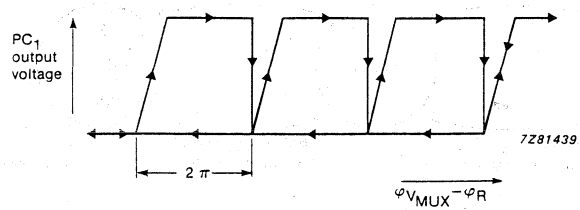


Fig. 6 Phase characteristic of output PC1.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 2 (see Fig. 7)

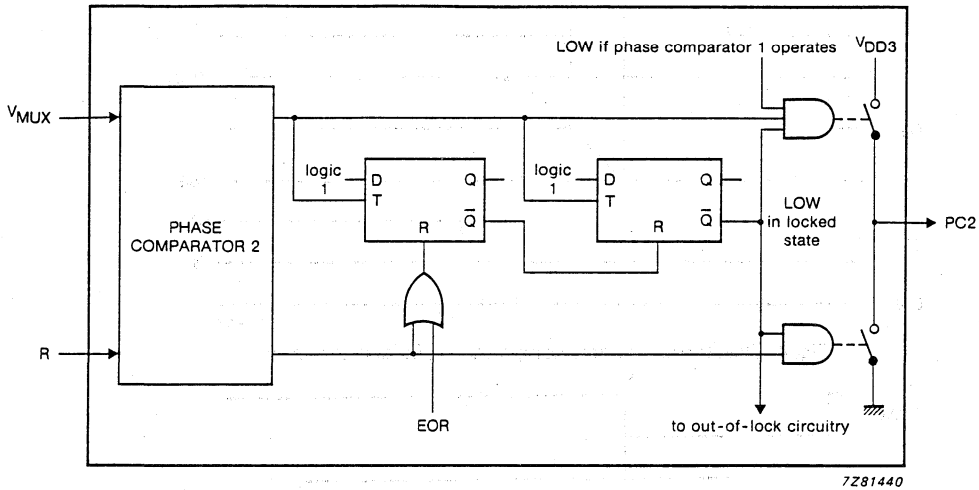


Fig. 7 Simplified block diagram of phase comparator 2.

The digital phase comparator (PC2) has three stable states:

- Reset
- V_{MUX} leads R
- R leads V_{MUX}

Table 1 Phase comparator 2: stable states and corresponding output levels

state	V_{MUX} leads R	R leads V_{MUX}
reset	0	0
V_{MUX} leads R	1	0
R leads V_{MUX}	0	1

Transition from one state to another takes place on command of either an active V_{MUX}-edge or an active R-edge as shown in Fig. 8.

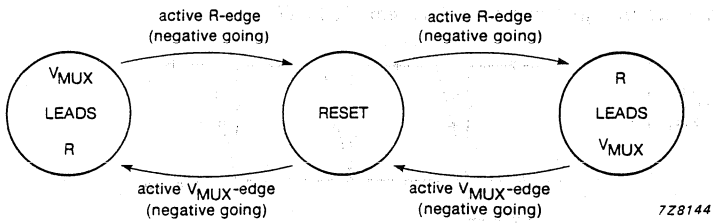


Fig. 8 Transition of state; phase comparator 2.

The output of phase comparator 2 produces positive or negative going pulses with variable width, dependent on the phase relationship of R and V_{MUX}.
The average output voltage is a linear function of the phase difference. Output at pin 3 (PC2) remains in the high impedance OFF-state in the region in which phase comparator 1 operates

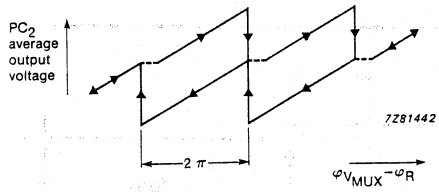


Fig. 9 Phase characteristic of output PC2.

To reach the reset state of phase comparator 2 it is necessary to apply:

- $2V_{MUX}$ + R*
  or
- 2R + V_{MUX}

Thus to achieve the R leads V_{MUX} state 2R must be applied; to achieve the V_{MUX1} leads R state $2V_{MUX}$ must be applied.

Out-of-lock function

There are several situations when the system goes from the locked to the out-of-lock state (OL output goes HIGH):

- V_{MUX} leads R, however out of the range of phase comparator 1
- R leads V_{MUX}
- R-pulse is missing
- V_{MUX}-pulse is missing

In the first three situations the locked state can be reset by applying two successive cycles within the range of phase comparator 1.
In the fourth situation the locked state can be reset by applying a V_{MUX} pulse followed by two successive cycles within the range of phase comparator 1.

Phase modulator (see Fig. 10)

The linear phase modulator applies a voltage controlled delay to the signal from the programmable divider to the phase comparator input. The gain of the phase modulator is adjustable via an external bias resistor (BRB) which is connected between pin 26 and ground.
The time delay introduced into the V path to the phase modulator is:

$$\frac{909}{I_{BRB}} \text{ ns/volt of input applied to pin 24 (MOD)}$$

When a positive-going transition appears at the V-input, the D type flip-flop produces a HIGH V' level and causes capacitor C_B to produce a positive-going ramp via switch S1 and constant current source I_1 starting at the V_{SS} potential. When the ramp has reached a value equal to the modulation input voltage (at MOD), the comparator resets the D type flip-flop, which terminates the V pulse. C_B now discharges to V_{SS} via switch S1 and constant current source I_2 and the circuit returns to the start position. Because the trailing edge of the V' pulse is the active edge for the phase comparators, a linear phase modulation is achieved. The associated waveforms are shown in Fig. 11. The phase modulator can be switched OFF, via the programming logic, to avoid superfluous dissipation. To achieve, this the M signal must be programmed to logic 0. The V pulse will then be connected via switch S2 to V_{MUX}.

* This means apply two successive active V_{MUX} edges followed by one active R edge.

FUNCTIONAL DESCRIPTION (continued)

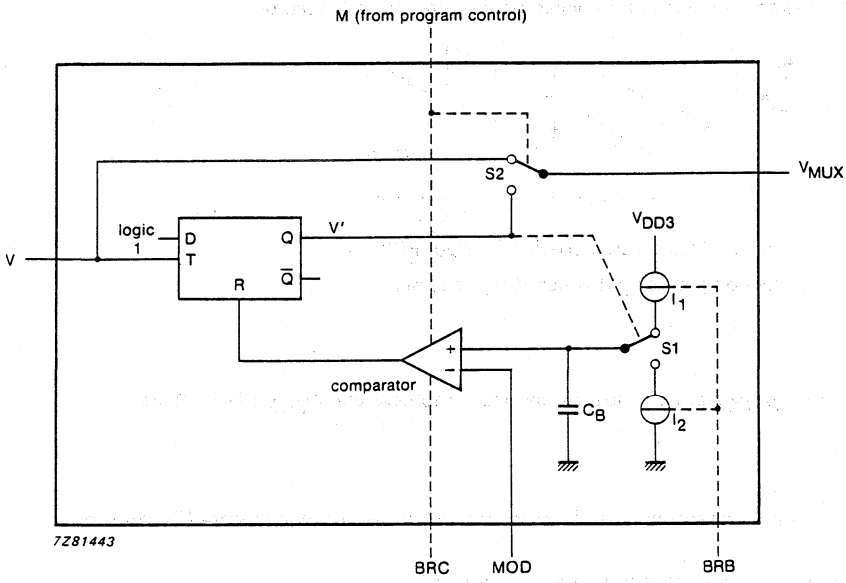


Fig. 10 Simplified block diagram of the phase modulator.

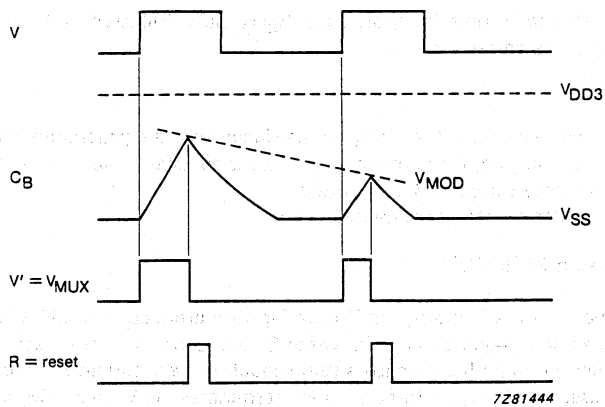


Fig. 11 Phase modulator waveforms; M = 1.

Program control

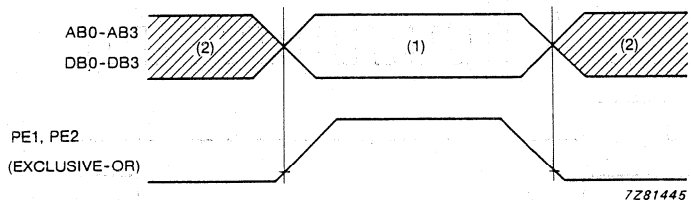
A multiplexed or bus structured sequence allows the TDD1742T to be interfaced to a microcontroller or a PROM.
The device is fully programmable in terms of:

- 6 bits to define the reference divider ratio
- 21 bits to define the main divider ratio
- 1 bit to switch the modulator
- 4 bits to determine the test status

Thus the TDD1742T is programmed with a total of 32 bits which are organized as eight 4-bit words. The address bus is 3 bits wide and the data bus is 4 bits wide. Both buses are TTL compatible. The data words are described in detail in Tables 3 to 7.

Microcontroller mode

If pin 25 ($\overline{\text{MEMEN}}$) is LOW at general reset, the device is set to the micro-controller mode. In this mode a 7-bit word, comprised of 3 address bits (AB0 to AB2) and 4 data bits (DB0 to DB3), may be strobed into the TDD1742T when the program enable pins PE1 and PE2 are set to opposite state (EXCLUSIVE -OR condition; see Fig. 12 and Table 2). One frame of 8 words is necessary to completely program the TDD1742T. Incoming data is not clocked into the internal counter latches until after the receipt of data corresponding to address 111. Upon subsequent reprogramming it is not necessary to change all eight words but a reprogramming sequence must always finish with the data corresponding to address 111.



(1) Address and data valid.
(2) Address and data not valid.

Fig. 12 Waveforms for program enable function; microcontroller mode.

Table 2 Truth table for program enable function; microcontroller mode

PE1	PE2	load
0	0	NO
1	0	YES
0	1	YES
1	1	NO

Program control (continued)

Memory mode (PROM)

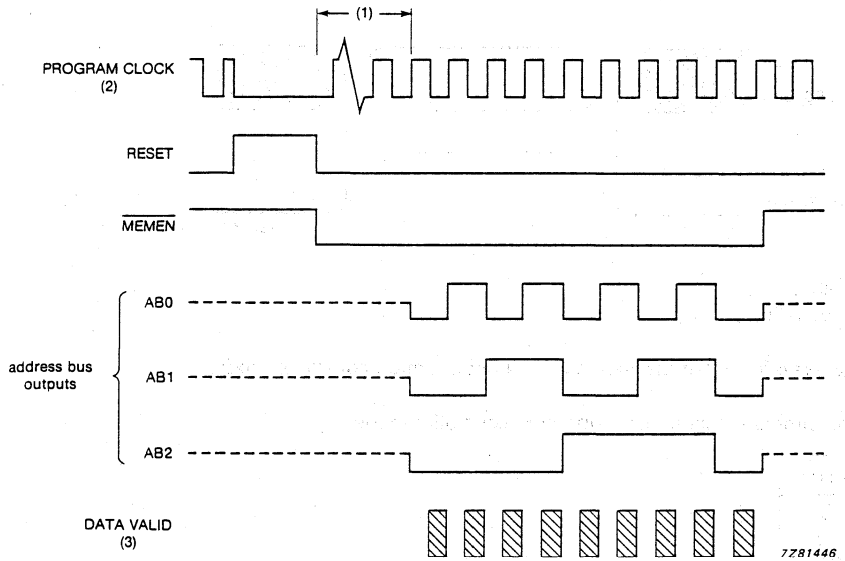
If pin 25 ($\overline{\text{MEMEN}}$) is HIGH at general reset, TDD1742T is set to the memory mode and a programming cycle is initiated. Subsequent reprogramming is performed by applying a pulse to program enable PE1 (pin 23) or PE2 (pin 22). If PE1 is LOW, programming will occur on the LOW-to-HIGH transition of PE2. If PE1 is HIGH, programming will occur on the HIGH-to-LOW transition of PE2. PE1 and PE2 are interchangeable. Reprogramming will also occur by applying a pulse to RESET (pin 11).

At the start of a programming sequence pin 25 goes LOW and may be used to apply power to the memory via an external driver. After a settling time the address bus outputs 000 followed by the remaining seven addresses. During the second half of each address period data, from the memory is latched into the TDD1742T so that the access time of the PROM is not critical.

Note

The program clock is derived from the reference divider chain and its frequency equals $f_{OSC}/4R_0$.

After the full 32 bits have been read the address returns to address 000 before going 3-state. This step transfers data from the internal data latches to the appropriate divider latches. Pin 25 now returns to a high impedance state and power is removed from the memory. Fig. 13 shows the timing for a reset initiated programming sequence; the timing is similar for program enable initiated sequence.



(1) Delay time for PROM settling.
(2) The program clock is derived from the reference divider chain.
(3) Data is valid during the shaded period.

Fig. 13 Timing diagram for TDD1742T PROM control.

Data memory maps

Table 3 Bit programming of the eight 4-bit words

address			data			
AB2	AB1	AB0	DB3	DB2	DB1	DB0
0	0	0	see Table 4			
0	0	1	$n_0 3$	$n_0 2$	$n_0 1$	$n_0 0$
0	1	0	$R_0 0$	$n_0 6$	$n_0 5$	$n_0 4$
0	1	1	$n_1 3$	$n_1 2$	$n_1 1$	$n_1 0$
1	0	0	$R_0 1$	$n_1 6$	$n_1 5$	$n_1 4$
1	0	1	$n_2 3$	$n_2 2$	$n_2 1$	$n_2 0$
1	1	0	M	$n_2 6$	$n_2 5$	$n_2 4$
1	1	1	$R_2 1$	$R_2 0$	$R_1 1$	$R_1 0$

In Table 3

n_0, n_1 and n_2 comprises the main programmable divider.

$n_0 0$ is the LSB of n_0, $n_0 6$ the MSB and so forth.

If M is 1 the modular is ON.

Table 4 Memory map for address 000

DB3	DB2	DB1	DB0	program clock to output CLK	mode
0	0	X	X	yes	idle
0	1	0	0	no	idle
all other combinations				not defined	not defined

Where

X = don't care.

For optimum performance (minimum crosstalk) 0100 should be programmed into address 000.

Memory maps (continued)

Table 5 Reference divider control; part 1

$R_0 1$	$R_0 0$	division ratio
0	0	12
0	1	13
1	0	14
1	1	15

In Table 5:

$R_0 0$ and $R_0 1$ control the ÷ 12/13/14/15 portion of the reference divider.

Table 6 Reference divider control; part 2

$R_1 1$	$R_1 0$	division ratio
0	0	9
0	1	5
1	0	6
1	1	7

In Table 6:

$R_1 0$ and $R_1 1$ control the ÷ 5/6/7/9 portion of the reference divider.

Table 7 Reference divider control; part 3

$R_2 1$	$R_2 0$	division ratio
0	0	1
0	1	2
1	0	4
1	1	8

In Table 7:

$R_2 0$ and $R_2 1$ control the ÷ 1/2/4/8 portion of the reference divider.

Current biassing

Current biassing is provided by 3 external bias resistors A, B and C.

Bias Resistor A: is connected between pin 28 (BRA) and ground. The value of the resistor must be such that I_{BRA} = 20 μA, which acts as gain control for analogue phase comparator 1.
Bias Resistor B: is connected between pin 26 (BRB) and ground. The value of the resistor must be such that I_{BRB} = 3 to 25 μA, which acts as gain control for the phase modulator.
Bias Resistor C: is connected between pin 27 (BRC) and ground. The value of the resistor must be such that I_{BRC} = 5 to 30 μA, which provides biassing for the remainder of the analogue circuitry.

Low power fequency synthesizer (LOPSY) TDD1742T

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges			
pin 14	V_{DD1}		−0,5 to + 15 V
pin 8	V_{DD2}		−0,5 to + 15 V
pin 1	V_{DD3}		−0,5 to + 15 V
Voltage on any input	V_I		−0,5 to V_{DD1} + 0,5 V
Relative supply voltage	V_{DD2}-V_{DD1}	max.	0,5 V
Relative supply voltage	V_{DD3}-V_{DD1}	max.	0,5 V
D.C. current into any input or output	± I	max.	10 mA
Power dissipation per package for T_{amb} = 0 to + 85 °C	P_{tot}	max.	400 mW
Power dissipation per output for T_{amb} = 0 to + 85 °C	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to 150 °C
Operating ambient temperature range	T_{amb}		−40 to 85 °C

D.C. CHARACTERISTICS

$V_{DD1} = V_{DD3} = 7{,}4$ V; $V_{DD2} = 5$ V; $V_{SS} = 0$ V; $T_{amb} = 25\ ^{o}C$ unless otherwise specified; for definitions see note 1.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage					
pin 14	V_{DD1}	7	–	10	V
pin 8	V_{DD2}	4,5	–	5	V
pin 1	V_{DD3}	7	–	10	V
Supply current					
pin 14 (phase modulator OFF)	I_{DD1}	–	–	1,5	mA
pin 8	I_{DD2}	–	–	100	μA
pin 1 (phase modulator OFF)	I_{DD3}	–	–	1,5	mA
Input leakage current (notes 2 and 3)					
logic inputs, MOD	$\pm I_{LI}$	–	–	300	nA
Output leakage current (notes 2 and 3)					
at ½ V_{DD}					
PC2 high impedance OFF state	$\pm I_{LO}$	–	–	50	nA
$\overline{MEMEN}$ high impedance state	$\pm I_{LO}$	–	–	1,6	μA
I/O current					
AB0 to AB2 high impedance state	$I_{I/O}$	5	–	30	μA
Logic input voltage LOW					
CMOS inputs; CMOS I/Os	V_{IL}	–	–	$0{,}3V_{DD1}$	V
TTL inputs; TTL I/Os	V_{IL}	–	–	0,8	V
Logic input voltage HIGH					
CMOS inputs; CMOS I/Os	V_{IH}	$0{,}7V_{DD1}$	–	–	V
TTL inputs; TTL I/Os	V_{IH}	2	–	–	V
Logic output voltage LOW (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	50	mV
Logic output voltage HIGH (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OH}	V_{DD1}-50	–	–	mV

parameter	symbol	min.	typ.	max.	unit
Logic output voltage LOW (note 2)					
$\overline{\text{MEMEN}}$ at I_{OL} = 4 mA	V_{OL}	–	–	1	V
PC2 at I_{OL} = 1,5 mA	V_{OL}	–	–	0,5	V
CLK; OL at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
XTAL at I_{OL} = 3 mA	V_{OL}	–	–	0,5	V
FB at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
AB0; AB1; AB2 at I_{OL} = 0,2 mA	V_{OL}	–	–	0,4	V
Logic output voltage HIGH (notes 2 and 3)					
PC2 at $-I_{OH}$ = 1,5 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
CLK; OL at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
XTAL at $-I_{OH}$ = 3 mA	V_{OH}	$V_{DD1}-1$	–	–	V
FB at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD2}-1$	–	–	V
AB0; AB1 at I_{OH} = 0,2 mA	V_{OH}	2,4	–	–	V
AB2 at I_{OH} = 0,8 mA	V_{OH}	2,4	–	–	V
Output PC1					
sink current (notes 2, 3 and Fig. 15)	I_O	1	–	–	mA
source current (notes 2, 3 and Fig. 16)	$-I_O$	1	–	–	mA
Internal resistance of phase comparator 1 (notes 2 and 3) locked state |output swing| < 200 mV specified output range: $0,5\ V_{DD}-0,5$ V to $0,5\ V_{DD}+0,5$ V	R_i	–	2,0	–	Ω

A.C. CHARACTERISTICS

A dynamic specification is given for the circuit, built-up with external components as shown in Fig. 14, under the following conditions; for definitions see note 1; V_{DD} = 7,4 ± 0,4 V; T_{amb} = 25 °C; input transition times ⩽ 40 ns; $C_A = C_B = C_C$ = 10 nF; R_A chosen so that I_{RA} = 20 μA ± 1 μA; R_B chosen so that I_{RB} = 3 to 25 μA; R_C chosen so that I_{RC} = 5 to 30 μA; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Main programmable divider (DIV(M); pin 7)					
input frequency all divider ratios (square wave input)	$f_{DIV(M)}$	8,5	–	–	MHz
Reference divider					
input frequency all divider ratios (square wave input)	$f_{DIV(R)}$	9	–	–	MHz
Oscillator frequency (OSC; pin 13)	f_{OSC}	9	12	–	MHz
Input capacitance					
DIV(M); OSC	C_I	–	–	3	pF
DB0 to DB3; PE1; PE2; AB0 to AB2	C_I	–	–	5	pF
Propagation delay (see Fig. 17)					
Feedback output to external prescaler					
DIV(M) → FB at C_L = 10 pF					
HIGH to LOW*	t_{PHL}	–	35	70	ns
LOW to HIGH*	t_{PLH}	–	35	70	ns
Average power supply current (notes 3 and 4)					
in-lock state	I_{DD1}	–	2	–	mA
	I_{DD2}	–	0,15	–	mA
	I_{DD3}	–	0,45	–	mA

* Measured from 30% point of negative-going edge at DIV(M) to 50% point of either output edge of FB.

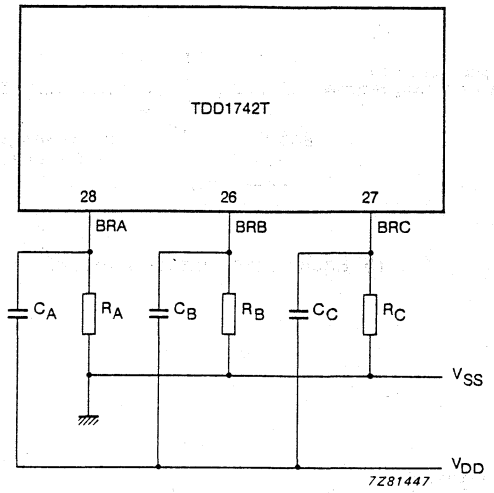


Fig. 14 Test circuit for measuring a.c. characteristics.

Notes to the characteristics

1. Definitions:
   R_A = external biassing resistor between pins BRA and V_{SS}.
   R_B = external biassing resistor between pins BRB and V_{SS}.
   R_C = external biassing resistor between pins BRC and V_{SS}.
   C_A = decoupling capacitor between pins BRA and V_{DD}.
   C_B = decoupling capacitor between pins BRB and V_{DD}.
   C_C = decoupling capacitor between pins BRC and V_{DD}.
   CMOS logic inputs: RESET, OSC.
   CMOS logic outputs: PC2, CLK, OL, XTAL.
   CMOS logic I/O: $\overline{\text{MEMEN}}$.
   TTL logic inputs: DB0 to DB3, PE2, PE1.
   TTL logic output: FB.
   TTL logic I/O: AB0 to AB2.
   Analogue inputs: DIV(M), MOD.
   Analogue output: PC1.
   Analogue biassing pins: BRA, BRB, BRC.
2. All logic inputs at V_{SS} or V_{DD}.
3. R_A connected; its value chosen such that $I_{BRA} = 20\ \mu A$.
   R_B connected; its value chosen such that $I_{BRB} = 20\ \mu A$.
   R_C connected; its value chosen such that $I_{BRC} = 20\ \mu A$.
4. Average power supply current measured at:
   f_{OSC} = 5 MHz, external clock, divider ratio 420;
   $f_{DIV(M)}$ = 2 MHz, divider ratio 168.

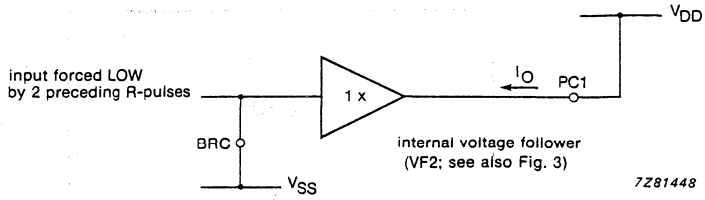


Fig. 15 Equivalent circuit for output PC1 sink current.

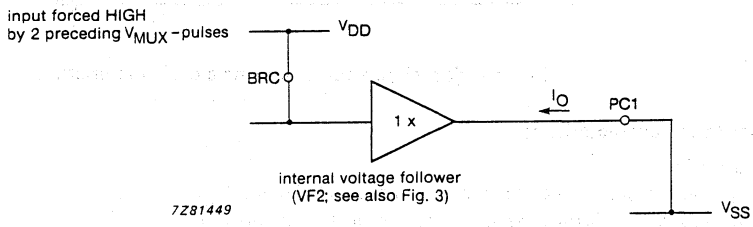


Fig. 16 Equivalent circuit for output PC1 source current.

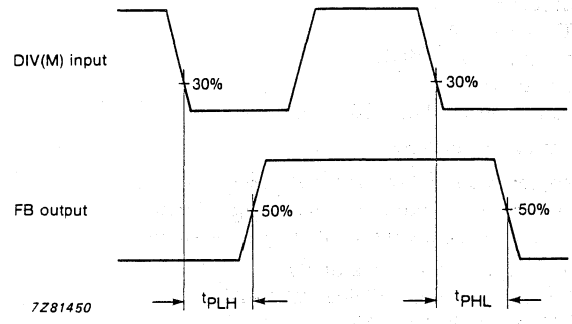


Fig. 17 Waveforms showing propagation delay; DIV (M) → FB.

APPLICATION INFORMATION

Fig. 18 shows a typical application circuit using the TDD1742T in the memory mode with the following design parameters:

Frequency range	150 to 155 MHz
VCO sensitivity	1 MHz/V
Reference frequency	12,5 kHz
Prescaler	÷ 80/81
Reference crystal frequency	5,25 MHz
Reference divider chain	÷ 15; ÷ 7; ÷ 1
Total division ratio	12000 to 12400
Loop bandwidth	300 Hz

APPLICATION INFORMATION (continued)

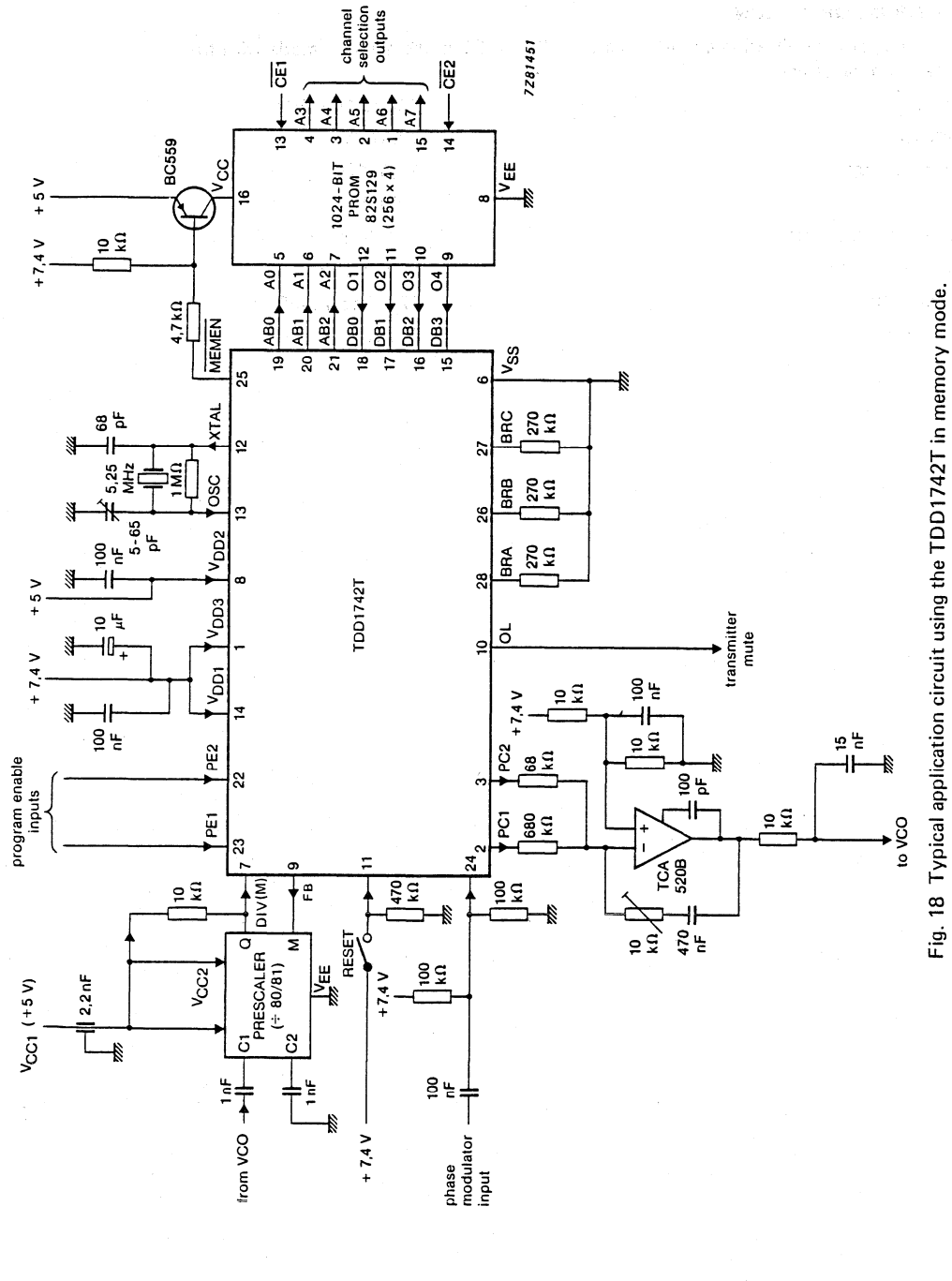


Fig. 18 Typical application circuit using the TDD1742T in memory mode.

Battery low-level indicator TEA1041T

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

FEATURES

- Optical signal following battery low-level detection
- Additional warning ('recharge needed') at end of system operation
- One or two LED indication
- Trigger level adjustable
- Low stand-by current
- Insensitive to interference
- Few external components

APPLICATIONS

- Battery operated systems

GENERAL DESCRIPTION

Intended for use with battery operated systems, the TEA1041T generates an optical alarm via one or two LEDs when the battery supply voltage falls below a preset threshold level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	1.8	-	4.0	V
I_{sb}	stand-by current	-	-	10	µA
P_{tot}	total power dissipation	-	-	150	mW
I_L	output current LED outputs	-	-	59	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1041T	8	SO8	plastic	SOT96A

FUNCTIONAL DESCRIPTION

Supply (pin 8)

The supply voltage, which may range from 1.8 to 4.0 V, is connected to pin 8.

Voltage sense input (pin 1)

Pin 1 is connected to a trigger circuit consisting of a trigger amplifier and a Schmitt trigger.

An up / down counter in the control and timing logic is enabled when the potential at pin 1 falls below 1.25 V. Unless this voltage increases above 1.25 V the counter will operate for approximately two seconds. When the voltage increases or the count is timed-out, the counter will then begin counting-down. The circuit is thus protected from any disturbance of less than two seconds duration. LED 1 becomes lit on the next occasion that for two seconds the potential on pin 1 is less than 1.25 V.

Following low level detection the circuit is de-activated by operation of S1. For a period of 4 seconds LEDs 1 and 2 will then each be alternately lit for a duration of approximately 500 ms.

LED 1 and LED 2 connections (pin 7, 6)

The cathodes of LEDs 1 and 2 must be connected respectively to pins 7 and 6. The circuit will also function with only LED 1 connected.

Oscillator capacitor connection (pin 4)

Circuit timing is provided by the internal oscillator, the frequency of which is determind by a capacitor connected to pin 4.

Forcing a current (max. 5 mA) into pin 4 permits direct monitoring of the trigger circuit at pins 6 and 7. When V_I is above 1.25 V, pin 7 will be LOW and pin 6 will be HIGH. Alternatively, when V_I is below the 1.25 V threshold level pin 7 will be HIGH while pin 6 will be rendered LOW. This feature facilitates easier circuit adjustment.

Pin 2 Test Pin

An external clock signal may be connected to pin 2 for test purposes. This may be used to shorten the test time (see also test and application information).

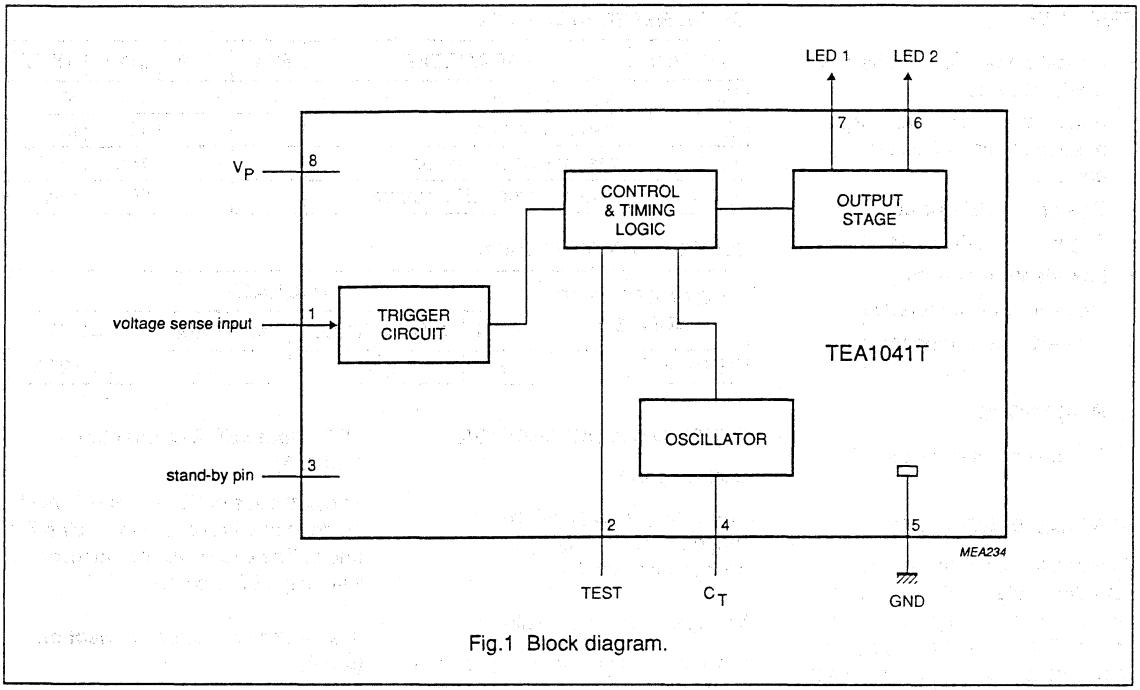


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_I	1	voltage sense input
TEST	2	test pin
V_{sw}	3	stand-by
C_T	4	oscillator capacitor
GND	5	ground
L2	6	LED 2
L1	7	LED 1
V_P	8	supply voltage

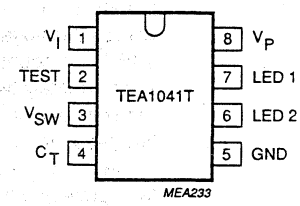


Fig.2 Pin configuration.

Versatile telephone transmission circuits with dialler interface

TEA1060 TEA1061

GENERAL DESCRIPTION

The TEA1060 and TEA1061 are bipolar integrated circuits performing all speech, and line interface functions required in fully electronic telephone sets. The circuits internally perform electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1061)
- Asymmetrical high-impedance input for electret microphone (TEA1061)
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
Line current operating range (pin 1)		I_{line}	10	–	140	mA
Internal supply current						
power down input LOW		I_{CC}	–	0.96	1.3	mA
power down input HIGH		I_{CC}	82	55	–	μA
Supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH					
	I_P = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_P = 1.7 mA	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier						
TEA1060		G_v	44	–	60	dB
TEA1061		G_v	30	–	46	dB
receiving amplifier		G_v	17	–	39	dB
Line loss compensation						
gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	24	–	60	V
Exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Operating ambient temperature range		T_{amb}	−25	–	+75	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

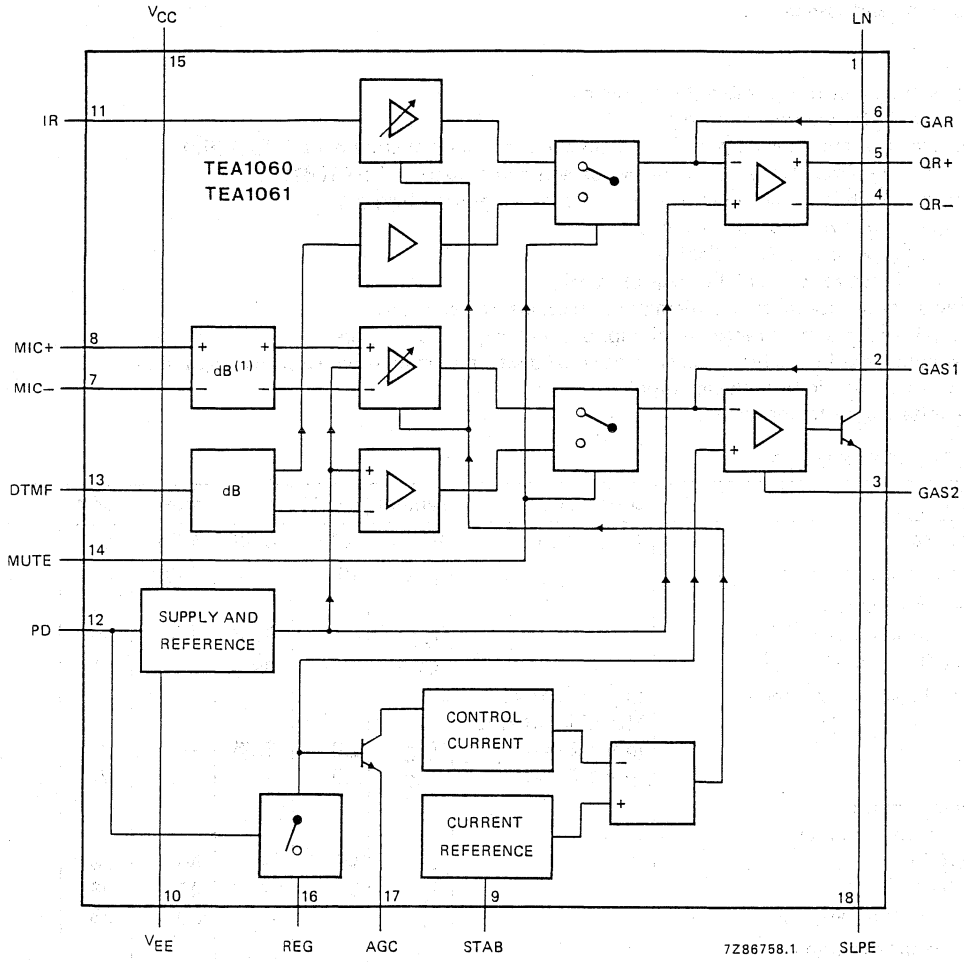


Fig.1 Block diagram.

The blocks marked "dB" are attenuators. The block marked (1) is only present in the TEA1061.

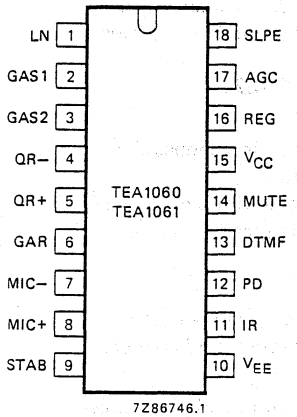


Fig.2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits are usually supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6 kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the subscriber line (R_{line}) and the DC voltage on the subscriber set (see Fig.4).

If the line current (I_{line}) exceeds the current I_{CC} + 0.5 mA required by the circuit itself (I_{CC} ca. 1 mA), plus the current Ip required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.
The voltage regulator adjusts the average voltage on LN to:
$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0.5 \times 10^{-3}\,A - I_p) \times R9$.

V_{ref} being an internally generated temperature compensated reference voltage of 4.2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value of R9 is 20 Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side tone and maximum output swing on LN.
Under normal conditions $I_{SLPE} \gg I_{CC}$ + 0.5 mA + Ip. The static behaviour of the circuit then equals a 4.2 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1. The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This resistor connected between pins 1 and 16 (LN and REG) will decrease the internal reference voltage. R_{VA} connected between pins 16 and 18 (REG and SLPE) will increase the internal reference voltage.

Supply: V_{CC}, LN, SLPE, REG and STAB (continued)

The current Ip available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Fig.5 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V, of which 3 V is the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MIC+ and MIC− and gain adjustment connections GAS1 and GAS2

The TEA1060 and TEA1061 have symmetrical microphone inputs.
The TEA1060 is intended for low-sensitivity low-impedance dynamic or magnetic microphones. Its input impedance is 8.2 kΩ (2 x 4.1 kΩ) and its voltage amplification is typ. 52 dB.
The TEA1061 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 40.8 kΩ (2 x 20.4 kΩ) and its voltage amplification is typ. 38 dB.
The arrangements with the microphone types mentioned are shown in Fig.6.

The gain of the microphone amplifier in both types can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor (C6) of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 25.5 dB and varies with R7 in the same way as the gain of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig.7). The gain from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB and differential drive becomes possible.
This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C7 = 10 x C4 = 1 nF are necessary to ensure stability.
A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.8 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range. If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum gain as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.
When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the antiside-tone network consisting of $R1//Z_{line}$, R2, R3, R8 and Z_{bal} (see Fig.11). Maximum compensation is obtained when the following conditions are fulfilled:

$$a)\ R9.R2 = R1[R3 + (R8//Z_{bal})]$$

$$b)\ [Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| \ll R3$.

To obtain optimum side-tone-suppression, condition (b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)Z_{line} = k.Z_{line}$$

where k is a scale factor; $k = (R8/R1)$

Scale factor k (value of R8) must be chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal} + R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal} equals the average line impedance.

The anti-side-tone network as used in the standard application (Fig.11) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side tone circuit. Both bridges can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

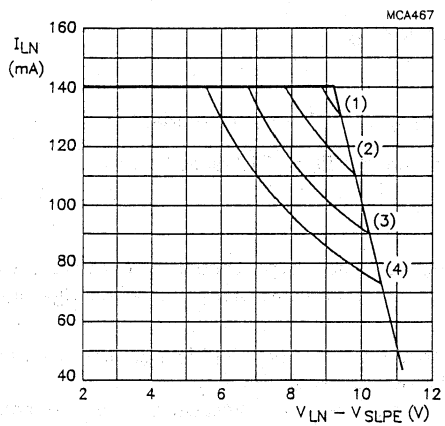
Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on or line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R10 = 13 Ω; R9 = 20 Ω; (see Fig.11)	V_{LN}	–	28	V
Line current TEA1060 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1061 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		$-V_i$	–	0.7	V
Total power dissipation (2)		P_{tot}	–	769	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

1. Mostly dependent on the maximum required T_{amb} and the voltage between LN and SLPE (see Fig.3).
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air
TEA1060 and TEA1061 $R_{th\ j\text{-}a}$ = 65 K/W



	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

Fig.3 TEA1060/1061 safe operating area.

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C, R9 = 20 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)						
Voltage drop over circuit	I_{line} = 5 mA	V_{LN}	3.95	4.25	4.55	V
	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
	I_{line} = 100 mA	V_{LN}	5.4	6.1	6.7	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Voltage drop over circuit	I_{line} = 15 mA $R_{VA} = R_{1\text{-}16}$ = 68 kΩ	V_{LN}	3.5	3.8	4.05	V
	$R_{VA} = R_{16\text{-}18}$ = 39 kΩ	V_{LN}	4.7	5.0	5.3	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	0.96	1.30	mA
	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuits	I_{line} = 15 mA; MUTE = HIGH					
	I_P = 0 mA	V_{CC}	3.5	3.75	–	V
	I_P = 1.2 mA	V_{CC}	2.8	3.05	–	V
Microphone inputs MIC+ and MIC− (pins 7 and 8)						
Input impedance						
TEA1060		$\lvert Z_i \rvert$	3.3	4.1	4.9	kΩ
TEA1061		$\lvert Z_i \rvert$	16.5	20.4	24.5	kΩ
Common-mode rejection ratio TEA1060		k_{CMR}	–	82	–	dB
Voltage gain	I_{line} = 15 mA; R7 = 68 kΩ					
TEA1060		G_v	51	52	53	dB
TEA1061		G_v	37	38	39	dB
Variation with frequency referred to 800 Hz	f = 300 and 3400 kHz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Variation with temperature referred to +25 °C	I_{line} = 50 mA; T_{amb} = −25 and +75 °C	ΔG_{vT}	–	±0.2	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF (pin 13)						
Input impedance		$\|Z_i\|$	16.8	20.7	24.6	kΩ
Voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Variation with frequency referred to 800 Hz	f = 300 and 3400 kHz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Variation with temperature referred to 800 Hz	I_{line} = 50 mA; T_{amb} = −25 and +75 °C	ΔG_{vT}	−	±0.2	−	dB
Gain adjustment GAS1 and GAS2 (pins 2 and 3)						
Gain variation with R7 connected between pins 2 and 3; transmitting amplifier		ΔG_v	−8	−	+8	dB
Transmitting amplifier output LN (pin 1)						
Output voltage	I_{line} = 15 mA; d_{tot} = 2%	$V_{LN(rms)}$	1.9	2.3	−	V
	d_{tot} = 10%	$V_{LN(rms)}$	−	2.6	−	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; pins 7 and 8 open circuit psophometrically weighted (P53 curve)	$V_{no(rms)}$	−	−70	−	dBmp
Receiving amplifier input IR (pin 11)						
Input impedance		$\|Z_i\|$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR− (pins 4 and 5)						
Output impedance; single-ended		$\|Z_o\|$	−	4	−	Ω
Voltage gain from pin 11 to pin 4 or 5	I_{line} = 15 mA; R4 = 100 kΩ					
single-ended	R_L = 300 Ω	G_v	24	25	26	dB
differential	R_L = 600 Ω	G_v	30	31	32	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Variation with frequency referred to 800 Hz	f = 300 and 3400 Hz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Variation with temperature referred to 800 Hz	I_{line} = 15 mA T_{amb} = −25 and +75 °C	ΔG_{vT}	–	±0.2	–	dB
Output voltage	I_P = 0 mA; d_{tot} = 2%;					
sine-wave drive	R4 = 100 kΩ					
single-ended	R_L = 150 Ω	$V_{o(rms)}$	0.3	0.38	–	V
single-ended	R_L = 450 Ω	$V_{o(rms)}$	0.4	0.52	–	V
differential	C_L = 47 nF					
R_{series} = 100 Ω	f = 3400 Hz	$V_{o(rms)}$	0.8	1.0	–	V
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; pin 11 open circuit psophometrically weighted (P53 curve)					
single-ended	R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR (pin 6)						
Gain variation with R4 connected between pins 6 and 5; receiving amplifier		ΔG_v	−8	–	+8	dB
MUTE input (pin 14)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Reduction of voltage gain from MIC+ and MIC− to LN	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH R4 = 100 kΩ					
single-ended load	R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD (pin 12)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic gain control input AGC (pin 17)						
Controlling the gain from IR to QR+/QR− and the gain from MIC+/MIC− to LN; R6 = 110 kΩ (connected between pins 17 and 10)						
Gain control range	I_{line} = 70 mA	$-\Delta G_v$	5.5	5.9	6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Lowest line current for lowest gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		$-\Delta G_v$	1.0	1.5	2.0	dB

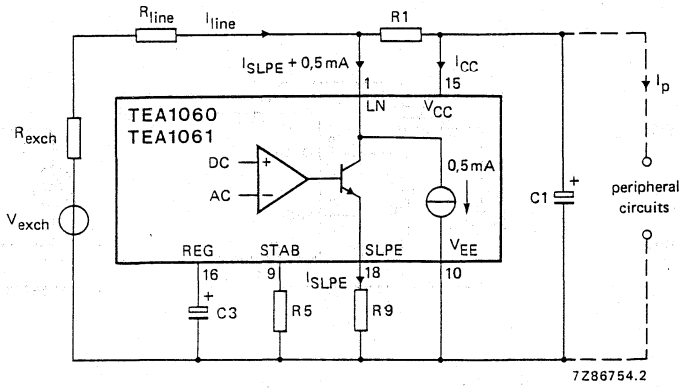
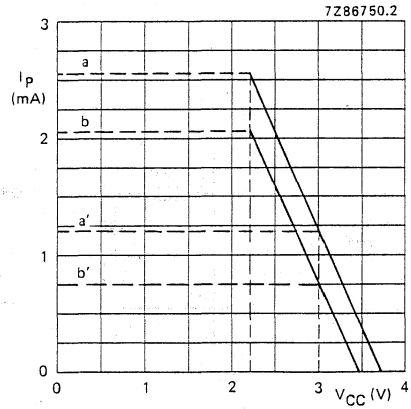


Fig.4 Supply arrangement.



I_{line} = 15 mA at
V_{LN} = 4.45 V;
R1 = 620 Ω, R9 = 20 Ω

Fig.5 Maximum current Ip available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2.2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH. Curves (b) and (b') are valid when MUTE = LOW and the receiving amplifier is driven. $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical).

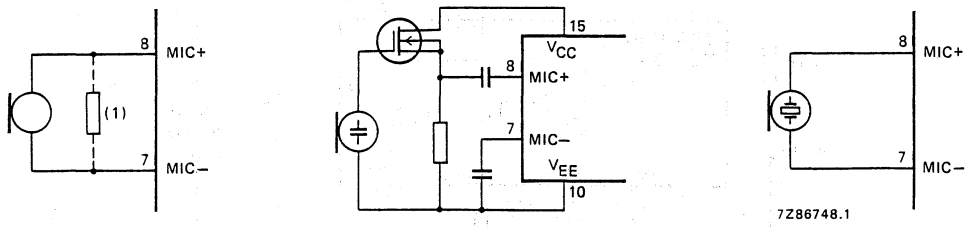


Fig.6 Alternative microphone arrangements: (a) magnetic or dynamic microphone for TEA1060, the resistor marked (1) may be connected to lower the terminating impedance, (b) electret microphone and (c) piezoelectric microphone for TEA1061.

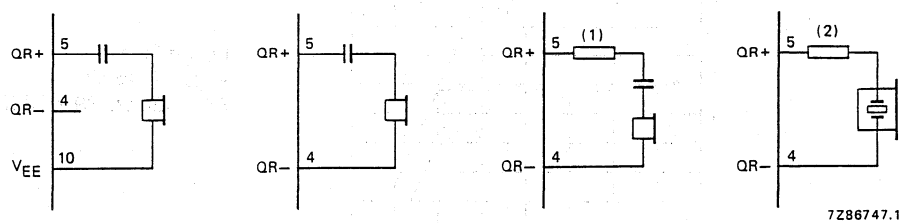


Fig.7 Alternative receiver arrangements: (a) dynamic earpiece with less than 450 Ω impedance, (b) dynamic earpiece with more than 450 Ω impedance, (c) magnetic earpiece. The resistor marked (1) may be connected to prevent distortion [inductive load (d)] piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

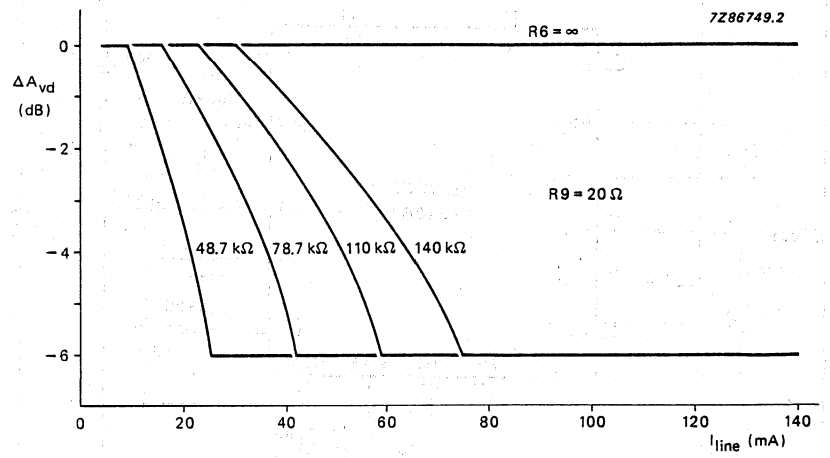


Fig.8 Variation of gain with line current with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

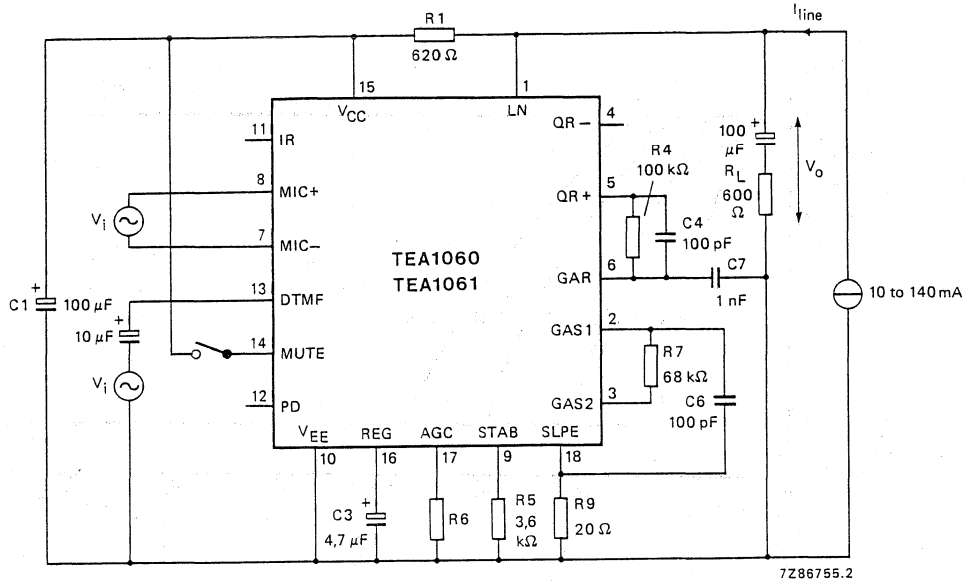


Fig.9 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_V = 20 \log |V_O/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open circuit. For measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open circuit.

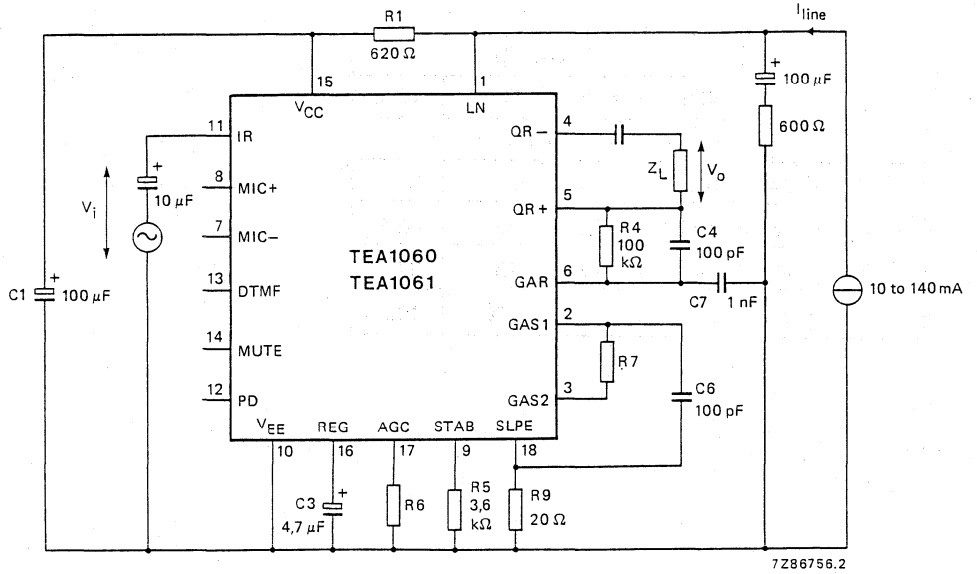


Fig.10 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_V = 20 \log |V_O/V_i|$.

APPLICATION INFORMATION

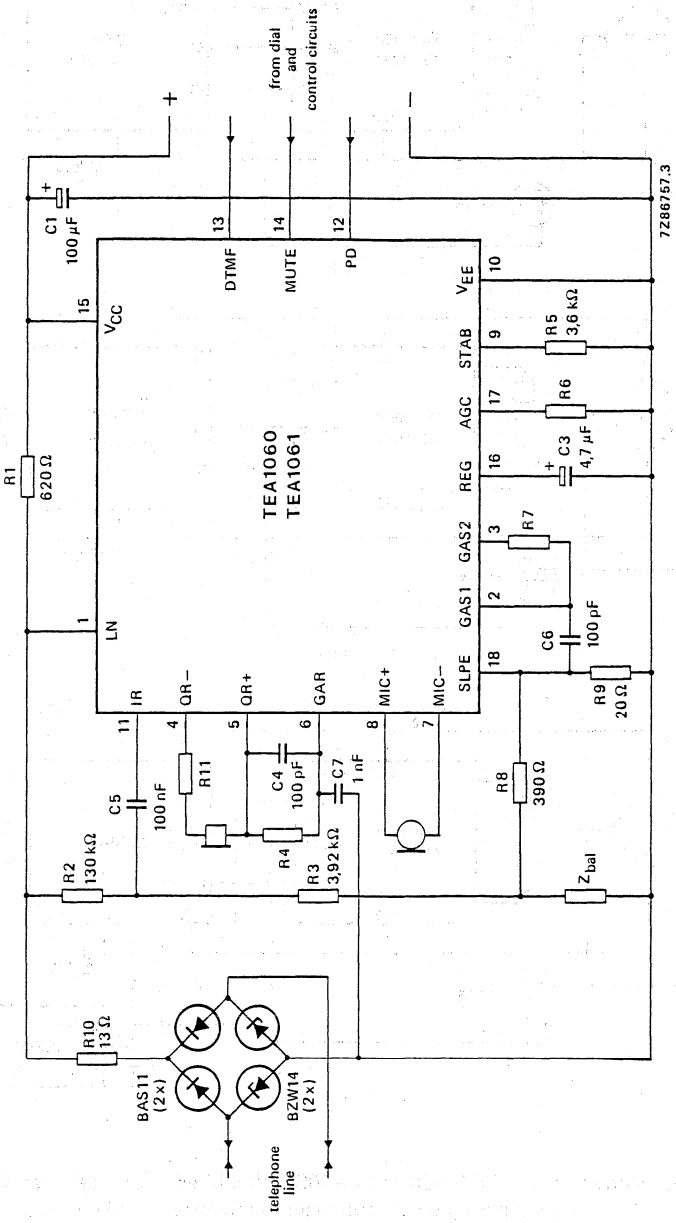


Fig.11 Typical application of the TEA1060 or TEA1061, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

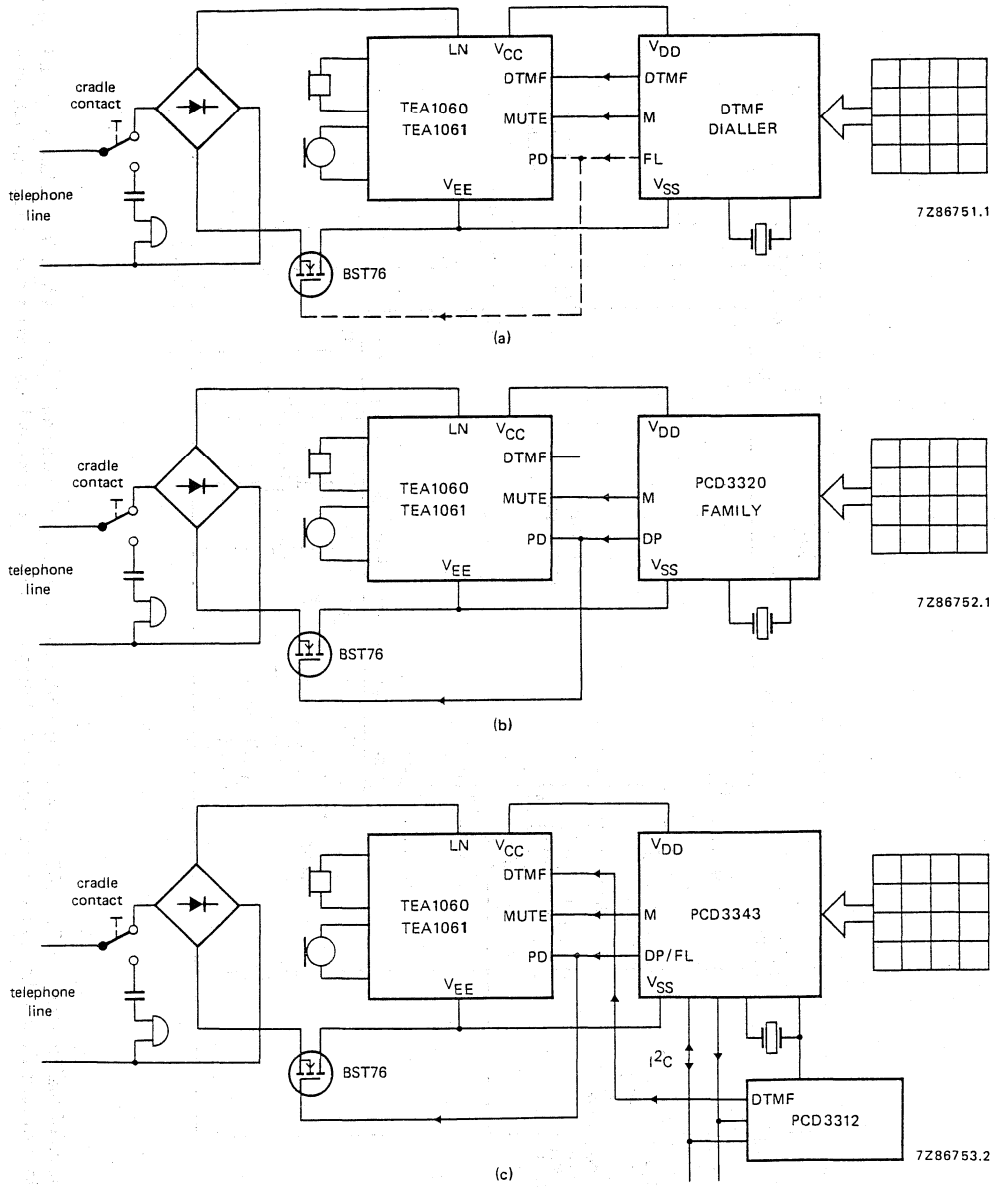


Fig.12 Typical applications of the TEA1060 or TEA1061 (simplified): (a) DTMF set with a CMOS DTMF dialling circuit, the dashed lines show an optional flash (register recall by timed loop break); (b) Pulse dial set with the one of the PCD3320 family of CMOS interrupted current-loop dialling circuits; (c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C-bus.

COMPARISON OF TRANSMISSION ICs

	60	61	64	66T	67	68
Microphones						
low sensitivity dynamic or magnetic	*			*		*
medium sensitivity magnetic or dynamic	*		*	*	*	*
electret with preamplifier		*	*	*	*	*
piezo electric		*	*	*	*	*
very accurate microphone matching			*		*	*
dynamic limiter			*			
Receivers						
dynamic or magnetic or piezo (17-39 dB)	*	*		*		*
dynamic or magnetic or piezo (20-45 dB)			*		*	
Power-down input	*	*	*	*	*	*
DTMF and mute inputs	*	*	*	*	*	*
Voltage regulator						
adjustable DC voltage/resistance	*	*	*	*	*	*
parallel operation			*		*	
Peripheral supply						
unregulated - limited power	*	*		*	*	*
unregulated - extended power			*			
stabilized - extended power			*			
Automatic line loss compensation AGC	*	*	*	*	*	*

Low voltage transmission circuit with dialler interface

TEA1062; TEA1062A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides a supply for external circuits
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
  - TEA1062: active HIGH (MUTE)
  - TEA1062A: active LOW ($\overline{\text{MUTE}}$)
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- Large gain setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers
- Gain control curve adaptable to exchange supply
- DC line voltage adjustment facility.

GENERAL DESCRIPTION

The TEA1062 and TEA1062A are integrated circuits that perform all speech and line interface functions required in fully electronic telephone sets. They perform electronic switching between dialling and speech. The ICs operate at line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel.

All statements and values refer to all versions unless otherwise specified.

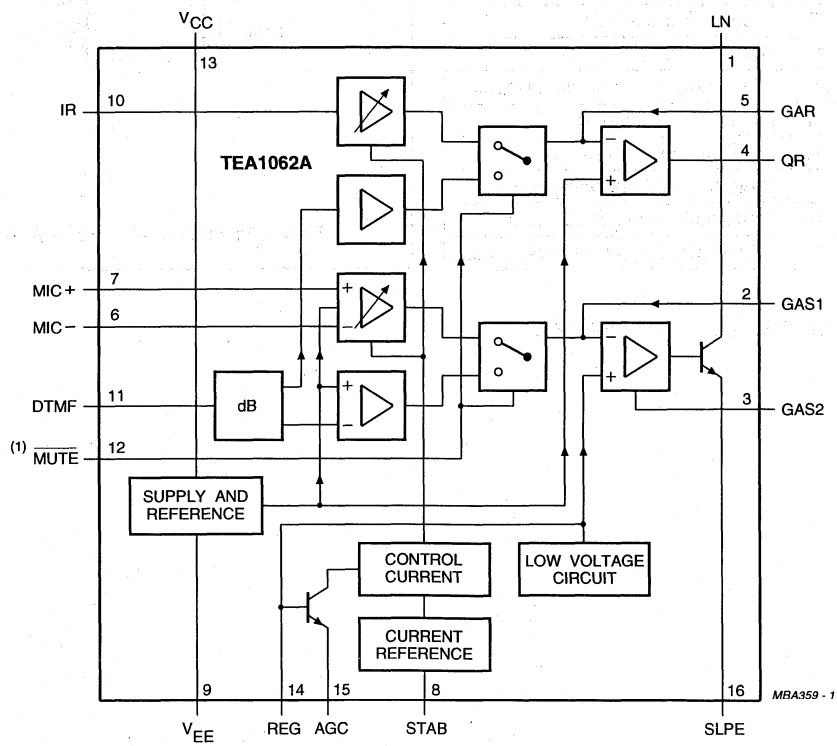
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	3.55	4.0	4.25	V
I_{line}	operating line current					
	normal operation		11	–	140	mA
	with reduced performance		1	–	11	mA
I_{CC}	internal supply current	V_{CC} = 2.8 V	–	0.9	1.35	mA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA				
	TEA1062	I_p = 1.2 mA; MUTE = HIGH	2.2	2.7	–	V
		I_p = 0 mA; MUTE = HIGH	–	3.4	–	V
	TEA1062A	I_p = 1.2 mA; $\overline{\text{MUTE}}$ = LOW	2.2	2.7	–	V
		I_p = 0 mA; $\overline{\text{MUTE}}$ = LOW	–	3.4	–	V
G_v	voltage gain					
	microphone amplifier		44	–	52	dB
	receiving amplifier		20	–	31	dB
T_{amb}	operating ambient temperature		–25	–	+75	°C
Line loss compensation						
ΔG_v	gain control		–	5.8	–	dB
V_{exch}	exchange supply voltage		36	–	60	V
R_{exch}	exchange feeding bridge resistance		0.4	–	1	kΩ

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1062	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TEA1062C3M1	IDF16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TEA1062C4M1	IDF16	plastic dual in-line package; 16 leads (300 mil)	SOT38-8
TEA1062A	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TEA1062T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TEA1062AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM



(1) Pin 12 is active HIGH (MUTE) for TEA1062.

Fig.1 Block diagram for TEA1062A.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; transmitting amplifier
GAS2	3	gain adjustment; transmitting amplifier
QR	4	non-inverting output; receiving amplifier
GAR	5	gain adjustment; receiving amplifier
MIC–	6	inverting microphone input
MIC+	7	non-inverting microphone input
STAB	8	current stabilizer
V_{EE}	9	negative line terminal
IR	10	receiving amplifier input
DTMF	11	dual-tone multi-frequency input
$\overline{MUTE}$	12	mute input (see note 1)
V_{CC}	13	positive supply decoupling
REG	14	voltage regulator decoupling
AGC	15	automatic gain control input
SLPE	16	slope (DC resistance) adjustment

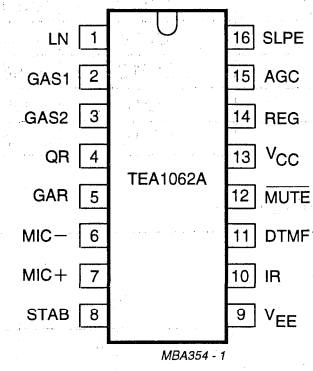


Fig.2 Pin configuration for TEA1062A.

Note

1. Pin 12 is active HIGH (MUTE) for TEA1062.

FUNCTIONAL DESCRIPTION

Supplies V_{CC}, LN, SLPE, REG and STAB

Power for the IC and its peripheral circuits is usually obtained from the telephone line. The supply voltage is derived from the line via a dropping resistor and regulated by the IC. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE}. The internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch} and the DC resistance of the telephone line R_{line}.

The circuit has an internal current stabilizer operating at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig.9). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.

The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9$$

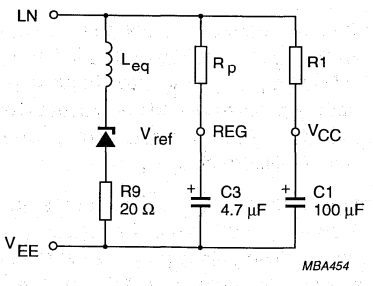
$$V_{LN} = V_{ref} + \{(I_{line} - I_{CC} - 0.5 \times 10^{-3}\ A) - I_p\} \times R9$$

V_{ref} is an internally generated temperature compensated reference voltage of 3.7 V and R9 is an external resistor connected between SLPE and V_{EE}.

In normal use the value of R9 would be 20 Ω.

Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, sidetone level, maximum output swing on LN and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} >> I_{CC} + 0.5\ mA + I_p$, the static behaviour of the circuit is that of a 3.7 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig.3 shows the equivalent impedance of the circuit.



$L_{eq} = C3 \times R9 \times R_p$.
$R_p = 16.2\ k\Omega$.

Fig.3 Equivalent impedance circuit.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that more sets can be operated in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor when connected between LN and REG will decrease the internal reference voltage and when connected between REG and SLPE will increase the internal reference voltage.

Current (I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig.10 shows this current for $V_{CC} > 2.2$ V. If MUTE is LOW (TEA1062) or $\overline{MUTE}$ is HIGH (TEA1062A) when the receiving amplifier is driven, the available current is further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1 as shown in Fig.19(c) and Fig.20(c), or by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE (Fig.18).

Microphone inputs MIC+ and MIC– and gain pins GAS1 and GAS2

The circuit has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 × 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Figures 14 and 15). Dynamic, magnetic, piezo-electric or electret (with built-in FET source followers) can be used. Microphone arrangements are illustrated in Fig.11.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2.

Stability is ensured by two external capacitors, C6 connected between GAS1 and SLPE and C8 connected between GAS1 and V_{EE}. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The value of C8 is 10 times the value of C6. The cut-off frequency corresponds to the time constant R7 × C6.

Input MUTE (TEA1062)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligible clicking on the line and earpiece output. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independent to the DC level applied to the MUTE input.

Input $\overline{\text{MUTE}}$ (TEA1062A)

When $\overline{\text{MUTE}}$ is LOW or open-circuit, the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when $\overline{\text{MUTE}}$ is HIGH. $\overline{\text{MUTE}}$ switching causes only negligible clicking on the line and earpiece output. If the number of parallel sets in use causes a drop in line current to below 6 mA the DTMF amplifier becomes active independent to the DC level applied to the $\overline{\text{MUTE}}$ input.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled dialling tones may be sent on to the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier IR, QR and GAR

The receiving amplifier has one input (IR) and a non-inverting output (QR). Earpiece arrangements are illustrated in Fig.12. The IR to QR gain is typically 31 dB (when R4 = 100 kΩ). It can be adjusted between 20 and 31 dB to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR. The overall receive gain, between LN and QR, is calculated by subtracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 times the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 × C4.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic gain control input AGC

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}.

The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.8 dB which corresponds to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and average attenuation of 1.2 dB/km). Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.13 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line-loss compensation is required the AGC pin may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Sidetone suppression

The anti-sidetone network, R1//Z_{line}, R2, R3, R8, R9 and Z_{bal}, (see Fig.4) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R9 \times R2 = R1 \times \left(R3 + \frac{R8 \times Z_{bal}}{R8 + Z_{bal}} \right) \quad (1)$$

$$\frac{Z_{bal}}{Z_{bal} + R8} = \frac{Z_{line}}{Z_{line} + R1} \quad (2)$$

If fixed values are chosen for R1, R2, R3 and R9, then condition (1) will always be fulfilled when $|R8//Z_{bal}| << R3$.

To obtain optimum sidetone suppression, condition (2) has to be fulfilled which results in:

$$Z_{bal} = \frac{R8}{R1} \times Z_{line} = k \times Z_{line}$$

Where k is a scale factor; $k = \frac{R8}{R1}$

The scale factor k, dependent on the value of R8, is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| << R3$ fulfilling condition (a) and thus ensuring correct anti-sidetone bridge operation
- $|Z_{bal} + R8| >> R9$ to avoid influencing the transmit gain.

In practise Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

EXAMPLE

The balance impedance Z_{bal} at which the optimum suppression is present can be calculated by:

Suppose Z_{line} = 210 Ω + (1265 Ω//140 nF) representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).

When k = 0.64 then R8 = 390 Ω;
Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig.4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Figure 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication *"TEA1060 Family versatile speech transmission ICs for electronic telephone sets, order number 9398 341 10011")*.

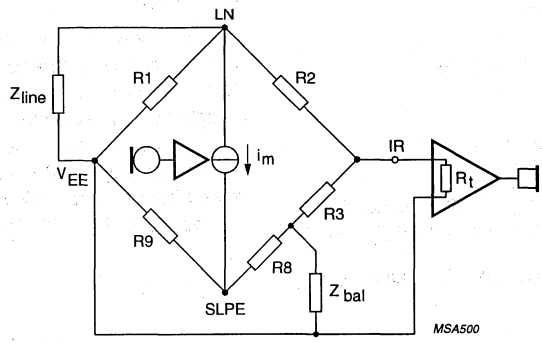


Fig.4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

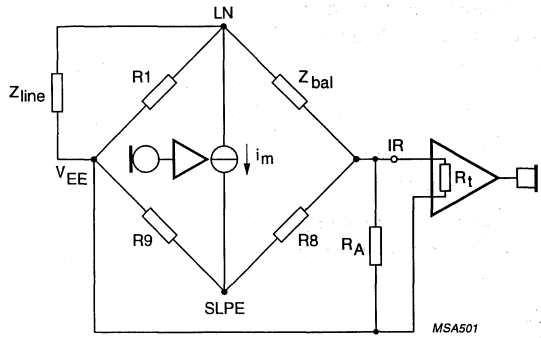


Fig.5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		–	12	V
$V_{LN(R)}$	repetitive line voltage during switch-on or line interruption		–	13.2	V
$V_{LN(RM)}$	repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; see Fig.18	–	28	V
I_{line}	line current	R9 = 20 Ω; note 1			
	TEA1062; TEA1062A		–	140	mA
	TEA1062T; TEA1062AT		–	140	mA
V_I	input voltage on all other pins	positive input voltage	–	VCC + 0.7	V
		negative input voltage	–	–0.7	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1062 (DIP16); TEA1062A		–	666	mW
	TEA1062 (IDF16)		–	617	mW
	TEA1062T; TEA1062AT		–	454	mW
T_{amb}	operating ambient temperature		–25	+75	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		–	+125	°C

Notes

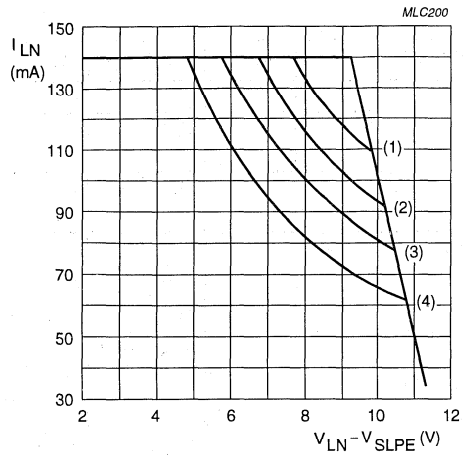
1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE (see Figs 6, 7 and 8).
2. Calculated for the maximum ambient temperature specified (T_{amb} = 75 °C) and a maximum junction temperature of 125 °C.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1062 (DIP16); TEA1062A	75	K/W
	TEA1062 (IDF16)	81	K/W
	TEA1062T; TEA1062AT (note 1)	110	K/W

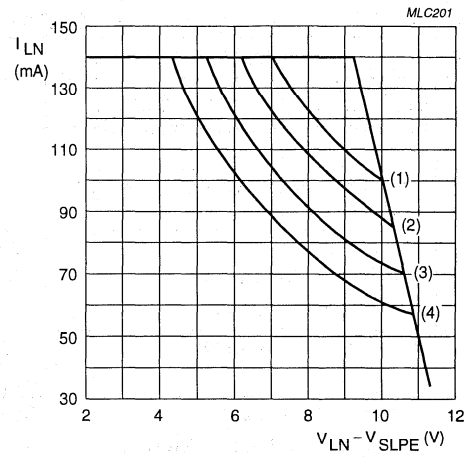
Note

1. Mounted on glass epoxy board 28.5 × 19.1 × 1.5 mm.



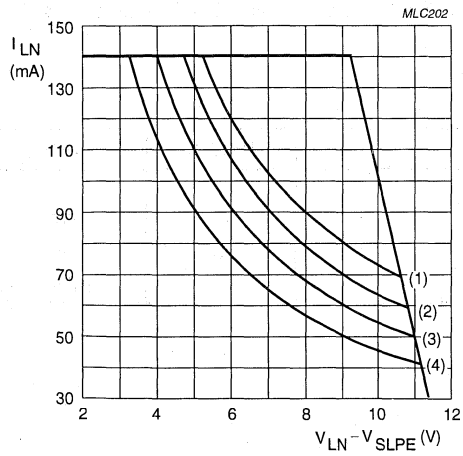
(1) T_{amb} = 45 °C; P_{tot} = 1068 mW.
(2) T_{amb} = 55 °C; P_{tot} = 934 mW.
(3) T_{amb} = 65 °C; P_{tot} = 800 mW.
(4) T_{amb} = 75 °C; P_{tot} = 666 mW.

Fig.6 TEA1062 (DIP16) and TEA1062A safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 988 mW.
(2) T_{amb} = 55 °C; P_{tot} = 864 mW.
(3) T_{amb} = 65 °C; P_{tot} = 741 mW.
(4) T_{amb} = 75 °C; P_{tot} = 617 mW.

Fig.7 TEA1062 (IDF16) safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 727 mW.
(2) T_{amb} = 55 °C; P_{tot} = 636 mW.
(3) T_{amb} = 65 °C; P_{tot} = 545 mW.
(4) T_{amb} = 75 °C; P_{tot} = 454 mW.

Fig.8 TEA1062T and TEA1062AT safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies LN and V_{CC} (pins 1 and 13)						
V_{LN}	voltage drop over circuit between LN and V_{EE}	MIC inputs open-circuit				
		I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	1.9	–	V
		I_{line} = 15 mA	3.55	4.0	4.25	V
		I_{line} = 100 mA	4.9	5.7	6.5	V
		I_{line} = 140 mA	–	–	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–	–0.3	–	mV/K
V_{LN}	voltage drop over circuit between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA				
		R_{VA} (LN to REG) = 68 kΩ	–	3.5	–	V
		R_{VA} (REG to SLPE) = 39 kΩ	–	4.5	–	V
I_{CC}	supply current	V_{CC} = 2.8 V	–	0.9	1.35	mA
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH				
	TEA1062	I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; $\overline{\text{MUTE}}$ = LOW				
	TEA1062A	I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
Microphone inputs MIC– and MIC+ (pins 6 and 7)						
$\lvert Z_i \rvert$	input impedance					
	differential	between MIC– and MIC+	–	64	–	kΩ
	single-ended	MIC– or MIC+ to V_{EE}	–	32	–	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain MIC+ or MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ	50.5	52.0	53.5	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 and +75 °C	–	±0.2	–	dB
DTMF input (pin 11)						
$\lvert Z_i \rvert$	input impedance		–	20.7	–	kΩ
G_v	voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	24.0	25.5	27.0	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	I_{line} = 50 mA; T_{amb} = –25 and +75 °C	–	±0.2	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain adjustment inputs GAS1 and GAS2 (pins 2 and 3)						
ΔG_v	transmitting amplifier gain variation by adjustment of R7 between GAS1 and GAS2		−8	−	0	dB
Sending amplifier output LN (pin 1)						
$V_{LN(rms)}$	output voltage (RMS value)	THD = 10%				
		I_{line} = 4 mA	−	0.8	−	V
		I_{line} = 15 mA	1.7	2.3	−	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC− and MIC+; psophometrically weighted (P53 curve)	−	−69	−	dBmp
Receiving amplifier input IR (pin 10)						
$\|Z_i\|$	input impedance		−	21	−	kΩ
Receiving amplifier output QR (pin 4)						
$\|Z_o\|$	output impedance		−	4	−	Ω
G_v	voltage gain from IR to QR	I_{line} = 15 mA; R_L = 300 Ω (from pin 9 to pin 4)	29.5	31	32.5	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	−	±0.2	−	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 and +75 °C	−	±0.2	−	dB
$V_{o(rms)}$	output voltage (RMS value)	THD = 2%; sine wave drive; R4 = 100 kΩ; I_{line} = 15 mA; I_p = 0 mA				
		R_L = 150 Ω	0.22	0.33	−	V
		R_L = 450 Ω	0.3	0.48	−	V
$V_{o(rms)}$	output voltage (RMS value)	THD = 10%; R4 = 100 kΩ; R_L = 150 Ω; I_{line} = 4 mA	−	15	−	mV
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted (P53 curve); R_L = 300 Ω	−	50	−	μV
Gain adjustment input GAR (pin 5)						
ΔG_v	receiving amplifier gain variation by adjustment of R4 between GAR and QR		−11	−	0	dB
Mute input (pin 12)						
V_{IH}	HIGH level input voltage		1.5	−	V_{CC}	V
V_{IL}	LOW level input voltage		−	−	0.3	V
I_{MUTE}	input current		−	8	15	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reduction of gain						
ΔG_v	MIC+ or MIC– to LN					
	TEA1062	MUTE = HIGH	–	70	–	dB
	TEA1062A	$\overline{MUTE}$ = LOW	–	70	–	dB
G_v	voltage gain from DTMF to QR	R4 = 100 kΩ; R_L = 300 Ω				
	TEA1062	MUTE = HIGH	–	–17	–	dB
	TEA1062A	$\overline{MUTE}$ = LOW	–	–17	–	dB
Automatic gain control input AGC (pin 15)						
ΔG_v	controlling the gain from IR to QR and the gain from MIC+, MIC– to LN gain control range	R6 = 110 kΩ (between AGC and V_{EE}) I_{line} = 70 mA	–	–5.8	–	dB
I_{lineH}	highest line current for maximum gain		–	23	–	mA
I_{lineL}	lowest line current for minimum gain		–	61	–	mA

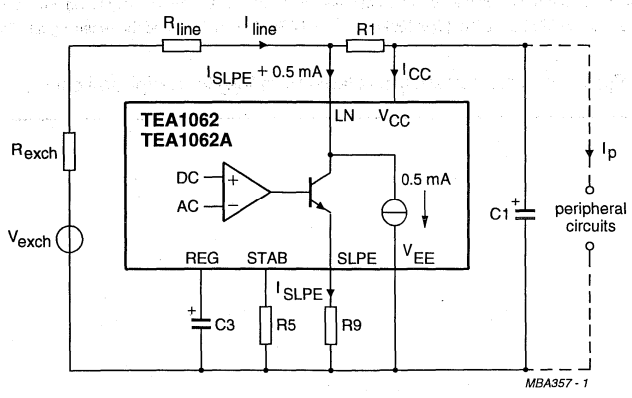
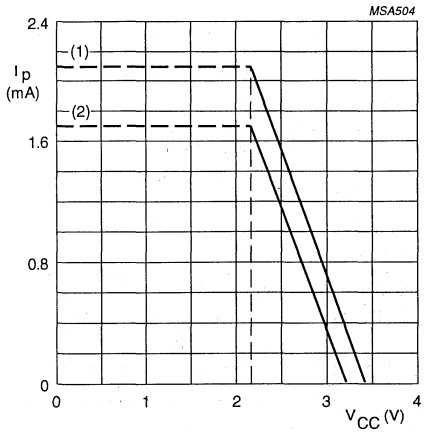


Fig.9 Supply arrangement.



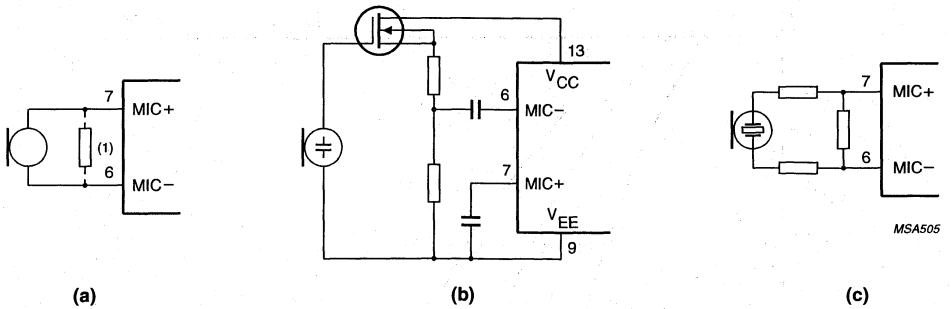
The supply possibilities can be increased by setting the voltage drop over the circuit V_{LN} to a higher value by resistor R_{VA} connected between REG and SLPE.

$V_{CC} > 2.2$ V; $I_{line} = 15$ mA at $V_{LN} = 4$ V; R1 = 620 Ω; R9 = 20 Ω.

(1) $I_p = 2.1$ mA. Curve (1) is valid when the receiving amplifier is not driven or when MUTE = HIGH (TEA1062), $\overline{MUTE}$ = LOW (TEA1062A).

(2) $I_p = 1.7$ mA. Curve (2) is valid when MUTE = LOW (TEA1062), $\overline{MUTE}$ = HIGH (TEA1062A) and the receiving amplifier is driven; $V_{o(rms)} = 150$ mV, $R_L = 150$ Ω.

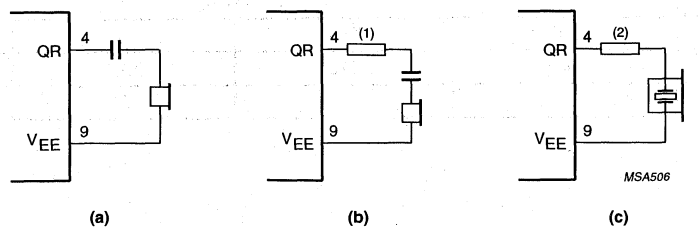
Fig.10 Typical current I_p available from V_{CC} for peripheral circuitry.



(a) Magnetic or dynamic microphone.
(b) Electret microphone.
(c) Piezo-electric microphone.

(1) Resistor may be connected to reduce the terminating impedance.

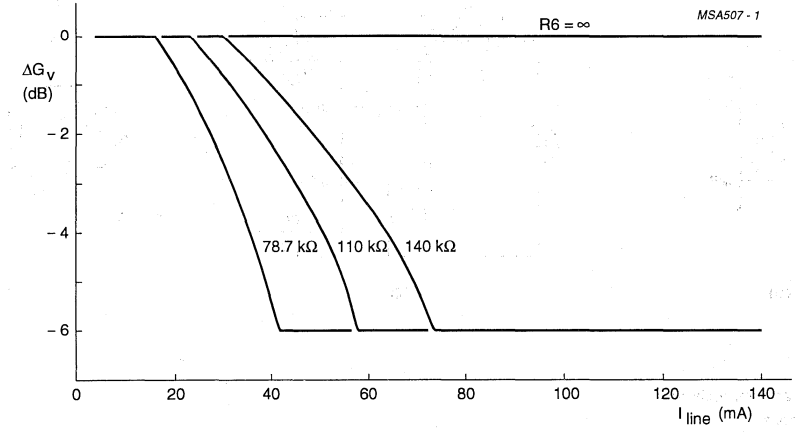
Fig.11 Alternative microphone arrangements.



(a) Dynamic earpiece.
(b) Magnetic earpiece.
(c) Piezo-electric earpiece.

(1) Resistor may be connected to prevent distortion (inductive load).
(2) Resistor is required to increase the phase margin (capacitive load).

Fig.12 Alternative receiver arrangements.

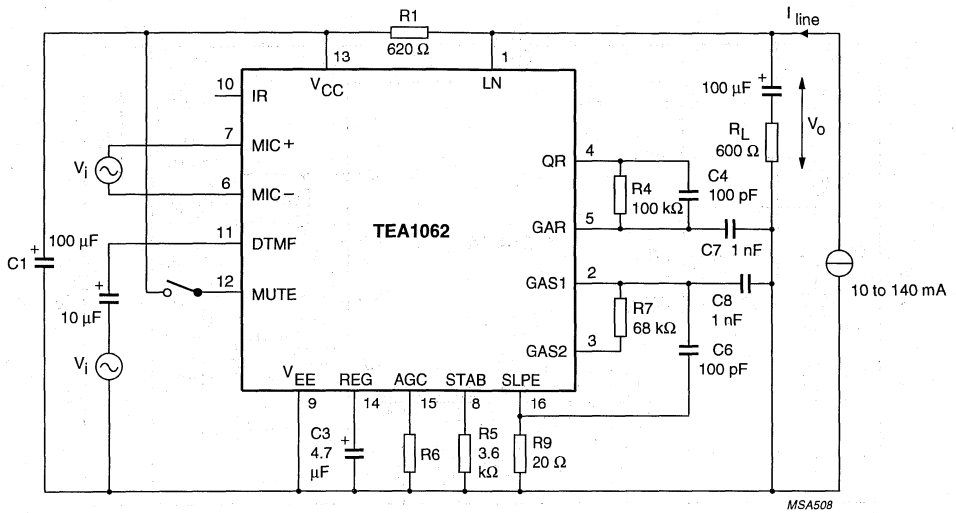


R9 = 20 Ω.

Fig.13 Variation of gain as a function of line current with R6 as a parameter.

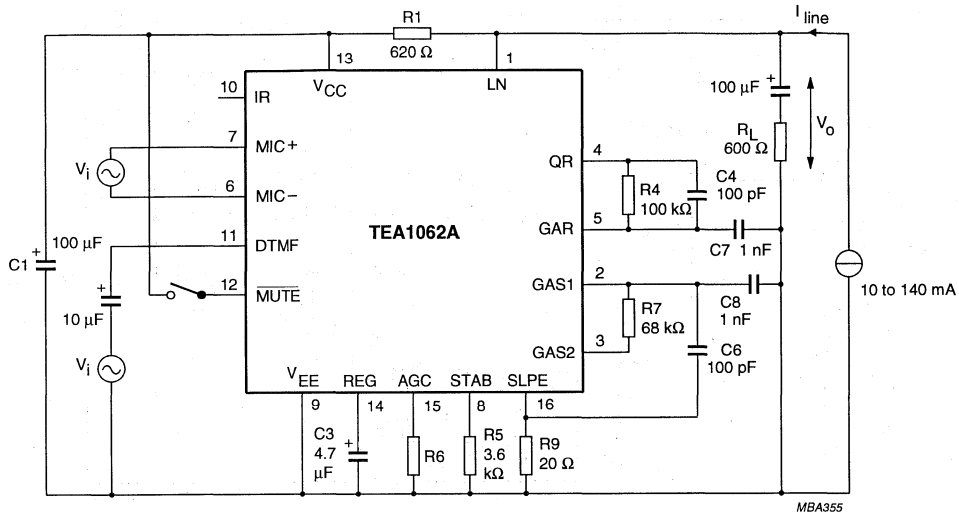
Table 1 Values of resistor R6 for optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

V_{exch} (V)	400 R_{exch} (Ω)	600 R_{exch} (Ω)	800 R_{exch} (Ω)	1000 R_{exch} (Ω)
	R6 (kΩ)			
36	100	78.7	–	–
48	140	110	93.1	82
60	–	–	120	102



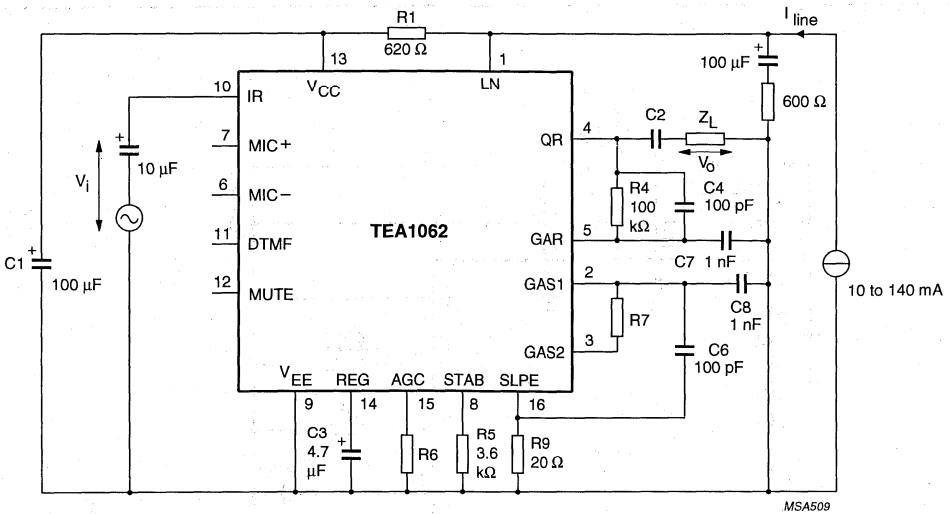
Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.
For measuring gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit.
For measuring the DTMF input, the MUTE input should be HIGH.
Inputs not being tested should be open-circuit.

Fig.14 Test circuit for defining TEA1062 voltage gain of MIC+, MIC− and DTMF inputs.



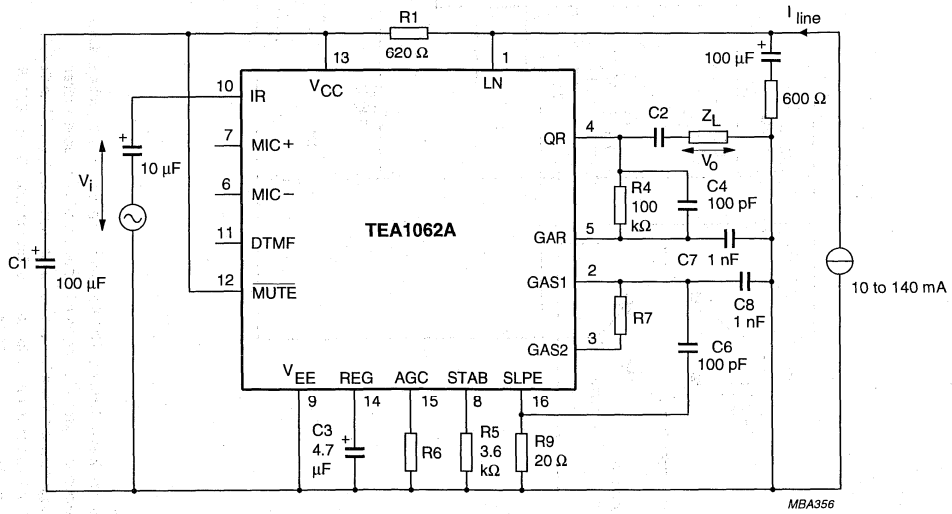
Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.
For measuring gain from MIC+ and MIC− the $\overline{\text{MUTE}}$ input should be HIGH.
For measuring the DTMF input, the $\overline{\text{MUTE}}$ input should be LOW or open-circuit.
Inputs not being tested should be open-circuit.

Fig.15 Test circuit for defining TEA1062A voltage gain of MIC+, MIC− and DTMF inputs.



Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

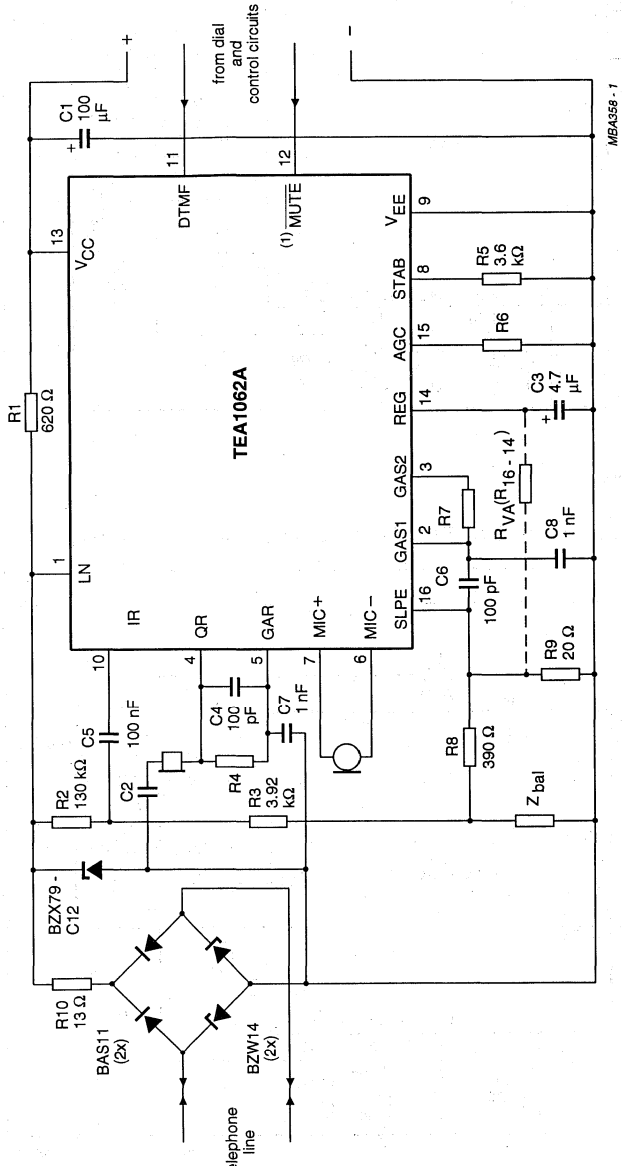
Fig.16 Test circuit for defining TEA1062 voltage gain of the receiving amplifier.



Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

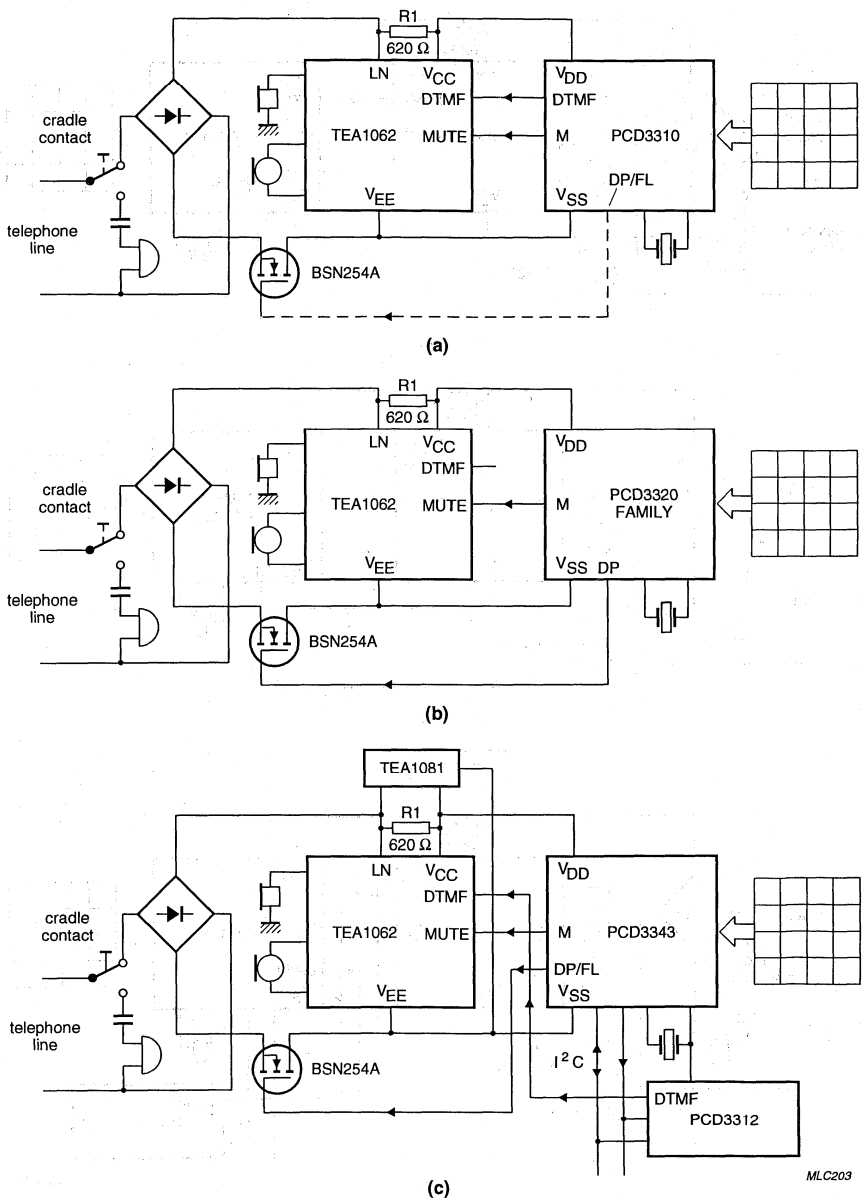
Fig.17 Test circuit for defining TEA1062A voltage gain of the receiving amplifier.

APPLICATION INFORMATION



The diode bridge, the Zener diode and R10 limit the current into, and the voltage across, the circuit during line transients.
A different protection arrangement is required for pulse dialling or register recall.
The DC line voltage can be set to a higher value by the resistor R_{VA} (REG to SLPE).
Further application information can be found in Application note *ETT/AN 89008*.
(1) Pin 12 is active HIGH (MUTE) for TEA1062.

Fig.18 Typical application of TEA1062A, with piezo-electric earpiece and DTMF dialling.

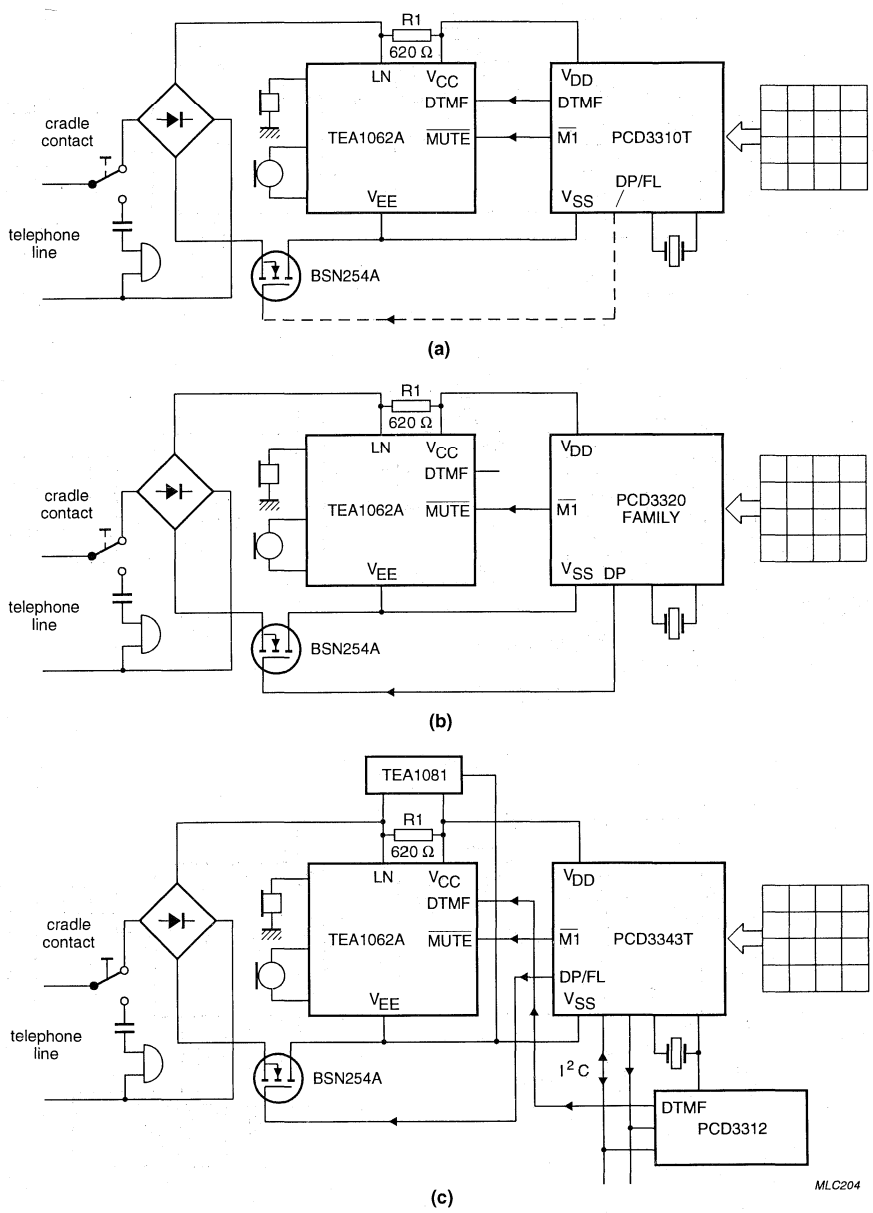


(a) DTMF pulse set with CMOS bilingual dialling circuit PCD3310. The dashed line shows an optional flash (register recall by timed loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual standard (pulse and DTMF) feature phone with the PCD3343 CMOS controller and the PCD3312 CMOS DTMF generator with I²C-bus. Supply is provided by the TEA1081 supply circuit.

Fig.19 Typical simplified applications of the TEA1062.



(a) DTMF pulse set with CMOS bilingual dialling circuit PCD3310T. The dashed line shows an optional flash (register recall by timed loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual standard (pulse and DTMF) feature phone with the PCD3343T CMOS controller and the PCD3312 CMOS DTMF generator with I²C-bus. Supply is provided by the TEA1081 supply circuit.

Fig.20 Typical simplified applications of the TEA1062A.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064A

GENERAL DESCRIPTION

The TEA1064A is a bipolar integrated circuit that performs all the speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech and has a powerful DC supply for peripheral circuits. The IC operates at line voltages down to 1.8 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel. The transmit signal on the line is dynamically limited (speech-controlled) to prevent distortion at high transmit levels of both the sending signal and the sidetone.

Features

- Low DC line voltage; operates down to 1.8 V (excluding polarity guard)
- Voltage regulator with low voltage drop and adjustable static resistance
- DC line voltage adjustment facility
- Provides a supply for external circuits in two options:
  unregulated supply, regulated line voltage;
  stabilized supply, line voltage varies with supply current
- Dynamic limiting (speech-controlled) in transmit direction prevents distortion of line signal and sidetone
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input
- Confidence tone in the earpiece during DTMF dialling
- Mute input for disabling speech during pulse or DTMF dialling
- Power-down input for improved performance during pulse dial or register recall (flash)
- Receiving amplifier for magnetic, dynamic or piezo-electric earpieces
- Large amplification setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers (not used for DTMF amplifier)
- Gain control curve adaptable to exchange supply
- Automatic disabling of the DTMF amplifier in extremely-low voltage conditions
- Microphone MUTE function available with switch

PACKAGE OUTLINES

TEA1064A : 20-lead DIL; plastic (SOT146).
TEA1064AT: 20-lead mini-pack; plastic (SO20; SOT163A).

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064A

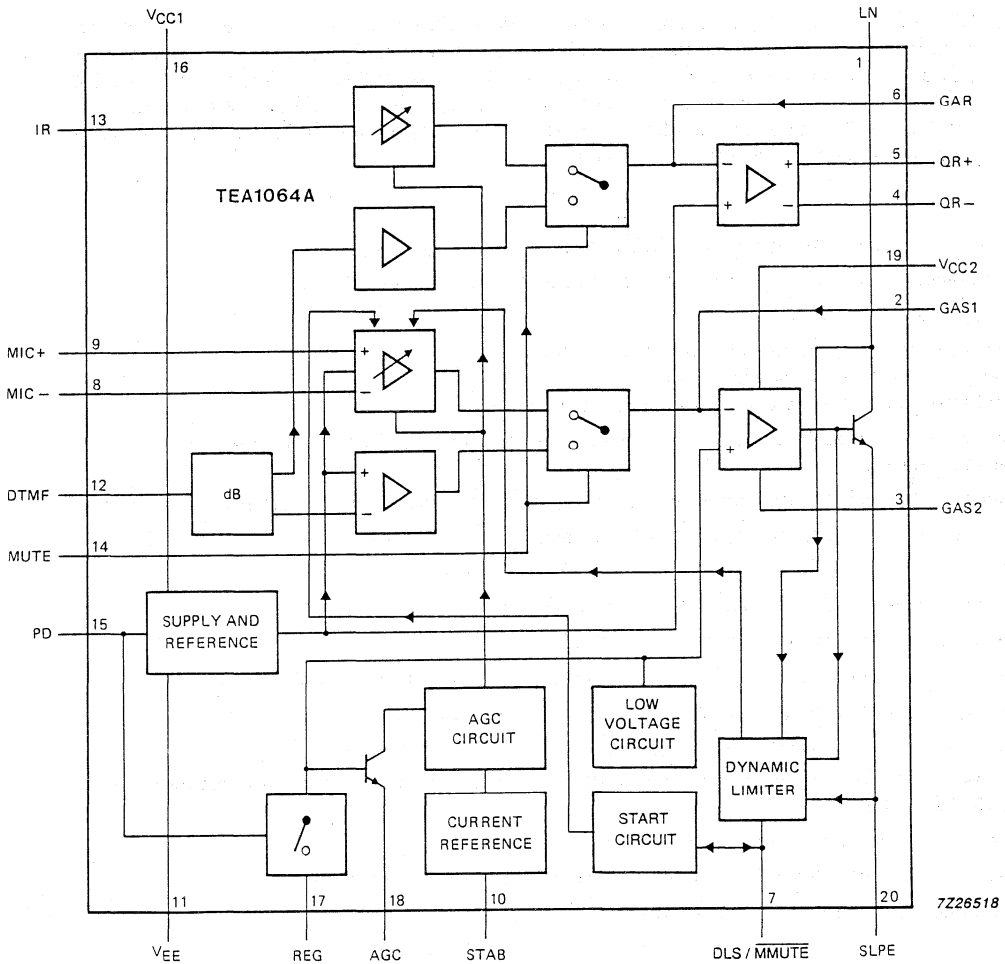


Fig. 1 Block diagram.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064A

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Operating ambient temperature range		T_{amb}	−25	–	+ 75	°C
Line current operating range:						
normal operation		I_{line}	11	–	140*	mA
with reduced performance		I_{line}	2	–	11	mA
Internal supply current:						
power-down input LOW	V_{CC1} = 2.8 V	I_{CC1}	–	1.3	1.6	mA
power-down input HIGH	V_{CC1} = 2.8 V	I_{CC1}	–	60	82	μA
Voltage gain range:						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	45	dB
Line loss compensation:						
gain control range		G_v	5.7	6.1	6.5	dB
exchange supply voltage range		V_{exch}	36	–	60	V
exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Maximum output voltage swing on LN (peak-to-peak value)	R15 + R16 = 448 Ω; I_{line} = 15 mA					
	I_p = 2 mA	$V_{LN(p-p)}$	3.7	3.95	4.2	V
	I_p = 4 mA	$V_{LN(p-p)}$	3.0	3.25	3.5	V
Regulated line voltage application						
	R15 = 0 Ω; R16 = 392 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_p = 1.4 mA	V_p	2.5	–	–	V
	I_p = 2.7 mA; $R_{REG-SLPE}$ = 20 kΩ	V_p	2.9	–	–	V
DC line voltage	I_{line} = 15 mA					
	without $R_{REG-SLPE}$	V_{LN}	–	3.57	–	V
	$R_{REG-SLPE}$ = 20 kΩ	V_{LN}	–	4.57	–	V
Stabilized supply voltage application						
	R15 = 392 Ω; R16 = 56 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_p = 0 to 4 mA	$V_{CC2-SLPE}$	3.05	3.3	3.55	V
DC line voltage	I_{line} = 15 mA					
	I_p = 2 mA	V_{LN}	4.2	4.4	4.8	V
	I_p = 4 mA	V_{LN}	4.9	5.1	5.5	V

* For TEA1064AT the maximum line current depends on the heat dissipating qualities of the mounted device.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064A

PINNING

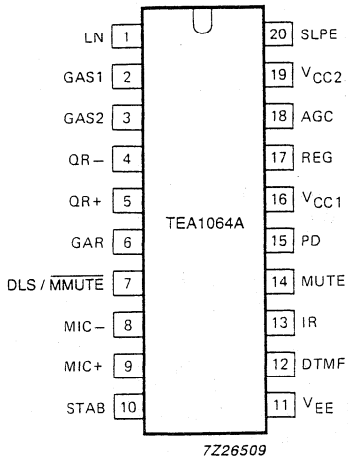


Fig. 2 Pinning diagram.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR−	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	DLS/$\overline{\text{MMUTE}}$	decoupling for transmit amplifier dynamic and microphone MUTE input
8	MIC−	inverting microphone input
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	DTMF	dual-tone multi-frequency input
13	IR	receiving amplifier input
14	MUTE	mute input
15	PD	power-down input
16	V_{CC1}	internal supply decoupling
17	REG	voltage regulator decoupling
18	AGC	automatic gain control input
19	V_{CC2}	reference voltage with respect to SLPE
20	SLPE	slope adjustment for DC curve/reference for peripheral circuits.

FUNCTIONAL DESCRIPTION

Supplies V_{CC1}, V_{CC2}, LN, SLPE, REG and STAB (Fig. 3)

Power for the TEA1064A and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC1} and regulates its voltage drop. The internal supply requires a decoupling capacitor between V_{CC1} and V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the subscriber line DC resistance R_{line} and the DC voltage (including polarity guard) on the subscriber set (see Fig. 3).

The internal voltage regulator generates a temperature-compensated reference voltage that is available between V_{CC2} and SLPE [$V_{ref} = V_{CC2\text{-}SLPE} = 3.3$ V (typ.)]. This internal voltage regulator requires decoupling by a capacitor between REG and V_{EE} (C3).

The reference voltage can be used to:

- regulate directly the line voltage (stabilized $V_{LN\text{-}SLPE} = V_{CC2\text{-}SLPE}$)*
- to stabilize the supply voltage for peripherals.

Regulated line voltage

In this application the V_{CC2} pin is connected to the LN pin as shown in Fig. 3. This configuration gives a stabilized voltage across pins LN and SLPE which, applied via the low-pass filter R16, C15, provides a supply to the peripherals that is independent of the line current and depends only on the peripheral supply current.

The value of R16 and the level of the DC voltage $V_{LN\text{-}SLPE}$ determine the supply capabilities. In the basic application R16 = 392 Ω and C15 = 220 μF. The worst-case peripheral supply current as a function of supply voltage is shown in Fig. 4. To increase the supply capabilities, the DC voltage $V_{LN\text{-}SLPE}$ can be increased by using $R_{VA(REG\text{-}SLPE)}$ or by decreasing the value of R16.

* The TEA1064A application with regulated line voltage is the same as is used for TEA1060/TEA1061, TEA1067 and TEA1068 integrated circuits.

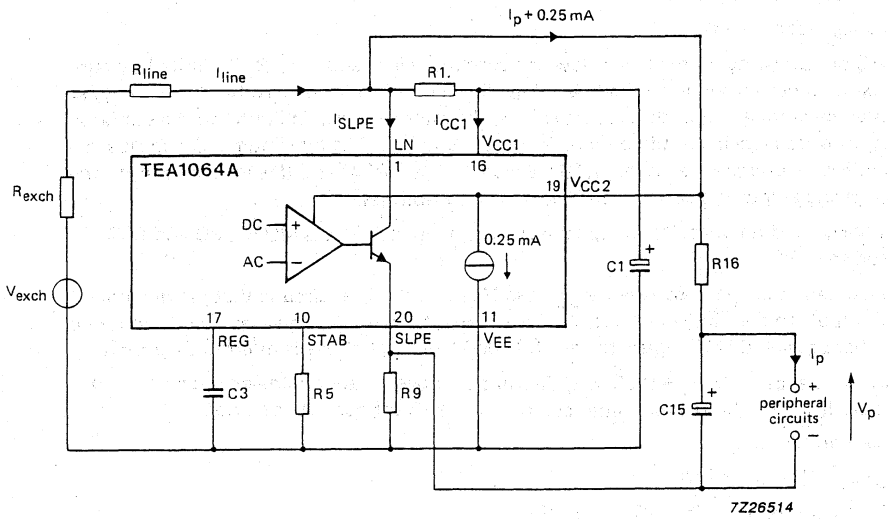


Fig. 3 Application with regulated line voltage (stabilized $V_{LN-SLPE}$). The voltage $V_{LN-SLPE}$ is fixed to V_{ref} = 3.3 ± 0.25 V. Resistor R16 together with the line current determine the supply capabilities and the maximum output swing on the line (no loop damping is necessary). The line voltage V_{LN} = V_{ref} + ([I_{line} - 1.55 mA] x R9).

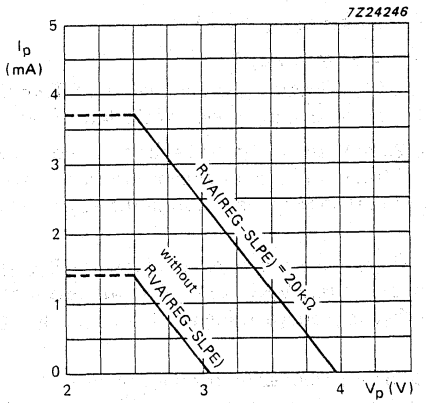


Fig. 4 Minimum supply current for peripherals (I_p) as a function of the peripheral supply voltage (V_p): I_{line} = 15 mA; R16 = 392 Ω; R15 = 0 Ω; valid for MUTE = 0 and 1. Line current has very little influence.

FUNCTIONAL DESCRIPTION (continued)

Regulated line voltage (continued)

The maximum AC output swing on the line at low line currents is influenced by R16 (limited by current) and the maximum output swing on the line at high line currents is influenced by the DC voltage $V_{LN-SLPE}$ (limited by voltage). In both these situations, the internal dynamic limiter in the sending channel prevents distortion when the microphone input is overdriven. The maximum AC output swing on LN is shown in Fig. 5; practical values for R16 are from 200 to 600 Ω and this influences both the maximum output swing at low line currents and the supply capabilities.

The SLPE pin is the ground reference for peripheral circuits, therefore inputs MUTE, PD and DTMF are also referenced to SLPE.

Active microphones can be supplied between V_{CC1} and V_{EE}. Low-power circuits that provide only MUTE and/or PD inputs to the TEA1064A also can be powered from V_{CC1}. However V_{CC1} cannot be used for circuits that provide DTMF signals to the TEA1064A because V_{CC1} is referred to ground.

If the line current I_{line} exceeds I_{CC1} + 0.25 mA, the voltage converter shunts the excess current to SLPE via LN; where $I_{CC1} \approx 1.3$ mA, the value required by the IC for normal operation.

The DC line voltage on LN is:

$$V_{LN} = V_{LN-SLPE} + (I_{SLPE} \times R9)$$

$$V_{LN} = V_{ref} + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3} A] \times R9)$$

in which

V_{ref} = 3.3 V ± 0.25 V is the internal reference voltage between V_{CC2} and SLPE; its value can be adjusted by external resistor R_{VA}

R9 = external resistor between SLPE and V_{EE} (20 Ω in basic application).

With R9 = 20 Ω, this results in:

V_{LN} = 3.57 ± 0.25 V at I_{line} = 15 mA

V_{LN} = 4.17 ± 0.3 V at I_{line} = 15 mA, $R_{VA(REG-SLPE)}$ = 33 kΩ

V_{LN} = 4.57 ± 0.35 V at I_{line} = 15 mA, $R_{VA(REG-SLPE)}$ = 20 kΩ

The preferred value for R9 is 20 Ω. Changing R9 influences microphone gain, DTMF gain, the gain control characteristics, sidetone, and the DC characteristics (especially the low voltage characteristics).

In normal conditions, $I_{SLPE} >> (I_{CC1} + 0.25$ mA) and the static behaviour is equivalent to a voltage regulator diode with an internal resistance of R9. In the audio frequency range the dynamic impedance is determined mainly by R1. The equivalent impedance of the circuit in the audio frequency range is shown in Fig. 6.

The internal reference voltage $V_{CC2-SLPE}$ can be increased by external resistor $R_{VA(REG-SLPE)}$ connected between REG and SLPE. The supply voltage $V_{CC2-SLPE}$ is shown as a function of $R_{VA(REG-SLPE)}$ in Fig. 7. Changing the reference voltage influences the output swing of both sending and receiving amplifiers.

At line currents below 8 mA (typ.), the DC voltage dropped across the circuit is adjusted to a lower level automatically (approximately 1.8 V at 2 mA). This gives the possibility of operating more telephone sets in parallel with DC line voltages (excluding polarity guard) down to an absolute minimum of 1.8 V. At line currents below 8 mA (typ.), the circuit has limited sending and receiving levels.

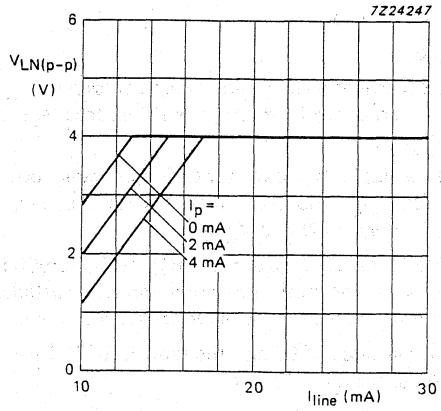


Fig. 5 Maximum AC output swing on the line as a function of line current with peripheral supply current as a parameter: R15 = 0 Ω; R16 = 392 Ω.

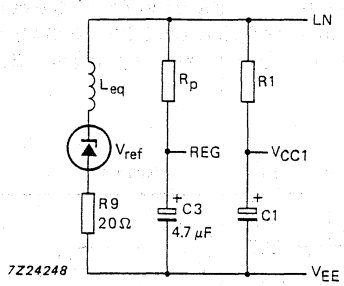


Fig. 6 Equivalent impedance between LN and V_{EE} in the application with stabilized $V_{LN-SLPE}$:
R15 = 0 Ω
L_{eq} = C3 x R9 x R_p
R_p = 15 kΩ

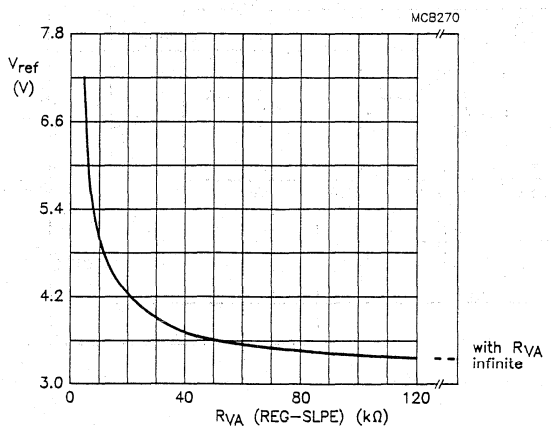


Fig. 7 Internal reference voltage $V_{CC2-SLPE}$ as a function of resistor $R_{VA(REG-SLPE)}$ for line currents between 11 and 140 mA.

In the stabilized supply application:

$$V_{LN} = V_{CC2-SLPE} + ([I_p + 0.25 \times 10^{-3}\,A] \times R15) + ([I_{line} - 1.55 \times 10^{-3}\,A] \times R9)$$

In the unregulated supply application (R15 = 0 Ω):

$$V_{LN} = V_{CC2-SLPE} + ([I_{line} - 1.55 \times 10^{-3}\,A] \times R9)$$

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage

The configuration shown in Fig. 8 provides a stabilized voltage across pins V_{CC2} and SPLE for peripheral circuits (such as dialling and control circuits); the DC voltage V_{LN} now varies with the peripheral supply current.

The $V_{CC2\text{-}SLPE}$ supply must be decoupled by capacitor C15. For stable loop operation, resistor R16 ($\approx 50\ \Omega$) is connected between V_{CC2} and SLPE in series with C15. The voltage regulator control loop is completed by resistor R15 between LN and V_{CC2}.

For sets with an impedance of 600 Ω, practical values are: R15 = 200 to 600 Ω; C15 = 220 μF; C3 = 470 nF. The ratio R15/R16 $\leqslant 8$ is for stable loop operation with sufficient phase margin, and R15/R16 $\geqslant 6$ is for satisfactory set impedance in the audio frequency range.

For sets with complex impedance, the value of C3 and the ratio R15/R16 are different (further information is given in the TEA1064A Application Report*).

The peripheral supply capability depends mainly on the available line current, the required AC output swing on the line, the maximum permitted DC voltage on the line and the values of external components (especially R15). With R15 = 392 Ω and R16 = 56 Ω (basic application) the maximum possible AC output swing on the line as a function of line current is as shown in Fig. 9, the curve parameter is the peripheral supply current (I_p). Different values for R15 (from 200 to 600 Ω) maintaining $6 < R15/R16 < 8$ give different results (these are described in the TEA1064A Application Report*).

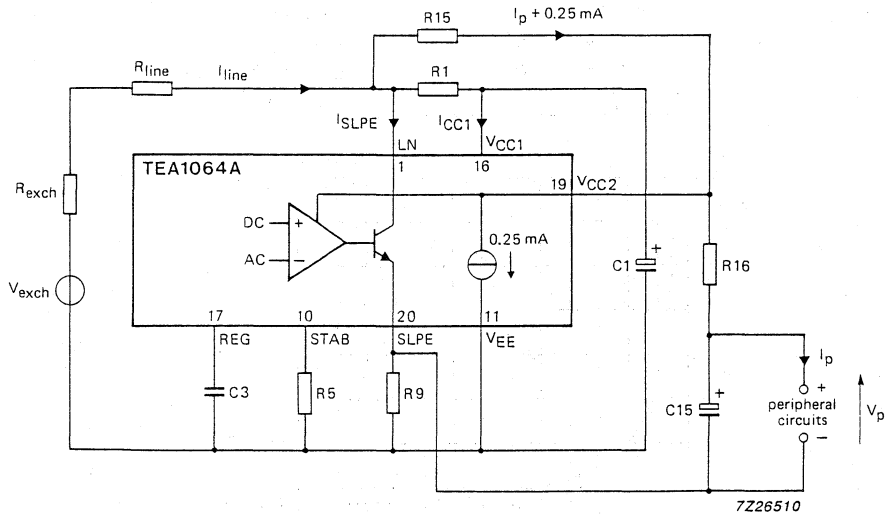


Fig. 8 Application with stabilized supply voltage for peripheral circuits: R15 = 392 Ω; R16 = 56 Ω.

* Supplied on request.

The DC line voltage on LN is

$$V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9).$$

Therefore

$$V_{LN} = V_{ref} + ([I_p + 0.25 \times 10^{-3}\,A] \times R15) + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3}\,A] \times R9)$$

in which:

V_{ref} is the internal reference voltage between V_{CC2} and SLPE (the value of V_{ref} can be adjusted by an external resistor, R_{VA}). V_{ref} = 3.3 V (typ.) without R_{VA}

I_p is the supply current used by peripheral circuits

R15 is an external resistor between LN and V_{CC2} (392 Ω in the basic application)

R9 is an external resistor between SLPE and V_{EE} (20 Ω in the basic application)

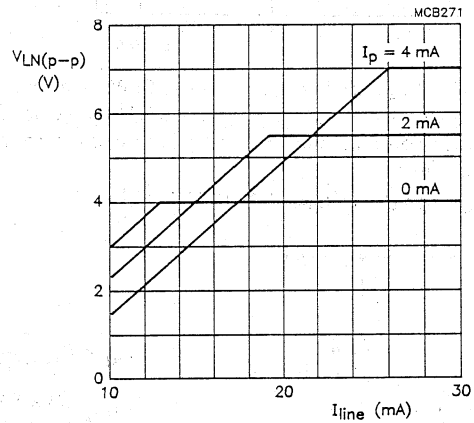


Fig. 9 Maximum output swing on line as a function of line current with the peripheral supply current as a parameter; R15 = 392 Ω; R16 = 56 Ω. As different values of R15 and R16 are allowed, different curves would then apply.

The DC voltage $V_{LN\text{-}SLPE}$ as a function of I_p with R15 as a parameter is shown in Fig. 10. In the audio frequency range, the dynamic impedance is determined mainly by R1. The equivalent impedance in the audio range of the circuit (Fig. 8) is shown in Fig. 11.

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage (continued)

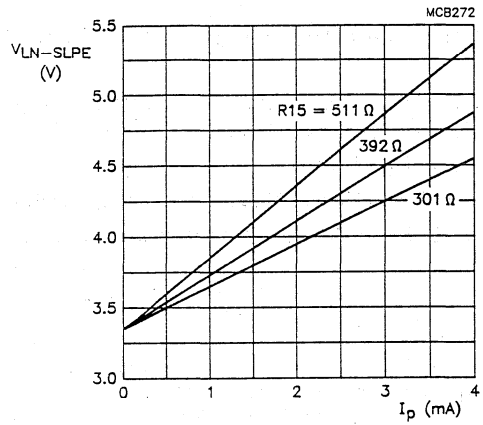
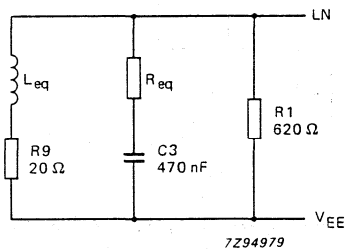


Fig. 10 Curves showing the typical voltage drop between LN and SLPE as a function of the supply current for peripherals with R15 as a parameter: $V_{CC2-SLPE}$ = 3.3 V (R_{VA} not connected). $V_{CC2-SLPE}$ can be adjusted between approximately 3.3 and 4.3 V by changing the value of R_{VA}, this results in a parallel-shift of the curves.
The total voltage drop $V_{LN} \approx V_{LN-SLPE} + ([I_{line} - 1.55\ mA] \times R9)$.



$$R_{eq} = R_p \left(\frac{R15}{R16} + 1\right)$$

$$L_{eq} = C3 \times R9 \times R_{eq}$$

with R_p = 15 kΩ

Fig. 11 Equivalent impedance between LN and V_{EE} at f > 300 Hz in the application with stabilized supply voltage for peripheral circuits.

Microphone inputs MIC+ and MIC− and gain pins GAS1 and GAS2

The TEA1064A has symmetrical microphone inputs, its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typ. 52 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezo-electric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphone types are shown in Fig. 12.

The gain of the microphone amplifier is proportional to external resistor R7 connected between GAS1 and GAS2 and with this it can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter with a cut-off frequency corresponding to the time constant R7 x C6.

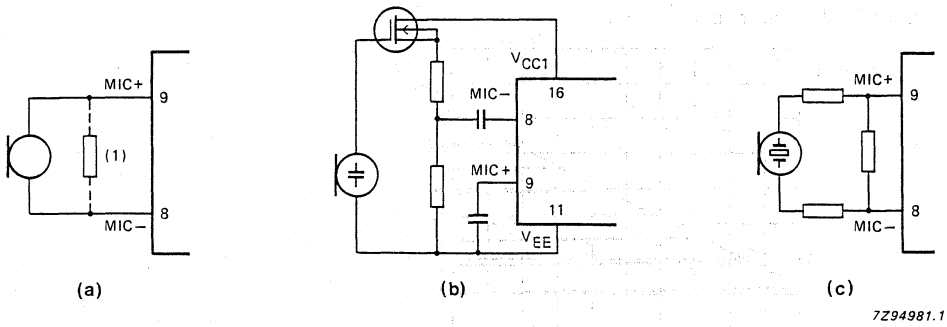


Fig. 12 Microphone arrangements: a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs; b) electret microphone; c) piezo-electric microphone.

Dynamic limiter (microphone) pin DLS/$\overline{\text{MMUTE}}$

A low level at the DLS/$\overline{\text{MMUTE}}$ pin inhibits the microphone inputs MIC+ and MIC− but has no influence on the receiving and DTMF amplifiers.
Removing the low level at the DLS/$\overline{\text{MMUTE}}$ pin provides the normal function of the microphone amplifier after a short time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ pin. The microphone mute function can be realised by a simple switch as shown in Fig.13.

To prevent distortion of the transmitted signal, the gain of the sending amplifier is reduced rapidly when peaks of the signal on the line exceed an internally-determined threshold. The time in which gain reduction is effected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ (release time).

The internal threshold adapts automatically to the DC voltage setting of the circuit (voltage $V_{LN-SLPE}$). This means that the maximum output swing on the line will be higher if the DC voltage dropped across the circuit is increased.

Fig. 14 shows the maximum possible output swing on the line as a function of the DC voltage drop ($V_{LN-SLPE}$) with $I_{line} - I_p$ as a parameter.

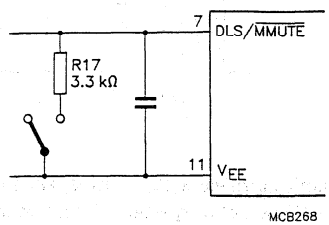


Fig. 13 Microphone-mute function.

FUNCTIONAL DESCRIPTION (continued)

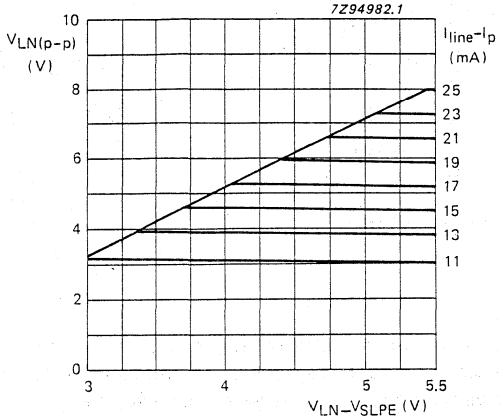


Fig. 14 Maximum output swing on line as a function of the DC voltage drop $V_{LN-SLPE}$ with $I_{line} - I_p$ as a parameter: R15 = 392 Ω; R16 = 56 Ω; or R15 = 0 Ω and R16 = 392 + 56 = 448 Ω.

The internal threshold level is lowered automatically if the DC current in the transmit output stage is insufficient. This prevents distortion of the sending signal in applications using parallel-connected telephones or telephones operating over long lines, for example.

Dynamic limiting also considerably improves sidetone performance in over-drive conditions (less distortion; limited sidetone level).

Receiving amplifier IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR− (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig. 15). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when the earpiece impedance exceeds 450 Ω as with high-impedance dynamic, magnetic or piezo-electric earpieces.

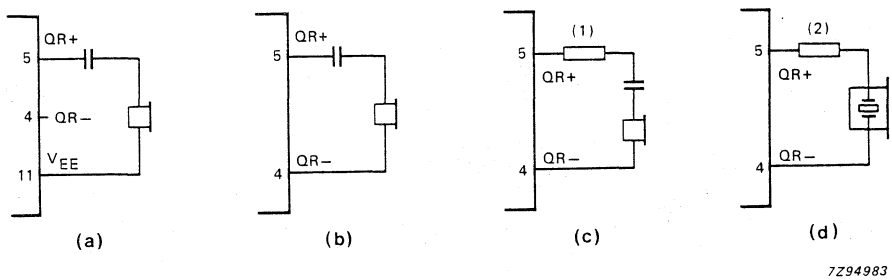


Fig. 15 Alternative receiver arrangements: a) dynamic earpiece with an impedance less than 450 Ω; b) dynamic earpiece with an impedance more than 450 Ω; c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load); d) piezo-electric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

The output voltage of the receiving amplifier is specified for continuous-wave drive. Fig. 16 shows the maximum output swing of the receiving amplifier as a function of the DC voltage drop (V_{LN}). The maximum output voltage will be higher under speech conditions, where the ratio of the peak to the RMS value is higher.

The gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer used. The adjustment range is between 20 dB and 39 dB with single-ended drive and between 26 dB and 45 dB with differential drive. The gain is proportional to the external resistor R4 connected between GAR and QR+. The overall gain between LN and QR+ can be found by subtracting the attenuation of the anti-sidetone network (32 dB) from the amplifier gain.

Two external capacitors (C4 = 100 pF and C7 = 10 x C4 = 1 nF) ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 x C4. The relationship C7 = 10 x C4 must be maintained.

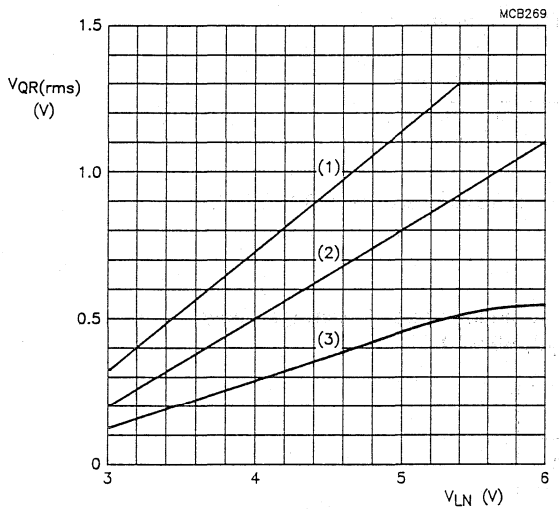


Fig. 16 Maximum output swing of the receiving amplifier as a function of DC voltage drop V_{LN} with the load at the receiver output as parameter: valid for both supply options; THD = 2%; I_{line} = 15 mA. Curve (1) is for a differential load of 47 nF (series resistance = 100 Ω); f = 3400 Hz. Curve (2) is for a differential load of 450 Ω; f = 1 kHz. Curve (3) is for a single-ended load of 150 Ω; f = 1 kHz.

Automatic gain control input AGC

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. This automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current. The control range is 6.1 dB; this corresponds to a 5 km line of 0.5 mm diameter copper twisted-pair cable (DC resistance = 176 Ω/km, average attenuation = 1.2 dB/km). The DTMF gain is not affected by this feature.

The value of R6 must be chosen with reference to the exchange supply voltage and its feeding bridge resistance (see Fig. 17 and Table 1). Different values of R6 give the same line current ratios at the start and the end of the control range. If automatic line-loss compensation is not required the AGC pin can be left open, the amplifiers then give their maximum gain.

FUNCTIONAL DESCRIPTION (continued)

Automatic gain control input AGC (continued)

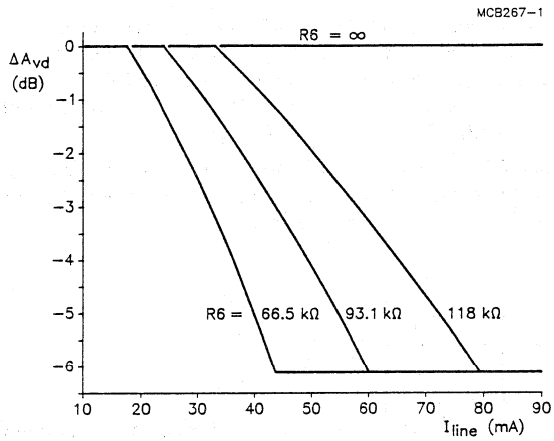


Fig. 17 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Table 1 Values of R6 giving optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	84.5	66.5	X	X
	48	118	93.1	77.8	66.5
	60	X	X	97.6	84.5

MUTE input (see notes 1 and 2)

MUTE = HIGH enables the DTMF input and inhibits the microphone and receiving amplifier inputs.

MUTE = LOW or open-circuit disables the DTMF input and enables the microphone and receiving amplifier inputs.

Switching MUTE gives negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF (see note 1)

When the DTMF input is enabled, dialling tones may be sent on to the line. The voltage gain between DTMF-SLPE and LN-V_{EE} is typ. 26 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier.
With R7 = 68 kΩ the gain is typically 26 dB.

The signalling tones can be heard in the earpiece at a low level (confidence tone).

Power-down input PD (see notes 1 and 2)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for the transmission circuit connected to V_{CC1} or for the peripherals between V_{CC2} and SLPE.
These supply gaps are bridged by the charges in the capacitors C1 and C15. The requirements on these capacitors are eased by applying a HIGH level to the PD input during the time of the loop break. This reduces the internal supply current I_{CC1} from (typ.) 1.3 mA to (typ.) 60 μA and switches off the voltage regulator to prevent discharge via LN and V_{CC2}.

A HIGH level at PD also internally disconnects the capacitor at REG so that the voltage stabilizer has no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the power-down facility is not required, the PD pin can be left open-circuit or connected to SLPE.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 18). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9 \times R2 = R1 \times (R3 + [R8//Z_{bal}])$

b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) is always fulfilled provided $|R8//Z_{bal}| \ll R3$.

To obtain optimum sidetone suppression, condition b) has to be fulfilled, resulting in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

where k is a scale factor; k = (R8/R1).

The scale factor k (value of R8) is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal};
- $|Z_{bal}//R8| \ll R3$ to fulfill condition a) and thus ensure correct anti-sidetone bridge operation;
- $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmit gain.

In practice Z_{line} varies considerably with the line length and line type. Therefore the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

The line impedance for which optimum suppression is to be obtained can be represented by 210 Ω + (1265 Ω // 140 nF). This represents a 5 km line of 0.5 mm diameter copper twisted-pair cable matched with 600 Ω (176 Ω/km; 38 nF/km).

With k = 0.64 this results in: R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω // 220 nF).

Side-tone suppression (continued)

The anti-sidetone network for the TEA1060 family shown in Fig. 18 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Alternatively a conventional Wheatstone bridge can be used as an anti-sidetone circuit (Fig. 19). Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011.)

Notes

1. The reference used for the MUTE, DTMF and PD inputs is SLPE.
2. A LOW level for any of these pins is defined by connection to SLPE, a HIGH level is defined as a voltage greater than V_{SLPE} + 1.5 V and smaller than V_{CC1} + 0.4 V.

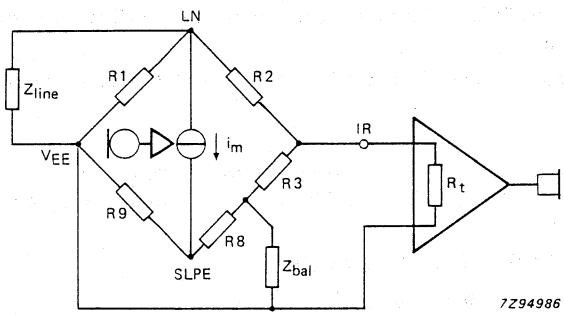


Fig. 18 Equivalent circuit of TEA1060 family anti-side-tone bridge.

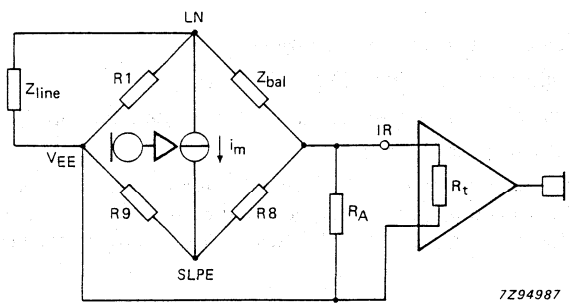


Fig. 19 Equivalent circuit of an anti-sidetone network in the Wheatstone bridge configuration.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage continuous		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage one 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 24)	V_{LN}	–	28	V
Line current TEA1064A (1)	R9 = 20 Ω	I_{LN}	–	140	mA
Line current TEA1064AT (1)	R9 = 20 Ω	I_{LN}	–	140	mA
Input voltage on pins other than LN and V_{CC2}		V_i	$V_{EE}-0.7$	$V_{CC1}+0.7$	V
Total power dissipation (2)	R9 = 20 Ω				
TEA1064A		P_{tot}	–	714	mW
TEA1064AT		P_{tot}	–	555	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

(1) Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 20 and 21 to determine the current as a function of the required voltage and the temperature.

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air

TEA1064A	$R_{th\ j\text{-}a}$	=	70	K/W
TEA1064AT mounted on glass epoxy board 41 x 19 x 1.5 mm	$R_{th\ j\text{-}a}$	=	90	K/W

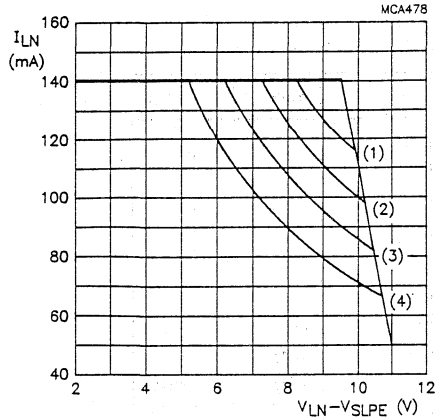


Fig. 20 TEA1064A safe operating area.

	T_{amb}	P_{tot}
(1)	45 °C	1143 mW
(2)	55 °C	1000 mW
(3)	65 °C	857 mW
(4)	75 °C	714 mW

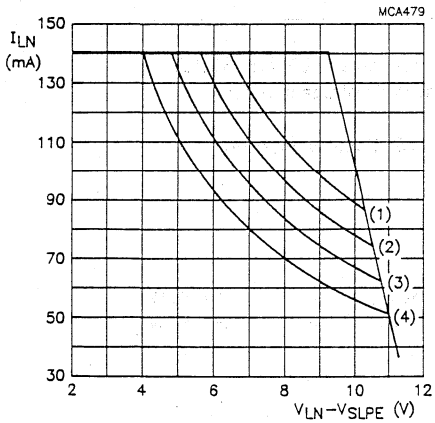


Fig. 21 TEA1064AT safe operating area.

	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R_L = 600 Ω; tested in the circuit of Fig. 22 or 23); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies LN, V_{CC1}, V_{CC2} (pins 1, 16, 19)						
Reference DC voltage between V_{CC2} and SLPE	I_{line} = 15 mA I_p = 0; 4 mA					
R_{VA} not connected		$V_{CC2-SLPE}$	3.05	3.3	3.55	V
Variation with temperature	I_{line} = 15 mA	$\frac{V_{CC2-SLPE}}{\Delta T}$	−3.0	−1.0	1.0	mV/K
Variation with line current referred to 15 mA	I_{line} = 100 mA	$\Delta V_{CC2-SLPE}$	–	60	–	mV
With R_{VA} connected between REG and SLPE	R_{VA} = 33 kΩ	$V_{CC2-SLPE}$	3.6	3.8	4.2	V
	R_{VA} = 20 kΩ	$V_{CC2-SLPE}$	3.95	4.2	4.65	V
DC line voltage: voltage drop between LN and V_{EE}	MIC−, MIC+ inputs open; R15 = 392 Ω; without R_{VA}					
at I_{line} = 15 mA	I_p = 0 mA	V_{LN}	3.4	3.6	4.0	V
	I_p = 2 mA	V_{LN}	4.2	4.4	4.8	V
	I_p = 4 mA	V_{LN}	4.9	5.1	5.5	V
at I_{line} = 100 mA	I_p = 2 mA	V_{LN}	–	6.1	7.0	V
at I_{line} = 140 mA	I_p = 2 mA	V_{LN}	–	7.0	7.8	V
Voltage drop under low current conditions	I_p = 0 mA					
	I_{line} = 2 mA	V_{LN}	–	1.8	–	V
	I_{line} = 4 mA	V_{LN}	–	2.2	–	V
	I_{line} = 7 mA	V_{LN}	–	3.2	–	V
	I_{line} = 11 mA	V_{LN}	–	3.5	–	V
Internal supply current I_{CC1}: current into pin V_{CC1}	V_{CC1} = 2.8 V					
	PD = LOW	I_{CC1}	–	1.3	1.6	mA
	PD = HIGH	I_{CC1}	–	60	82	μA
Microphone inputs MIC−, MIC+ (pins 8, 9)						
Input impedance:						
differential		Z_i	51	64	77	kΩ
single-ended		Z_i	25.5	32.0	38.5	kΩ

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Common mode rejection ratio		CMRR	–	82	–	dB
Voltage gain (see Fig. 22)	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB
Variation of G_v with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v f$	−0.5	± 0.1	+ 0.5	dB
Variation of G_v with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta G_v T$	–	± 0.2	–	dB
DTMF input (pin 12)						
Input impedance		Z_i	16.8	20.7	24.6	kΩ
Voltage gain (see Fig. 22)	I_{line} = 15 mA; R7 = 68 kΩ	G_v	25	26	27	dB
Variation of G_v with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v f$	−0.5	± 0.1	+ 0.5	dB
	f = 697 and 1633 Hz	$\Delta G_v f$	−0.2	± 0.05	+ 0.2	dB
Variation of G_v with temperature, referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta G_v T$	–	± 0.2	0.5	dB
Gain adjustment inputs GAS1, GAS2 (pins 2, 3)						
Transmitting amplifier, gain adjustment range		ΔG_v	−8	–	+ 0	dB
Sending amplifier output LN (pin 1)						
Dynamic limiter						
Output voltage swing (peak-to-peak value)	I_{line} = 15 mA; R7 = 68 kΩ; I_p = 0 mA; $V_{i(rms)}$ = 3.6 mV	$V_{LN(p-p)}$	3.6	4.0	4.5	V
Total harmonic distortion	V_i = 3.6 mV + 10 dB	THD	–	1.5	2.0	%
	V_i = 3.6 mV + 15 dB	THD	–	2.8	10.0	%
Output voltage swing (peak-to-peak value)	V_i = 3.6 mV + 10 dB					
	I_p = 2 mA	$V_{LN(p-p)}$	3.7	3.95	4.2	V
	I_p = 4 mA	$V_{LN(p-p)}$	3.0	3.25	3.5	V
	I_p = 0 mA; I_{line} = 7 mA	$V_{LN(p-p)}$	–	2	–	V
	I_p = 0 mA; I_{line} = 4 mA	$V_{LN(p-p)}$	–	1	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
LN output (continued)						
Dynamic behaviour of limiter	C16 = 470 nF					
attack time, V_{mic} jumps from 2 mV to 40 mV		t_{att}	–	1.5	5.0	ms
release time, V_{mic} jumps from 40 mV to 2 mV		t_{rel}	50	150	–	ms
Noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp
Receiving amplifier input IR (pin 13)						
Input impedance		Z_i	17	21	25	kΩ
Receiving amplifier outputs QR– QR+ (pins 4, 5)						
Output impedance	single-ended	Z_o	–	4	–	Ω
Voltage gain	Fig. 23; I_{line} = 15 mA; R4 = 100 kΩ					
single-ended; R_T = 300 Ω		G_v	30	31	32	dB
differential; R_T = 600 Ω		G_v	36	37	38	dB
Variation with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v f$	–0.5	–0.2	0	dB
Variation with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 to +75 °C	$\Delta G_v T$	–	± 0.2	–	dB
Output voltage (RMS value)	THD = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA					
single-ended; R_T = 150 Ω	I_p = 0 mA	$V_{o(rms)}$	–	0.22	–	V
	I_p = 2 mA	$V_{o(rms)}$	–	0.35	–	V
differential; R_T = 450 Ω	I_p = 0 mA	$V_{o(rms)}$	–	0.39	–	V
	I_p = 2 mA	$V_{o(rms)}$	–	0.64	–	V
differential; C_T = 47 nF; (100 Ω series resistor); f = 3400 Hz	I_p = 0 mA	$V_{o(rms)}$	–	0.57	–	V
	I_p = 2 mA	$V_{o(rms)}$	–	0.9	–	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (RMS value)	I_p = 0 mA; THD = 10%; sinewave drive; R4 = 100 kΩ; single-ended; R_T = 150 Ω;					
	I_{line} = 4 mA	$V_{o(rms)}$	–	25	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	160	–	mV
Noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve); pin IR open					
	single-ended; R_T = 300 Ω	$V_{no(rms)}$	–	45	–	μV
	differential; R_T = 600 Ω	$V_{no(rms)}$	–	90	–	μV
Noise output voltage (RMS value)	in circuit of Fig. 23; S1 in position 2; 200 Ω between MIC+ and MIC−; single-ended; R_T = 300 Ω					
	R7 = 68 kΩ	$V_{no(rms)}$	–	100	–	μV
	R7 = 24.9 kΩ	$V_{no(rms)}$	–	65	–	μV
Gain adjustment input GAR (pin 6)						
Receiving amplifier, gain adjustment range		ΔG_v	−11	–	+8	dB
MUTE INPUT (pin 14)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{mute}	–	11	20	μA
Change of microphone amplifier gain at mute-ON	MUTE = HIGH	$-\Delta G_v$	–	100	–	dB
Voltage gain from input DTMF-SLPE to QR+ output with mute-ON	MUTE = HIGH; single-ended load; R_L = 300 Ω	G_v	–	−18	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Power-down input PD (pin 15)						
Input voltage HIGH		V_{IH}	$1.5 + V_{SLPE}$	–	$V_{CC1} + 0.4$	V
Input voltage LOW		V_{IL}	0	–	$0.3 + V_{SLPE}$	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC (pin 18)						
Controlling the gain from IR (pin 13) to QR+, QR– (pins 4, 5) and the gain from MIC+, MIC– (pins 8, 9) to LN (pin 1)	R6 = 93.1 kΩ (between pins 18 and 11)					
gain control range with respect to I_{line} = 15 mA	I_{line} = 75 mA	$-G_v$	5.7	6.1	6.5	dB
Highest line current for maximum gain		I_{line}	–	24	–	mA
Lowest line current for minimum gain		I_{line}	–	61	–	mA
Change of gain between I_{line} = 15 and 35 mA		$-\Delta G_v$	0.9	1.4	1.9	dB
Microphone mute input DLS/$\overline{\text{MMUTE}}$ (pin 7)						
Input voltage low		V_{IL}	V_{EE}	–	$V_{EE} + 0.3$	V
Input current at low input voltage		I_{IL}	–85	–60	–35	μA
Release time after a low level on pin 7	C16 = 470 nF	t_{rel}	–	30	–	ms
Change of microphone amplifier gain at low input voltage on pin 7		$-\Delta G_v$	–	100	–	dB

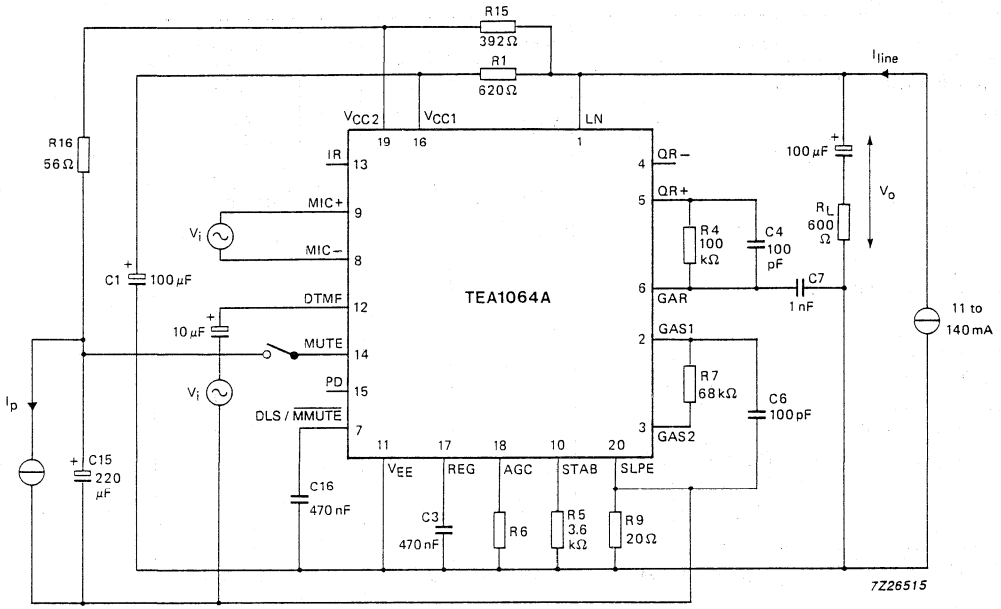


Fig. 22 Test circuit for defining voltage gain of MIC−, MIC+ and DTMF inputs; voltage gain (G_V) is defined as 20 log$|V_o/V_i|$. For measuring the gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit; for measuring the DTMF input, the MUTE input should be HIGH. Inputs not being tested should be open-circuit.

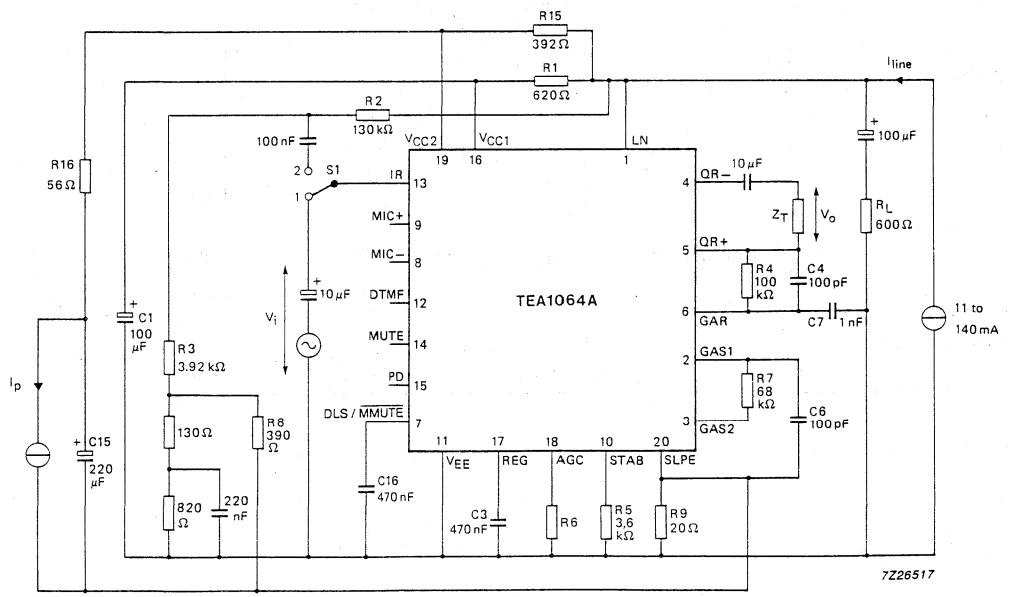


Fig. 23 Test circuit for defining voltage gain of the receiving amplifier, voltage gain (G_V) is defined as 20 log$|V_o/V_i|$ (with S1 in position 1).

APPLICATION INFORMATION

The basic application circuit is shown in Fig. 24 and some typical applications are shown in Figs 25, 26 and 27.

In the basic application, the circuit provides two possibilities for supplies to peripheral circuits:

- regulated line voltage V_{LN} (stabilized $V_{LN\text{-}SLPE}$) and unregulated supply voltage for peripheral circuits, the supply voltage is dependent only on the peripheral supply current. This application is the same as that used for TEA1060/TEA1061, TEA1067 and TEA1068;
- stabilized supply voltage for peripherals ($V_{CC2\text{-}SLPE}$), the DC line voltage depends on the current flowing to the peripheral circuits.

APPLICATION INFORMATION (continued)

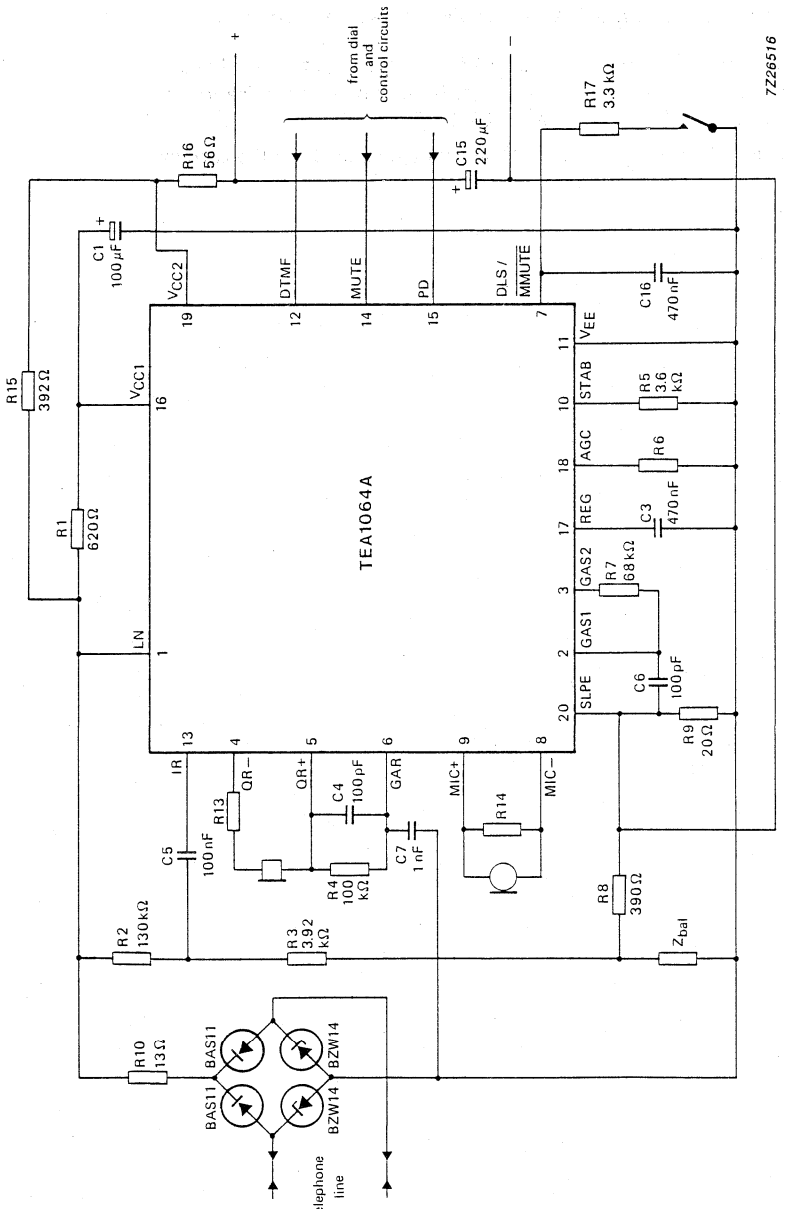


Fig. 24 Basic application of the TEA1064A with stabilized supply for peripherals, shown here with a piezo-electric earpiece and DTMF dialling. The diode bridge and R10 limit the current into, and the voltage across, the circuit during line transients. A different protection arrangement is required for pulse dialling or register recall.

For the basic application giving regulated line voltage the above circuit is changed as follows:

- R15 must be short-circuited;
- the value of R16 is changed to 392 Ω;
- the value of C3 is changed to 4.7 µF.

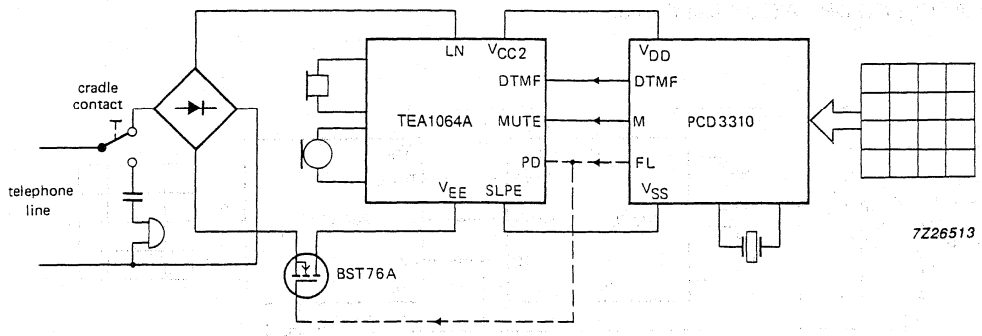


Fig. 25 Typical DTMF-pulse set application circuit (simplified) showing the TEA1064A with the CMOS bilingual dialling circuit PCD3310; the broken line indicates optional flash (register recall by timed loop break).

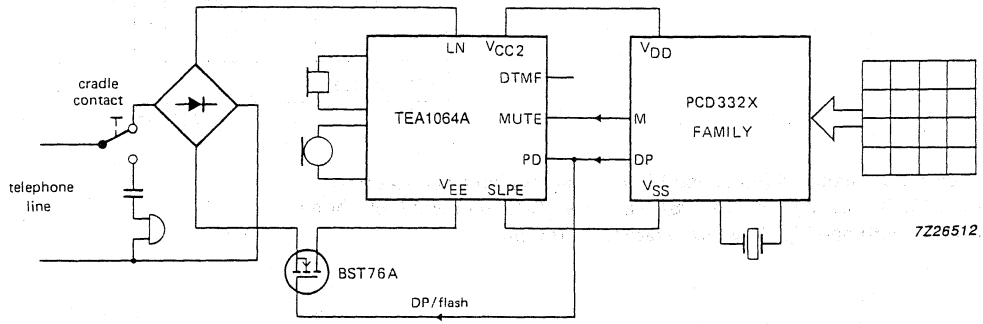


Fig. 26 Typical pulse dial set application circuit (simplified) showing the TEA1064A with one of the PCD332X family of CMOS interrupted current-loop dialling circuits.

APPLICATION INFORMATION (continued)

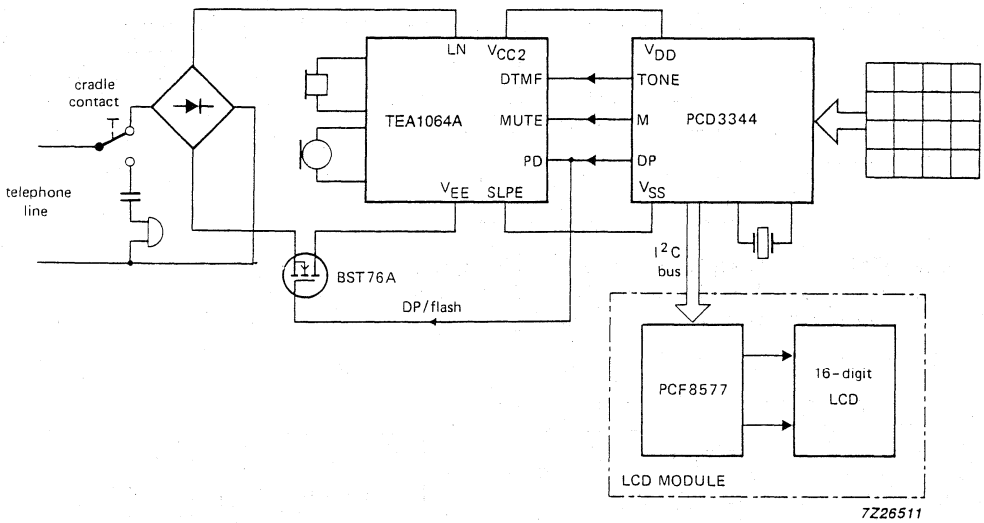


Fig. 27 Typical dual-standard (pulse and DTMF) feature phone application circuit (simplified) showing the TEA1064A and the PCD3344 CMOS telephone microcontroller with on-chip DTMF generator plus I^2C-bus.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064B

FEATURES

- Low DC line voltage; operates down to 1.8 V (excluding polarity guard)
- Voltage regulator with low voltage drop and adjustable static resistance
- DC line voltage adjustment facility
- Provides a supply for external circuits
- Dynamic limiting (speech-controlled) in transmit direction prevents distortion of line signal and sidetone
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input
- Confidence tone in the earpiece during DTMF dialling
- Mute input for disabling speech during pulse or DTMF dialling
- Power-down input for improved performance during pulse dial or register recall (flash)
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- Large amplification setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers (not used for DTMF amplifier)
- Gain control curve adaptable to exchange supply
- Automatic disabling of the DTMF amplifier in extremely-low voltage conditions
- Microphone MUTE function available with switch
- MUTE, POWER-DOWN and DTMF input reference (pin V_{EE2}) can be connected either to V_{EE1} or SLPE.

GENERAL DESCRIPTION

The TEA1064B is a bipolar integrated circuit that performs all the speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The IC operates at line voltages down to 1.8 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel. The transmit signal on the line is dynamically limited (speech-controlled) to prevent distortion at high transmit levels of both the sending signal and the sidetone.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1064B	20	DIL	plastic	SOT146
TEA1064BT	20	mini-pack	plastic	SO20; SOT163A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range					
	normal operation	note 1	11	–	140	mA
	with reduced performance		2	–	11	mA
I_{CC}	internal supply current	V_{CC} = 2.8 V				
	power-down input LOW		–	1.3	1.6	mA
	power-down input HIGH		–	60	82	µA
G_v	voltage gain range					
	microphone amplifier		44	–	52	dB
	receiving amplifier		20	–	45	dB
	line loss compensation ranges					
G_v	gain control		5.7	6.1	6.5	dB
V_{exch}	exchange supply voltage		36	–	60	V
R_{exch}	exchange feeding bridge resistance		400	–	1000	Ω
$V_{LN(p-p)}$	maximum output voltage swing on LN (peak-to-peak value)	R16 = 392 Ω; I_{line} = 15 mA				
		I_p = 1.4 mA	3.55	3.80	4.05	V
		I_p = 2.7 mA	3.25	3.50	3.75	V
V_p	supply for peripherals	I_{line} = 15 mA				
		I_p = 1.4 mA	2.5	2.7	–	V
		I_p = 2.7 mA; $R_{REG-SLPE}$ = 20 kΩ	2.9	3.1	–	V
V_{LN}	DC line voltage	I_{line} = 15 mA				
		without $R_{REG-SLPE}$	3.25	3.5	3.75	V
		$R_{REG-SLPE}$ = 20 kΩ	4.05	4.4	4.75	V
T_{amb}	operating ambient temperature range		−25	–	+75	°C

Note

1. For the TEA1064BT the maximum line current depends on the heat dissipating qualities of the mounted device.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064B

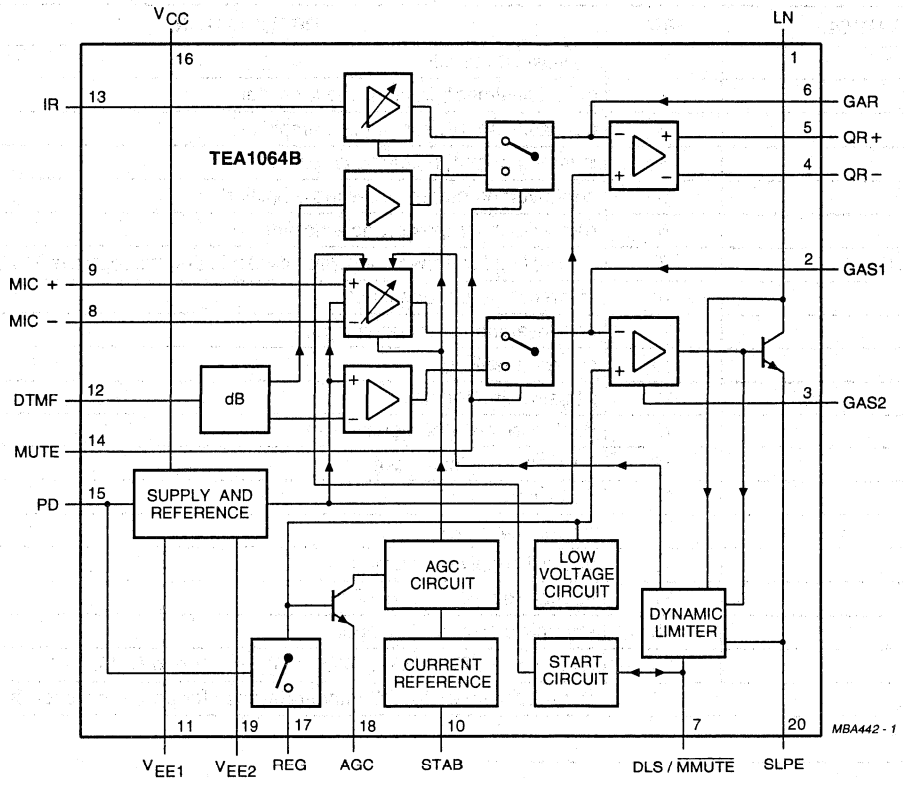


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; transmitting amplifier
GAS2	3	gain adjustment; transmitting amplifier
QR–	4	inverting output; receiving amplifier
QR+	5	non-inverting output; receiving amplifier
GAR	6	gain adjustment; receiving amplifier
DLS/$\overline{\text{MMUTE}}$	7	decoupling for transmit amplifier dynamic and microphone MUTE input
MIC–	8	inverting microphone input
MIC+	9	non-inverting microphone input
STAB	10	current stabilizer
V_{EE1}	11	negative line terminal
DTMF	12	dual-tone multi-frequency input
IR	13	receiving amplifier input
MUTE	14	mute input
PD	15	power-down input
V_{CC}	16	internal supply decoupling
REG	17	voltage regulator decoupling
AGC	18	automatic gain control input
V_{EE2}	19	reference for POWER-DOWN (PD), MUTE and DTMF
SLPE	20	slope adjustment for DC curve/reference for peripheral circuits

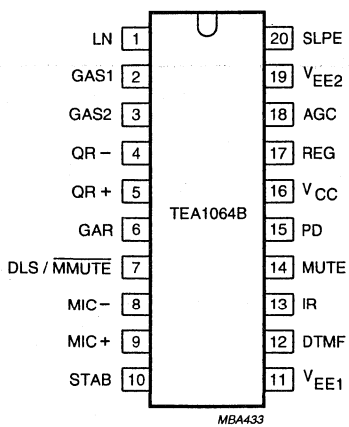


Fig.2 Pin configuration.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064B

FUNCTIONAL DESCRIPTION

Supplies V_{CC}, V_{EE2}, LN, SLPE, REG and STAB (Figs 3 and 5)

Power for the TEA1064B and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC} and regulates its voltage drop. The internal supply requires a decoupling capacitor between V_{CC} and V_{EE1}. The internal current stabilizer is set by a 3.6 kΩ resistor between STAB and V_{EE1}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the subscriber line DC resistance R_{line} and the DC voltage (including polarity guard) on the subscriber set (see Fig.3).

The internal voltage regulator generates a temperature-compensated reference voltage that is available between LN and SLPE ($V_{ref} = V_{LN-SLPE} = 3.23$ V typ.). This internal voltage regulator requires decoupling by a capacitor between REG and V_{EE1} (C3).

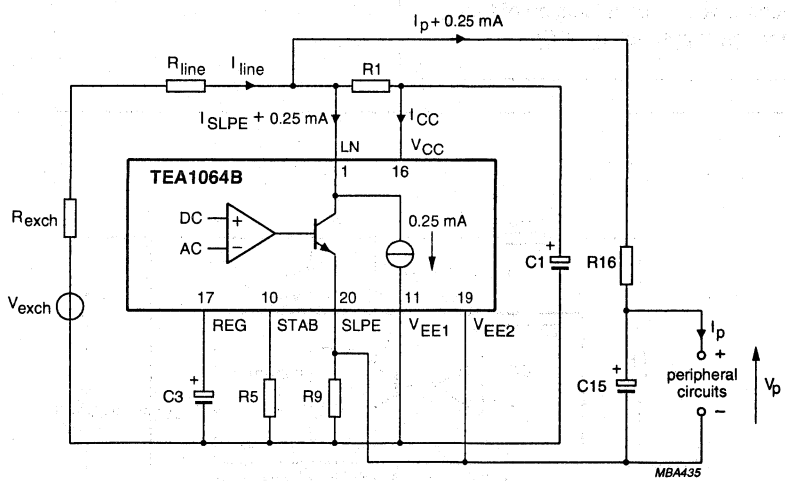
The configuration shown in Fig.3, gives a stabilized voltage across pins LN and SLPE which, applied via the low-pass filter R16, C15, provides a supply to the peripherals that is indendent of the line current and depends only on the peripheral supply current.

The value of R16 and the level of the DC voltage $V_{LN-SLPE}$ determine the supply capabilities. In the basic application R16 = 392 Ω and C15 = 220 µF. The worst-case peripheral supply current as a function of supply voltage is shown in Fig.4.

To increase the supply capabilities, the value of R16 can be decreased or the DC voltage $V_{LN-SLPE}$ can be increased by using $R_{VA(REG-SLPE)}$.

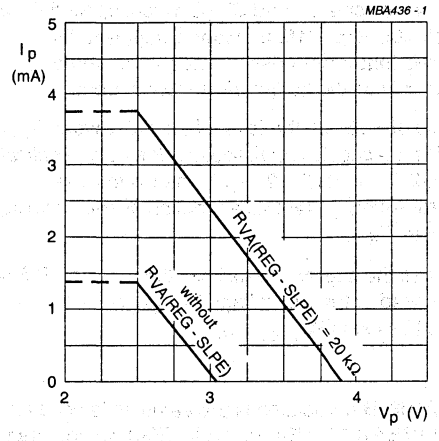
Note

The TEA1064B application is the same as is used for TEA1060/TEA1061, TEA1067 and TEA1068 integrated circuits.



The voltage $V_{LN-SLPE}$ is fixed to $V_{ref} = 3.323 \pm 0.25$ V.
Resistor R16 together with the line current determine the supply capabilities and the maximum output swing on the line (no loop damping is necessary).
The line voltage $V_{LN} = V_{ref} + (\{I_{line} - 1.55\ mA\} \times R9)$.

Fig.3 Supply arrangement with reference to SLPE.



I_{line} = 15 mA; R16 = 392 Ω; valid for MUTE = 0 and 1.
Line current has very little influence.

Fig.4 Maximum supply current with respect to Fig.3 for peripherals (I_p) as a function of the peripheral supply voltage (V_p).

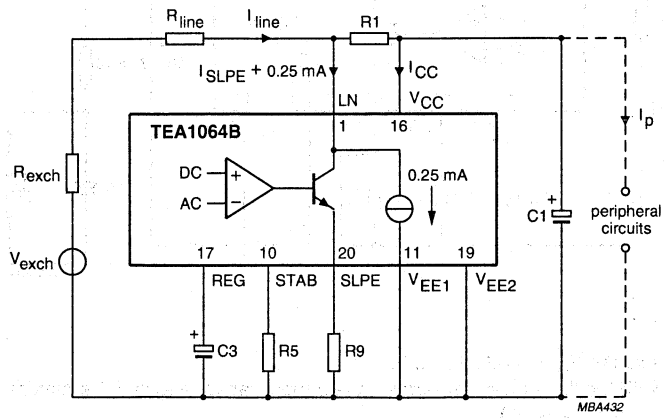
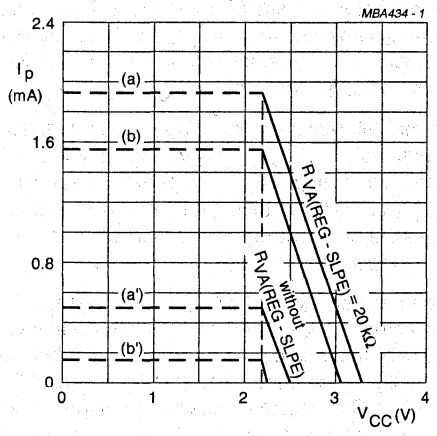


Fig.5 Supply arrangement with reference to V_{EE1}.



(a) I_p = 1.94 mA
(b) I_p = 1.54 mA
(a') I_p = 0.54 mA
(b') I_p = 0.16 mA
I_{line} = 15 mA
R1 = 620 Ω and R9 = 20 Ω
Curve (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH.
Curve (b) and (b') are valid when the receiving amplifier is driven and when MUTE = LOW.
$V_{o(RMS)}$ = 150 mV, R_T = 150 Ω.

Fig.6 Maximum current I_p with respect to Fig.5 available from V_{CC} for peripheral circuitry with V_{CC} > 2.2 V.

The maximum AC output swing on the line at low currents is influenced by R16 (limited by current) and the maximum output swing on the line at high currents is influenced by DC voltage $V_{LN-SLPE}$ (limited by voltage). In both these situations, the internal dynamic limiter in the sending channel prevents distortion when the microphone is overdriven. The maximum AC output swing on LN is shown in Fig.7; practical values for R16 are from 200 Ω to 600 Ω and this influences both maximum output swing at low line currents and the supply capabilities.

When the SLPE pin is the reference for peripheral circuits, inputs MUTE, PD and DTMF must be referenced to SLPE. This is achieved by connecting pin V_{EE2} to pin SLPE; V_{EE2} being the reference of MUTE, PD and DTMF input stages.

Active microphones can be supplied between V_{CC} and V_{EE1} as shown in Fig.5. Low power circuits that provide MUTE, PD and DTMF inputs to the TEA1064B can also be powered from V_{CC} (see Fig.6 for the supply capability of V_{CC}). MUTE, PD and DTMF are then referenced to V_{EE1} and the pin V_{EE2} must therefore be connected to V_{EE1}.
If the line current I_{line} exceeds I_{CC} + 0.25 mA, the voltage converter shunts the excess current to SLPE via LN; where $I_{CC} \approx$ 1.3 mA, the value required by the IC for normal operation.

The DC line voltage on LN is:

- $V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9)$
- $V_{LN} = V_{ref} + (\{I_{line} - I_{CC} - 0.25 \times 10^{-3}\ A\} \times R9)$

in which:

- V_{ref} = 3.23 V ± 0.25 V is the internal reference voltage between LN and SLPE; its value can be adjusted by external resistor R_{VA}.
- R9 = external resistor between SLPE and V_{EE1} (20 Ω in basic operation).

With R9 = 20 Ω, this results in:

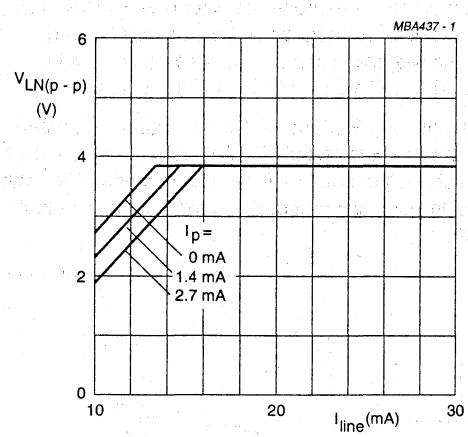
- V_{LN} = 3.3 ± 0.25 V at I_{line} = 15 mA
- V_{LN} = 4.1 ± 0.3 V at I_{line} = 15 mA, $R_{VA(REG\text{-}SLPE)}$ = 33 kΩ
- V_{LN} = 4.4 ± 0.35 V at I_{line} = 15 mA, $R_{VA(REG\text{-}SLPE)}$ = 20 kΩ

The preferred value for R9 is 20 Ω. Changing R9 influences microphone gain, DTMF gain, the gain control characteristics, sidetone and the DC characteristics (especially the low voltage characteristics).

In normal conditions, $I_{SLPE} >> (I_{CC}$ + 0.25 mA) and the static behaviour is equivalent to a voltage regulator diode with an internal resistance of R9. In the audio frequency range the dynamic impedance is determined mainly by R1. The equivalent impedance of the circuit in audio frequency range is shown in Fig.8.

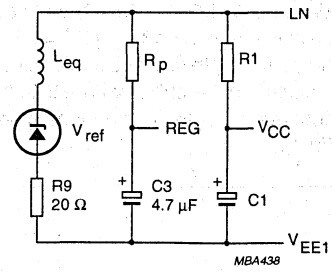
The internal reference voltage $V_{LN\text{-}SLPE}$ can be increased by external resistor $R_{VA(REG\text{-}SLPE)}$ connected between REG and SLPE. The voltage $V_{LN\text{-}SLPE}$ is shown as a function of $R_{VA(REG\text{-}SLPE)}$ in Fig.9. Changing the reference voltage influences the output swing of both sending and receiving amplifiers.

At line currents below 8 mA (typ.), the DC voltage dropped across the circuit is adjusted to a lower level automatically (approximately 1.8 V at 2 mA). This gives the possibility of operating more telephone sets in parallel with DC line voltages (excluding polarity guard) down to an absolute minimum of 1.8 V. At line currents below 8 mA (typ.), the circuit has limited sending and receiving levels.



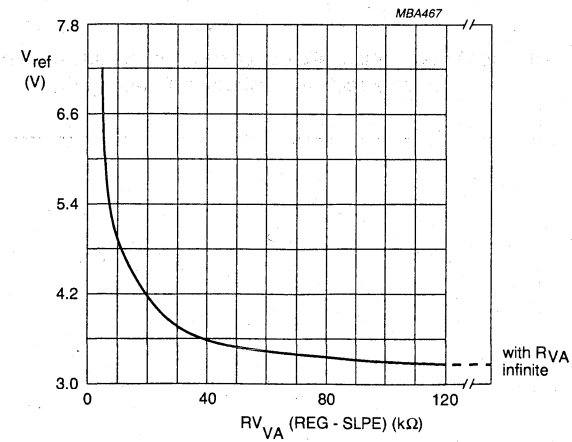
R16 = 392 Ω; I_p with respect to Fig.3.

Fig.7 Typical AC output swing at total harmonic distortion (THD) = 2% on the line as a function of line current with peripheral supply current as a parameter.



$L_{eq} = C3 \times R9 \times R_p$
R_p = 15 kΩ

Fig.8 Equivalent impedance between LN and V_{EE}.



$V_{LN} = V_{LN\text{-}SLPE} + (\{I_{line} - 1.55 \times 10^{-3}\ A\} \times R9)$.

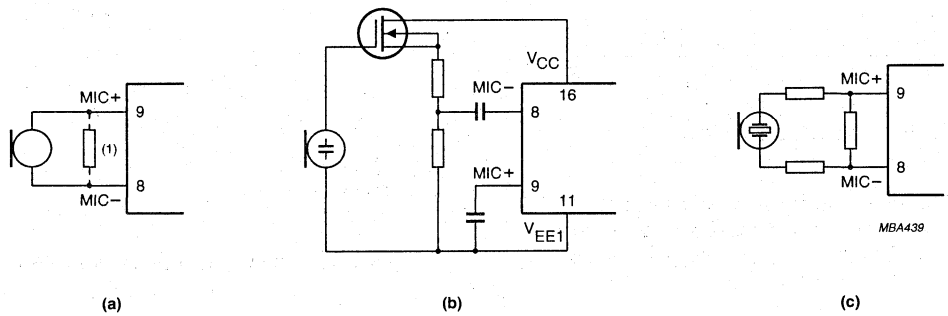
Fig.9 Internal reference voltage $V_{LN\text{-}SLPE}$ as a function of resistor $R_{VA(REG\text{-}SLPE)}$ for line currents between 11 mA and 140 mA.

Microphone inputs MIC+ and MIC– and gain pins GAS1 and GAS2

The TEA1064B has symmetrical microphone inputs, its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typicallly 52 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezo-electric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphone types are shown in Fig.10.

The gain of the microphone amplifier is proportional to external resistor R7 connected between GAS1 and GAS2 and with this it can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter with a cut-off frequency corresponding to the time constant R7 x C6.



Resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs.

Fig.10 Microphone arrangements (a) magnetic or dynamic microphone (b) electret microphone (c) piezo-electric microphone currents.

Dynamic limiter (microphone) pin DLS/$\overline{\text{MMUTE}}$

A low level at the DLS/$\overline{\text{MMUTE}}$ pin inhibits the microphone inputs MIC+ and MIC– but has no influence on the receiving and DTMF amplifiers.
Removing the low level at the DLS/$\overline{\text{MMUTE}}$ pin provides the normal function of the microphone amplifier after a short time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ pin. The microphone mute function can be realised by a simple switch as shown in Fig.11.

To prevent distortion of the transmitted signal, the gain of the sending amplifier is reduced rapidly when peaks of the signal on the line exceed an internally-determined threshold. The time in which gain reduction is effected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a a time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ (release time).

The internal threshold adapts automatically to the DC voltage setting of the circuit ($V_{LN\text{-}SLPE}$). This means that the maximum output swing on the line will be higher if the DC voltage dropped across the circuit is increased. Fig.12 shows the maximum possible output swing on the line as a function of the DC voltage drop ($V_{LN\text{-}SLPE}$) with I_{line} -I_p as a parameter.

The internal threshold level is lowered automatically if the DC current in the transmit output stage is insufficient. This prevents distortion of the sending signal in applications using parallel-connected telephones or telephones operating over long lines, for example.

Dynamic limiting also considerably improves sidetone performance in over-drive conditions (less distortion; limited sidetone level).

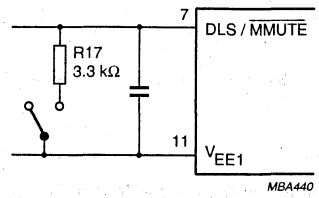
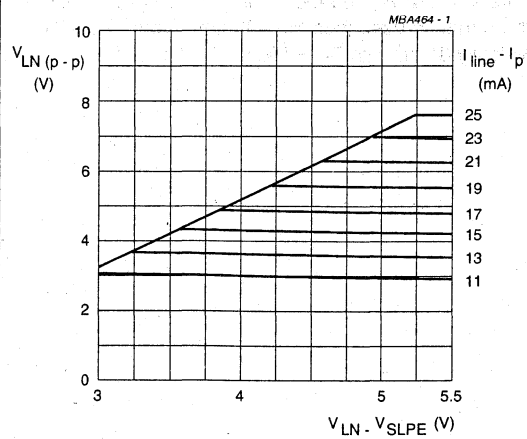
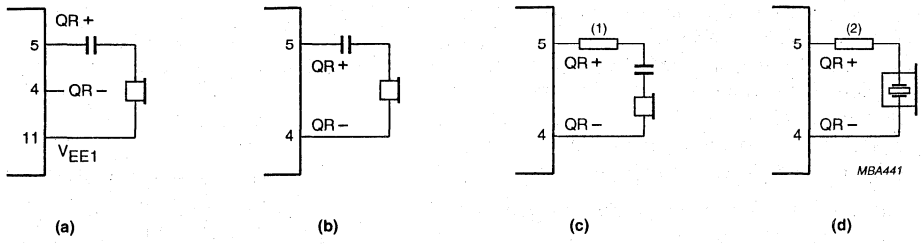


Fig.11 Microphone-mute function.



R16 = 392 Ω.

Fig.12 Typical output swing on line as a function of the DC voltage drop $V_{LN\text{-}SLPE}$ with I_{line} - I_p as a parameter.

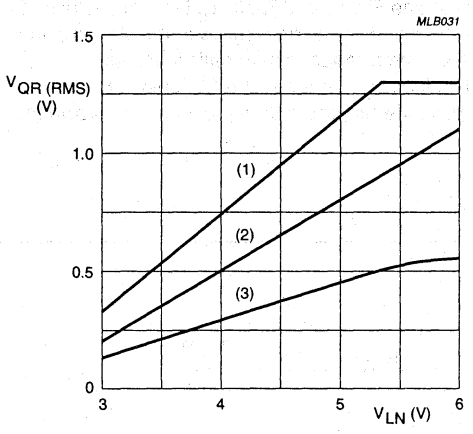


Resistor (1) may be connected to prevent distortion (inductive load).
Resistor (2) is required to increase the phase margin (stability with capacitive load).

Fig.13 Alternative receiver arrangements (a) dynamic earpiece with an impedance less than 450 Ω (b) dynamic earpiece with an impedance more than 450 Ω (c) magnetic earpiece with an impedance more than 450 Ω (d) piezo-electric earpiece.

Receiving amplifier IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complimentary outputs, QR+ (non-inverting) and QR− (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig.13). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when the earpiece impedance exceeds 450 Ω as with high-impedance dynamic, magnetic or piezo-electric earpieces.



Valid for both options; THD = 2%; I_{line} = 15 mA.
Curve (1) is for a differential load of 47 nF (series resistance = 100 Ω; f = 3400 Hz.
Curve (2) is for a differential load of 450 Ω; f = 1 kHz.
Curve (3) is for a single-ended load of 150 Ω; f = 1 kHz.

Fig.14 Typical output swing of the receiving amplifier as a function of DC voltage drop V_{LN} with the load at the receiver output as parameter.

The output voltage of the receiving amplifier is specified for continuous-wave drive. Fig.14 shows the maximum output swing of the receiving amplifier as a function of the DC voltage drop (V_{LN}). The maximum output voltage will be higher under speech conditions, where the ratio of the peak to the RMS value is higher.

The gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer used. The adjustment range is between 20 dB and 39 dB with single-ended drive and between 26 dB and 45 dB with differential drive. The gain is proportional to the external resistor R4 connected between GAR and QR+. The overall gain between LN and QR+ can be found by subtracting the attenuation of the anti-sidetone network (32 dB) from the amplifier gain.

Two external capacitors (C4 = 100 pF and C7 = 10 x C4 = 1 nF) ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with time constant R4 x C4. The relationship C7 = 10 x C4 must be maintained.

Automatic gain control input AGC

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE1}. This automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current. The control range is 6.1 dB; this corresponds to a 5 km line of 0.5 dB diameter copper twisted-pair cable (DC resistance = 176 Ω/km, average attenuation = 1.2 dB/km). The DTMF gain is not affected by this feature.

The value of R6 must be chosen with reference to the exchange supply voltage and its feeding bridge resistance (see Fig.15 and Table 1). Different values of R6 give the same line current ratios at the start and the end of the control range. If automatic line-loss compensation is not required the AGC pin can be left open-circuit, the amplifiers then provide their maximum gain.

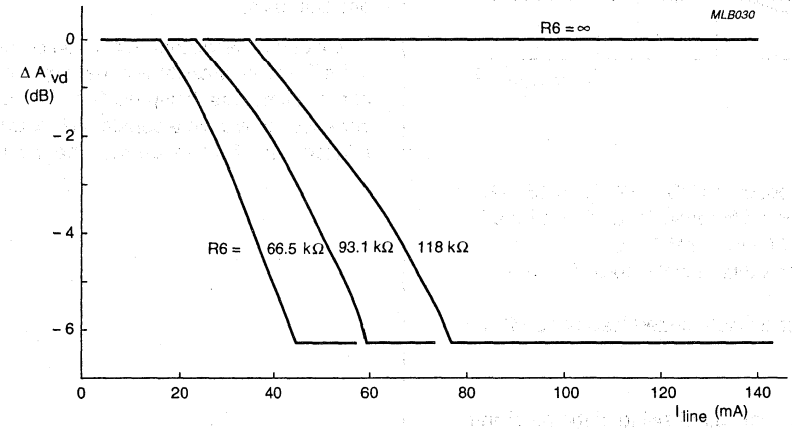


Fig.15 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Table 1 Values of R6 giving optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	35	84.5	66.5	x	x
	48	118	93.1	77.8	66.5
	60	x	x	97.6	84.5

V_{EE2} input

V_{EE2} is the reference for MUTE, POWER-DOWN and DTMF inputs. These signals are referenced to V_{EE1} when generated by peripherals powered between V_{CC} and V_{EE1}, but they can also be referenced to SLPE when peripherals are powered as shown in Fig.3. In the first instance (reference to V_{EE1}), V_{EE2} has to be connected to V_{EE1}. In the second instance (reference to SLPE), V_{EE2} has to be connected to SLPE.

MUTE input (see notes 1 and 2)

MUTE = HIGH enables the DTMF input and inhibits the microphone and receiving amplifier inputs.

MUTE = LOW or open-circuit disables the DTMF input and enables the microphone and receiving amplifier inputs.

Switching MUTE gives negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF (see note 1)

When the DTMF input is enabled, dialling tones may be sent on the line. The voltage gain between DTMF-V_{EE2} and LN-V_{EE1} is typically 26.5 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier.
With R7 = 68 kΩ the gain is typically 25.5 dB.

The signalling tones can be heard in the earpiece at a low level (confidence tone).

Power-down input PD (see notes 1 and 2)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for the transmission circuit connected to V_{CC} or for the peripherals between V_{LN} and SLPE. These supply gaps are bridged by the charges in the capacitors C1 and C15. The requirements on these capacitors are eased by an applied HIGH level to the PD input during the time of the loop break. This reduces the internal supply current I_{CC1} from 1.3 mA (typ.) to 60 µA (typ.) and switches off the voltage regulator to prevent discharge via LN to V_{CC2}.

A HIGH level at PD also internally disconnects the capacitor at REG so that the voltage stabilizer has no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the power-down facility is not required, the PD pin can be left open-circuit or connected to V_{EE2}.

Sidetone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig.16). Maximum compensation is obtained when the following conditions are fulfilled:

(a) $R9 \times R2 = R1 \times (R3 + \{R8//Z_{bal}\})$

(b) $(Z_{bal}/\{Z_{bal} + R8\}) = (Z_{line}/\{Z_{line} + R1\})$

If fixed values are chosen for R1, R2, R3 and R9, then condition (a) is always fulfilled provided $|R8//Z_{bal}| \ll R3$

To obtain optimum sidetone suppression, condition (b) has to be fulfilled, resulting in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

Where k is a scale factor; k = (R8/R1).

The scale factor k (value of R8) is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensure correct anti-sidetone bridge operation
- $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmit gain

In practise Z_{line} varies considerably with the line length and line type. Therefore the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

EXAMPLE

The line impedance for which optimum suppression is to be obtained can be represented by 210 Ω + (1265 Ω//140 nF). This represents a 5 km line of 0.5 mm diameter copper twisted-pair cable matched with 600 Ω (176 Ω/km; 38 nF/km).

With k = 0.64 this results in : R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig.16 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Alternatively a conventional Wheatstone bridge can be used as an anti-sidetone circuit (see Fig.17). Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011).

Notes

1. The reference level used for the MUTE, DTMF and PD inputs is V_{EE2}.
2. A LOW level for any of these pins is defined by connection to V_{EE2}, a HIGH level is defined as a voltage greater than V_{EE2} + 1.5 V and smaller than V_{CC} + 0.4 V.

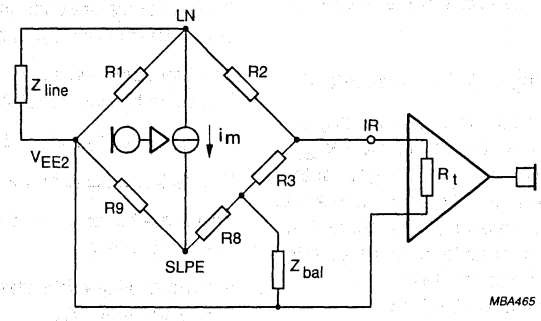


Fig.16 Equivalent circuit of TEA1060 family anti-sidetone bridge.

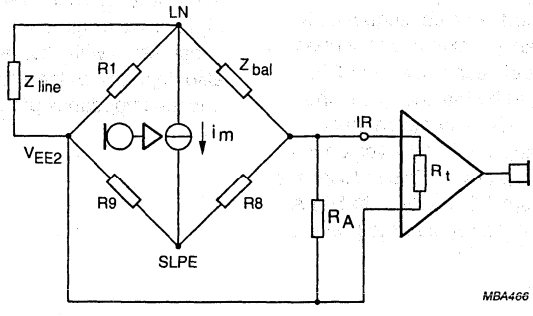


Fig.17 Equivalent circuit of an anti-sidetone network in the Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage continuous		–	12	V
V_{LN}	repetitive line voltage during switch-on line interruption		–	13.2	V
V_{LN}	repetitive peak line voltage one 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; see Fig.22	–	28	V
I_{LN}	line current	R9 = 20 Ω			
	TEA1064B	note 1	–	140	mA
	TEA1064BT	note 1	–	140	mA
V_i	input voltage on pins other than LN		V_{EE1}–0.7	V_{CC}+0.7	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1064B		–	717	mW
	TEA1064BT		–	555	mW
T_{amb}	operating ambient temperature		–25	+75	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		–	+125	°C

Notes

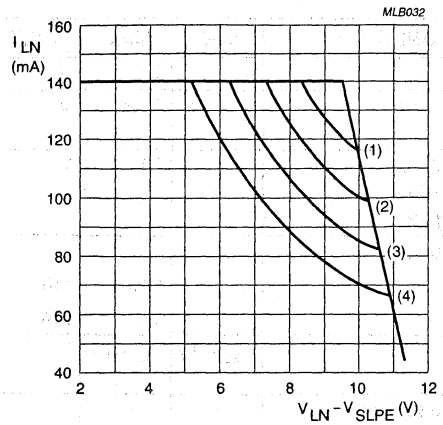
1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs18 and 19 to determine the current as a function of the required voltage and the temperature.
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT146	70 K/W
	SOT163A (note 1)	90 K/W

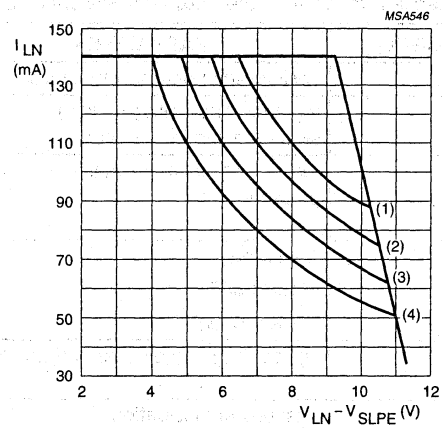
Note

1. Mounted on glass epoxy board 41 x 19 x 1.5 mm.



(1) T_{amb} = 45 °C; P_{tot} = 1143 mW.
(2) T_{amb} = 55 °C; P_{tot} = 1000 mW.
(3) T_{amb} = 65 °C; P_{tot} = 857 mW.
(4) T_{amb} = 75 °C; P_{tot} = 714 mW.

Fig.18 TEA1064B safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 888 mW.
(2) T_{amb} = 55 °C; P_{tot} = 777 mW.
(3) T_{amb} = 65 °C; P_{tot} = 666 mW.
(4) T_{amb} = 75 °C; P_{tot} = 555 mW.

Fig.19 TEA1064BT safe operating area.

CHARACTERISTICS

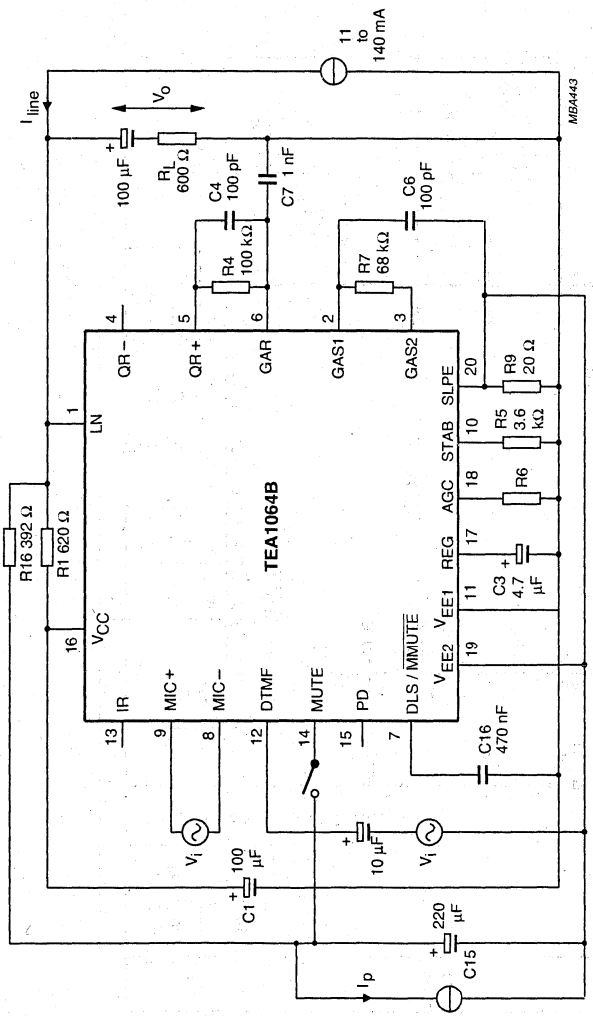
I_{line} = 11 to 140 mA; V_{EE1} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R_L = 600 Ω; tested in the circuits of Fig.20 or Fig.21; V_{EE2} connected to SLPE; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies LN and V_{CC} (pins 1 and 16)						
V_{LN}	DC line voltage: voltage drop between LN and V_{EE1}	MIC–, MIC+ inputs open-circuit; without R_{VA}				
		I_{line} = 2 mA	–	1.8	–	V
		I_{line} = 4 mA	–	2.2	–	V
		I_{line} = 7 mA	–	3.2	–	V
		I_{line} = 11 mA	–	3.4	–	V
		I_{line} = 15 mA	3.25	3.5	3.75	V
		I_{line} = 100 mA	–	5.25	6.05	V
		I_{line} = 140 mA	–	6.1	7.0	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–3	–1	+1	mV/K
V_{LN}	voltage drop over circuit with R_{VA} connected between REG and SLPE					
		R_{VA} = 33 kΩ	3.8	4.1	4.4	V
		R_{VA} = 20 kΩ	4.05	4.4	4.75	V
I_{CC}	internal supply current into pin 16	V_{CC} = 2.8 V				
		PD = LOW	–	1.3	1.6	mA
		PD = HIGH	–	60	82	μA
V_{CC}	supply voltage available for peripheral circuitry V_{EE2} connected to V_{EE1}	I_{line} = 15 mA; MUTE = HIGH; see Fig.5				
		I_p = 0.54 mA	2.2	2.4	–	V
		I_p = 0 mA	2.5	2.7	–	V
V_p	supply voltage available for peripheral circuitry	I_{line} = 15 mA				
		I_p = 1.4 mA	2.5	2.7	–	V
		I_p = 2.7 mA; $R_{REG-SLPE}$ = 20 kΩ	2.9	3.1	–	V
Microphone inputs MIC– and MIC+ (pins 8 and 9)						
Z_i	input impedance					
	differential		51	64	77	kΩ
	single-ended		25.5	32.0	38.5	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain (see Fig.20)	I_{line} = 15 mA; R7 = 68 kΩ	51	52	53	dB
$\Delta G_v f$	variation of G_v with frequency referred to 0.8 kHz	f = 300 and 3400 Hz	–0.5	±0.1	+0.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta G_v T$	variation of G_v with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to +75 °C	–	±0.2	–	dB
DTMF input (pin 12)						
Z_i	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain (see Fig.20)	I_{line} = 15 mA; R7 = 68 kΩ	24.5	25.5	26.5	dB
$\Delta G_v f$	variation of G_v with frequency referred to 0.8 kHz					
		f = 300 and 3400 Hz	−0.5	±0.01	+0.5	dB
		f = 697 and 1633 Hz	−0.2	±0.05	+0.2	dB
$\Delta G_v T$	variation of G_v with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to +75 °C	–	±0.2	0.5	dB
Gain adjustment inputs GAS1 and GAS2 (pins 2 and 3)						
ΔG_v	transmitting amplifier gain adjustment range		−8	–	+0	dB
Sending amplifier output LN (pin 1)						
DYNAMIC LIMITER						
$V_{LN(p-p)}$	output voltage swing (peak-to-peak value)	I_{line} = 15 mA; R7 = 68 kΩ; $V_{i(RMS)}$ = 3.6 mV	3.4	3.8	4.2	V
THD	total harmonic distortion					
		V_i = 3.6 mV +10 dB	–	1.5	–	%
		V_i = 3.6 mV +15 dB	–	2.8	–	%
$V_{LN(p-p)}$	output voltage swing (peak-to-peak value)	V_i = 3.6 mV +10 dB				
		I_p = 1.4 mA	3.55	3.8	4.05	V
		I_p = 2.7 mA	3.25	3.5	3.75	V
		I_p = 0 mA; I_{line} = 7 mA	–	1.8	–	V
		I_p = 0 mA; I_{line} = 4 mA	–	0.9	–	V
	dynamic behaviour of limiter	C16 = 470 nF				
t_{att}	attack time V_{mic} jumps from 2 mV to 40 mV		–	1.5	5.0	ms
t_{rel}	release time V_{mic} jumps from 40 mV to 2 mV		50	150	–	ms
$V_{no(RMS)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC− and MIC+; psophometrically weighted (P53 curve)	–	−72	–	dBmp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiving amplifier input IR (pin 13)						
Z_i	input impedance		17	21	25	kΩ
Receiving amplifier outputs QR– and QR+ (pins 4 and 5)						
Z_o	output impedance	single-ended	–	4	–	Ω
G_v	voltage gain (see Fig.21)	I_{line} = 15 mA; R4 = 100 kΩ				
	single-ended	R_T = 300 Ω	30	31	32	dB
	differential	R_T = 600 Ω	36	37	38	dB
$\Delta G_v f$	variation of G_v with frequency referred to 0.8 kHz	f = 300 and 3400 Hz	−0.5	−0.2	0	dB
$\Delta G_v T$	variation of G_v with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to +75 °C	–	±0.2	–	dB
$V_{o(RMS)}$	output voltage (RMS value)	TDA = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA				
	single-ended	R_T = 150 Ω	–	0.2	–	V
	differential	R_T = 450 Ω	–	0.37	–	V
	differential	C_T = 47 nF; R_s = 100 Ω; f = 3400 Hz	–	0.52	–	V
$V_{o(RMS)}$	output voltage (RMS value)	I_p = 0 mA; TDA = 10%; sinewave drive; R4 = 100 kΩ; R_T = 150 Ω				
		I_{line} = 4 mA	–	20	–	mV
		I_{line} = 7 mA	–	160	–	mV
$V_{no(RMS)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve); pin IR open-circuit				
	single-ended	R_T = 300 Ω	–	45	–	μV
	differential	R_T = 600 Ω	–	90	–	μV
$V_{no(RMS)}$	noise output voltage (RMS value)	see Fig.21; S1 in position 2; 200 Ω between MIC– and MIC+; single-ended; R_T = 300 Ω				
		R7 = 68 kΩ	–	100	–	μV
		R7 = 24.9 kΩ	–	65	–	μV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain adjustment input GAR (pin 6)						
ΔG_v	receiving amplifier gain adjustment range		−11	–	+8	dB
MUTE input (pin 14)						
V_{IH}	HIGH level input voltage		1.5 +V_{EE2}	–	V_{CC} +0.4	V
V_{IL}	LOW level input voltage		0	–	0.3 +V_{EE2}	V
I_{mute}	input current		–	11	20	μA
ΔG_v	change of microphone amplifier gain at mute on	MUTE = HIGH	–	−100	–	dB
G_v	voltage gain from input DTMF-SLPE to QR+ output with mute on	MUTE = HIGH; single-ended load; R_L = 300 Ω	–	−18	–	dB
Power-down input PD (pin 15)						
V_{IH}	HIGH level input voltage		1.5 +V_{EE2}	–	V_{CC1} +0.4	V
V_{IL}	LOW level input voltage		0	–	0.3 +V_{EE2}	V
I_{PD}	input current		–	5	10	μA
Automatic gain control input AGC (pin 18)						
	controlling the gain from IR (pin13) to QR+, QR− (pins 4, 5) and the gain from MIC+, MIC− (pins 8, 9) to LN (pin 1)	R6 = 93.1 kΩ (between pins 18 and 11)				
G_v	gain control range with respect to I_{line} = 15 mA	I_{line} = 75 mA	−5.7	−6.1	−6.5	dB
I_{line}	highest line current for maximum gain		–	24	–	mA
I_{line}	lowest line current for minimum gain		–	61	–	mA
ΔG_v	change of gain between I_{line} = 15 and 35 mA		−0.9	−1.4	−1.9	dB
Microphone mute input DLS/$\overline{\text{MMUTE}}$ (pin 7)						
V_{IL}	LOW level input voltage		V_{EE1}	–	V_{EE1} +0.3	V
I_{IL}	input current at LOW level input voltage		−85	−60	−35	μA
t_{rel}	release time after a LOW level on pin 7	C16 = 470 nF	–	30	–	ms
ΔG_v	change of microphone amplifier gain at LOW level input voltage on pin 7		–	−100	–	dB



For measuring gain from MIC+ amd MIC− the MUTE input should be LOW or open-circuit.
For measuring the DTMF input, the MUTE input should be HIGH.
Inputs not being tested should be open-circuit.

Fig.20 Test circuit for defining voltage gain of MIC−, MIC+ and DTMF inputs; voltage gain (G_v) is defined as $20\log|V_o/V_i|$.

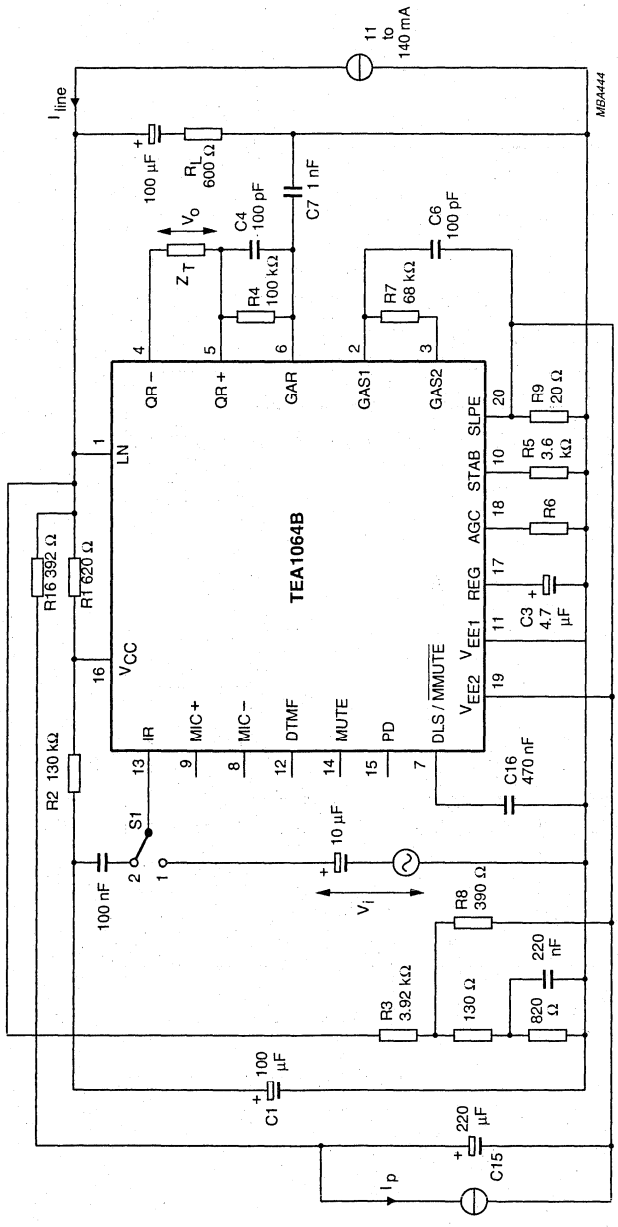


Fig.21 Test circuit for defining voltage gain of the receiving amplifier; voltage gain (G_v) is defined as $20\log|V_o/V_i|$ (with S1 in position 1).

APPLICATION INFORMATION

The basic application circuit is shown in Fig.22 and some typical application are shown in Fig.23, Fig.24 and Fig.25.

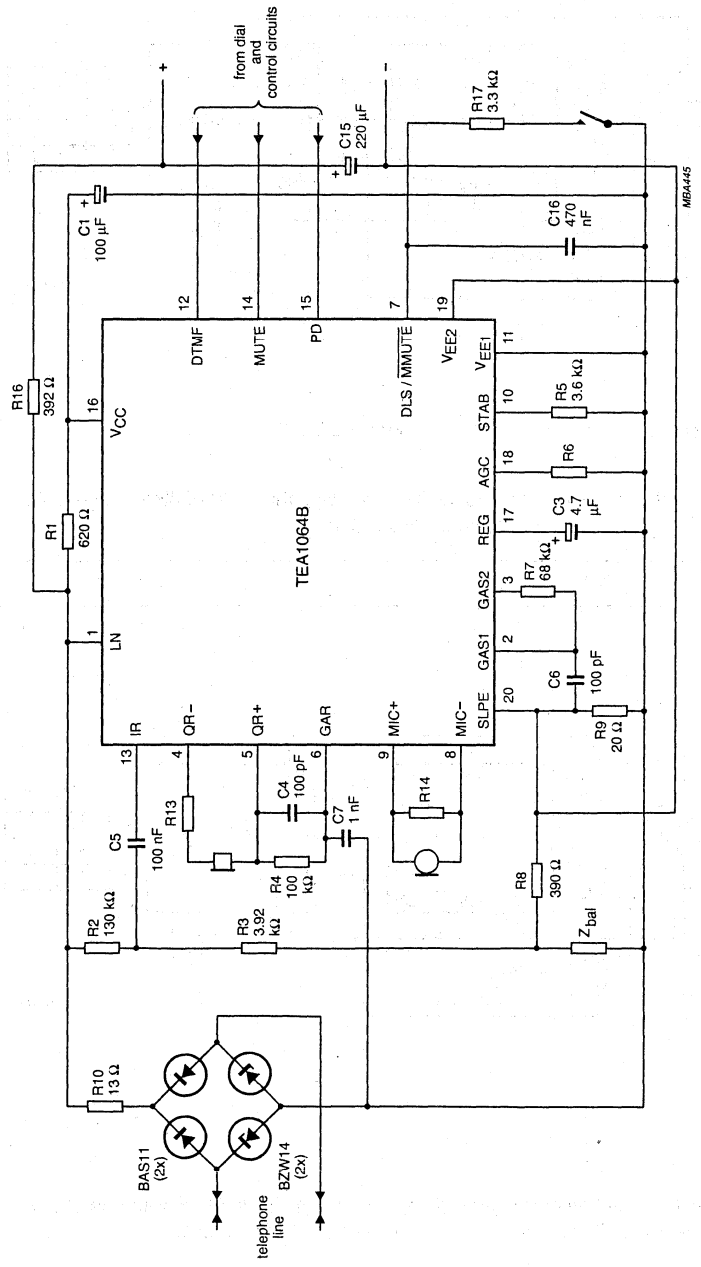
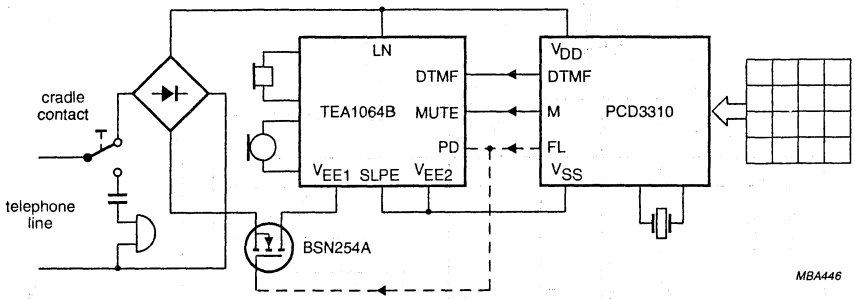


Fig.22 Basic application of TEA1064B with SLPE as supply reference for peripherals, shown here with piezo-electric earpiece and DTMF dialling.

The diode bridge and R10 limit the current into, and the voltage across, the circuit during line transients. A different protection arrangement is required for pulse dialling or register recall.



The broken line indicates optional flash (register recall by timed loop break).

Fig.23 Typical DTMF-pulse set application circuit (simplified) showing the TEA1064B with the CMOS bilingual dialling circuit PCD3310.

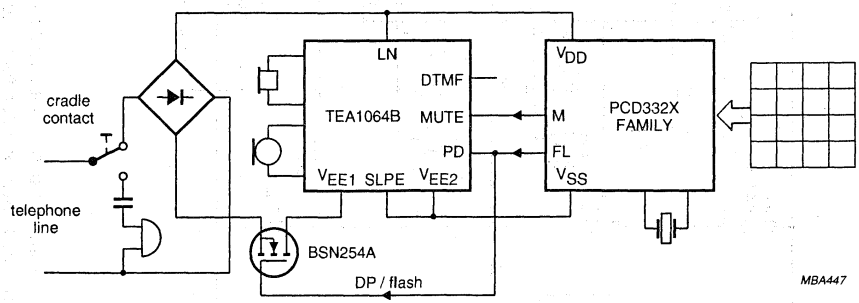


Fig.24 Typical pulse dial set application circuit (simplified) showing the TEA1064B with one of the PCD331X family of CMOS interrupted current-loop dialling circuits.

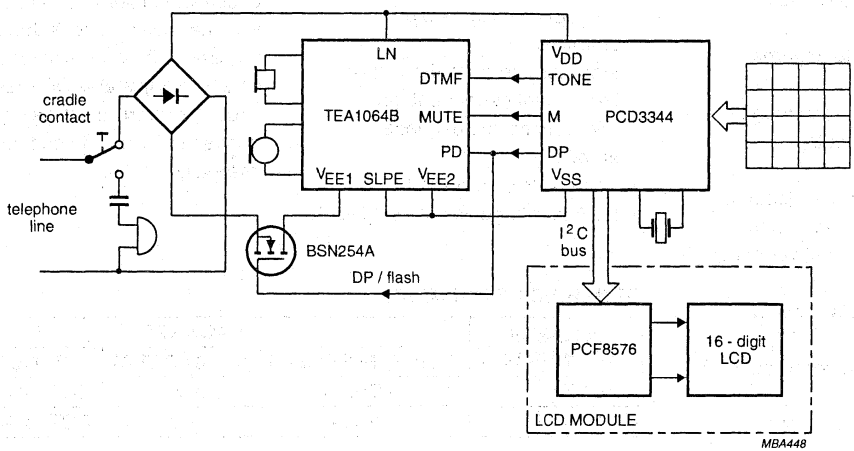


Fig.25 Typical dual-standard (pulse and DTMF) feature phone application circuit (simplified) showing the TEA1064B and the PCD3344 CMOS telephone microcontroller with on-chip DTMF generator plus I²C-bus.

Versatile telephone transmission circuit with dialler interface

TEA1065

FEATURES

- Current and voltage regulator mode with adjustable static resistances
- Provides supply for external circuitry
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power-down input for pulse dial or register recall
- Digital pulse input to drive an external switch transistor
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (on microphone and earpiece amplifiers)
- Adjustable gain control
- DC line voltage adjustment facility

GENERAL DESCRIPTION

The TEA1065 is a bipolar integrated circuit which performs all speech and line interface functions that are required in fully electronic telephone sets with adjustable DC mask. The circuit performs electronic switching between dialling and speech internally.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1065	24	DIL	plastic	SOT101L
TEA1065T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	4.25	4.45	4.65	V
I_{line}	normal operation line current range		10	-	150	mA
I_{CC}	internal supply consumption power-down input LOW power-down input HIGH		 - -	 1.14 73	 1.5 105	 mA µA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH I_P = 1.2 mA I_P = 1.55 mA	 2.7 2.5	 - -	 - -	 V V
G_V	voltage gain range microphone amplifier earpiece amplifier		 30 20	 - -	 46 45	 dB dB
ΔG_V	line loss compensation gain control range		-5.5	-5.9	-6.3	dB
T_{amb}	operating ambient temperature range		-25	-	+75	°C

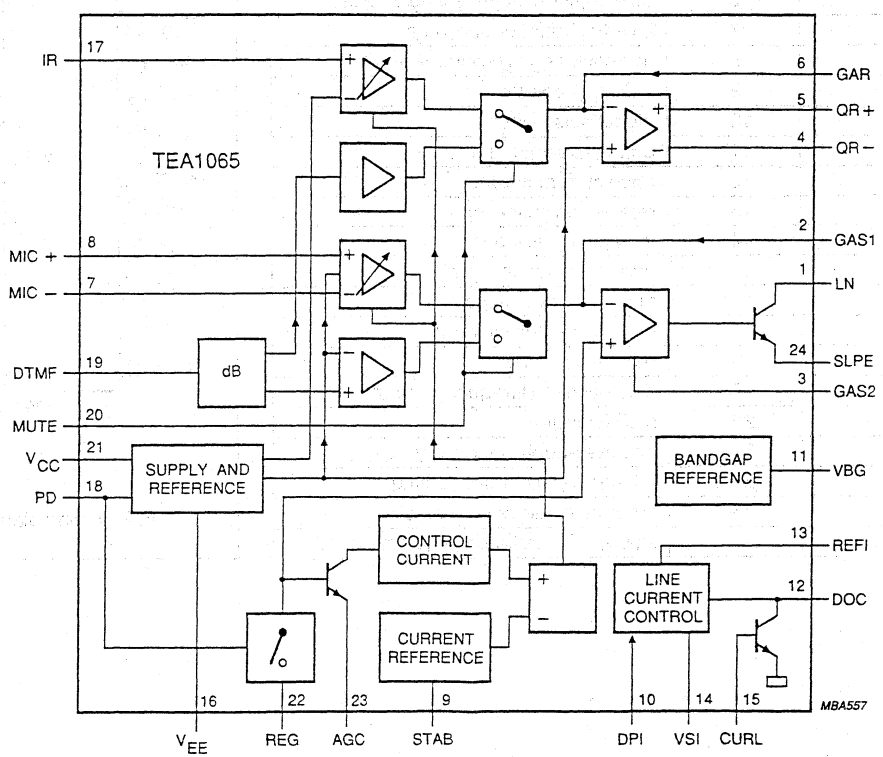


Fig.1 Block diagram.

Versatile telephone transmission circuit with dialler interface

TEA1065

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; sending amplifier
GAS2	3	gain adjustment; sending amplifier
QR–	4	inverting output; receiving amplifier
QR+	5	non-inverting output; receiving amplifier
GAR	6	gain adjustment; receiving amplifier
MIC–	7	inverting microphone input
MIC+	8	non-inverting microphone input
STAB	9	current stabilizer
DPI	10	digital pulse input
VBG	11	bandgap output reference
DOC	12	drive current output
REFI	13	reference voltage input
VSI	14	voltage sense input
CURL	15	current limitation input
V_{EE}	16	negative line terminal
IR	17	receiving amplifier input
PD	18	power-down input
DTMF	19	dual-tone multifrequency input
MUTE	20	MUTE input
V_{CC}	21	positive supply decoupling
REG	22	voltage regulator decoupling
AGC	23	automatic gain control input
SLPE	24	slope (DC resistance) adjustment

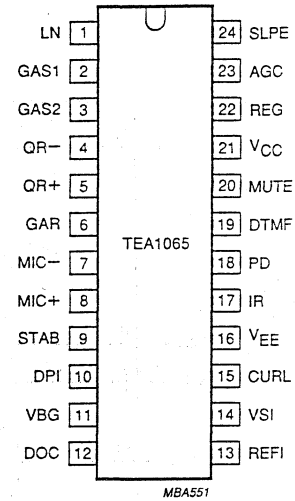


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripherals are usually supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} (pin 21) and regulates its voltage drop between LN and SLPE (pins 1 and 24). The internal supply requires a decoupling capacitor between V_{CC} and V_{EE} (pin 16); the internal voltage regulator has to be decoupled by a capacitor from REG (pin 22) to V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor connected between STAB (pin 9) and V_{EE}.
The TEA1065 can be set either in a DC voltage regulator mode or in a DC current regulator mode. The DC mask can be selected by connecting the appropriate external components to the dedicated pins (VSI, REFI, DOC, VBG).
When the DC current regulator mode is not required it can be cancelled by connecting pin VSI to V_{EE}; pins REFI, VBG and DOC are left open-circuit.

Voltage regulator mode

The voltage regulator mode is achieved when the line current is less than the current I_{knee} as illustrated in Fig.3. With R13 = R14 = 30 kΩ, the current I_{knee} = 30 mA (I_P = 0 mA).

This line current value will be reached when the voltage on pin VSI (almost equal to the voltage on pin SLPE) exceeds the voltage on pin REFI (equal to the voltage on pin VBG divided by the resistor tap R13, R14). For other values of R13 and R14, the I_{knee} current is given by the following formula:

$$I_{knee} = I_{CC} + I_P + (VBG/R9) \times \{R14/(R14 + R13)\} - (R15/R9) \times I_{O(VSI)}$$

I_{CC} is the current required by the circuit itself (typ. 1.14 mA).
I_P is the current required by the peripheral circuits connected between V_{CC} and V_{EE}. $I_{O(VSI)}$ is the output current from pin VSI (typ. 2.5 µA).

The DC slope of the V_{line}/I_{line} curve is, in this mode, determined by R9(R9 = R9a + R9b) in series with the r_{ds} of the external line current control transistor (see Fig.4; $r_{ds} = \partial V_{GS}/\partial I_D$ at $V_{GS} = V_{DS}$).

Current regulator mode

The current regulator mode is achieved when the line current is greater than I_{knee}. In this mode, the slope of the V_{line}/I_{line} curve is approximately 1300 Ω with R9 = 20 Ω, R16 = 1 MΩ, R13 = R14 = 30 kΩ. For other values of these resistances, the slope value can be approximated by the following formula:

$$R9 \times \{1 + R16 \times (1/R13 + 1/R14)\}$$

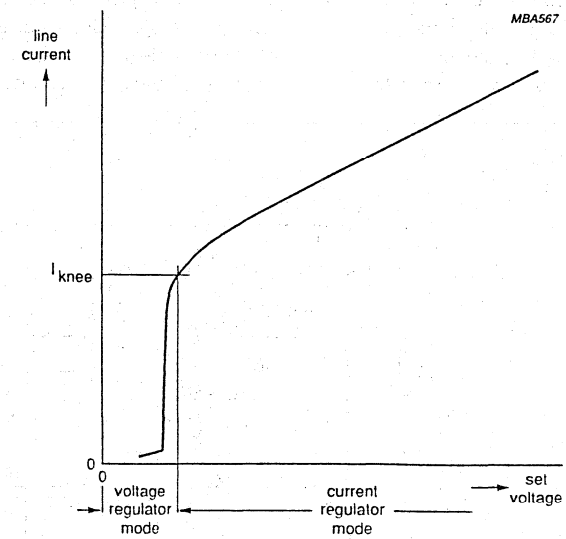


Fig.3 Voltage and current regulator mode.

The DC current flowing into the set is determined by the exchange supply voltage (V_{exch}), the DC resistance of the subscriber line (R_{line}) and the DC voltage on the subscriber set (see Fig.4).
If the line current exceeds I_{CC} +0.3 mA, required by the circuit itself ($I_{CC} \approx 1.14$ mA), plus the current I_p required by the peripheral circuits connected to V_{CC} then the voltage regulator will divert the excess current via LN.

$$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0.3 \times 10^{-3} - I_p) \times R9$$

where: V_{ref} is an internally generated temperature compensated reference voltage of 4.18 V and R9 is an external resistor connected between SLPE and V_{EE}.

The preferred value of R9 is 20 Ω. Changing R9 will influence the microphone gain, gain control characteristics, sidetone and the maximum output swing on LN. In this instance, the voltage on the line (excluding the diode rectifier bridge; see Fig.4) is:

$$V_{line} = V_{LN} + V_{GS} + R16 \times I_{DOC}$$

where: V_{GS} is the voltage drop between the gate and source terminal of the external line current control transistor and I_{DOC} is the current sunk by pin DOC ($I_{DOC} = 0$ in the voltage regulator mode and increases with I_{line} in the current regulator mode).
Under normal conditions $I_{SLPE} >> I_{CC} + 0.3$ mA + I_p and for the voltage regulator mode ($I_{line} < I_{knee}$), the static behavior of the circuit is equal to a 4.18 V voltage regulator diode with an internal resistance of R9 in series with the V_{GSon} of the external line current control transistor. For the current regulator mode ($I_{line} > I_{knee}$), the static behaviour of the circuit is equal to a 4.18 V voltage regulator diode with an internal resistance of R9 in series with the V_{GSon} of the external line current control transistor and also in series with a DC voltage source R16 x I_{DOC} (the preferred value of R16 is 1 MΩ at this value the current I_{DOC} is negligible compared to I_{line}).

In the audio frequency range the dynamic impedance between LN and V_{EE} is equal to R1 (see Fig.8). The internal reference voltage V_{ref} can be adjusted by means of an external resistor R_{VA}. This resistor, connected between LN and REG, will decrease the internal reference voltage. When R_{VA} is connected between REG and SLPE the internal reference voltage will increase.
The maximum allowed line current is given in Figs 5 and 6, where the current is shown as a function of the required reference voltage, ambient temperature and applied package.

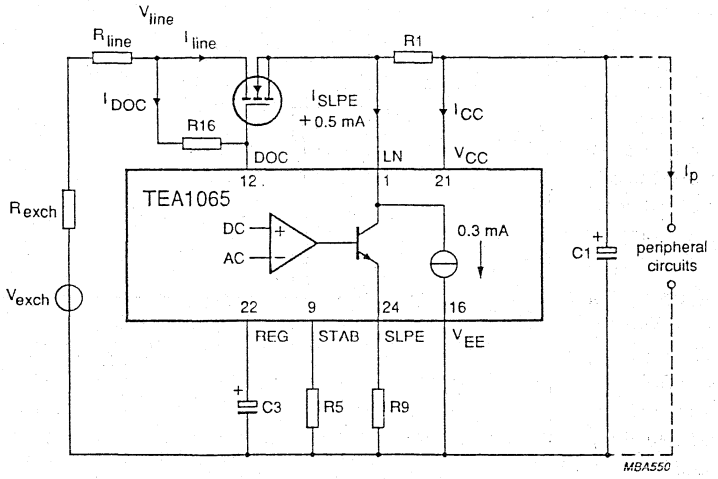
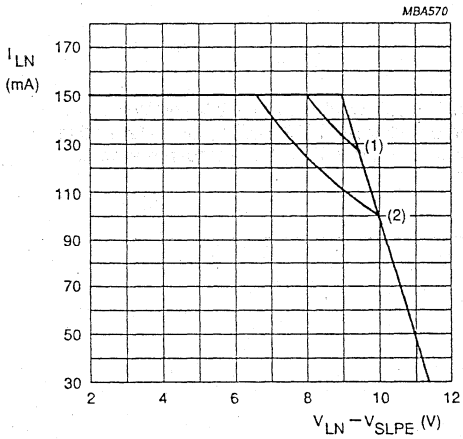


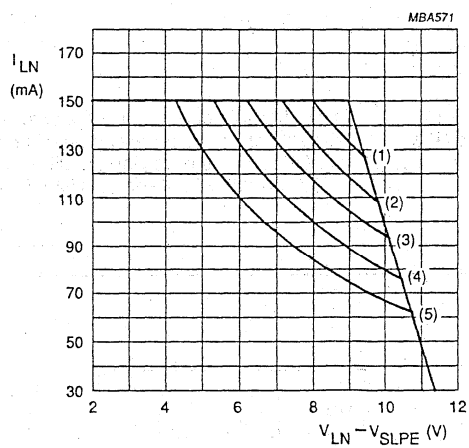
Fig.4 Supply arrangement.

The current I_p, available from V_{CC} for supplying peripheral circuits, depends on the external components and on the line current. Fig.7 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V, where 3 V is the minimum supply voltage for most CMOS circuits including a diode voltage drop for a back-up diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven (earpiece amplifier supplied from V_{CC}).



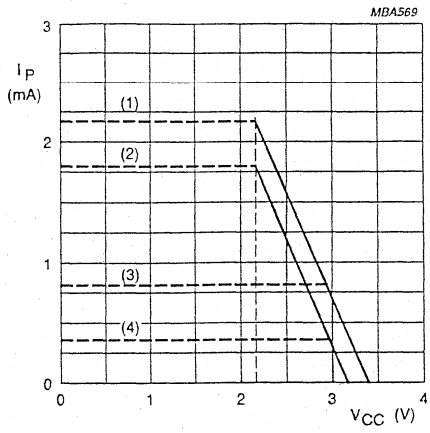
	T_{amb}	P_{tot}
(1)	65 °C	1.2 W
(2)	75 °C	1.0 W

Fig.5 TEA1065 safe operating area.



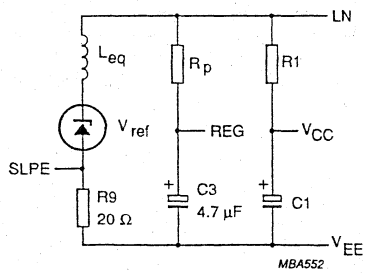
	T_{amb}	P_{tot}
(1)	35 °C	1.2 W
(2)	45 °C	1.07 W
(3)	55 °C	0.93 W
(4)	65 °C	0.8 W
(5)	75 °C	0.67 W

Fig.6 TEA1065T safe operating area.



I_{line} = 15 mA at V_{LN} = 4.45 V
R1 = 620 Ω
R9 = 20 Ω

Fig.7 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with V_{CC} > 2.2 V and V_{CC} > 3 V. Curve (1) and (3) are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (2) and (4) are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical). (1) = 2.2 mA; (2) = 1.77 mA; (3) = 0.78 mA and (4) = 0.36 mA.



L_{eq} = C3 x R9 x R_p
R_p = 17.5 kΩ

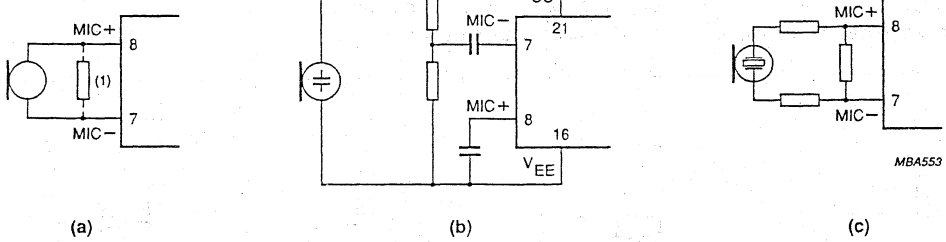
Fig.8 Equivalent circuit impedance between LN and V_{EE}.

Microphone inputs MIC+ and MIC− and gain adjustment connections GAS1 and GAS2

The TEA1065 has symmetrical microphone inputs, its input impedance is 40.8 kΩ (2 x 20.4 kΩ) and its voltage gain is typ. 38 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezoelectric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphones types are illustrated in Fig.9.

The gain of the microphone amplifier is proportional to external resistor R7, connected between GAS1 and GAS2, which can be adjusted between 30 dB and 46 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R7 x C6.



(a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs;

(b) electret microphone;

(c) piezoelectric microphone.

Fig.9 Microphone arrangements.

MUTE input

When MUTE = HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. When MUTE = LOW or open-circuit the DTMF input is inhibited and the microphone and receiving amplifier inputs are enabled. Switching the MUTE input will cause negligible clicks at the earpiece outputs and on the line. An electrostatic discharge protection diode is connected between pin MUTE and pin V_{CC} (pins 20 and 21).

Dual-tone multifrequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 12.5 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier. When R7 = 68 kΩ the gain is typically 25.5 dB. The signaling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifiers: IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR– (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig.10). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, which is sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when earpiece impedance exceeds 450 Ω as with high impedance dynamic, magnetic or piezoelectric earpieces.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of −11 dB to +8 dB to suit the sensitivity of the transducer that is used. The gain is proportional to external resistor R4 connected between GAR and QR+.

Two external capacitors, C4 = 100 pF and C7 = 1 nF, are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

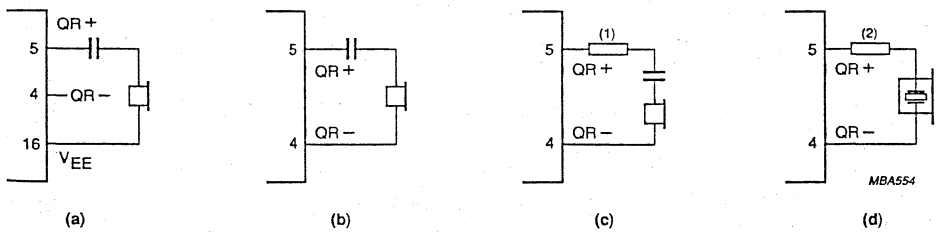


Fig.10 Alternative receiver arrangements: (a) dynamic earpiece with an impedance less than 450 Ω; (b) dynamic earpiece with an impedance more than 450 Ω; (c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load); (d) piezoelectric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

Automatic gain control

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current (see Fig.12). The control range is 5.9 dB; this corresponds to a line length of 3.5 km of twisted pair cable (see Fig.11). The DTMF gain is not affected by this feature.

If automatic line loss compensation is not required the AGC pin can be left open-circuit, the amplifiers then give their maximum gain.

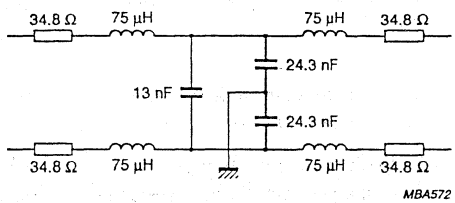


Fig.11 Typical 0.5 km line cell model used for automatic gain control optimization.

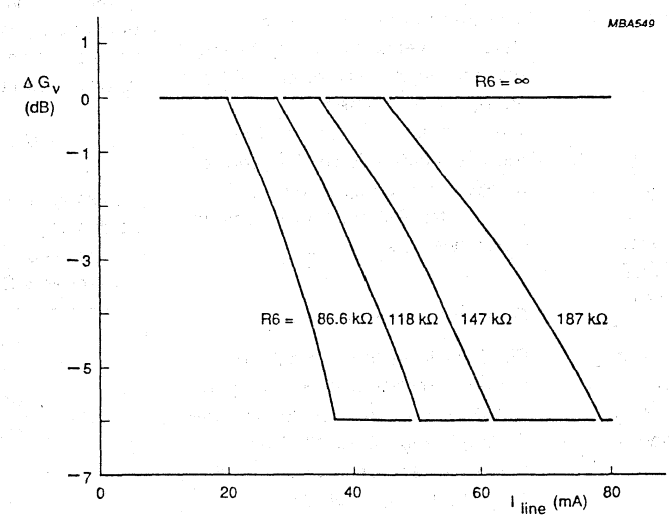


Fig.12 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Power-down input PD

During pulse dialling or register recall (timed-loop-break) the telephone line is interrupted, consequently it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirement on this capacitor is relaxed by applying a HIGH level to the PD input during the loop-break. This reduces the internal supply current from typ. 1.14 mA to 73 µA.

A HIGH level at PD also disconnects the capacitor at REG which results in the voltage stabilizer having no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit or connected to V_{EE}. An electrostatic discharge protection diode is connected between pin PD and V_{CC}.

Digital pulse input DPI

A HIGH level at DPI creates a current which flows from pin DOC to V_{EE} in order to interrupt the line current by the external line current control transistor (see Fig.18; MOSFET BUK554). A LOW level (or pin left open-circuit) disables this current to provide the normal DC regulation (voltage or current). A simple application without regulation of current in pulse dialling mode is given in Fig.18.

When DPI is activated (HIGH level), the external line current control transistor is switched off resulting in no current in the TEA1065. The voltage on pin SLPE becomes zero and capacitor C15 discharges cancelling the current regulation when DPI becomes inactive (LOW level).

To provide a constant regulation (in speech mode and pulse mode), an external transistor is required to keep C15 charged during DPI active (see Fig.19 in which the Field Effect Transistor BSJ177 is directly driven by the DPI signal).
An electrostatic discharge protection diode is connected between pin DPI and pin V_{CC}.

Voltage sense input and reference voltage input VSI and REFI

The voltage on pin VSI represents the DC voltage of pin SLPE. The RC filter (R15 x C15) is also intended to disable the DC regulation when C15 is shunted or not yet charged (especially directly after hook-off). The time constant R15 x C15 determines approximatively the time when no regulation (except CURL pin limitation) is activated.
The voltage applied on pin REFI represents a fraction of the bandgap reference voltage given by pin VBG (resistor tap R13 and R14) in order to determine I_{knee}.

Drive current output DOC

Pin DOC drives the external line current control transistor in order to achieve line interruption during pulse dialling (or register recall) and also the DC slope when $I_{line} > I_{knee}$. The current sunk by pin DOC is determined by the voltage on pin VSI in comparison with the voltage on pin VBG divided by the resistor tap R13 and R14.
When pin DPI is activated, pin DOC changes to a low voltage (by trying to sink typ. 900 µA to V_{EE}) to switch off the external line current control transistor.

Bandgap reference output VBG

This output provides a voltage reference to set the knee line current with the following formula:

$I_{knee} = I_{CC} + I_P + (VBG/R9) \times \{R14/(R14 + R13)\} \quad (R15/R9) \times 2.5 \times 10^{-6}$

In order to improve stability, a capacitive load is not allowed on this output.

Current limit input CURL

This input is applied to the base of an internal NPN transistor which has its collector connected to pin DOC and its emitter to V_{EE} (see Fig.13). The transistor limits the line current just after hook-off or during line transients to a value given by the following formula:

$I_{hook\text{-}off} = I(R1) + V_{BE}/R9b$

V_{BE} is the base-emitter voltage of the transistor (typ. 700 mV at 25 °C).
I(R1) is the current flowing through R1 to charge C1 just after hook-off.

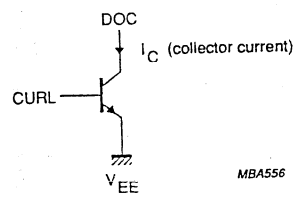


Fig.13 Internal current limiting transistor.

The maximum hook-off current then becomes:

$I_{hook\text{-}off} = V_Z/R1 + V_{BE} \times (R9a + R9b + R1)/(R1 \times R9b)$

where V_Z is the Zener voltage of diode D5 (see Fig.18).

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising $R1//Z_{line}$, R2, R3, R9 and Z_{bal} (see Fig.18). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9 \times R2 = R1 \times (R3 + R8)$

b) $k = R3 \times (R8 + R9)/(R2 \times R9)$

c) $Z_{bal} = k \times Z_{line}$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice Z_{line} varies considerably with the line length and line type. Therefore, the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with long and short times. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

With k = 1, R1 = 619 Ω, R9 = 20 Ω and an average line impedance represented by 270 Ω + (120 nF // 1100 Ω), the calculation results in:

- R2 = 130 kΩ
- R3 = 3650 Ω
- R8 = 715 Ω

The anti-sidetone network for the TEA1060 family, shown in Fig.15, attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Note

More information on the balancing of the anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011.

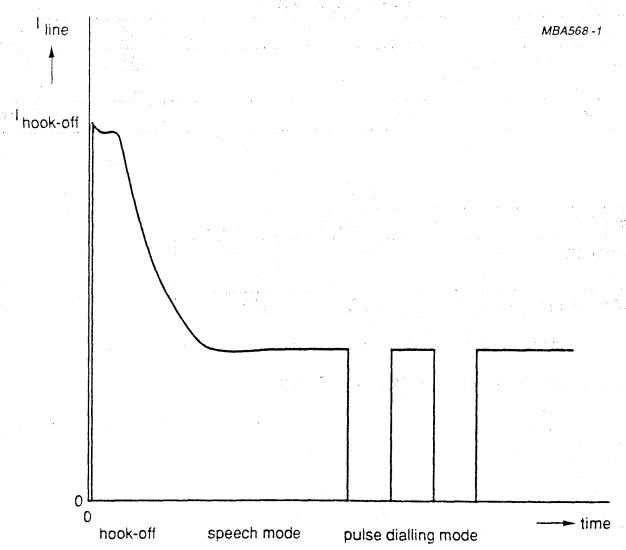


Fig.14 Example of line current shape in pulse dialling mode (see also Fig.18).

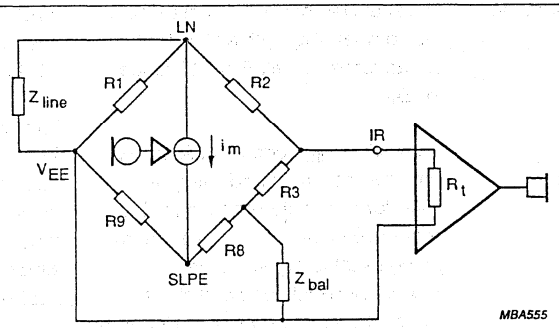


Fig.15 Equivalent circuit of TEA1060 family anti-sidetone bridge.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage continuous		-	12	V
V_{DOC}	positive DOC voltage continuous		-	12	V
V_{LN}	repetitive line voltage during switch-on or line interruption		-	13.2	V
I_{LN}	line current (see also Fig.5 and 6)		-	150	mA
V_I	input voltage on pins other than LN, DOC, VSI, REFI and CURL		V_{EE}-0.7	V_{CC}+0.7	V
P_{tot}	total power dissipation	see Figs 5 and 6			
T_{stg}	storage temperature range		–40	+125	°C
T_{amb}	operating ambient temperature range		–25	+75	°C
T_j	junction temperature		-	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	50	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	75	K/W

TEA1065T is mounted on glassy epoxy board 28.5 x 19.1 x 1.5 mm

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2, method 3015 (HBM 1500 Ω, 100 pF, 3 positive pulses and 3 negative pulses on each pin as a function of pin V_{EE}.

CHARACTERISTICS

I_{LN} = 10 to 150 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R9 = 20 Ω; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply LN and V_{CC} (pins 1 and 21)						
V_{LN}	voltage drop over circuit	I_{line} = 5 mA	3.95	4.25	4.55	V
		I_{line} = 15 mA	4.25	4.45	4.65	V
		I_{line} = 100 mA	5.4	6.1	6.7	V
		I_{line} = 140 mA	-	-	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	−3	−1	+1	mV/K
V_{LN}	voltage drop over circuit	I_{line} = 15 mA				
		$R_{VA} = R_{1\text{-}22}$ = 68 kΩ	3.6	3.9	4.15	V
		$R_{VA} = R_{22\text{-}24}$ = 39 kΩ	4.7	5.0	5.3	V
I_{CC}	supply current	PD = LOW; V_{CC} = 2.8 V	-	1.14	1.5	mA
		PD = HIGH; V_{CC} = 2.8 V	-	73	105	µA
Microphone inputs MIC+ and MIC− (pins 8 and 7)						
$\|Z_I\|$	input impedance		18.5	20.4	24.3	kΩ
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	37	38	39	dB
$\Delta G_v f$	variation with frequency referred to 800 Hz	I_{line} = 15 mA; f = 300 to 3400 Hz	−0.5	±0.2	+0.5	dB
$\Delta G_v T$	variation with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to 75 °C; without R6	-	±0.5	-	dB
Dual-tone multi-frequency input DTMF (pin 19)						
$\|Z_I\|$	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	24.5	25.5	26.5	dB
$\Delta G_v f$	variation with frequency referred to 800 Hz	I_{line} = 15 mA f = 300 to 3400 Hz	−0.5	±0.2	+0.5	dB
$\Delta G_v T$	variation with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to +75 °C	-	±0.5	-	dB
Gain adjustment GAS1 and GAS2 (pin 2 and 3)						
ΔG_v	gain variation with R7 connected between pins 2 and 3; transmitting amplifier		−8	-	+8	dB
Transmitting amplifier output LN (pin 1)						
$V_{LN(rms)}$	output voltage (RMS value)	I_{line} = 15 mA				
		d_{tot} = 2%	1.9	2.3	-	V
		d_{tot} = 10%	-	2.6	-	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; pin 7 and 8 open-circuit psophometrically weighted (P53 curve); control transistor included (MOS BUK554 type see Fig.18)	-	−68	-	dBmp
Receiving amplifier input IR (pin 17)						
Z_I	input impedance		17	21	25	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiving amplifier outputs QR+ and QR− (pin 5 and 4)						
Z_O	output impedance		-	4	-	Ω
G_v	voltage gain	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; RT = 300 Ω	30	31	32	dB
		differential; RT = 600 Ω	36	37	38	dB
$\Delta G_v f$	variation with frequency referred to 800 Hz	f = 300 to 3400 Hz	−0.5	±0.2	+0.5	dB
$\Delta G_v T$	variation with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to +75 °C	-	±0.2	-	dB
$V_{O(rms)}$	output voltage (RMS value)	I_{line} = 15 mA; THD = 2 %; sinewave drive; R4 = 100 kΩ				
		single-ended; RT = 150 Ω	0.3	0.38	-	V
		differential; RT = 450 Ω	0.56	0.72	-	V
		differential; CT = 60 nF; (1500 Ω series resistor); f = 3400 Hz	0.87	1.07	-	V
		I_{line} = 30 mA; differential; CT = 60 nF; (1500 Ω series resistor); f = 3400 Hz	1.02	1.22	-	V
$V_{O(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; RT = 300 Ω	-	50	-	μV
		differential; RT = 600 Ω	-	100	-	μV
Gain adjustment GAR (pin 6)						
ΔG_v	receiving amplifier, gain adjustment range		−11	-	+8	dB
Mute input MUTE (pin 20)						
V_{IH}	input voltage HIGH		1.5	-	V_{CC}	V
V_{IL}	input voltage LOW		-	-	0.3	V
I_{MUTE}	input current		-	8	15	μA
ΔG_v	change of microphone amplifier gain	MUTE = HIGH	-	−70	-	dB
G_v	voltage gain from DTMF input to QR+ or QR−	MUTE = HIGH; R4 = 100 kΩ single-ended; RT = 300 Ω	−19	−17	−15	dB
Power-down input PD (pin 18)						
V_{IH}	input voltage HIGH		1.5	-	V_{CC}	V
V_{IL}	input voltage LOW		-	-	0.3	V
I_{PD}	input current		-	2.5	5.0	μA
Automatic gain control input AGC (pin 23)						
ΔG_v	controlling the gain from IR to QR+, QR− and the gain from MIC+, MIC− to LN; gain control range with respect to I_{line} = 15 mA	R6 = 118 kΩ	−5.5	−5.9	−6.3	dB
I_{line}	highest line current for maximum gain		-	28	-	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	lowest line current for minimum gain		-	50	-	mA
ΔG_v	change of gain between I_{line} = 15 and 35.5 mA		–	-1.5	–	dB
Current limiting input CURL (pin 15)						
V_{BE}	base-emitter voltage drop of internal transistor	see Fig.13; I_C = 50 µA = I_{DOC}	-	0.7	-	V
H_{FE}	current gain of internal transistor	see Fig.13; I_C = 50 µA = I_{DOC}	60	120	-	
$I_{C(max)}$	maximum collector current of internal transistor	see Fig.13	-	-	2	mA
Bandgap reference voltage output VBG (pin 12)						
V_{BG}	reference voltage		–	1.22	–	V
I_{BG}	output drive capability	note 1	–100	-	+50	µA
Z_O	output impedance		-	12	-	Ω
Voltage sense input VSI (pin 14)						
I_O	output current	pin VSI connected to V_{EE}	-	-2.5	-	µA
Reference input REFI (pin 13)						
I_O	output current		-	-	2.0	mA
Drive current output DOC (pin 11)						
I_O	output current	REFI connected to V_{EE}; VSI not connected; DPI = LOW	120	300	-	µA
		REFI not connected; VSI connected to V_{EE}; DPI = HIGH	200	900	-	µA
Digital pulse input DPI (pin 10)						
V_{IH}	input voltage HIGH		1.5	-	V_{CC}	V
V_{IL}	input voltage LOW		-	-	0.3	V
I_{DPI}	input current		-	2.5	5	µA

Note to the characteristics

1. No capacitive load on the V_{BG} output. Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

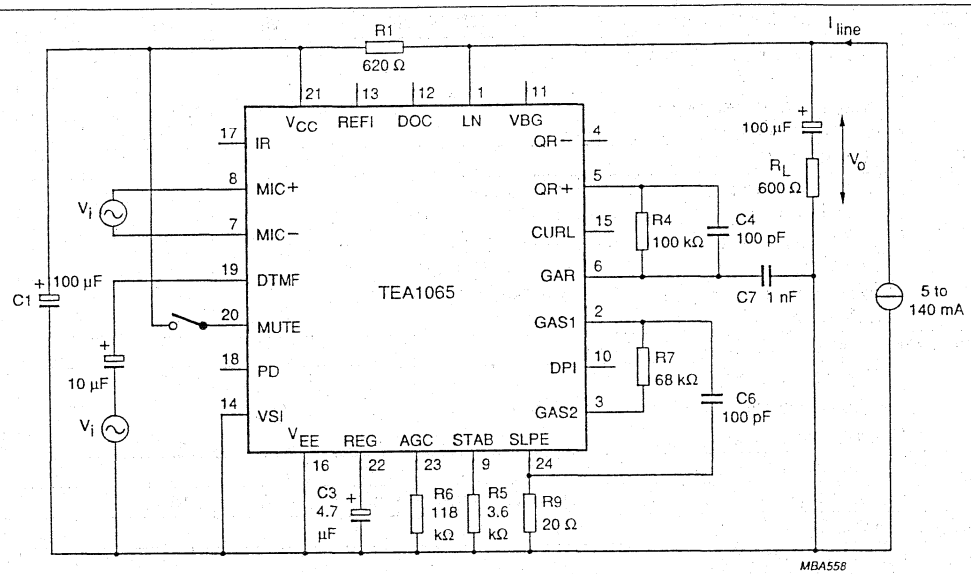


Fig.16 Test circuit for defining voltage gain of MIC+, MIC− and DTMF inputs. Voltage gain is defined as $G_v = 20 \text{ Log} |V_o/V_i|$. For measuring the gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open-circuit except VSI that should be connected to V_{EE}.

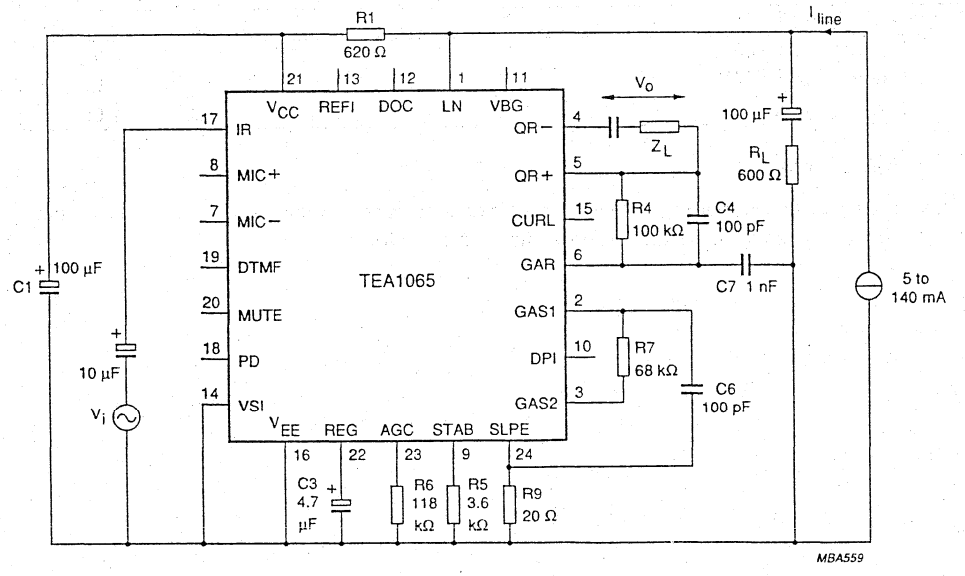


Fig.17 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as $G_v = 20 \text{ Log } |V_o/V_i|$.

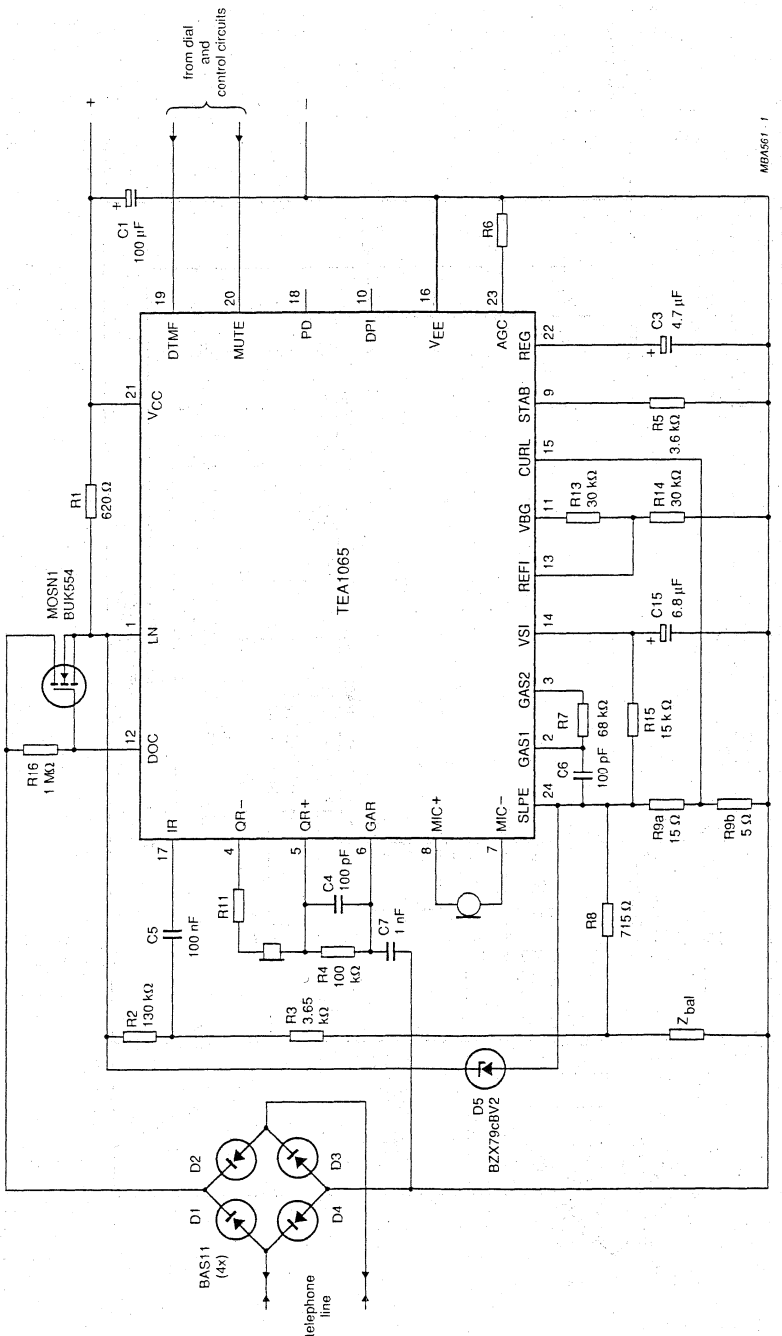


Fig.18 Typical application of the TEA1065, with a piezoelectric earpiece and DTMF dialling.

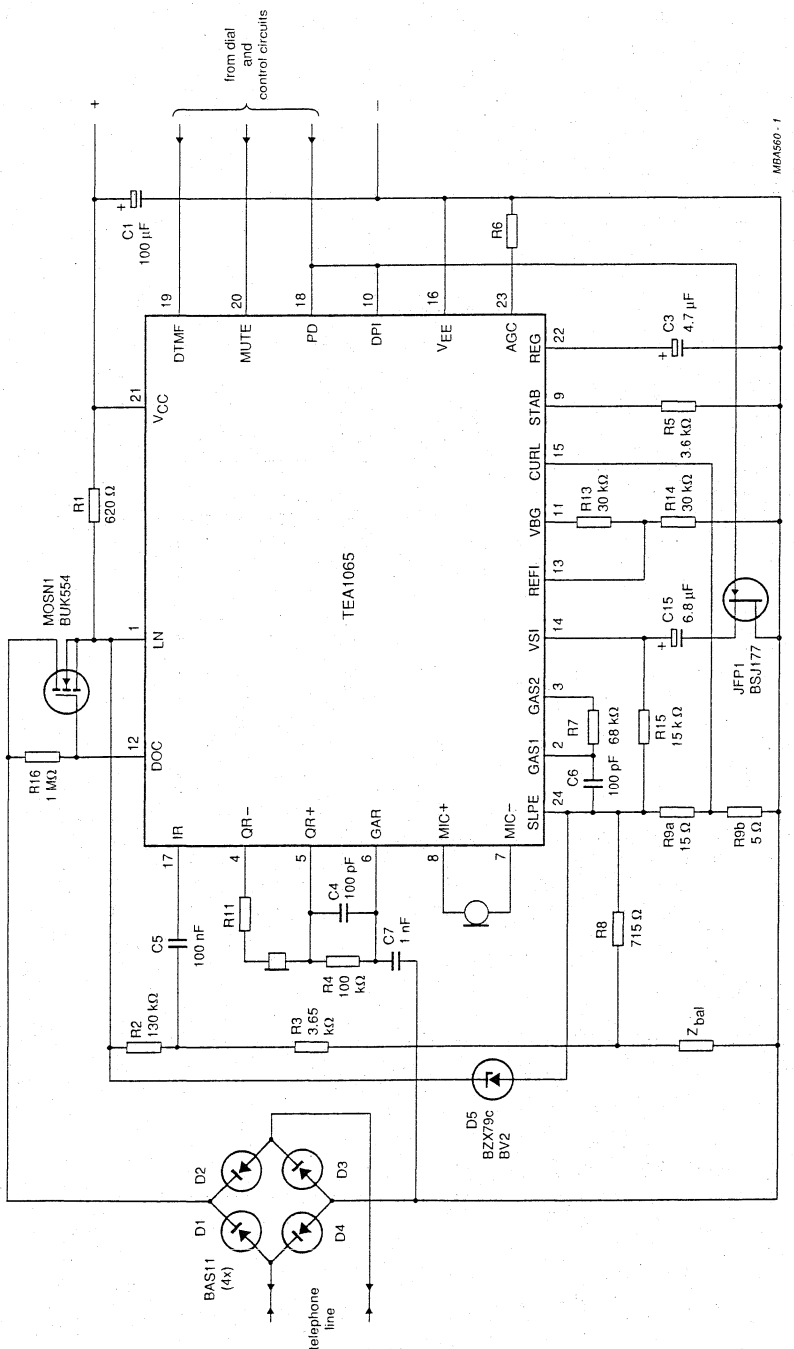


Fig.19 Typical application of the TEA1065, with a piezoelectric earpiece and pulse dialling. DTMF dialling requires a different protection arrangement.

Versatile telephone transmission circuit with dialler interface

TEA1066T

GENERAL DESCRIPTION

The TEA1066T is a bipolar integrated circuit which performs all speech and line interface functions that are required in fully electronic telephone sets. The circuit performs electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
Line current operating range		I_{line}	10	–	100	mA
Internal supply current						
power down input LOW		I_{CC}	–	0.96	1.3	mA
power down input HIGH		I_{CC}	–	55	82	μA
Supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH					
	I_p = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_p = 1.7 mA	V_{CC}	2.5	–	–	V
Voltage gain range for microphone amplifier						
Low impedance inputs (pins 9 and 7)		G_v	44	–	60	dB
High impedance inputs (pins 10 and 8)		G_v	30	–	46	dB
Receiving amplifier		G_v	17	–	39	dB
Line loss compensation						
Gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	24	–	60	V
Exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Operating ambient temperature range		T_{amb}	−25	–	+ 75	°C

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).

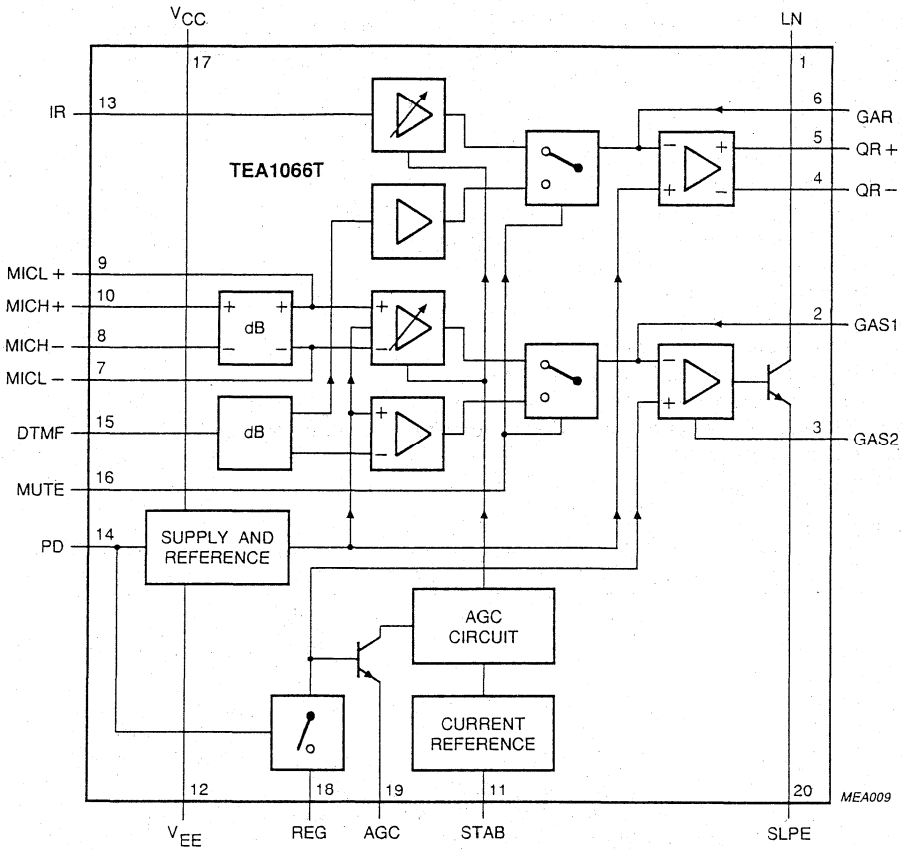


Fig. 1 Block diagram.

The blocks marked "dB" are attenuators.

Versatile telephone transmission circuit with dialler interface

TEA1066T

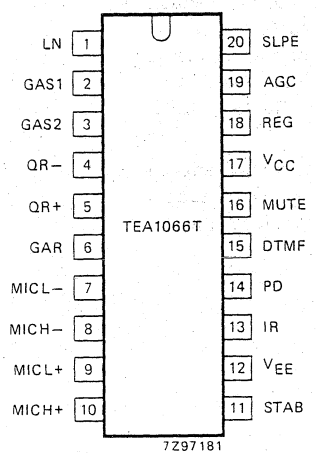


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment transmitting amplifier
3	GAS2	gain adjustment transmitting amplifier
4	QR−	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment receiving amplifier
7	MICL−	inverting microphone input, low impedance
8	MICH−	inverting microphone input, high impedance
9	MICL+	non-inverting microphone input, low impedance
10	MICH+	non-inverting microphone input, high impedance
11	STAB	current stabilizer
12	V_{EE}	negative line terminal
13	IR	receiving amplifier input
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1066T and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6 kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the DC resistance of the subscriber line R_{line} and the DC voltage on the subscriber set (see Fig. 7).

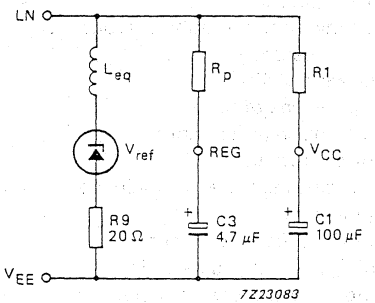
If the line current I_{line} exceeds the current I_{CC} + 0.5 mA required by the circuit itself, about 1 mA, plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:
$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0.5 \times 10^{-3} A - I_p) \times R9$, where V_{ref} is an internally generated temperature compensated reference voltage of 4,2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value for R9 is 20 Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side-tone level and maximum output swing on LN.

FUNCTIONAL DESCRIPTION (continued)

Under normal conditions $I_{SLPE} \gg I_{CC} + 0.5$ mA + I_P. The static behaviour of the circuit then equals a 4.2 V voltage regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1 (see Fig. 3). The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This R_{VA} connected between LN and REG (pins 1 and 18) will decrease the internal reference voltage. R_{VA} connected between REG and SLPE (pins 18 and 20) will increase the internal reference voltage.

Current I_P, available from V_{CC} for supplying peripheral circuits, depends on external components and on the line current. Fig. 8 shows this current for $V_{CC} > 2.2$ V and > 3 V (being the minimum supply voltage for most CMOS circuits including voltage drop for an enable diode). If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.



R_p = 17.5 kΩ
L_{eq} = C3 x R9 x R_p

Fig. 3 Equivalent impedance circuit.

Microphone inputs MICL+, MICH+, MICL− and MICH− and amplification adjustment connections GAS1 and GAS2

The TEA1066T has symmetrical microphone inputs. The MICL+ and MICL− inputs are intended for low-sensitivity, low-impedance dynamic or magnetic microphones. Input impedance is 8.2 kΩ (2 x 4.1 kΩ) and its voltage gain is typ. 52 dB. The MICH+ and MICH− inputs are intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 40.8 kΩ (2 x 20.4 kΩ) and its voltage gain is typical 38 dB. The arrangements with the microphone types mentioned are shown in Fig. 9.

The gain of the microphone amplifier in both types can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier; a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the earpiece outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 25.5 dB and varies with R7 in the same way as the gain of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 10). Gain from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB and differential drive becomes possible. This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezo-electric earpieces.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C6 = 10 x C4 = 1 nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic amplification control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 11 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum gain as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.
When this facility is not required PD may be left open.

FUNCTIONAL DESCRIPTION (continued)

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 14). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9.R2 = R1(R3 + [R8//Z_{bal}])$

b) $[Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| < R3$.
To obtain optimum side tone suppression, condition b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$$

where k is a scale factor; $k = (R8/R1)$.

Scale factor k (value of R8) must be chosen to meet the following criteria:
- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal}+R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal}/k equals the average line impedance.

Example

The balanced line impedance $|Z_{bal}|$ at which the optimum suppression is preset can be calculated by: suppose $Z_{line} = 210\ \Omega + (1265\ \Omega/140\ nF)$, representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; $Z_{bal} = 130\ \Omega + (820\ \Omega//220\ nF)$.

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

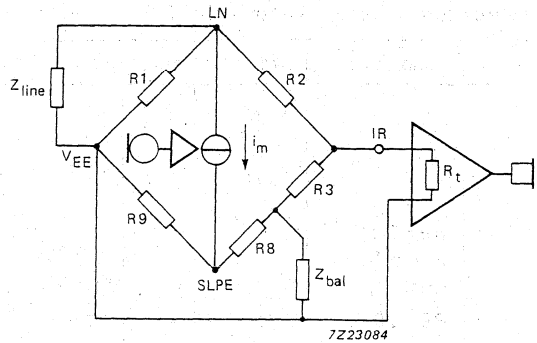


Fig. 4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

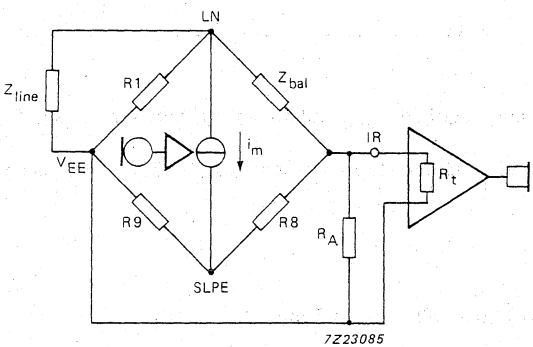


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

FUNCTIONAL DESCRIPTION (continued)

The anti-sidetone network as used in the standard application (Fig. 13) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special TEA1066 bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-sidetone circuit. Both bridge types can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage continuous		V_{LN}	–	12	V
Repetitive line voltage during switch-on or line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 10)	V_{LN}	–	28	V
Line current (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		$-V_i$	–	0.7	V
Total power dissipation (2)	R9 = 20 Ω	P_{tot}	–	555	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

Notes to the ratings

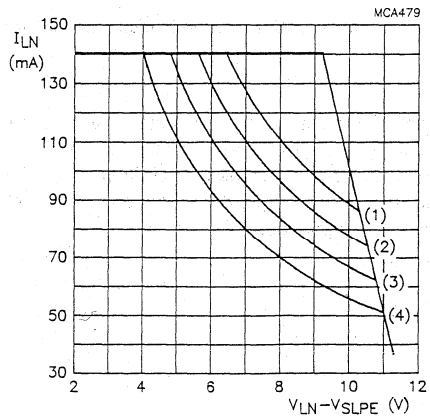
(1) Mostly dependent on the maximum required T_{amb} and the voltage between LN and SLPE (see Fig. 6).

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air

TEA1066T mounted on glass epoxy board 41 x 19 x 1.5 mm $R_{th\ j\text{-}a}$ = 90 K/W



	T_{amb}	P_{tot}
(1)	45 °C	888
(2)	55 °C	777
(3)	65 °C	666
(4)	75 °C	555

Fig. 6 Safe operating area.

CHARACTERISTICS

I_{line} = 10 to 100 mA; V_{EE} = 0 V; f = 800 Hz; R9 = 20 Ω; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 17)						
Voltage drop over circuit	I_{line} = 5 mA	V_{LN}	3.95	4.25	4.55	V
	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
	I_{line} = 100 mA	V_{LN}	5.40	6.10	6.70	V
	I_{line} = 140 mA	V_{LN}	–	–	7.50	V
Voltage drop variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Voltage drop over circuit	I_{line} = 15 mA; R_{VA} = R1-18 = 68 kΩ	V_{LN}	3.50	3.80	4.05	V
	R_{VA} = R18-20 = 39 kΩ	V_{LN}	4.70	5.0	5.30	V
Supply current (pin 17)						
PD (pin 14) = LOW	V_{CC} = 2.8 V	I_{CC}	–	0.96	1.3	mA
PD (pin 14) = HIGH	V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuits	I_{line} = 15 mA; MUTE = HIGH					
	I_P = 0 mA	V_{CC}	3.5	3.75	–	V
	I_P = 1.2 mA	V_{CC}	2.8	3.05	–	V
Microphone inputs MICL+ and MICL−; MICH+ and MICH−						
Input impedance						
MICL+ (pin 9); MICL− (pin 7)		$\|Z_i\|$	3.3	4.1	4.9	kΩ
MICH+ (pin 10); MICH− (pin 8)		$\|Z_i\|$	16.5	20.4	24.5	kΩ
Common-mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain	I_{line} = 15 mA; R7 = 68 kΩ					
MICL+/MICL− to LN		G_v	51	52	53	dB
MICH+/MICH− to LN		G_v	37	38	39	dB
gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	±0.2	+ 0.5	dB
gain variation with temperature at T_{amb} = −25 °C and + 75 °C	I_{line} = 50 mA; w.r.t. 800 Hz	ΔG_{vT}	–	±0.2	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF (pin 15)						
Input impedance		$\|Z_i\|$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	±0.2	+ 0.5	dB
gain variation with temperature at T_{amb} = −25 °C and + 75 °C	I_{line} = 50 mA; w.r.t. 25 °C	ΔG_{vT}	−	±0.2	−	dB
Gain adjustment connections GAS1 and GAS2 (pins 2 and 3)						
Gain variation with R7, transmitting amplifier		ΔG_v	−8	−	+ 8	dB
Transmitting amplifier output LN (pin 1)						
Output voltage	I_{line} = 15 mA; THD = 2%	$V_{LN(rms)}$	1.9	2.3	−	V
	THD = 10%	$V_{LN(rms)}$	−	2.6	−	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; microphone inputs open psophometrically weighted (P53 curve)	$V_{no(rms)}$	−	−70	−	dBmp
Receiving amplifier input IR (pin 13)						
Input impedance		$\|Z_i\|$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR− (pins 5 and 4)						
Output impedance	single-ended	$\|Z_o\|$	−	4	−	Ω
Voltage gain from IR to QR+ or QR−	I_{line} = 15 mA; R4 = 100 kΩ; single-ended R_L = 300 Ω	G_v	24	25	26	dB
	differential R_L = 600 Ω	G_v	30	31	32	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	±0.2	+ 0.5	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier outputs QR+ and QR− (continued)						
Gain variation with temperature at T_{amb} = −25 °C and + 75 °C	I_{line} = 50 mA; w.r.t. 25 °C	ΔG_{vT}	–	±0.2	–	dB
Output voltage	I_P = 0 mA; I_{line} = 15 mA; THD = 2%; R4 = 100 kΩ					
sine-wave drive						
single-ended	R_L = 150 Ω	$V_{o(rms)}$	0.30	0.38	–	V
	R_L = 450 Ω	$V_{o(rms)}$	0.4	0.52	–	V
differential	C_L = 47 nF R series = 100 Ω; f = 3400 Hz	$V_{o(rms)}$	0.8	1.0	–	V
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; pin 13 (IR) open psophometrically weighted (P53 curve)					
single-ended	R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR (pin 6)						
Gain variation with R4 connected between pin 6 and pin 5 receiving amplifier		ΔG_v	−8	–	+ 8	dB
MUTE input (pin 16)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	5	10	μA
Reduction of voltage gain from MICL+ (pin 9) and MICL− (pin 7) to LN (pin 1)	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH; R4 = 100 kΩ					
single-ended	R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD (pin 14)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic gain control input AGC (pin 19)						
Gain control range from IR to QR+/QR− and from MIC+/MIC− to LN; R6 = 110 kΩ between AGC and V_{EE}						
Gain control range	I_{line} = 70 mA	$-\Delta G_v$	−5.5	−5.9	−6.3	dB
Highest line current for maximum gain	I_{line}	–	–	23	–	mA
Lowest line current for minimum gain	I_{line}	–	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		$-\Delta G_v$	−1.0	−1.5	−2.0	dB

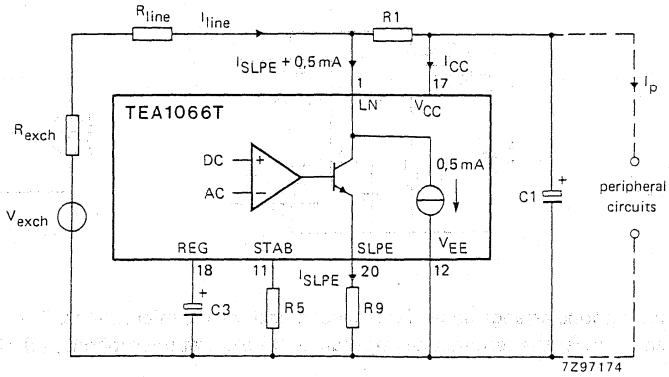


Fig. 7 Supply arrangement.

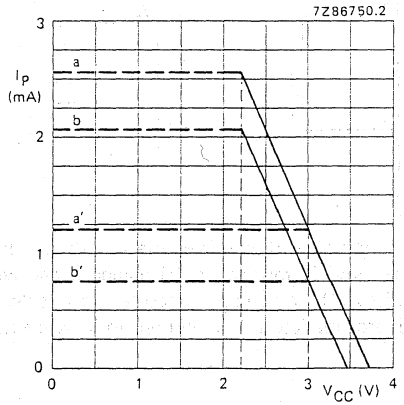


Fig. 8 Typicalmum current I_P available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2.2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (b) and (b') are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)} = 150$ mV, $R_L = 150\ \Omega$ (asymmetrical).
$I_{line} = 15$ mA; $V_{LN} = 4.45$ V; R1 = 620 Ω and R9 = 20 Ω.
(a) = 2.55 mA; (b) = 2.1 mA; (a') = 1.2 mA and (b') = 0.75 mA.

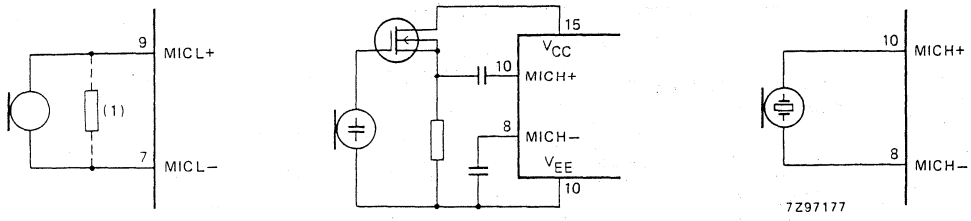


Fig. 9 Alternative microphone arrangements. (a) magnetic or dynamic microphone. The resistor marked (1) may be connected to lower the terminating impedance. (b) electret microphone, (c) piezo-electric microphone.

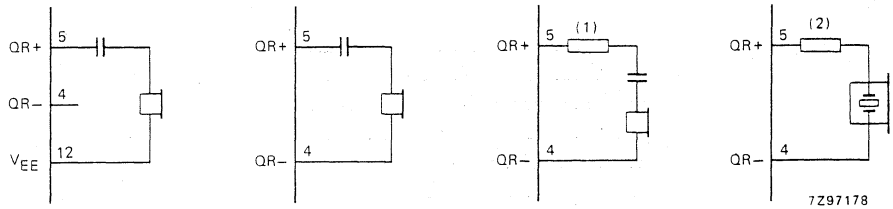


Fig. 10 Alternative receiver arrangements. (a) dynamic earpiece with less than 450 Ω impedance. (b) dynamic earpiece with more than 450 Ω impedance. (c) magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load). (d) piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

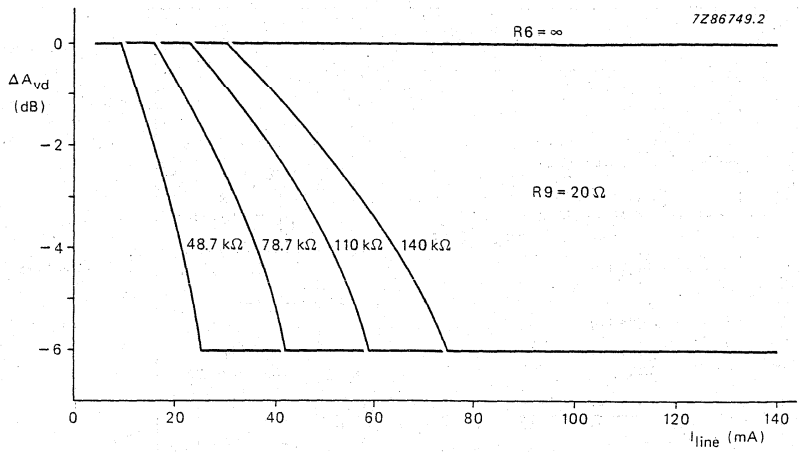


Fig. 11 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

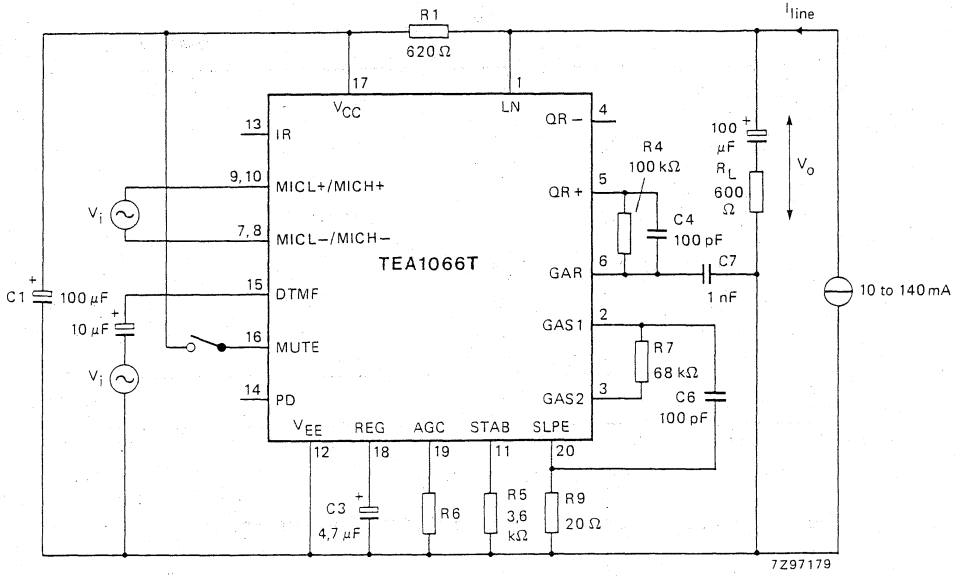


Fig. 12 Test circuit for defining voltage gain of MICL+, MICL−, MICH+ and MICH− DTMF inputs. Voltage gain is defined as: $G_V = 20 \log |V_o/V_i|$. For measuring the gain from MICL+, MICL− or MICH+ and MICH− the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

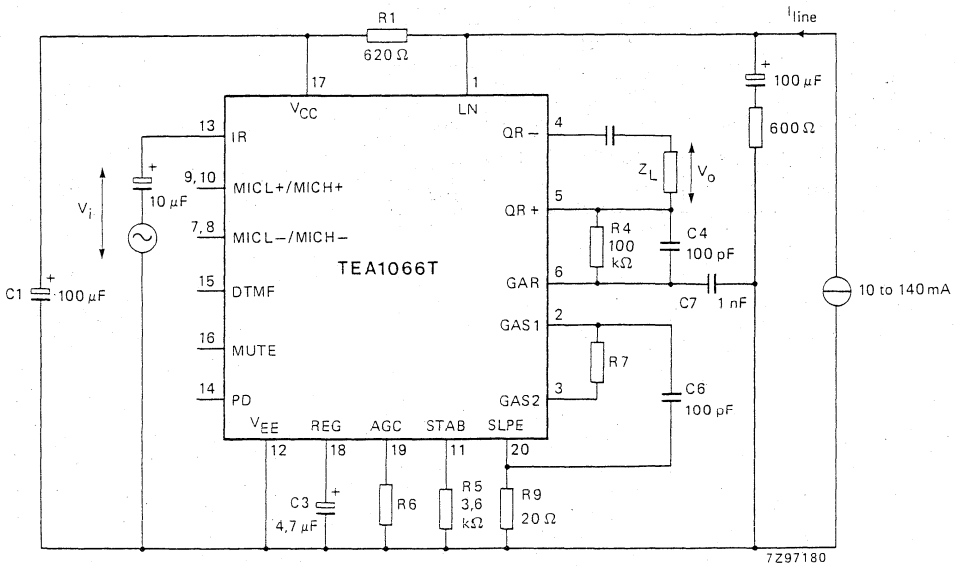


Fig. 13 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as: $G_V = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

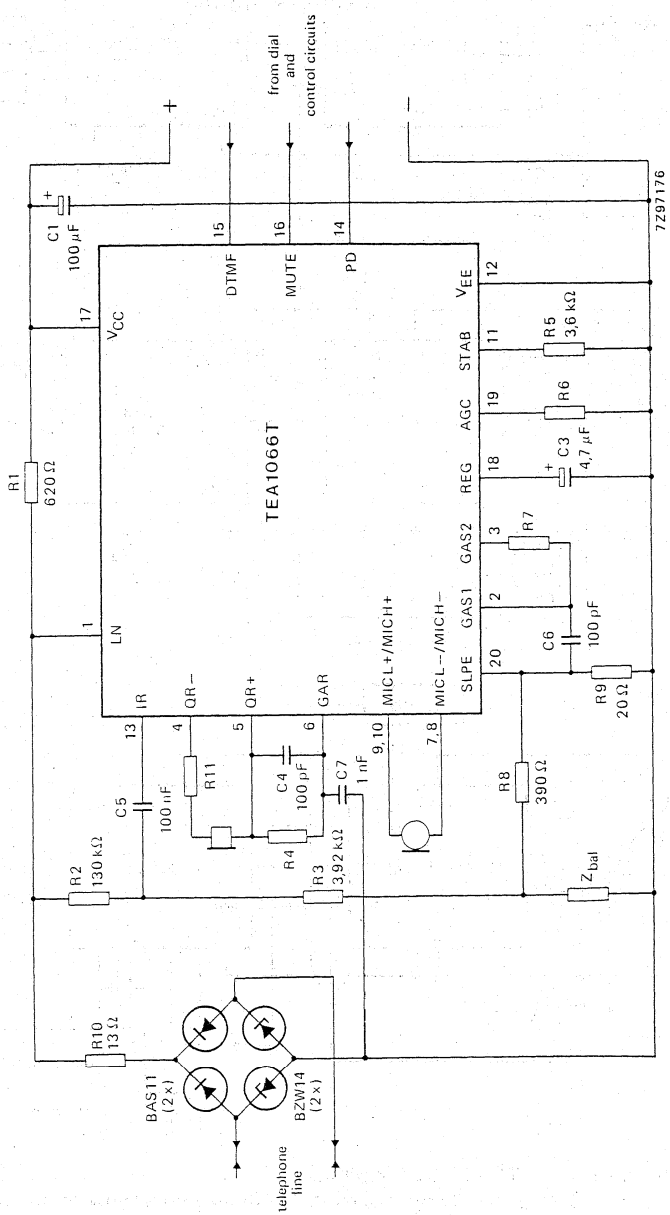
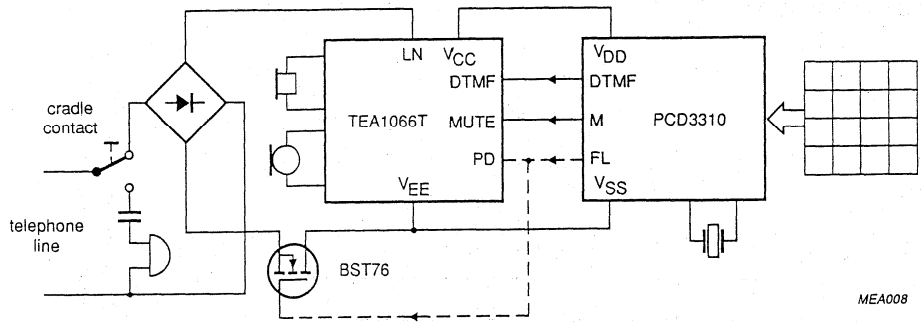
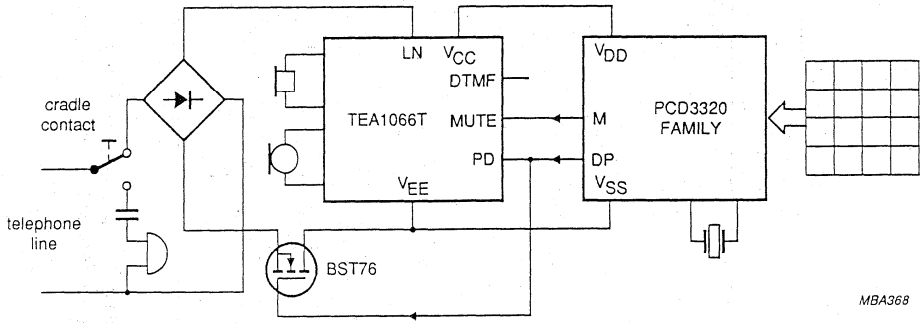


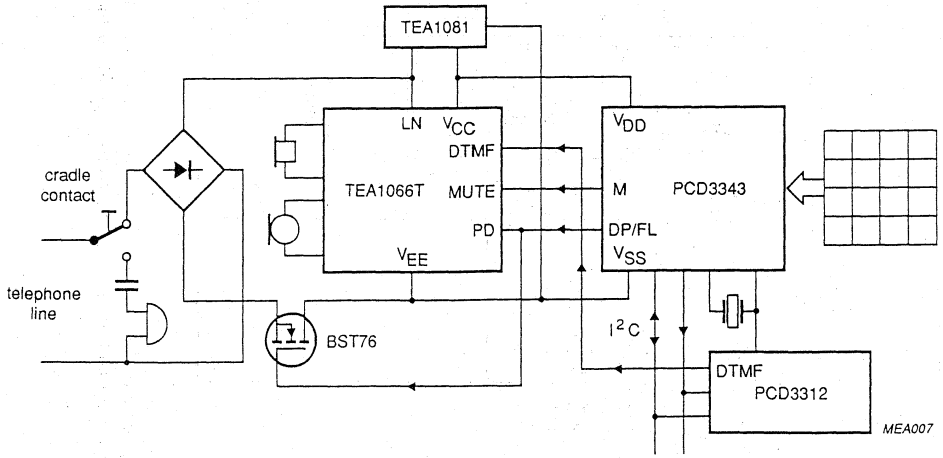
Fig. 14 Typical application of the TEA1066T, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.



(a)



(b)



(c)

Fig.15 Typical applications of the TEA1066T (simplified).

(a) DTMF pulse set with CMOS PCD3310 dialling circuit. The dashed lines show an optional flash (register recall by timed loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

Low voltage versatile telephone transmission circuit with dialler interface

TEA1067

GENERAL DESCRIPTION

The TEA1067 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The circuit is able to operate down to a DC line voltage of 1.6 V (with reduced performance) to facilitate the use of more telephone sets in parallel.

Features

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides supply with limited current for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment capability

QUICK REFERENCE DATA

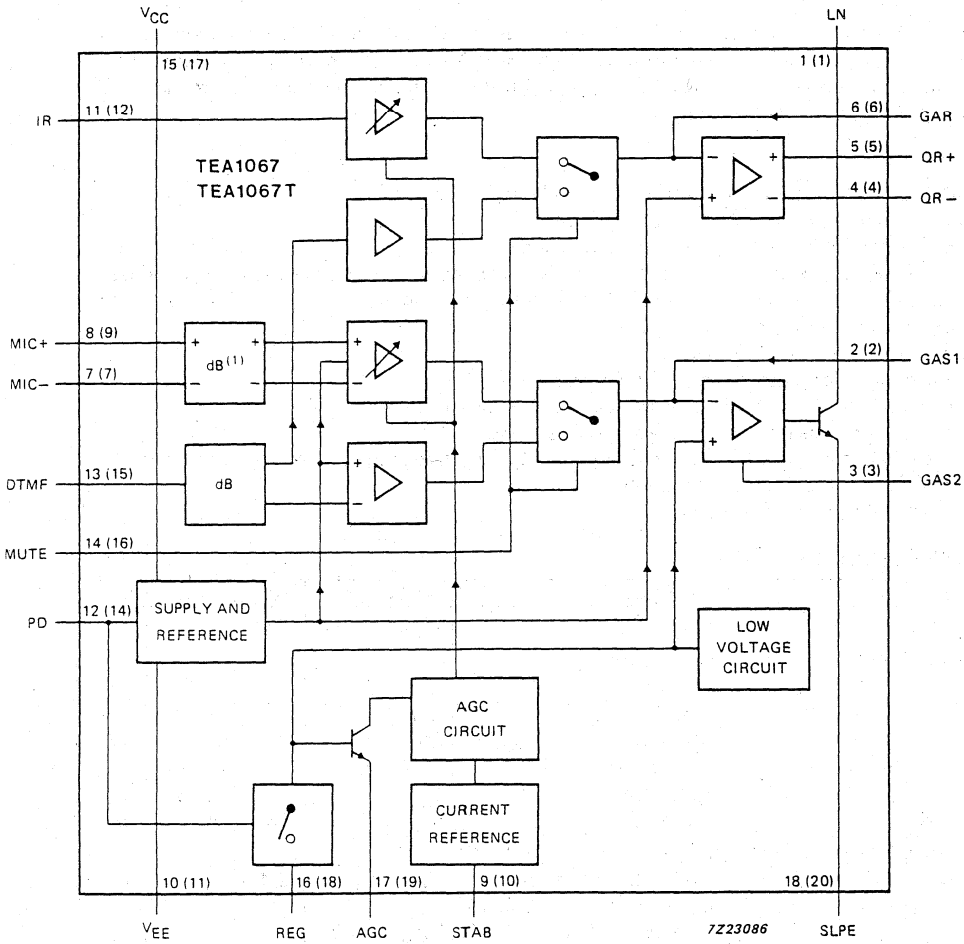
parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	3.65	3.9	4.15	V
Line current operating range	normal operation					
	TEA1067	I_{line}	11	–	140	mA
	TEA1067T	I_{line}	11	–	140	mA
	with reduced performance	I_{line}	1	–	11	mA
Internal supply current	power down					
	input LOW	I_{CC}	-	1	1.35	mA
	input HIGH	I_{CC}	–	55	82	μA
Supply voltage for peripherals	I_{line} = 15 mA; I_p = 1.4 mA; mute input HIGH	V_{CC}	2.2	2.4	–	V
	I_{line} = 15 mA; I_p = 0.9 mA; mute input HIGH	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	45	dB
Line loss compensation gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	36	–	60	V
Exchange feeding bridge resistance range		R_{exch}	0.4	–	1	kΩ

PACKAGE OUTLINES

TEA1067: 18-lead DIL; plastic (SOT102).
TEA1067T: 20-lead mini-pack; plastic (SO20; SOT163A).

Low voltage versatile telephone transmission circuit with dialler interface

TEA1067



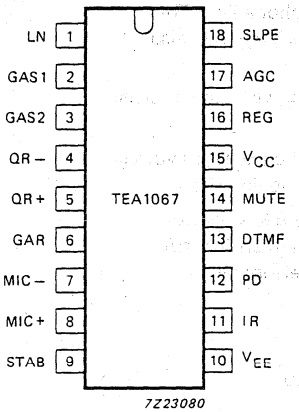
Figures in parenthesis refer to TEA1067T.

Fig. 1 Block diagram.

Low voltage versatile telephone transmission circuit with dialler interface

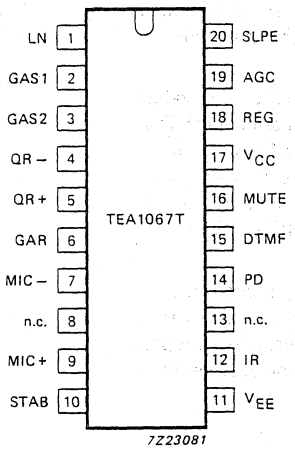
TEA1067

PINNING



1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

Fig. 2 (a) Pinning diagram for TEA1067 18-lead DIL version.



1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment, receiving amplifier
7	MIC–	inverting microphone input
8	n.c.	not connected
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	IR	receiving amplifier input
13	n.c.	not connected
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

Fig. 2 (b) Pinning diagram for TEA1067T 20-lead mini-pack version.

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1067 and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

The TEA1067 has an internal current stabilizer working at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig. 6). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.
The regulated voltage on the line terminal (V_{LN}) can be calculated as:

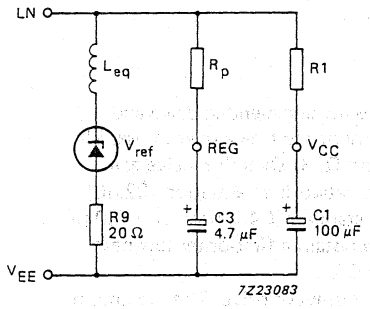
$$V_{LN} = V_{ref} + I_{SLPE} \times R9; \text{ or } V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^{-3}\,A) - I_p] \times R9$$

Where V_{ref} is an internally generated temperature compensated reference voltage of 3.6 V and R9 is an external resistor connected between SLPE and V_{EE}. In normal use the value of R9 would be 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, side-tone level and maximum output swing on LN, and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} \gg I_{CC} + 0.5\,mA + I_p$, the static behaviour of the circuit is that of a 3.6 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig. 3 shows the equivalent impedance of the circuit.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that the operation of more sets in parallel is possible with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. With line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor connected between LN and REG will decrease the internal reference voltage, connected between REG and SLPE it will increase the internal reference voltage.

Current (I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig. 9 shows this current for $V_{CC} > 2.2$ V. If MUTE is LOW when the receiving amplifier is driven the available current is further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1, as shown in Fig. 16 (c), or by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE.



$R_p = 16.2\ k\Omega$
$L_{eq} = C3 \times R9 \times R_p$

Fig. 3 Equivalent impedance circuit.

Microphone inputs (MIC+ and MIC−) and gain adjustment pins (GAS1 and GAS2)

The TEA1067 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Fig. 13). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are shown in Fig. 10.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by the external capacitor C6 which is connected between GAS1 and SLPE. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The cut-off frequency corresponds to the time constant R7 x C6.

Mute input (MUTE)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligible clicking on the earpiece outputs and line. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independent to the DC level applied to the MUTE input.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving Amplifier (IR, QR+, QR− and GAR)

The receiving amplifier has one input (IR), one non-inverting complementary output (QR+) and an inverting complementary output (QR−). These outputs may be used for single-ended or differential drive depending on the sensitivity and type of earpiece used (see Fig. 11). IR to QR + gain is typically 31 dB (when R4 = 100 kΩ), this is sufficient for low-impedance magnetic or dynamic microphones which are suited for single-ended drive. Using both outputs for differential drive gives an additional gain of 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω (high-impedance dynamic or piezoelectric types).

FUNCTIONAL DESCRIPTION (continued)

Receiving Amplifier (IR, QR+, QR− and GAR) (continued)

The receiving amplifier gain can be adjusted between 20 and 39 dB with single-ended drive and between 26 and 45 dB with differential drive, to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by substracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 x the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 x C4.
The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic gain control input (AGC)

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 12 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Power-down input (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted. During these interruptions the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input which reduces the typical supply current from 1 mA to 55 μA and switches off the voltage regulator preventing discharge through LN. When PD is HIGH the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit.

Side-tone suppression

The anti-sidetone network, $R1//Z_{line}$, R2, R3, R9 and Z_{bal}, (see Fig. 4) suppresses transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

(a) $R9 \times R2 = R1\ (R3 + [R8//Z_{bal}])$;

(b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3, and R9 then condition (a) will always be fulfilled when $|R8//Z_{bal}| \ll R3$. To obtain optimum side-tone suppression condition (b) has to be fulfilled resulting in:

$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$ where k is a scale factor; $k = (R8/R1)$

The scale factor (k), dependent on the value of R8, is chosen to meet the following criteria:

(a) Compatability with a standard capacitor from the E6 or E12 range for Z_{bal}

(b) $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensuring correct anti-sidetone bridge operation

(c) $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmitter gain

In practice Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The line balance impedance (Z_{bal}) at which the optimum suppression is present can be calculated by: suppose Z_{line} = 210 Ω + (1265 Ω/140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

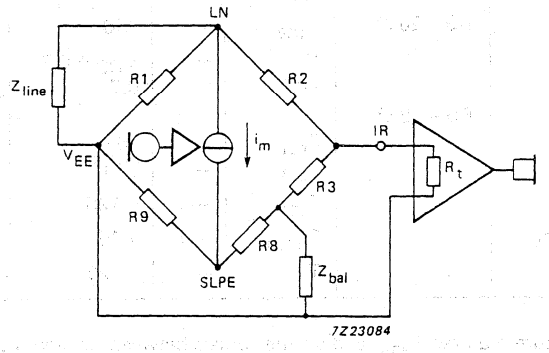


Fig. 4 Equivalent circuit of TEA1060 anti-sidetone bridge.

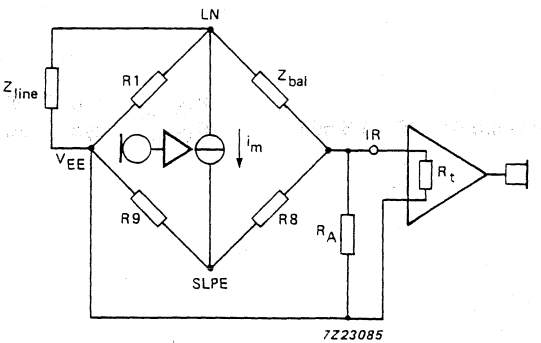


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

More information can be found in the designer guide; 9398 341 10011

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 15)	V_{LN}	–	28	V
Line current TEA1067(1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1067T (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		$-V_i$	–	0.7	V
Total power dissipation (2)	R9 = 20 Ω				
TEA1067		P_{tot}	–	769	mW
TEA1067T		P_{tot}	–	550	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

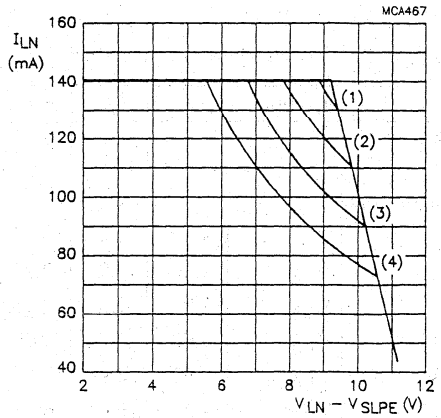
(1) Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 6 and 7 to determine the current as a function of the required voltage and the temperature.

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

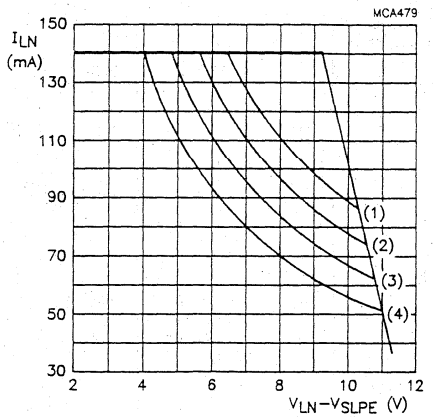
From junction to ambient in free air

TEA1067	$R_{th\ j\text{-}a}$	typ.	65	K/W
TEA1067T mounted on glass epoxy board 41 x 19 x 1.5 mm	$R_{th\ j\text{-}a}$	typ.	90	K/W



	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

Fig. 6 TEA1067 safe operating area.



	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

Fig. 7 TEA1067T safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply; LN and V_{CC}						
Voltage drop over circuit, between LN and V_{EE}	microphone inputs open					
	I_{line} = 1 mA	V_{LN}	–	1.6	–	V
	I_{line} = 4 mA	V_{LN}	1.75	2.0	2.25	V
	I_{line} = 7 mA	V_{LN}	2.25	2.8	3.35	V
	I_{line} = 11 mA	V_{LN}	3.55	3.8	4.05	V
	I_{line} = 15 mA	V_{LN}	3.65	3.9	4.15	V
	I_{line} = 100 mA	V_{LN}	4.9	5.6	6.5	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−3	−1	1	mV/K
Voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA; R_{VA} (LN to REG) = 68 kΩ		3.1	3.4	3.7	V
	I_{line} = 15 mA; R_{VA} (REG to SLPE) = 39 kΩ		4.2	4.5	4.8	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	1.0	1.35	mA
Supply current	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH					
	I_p = 1.4 mA	V_{CC}	2.2	2.4	–	V
	I_p = 0 mA	V_{CC}	2.95	3.2	–	V
Microphone inputs MIC+ and MIC−						
Input impedance (differential) between MIC− and MIC+		$\|Z_i\|$	51	64	77	kΩ
Input impedance (single-ended) MIC− or MIC+ to V_{EE}		$\|Z_i\|$	25.5	32	38.5	kΩ
Common mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain MIC+/MIC− to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Microphone inputs MIC+ and MIC− (continued)						
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	± 0.2	+0.5	dB
Gain variation with temperature at −25 °C and +75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	−	± 0.2	−	dB
Dual-tone multi-frequency input DTMF						
Input impedance		$\lvert Z_i \rvert$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t 800 Hz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Gain variation with temperature at −25 °C and +75 °C	w.r.t. 25 °C I_{line} = 50 mA	ΔG_{vT}	−	±0.2	−	dB
Gain adjustment GAS1 and GAS2						
Gain variation of the transmitting amplifier by varying R7 between GAS1 and GAS2		ΔG_v	−8	−	0	dB
Sending amplifier output LN						
Output voltage	I_{line} = 15 mA THD = 2%	$V_{LN(rms)}$	−	1.9	−	V
	THD = 10%	$V_{LN(rms)}$	1.9	2.2	−	V
	I_{line} = 4 mA; THD = 10%	$V_{LN(rms)}$	−	0.8	−	V
	I_{line} = 7 mA; THD = 10%	$V_{LN(rms)}$	−	1.4	−	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC− and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	−	−72	−	dBmp

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier input IR						
Input impedance		$\|Z_i\|$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR−						
Output impedance (single-ended)		$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR+ or QR−	I_{line} = 15 mA R4 = 100 kΩ					
single-ended	R_L (from QR+ or QR−) = 300 Ω	G_v	30	31	32	dB
differential	R_L (from QR+ or QR−) = 600 Ω	G_v	36	37	38	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	−0.2	0	dB
Gain variation with temperature at −25 °C and +75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	–	±0.2	–	dB
Output voltage	sinewave drive I_{line} = 15 mA; I_p = 0 mA; THD = 2% R4 = 100 kΩ					
single-ended	RL = 150 Ω	$V_{o(rms)}$	0.25	0.29	–	V
	RL = 450 Ω	$V_{o(rms)}$	0.45	0.55	–	V
differential	f = 3400 Hz; series R = 100 Ω; C_L = 47 nF	$V_{o(rms)}$	0.65	0.80	–	V
Output voltage	THD = 10%; RL = 150 Ω R4 = 100 kΩ					
	I_{line} = 4 mA	$V_{o(rms)}$	–	15	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	130	–	mV
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted; (P53 curve)					
single-ended	RL = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	RL = 600 Ω	$V_{no(rms)}$	–	100	–	μV

parameter	conditions	symbol	min.	typ.	max.	unit
Gain adjustment GAR						
Gain variation of receiving amplifier achievable by varying R4 between GAR and QR		ΔG_v	−11	–	+8	dB
Mute input						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Gain reduction MIC+ or MIC− to LN	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC Controlling the gain from IR to QR+/QR− and the gain from MIC+/MIC− to LN; R6 between AGC and V_{EE}	R6 = 110 kΩ					
Gain control range	I_{line} = 70 mA	ΔG_v	−5.5	−5.9	−6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Minimum line current for minimum gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		ΔG_v	−1.0	−1.5	−2.0	dB

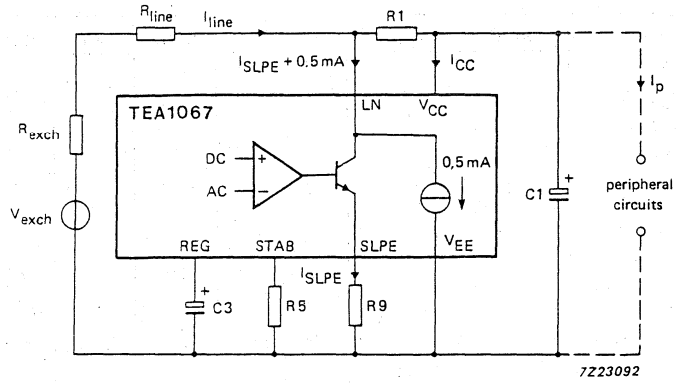
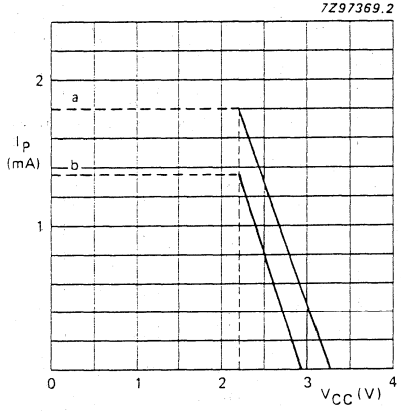


Fig. 8 Supply arrangement.



(a) I_p = 1.8 mA
(b) I_p = 1.35 mA
I_{line} = 15 mA at V_{LN} = 3.9 V
R1 = 620 Ω and R9 = 20 Ω.

Fig. 9 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} >= 2.2$ V. Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)}$ = 150 mV, R_L = 150 Ω asymmetrical.
The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

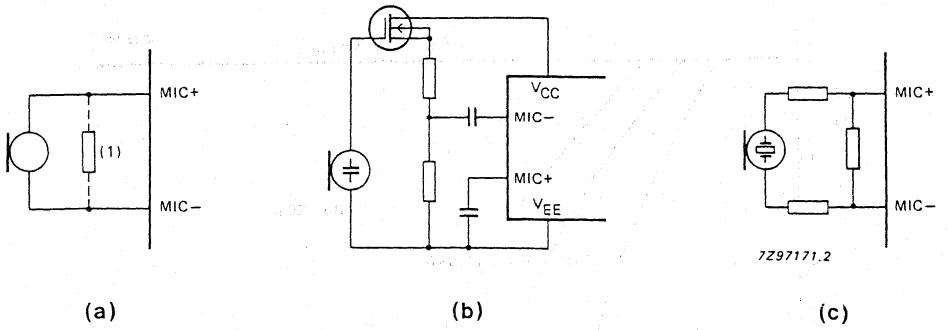


Fig. 10 Alternative microphone arrangements.

(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.
(b) Electret microphone.
(c) Piezoelectric microphone.

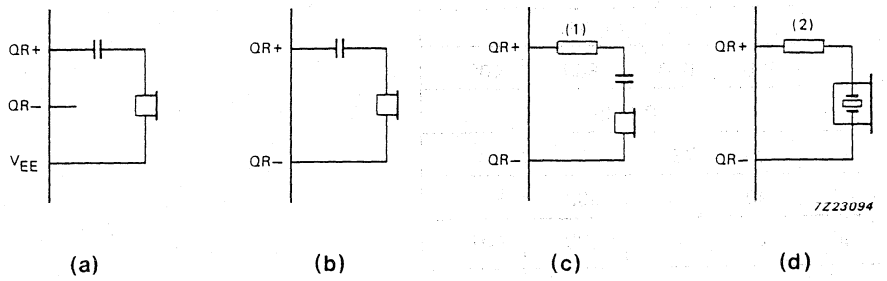


Fig. 11 Alternative receiver arrangements.

(a) Dynamic earpiece with less than 450 Ω impedance.
(b) Dynamic earpiece with more than 450 Ω impedance.
(c) Magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load).
(d) Piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

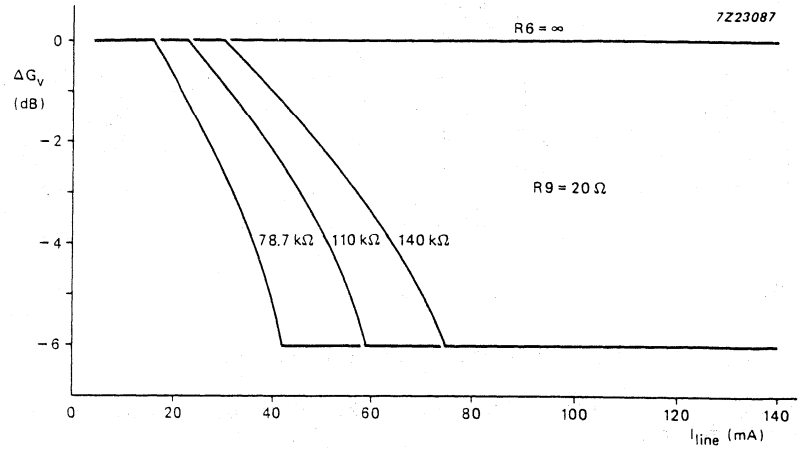


Fig. 12 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	100	78.7	X	X
	48	140	110	93.1	82
	60	X	X	120	102

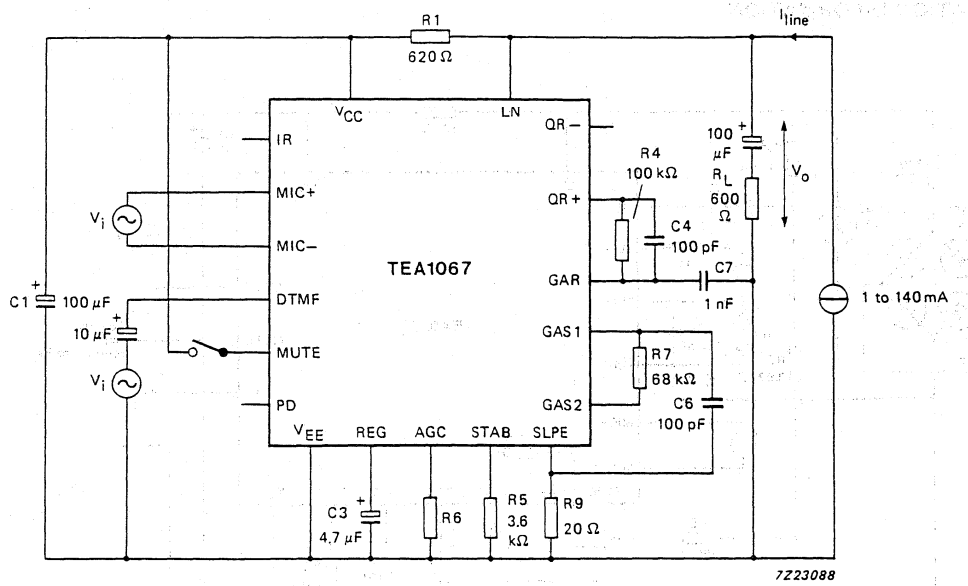


Fig. 13 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_V = 20 \log |V_O/V_I|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

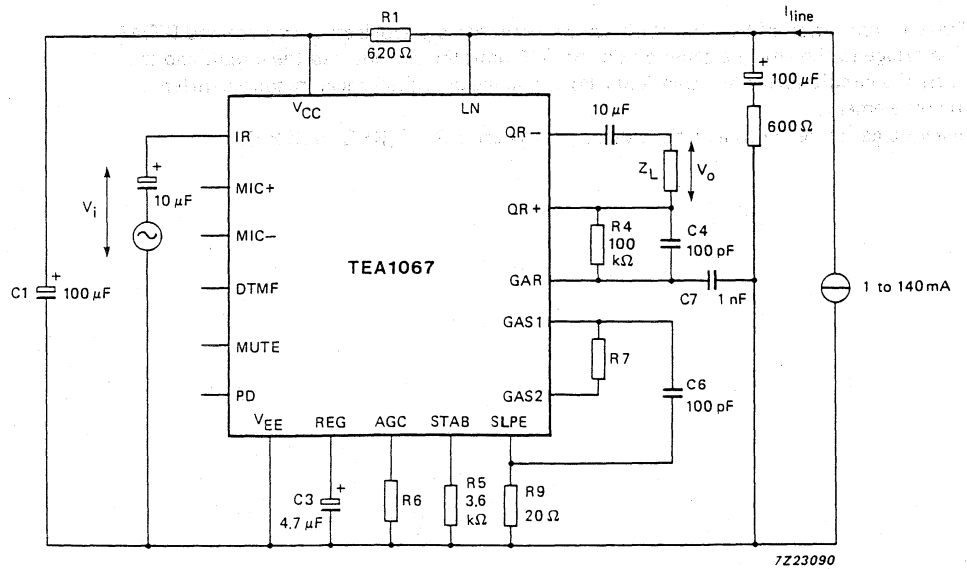


Fig. 14 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_V = 20 \log |V_O/V_I|$.

APPLICATION INFORMATION

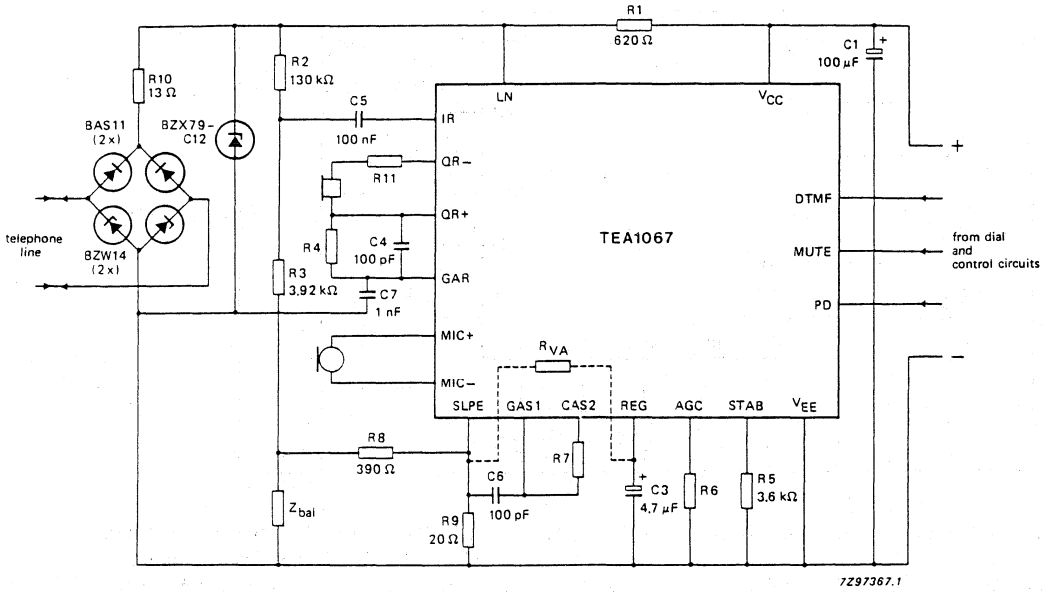


Fig. 15 Typical application of the TEA1067, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left, the zener diode and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.
The DC line voltage can be set to a higher value by the resistor R_{VA} (REG to SLPE).

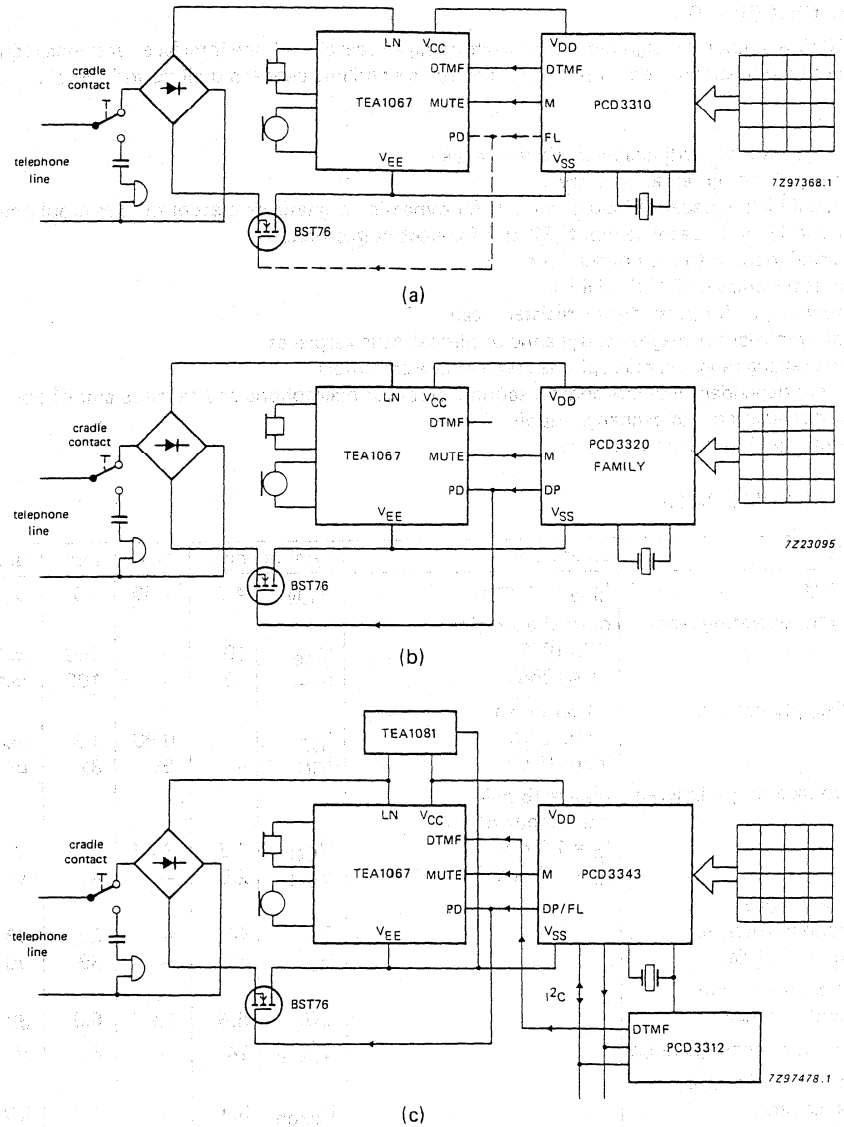


Fig. 16 Typical applications of the TEA1067 (simplified).

(a) DTMF-Pulse set with CMOS dialling circuit PCD3310.
The dashed lines show an optional flash (register recall by timed loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

Versatile telephone transmission circuit with dialler interface

TEA1068

GENERAL DESCRIPTION

The TEA1068 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech.

Features

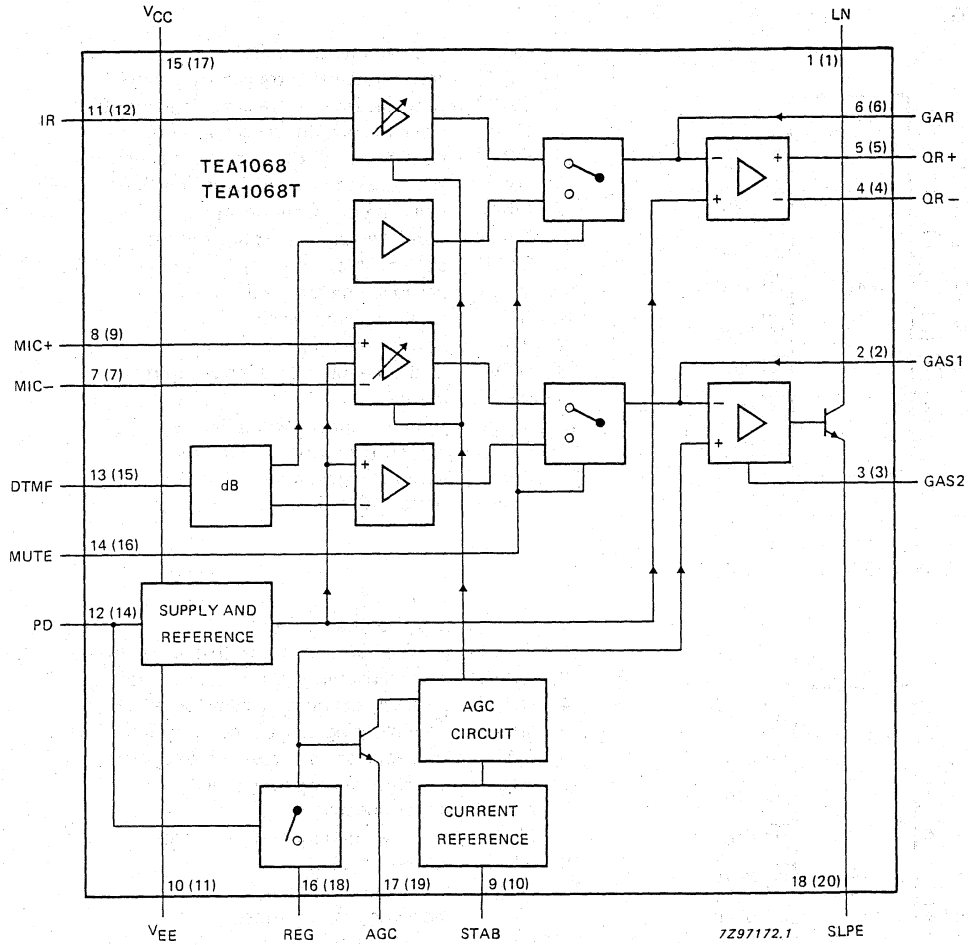
- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment capability.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	4.2	4.45	4.7	V
Line current operating range	normal operation					
	TEA1068	I_{line}	10	–	140	mA
	TEA1068T	I_{line}	10	–	100	mA
Internal supply current	power down					
	input LOW	I_{CC}	–	0.96	1.3	mA
	input HIGH	I_{CC}	–	55	82	μA
Supply voltage for peripherals	I_{line} = 15 mA; mute input HIGH					
	I_p = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_p = 1.7 mA	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier		G_v	44	–	60	dB
receiving amplifier		G_v	17	–	39	dB
Line loss compensation gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	24	–	60	V
Exchange feeding bridge resistance range		R_{exch}	0.4	–	1	kΩ

PACKAGE OUTLINES

TEA1068: 18-lead DIL; plastic (SOT102).
TEA1068T: 20-lead mini-pack; plastic (SO20; SOT163A).



Figures in parenthesis refer to TEA1068T.

Fig. 1 Block diagram.

Versatile telephone transmission circuit with dialler interface

TEA1068

PINNING

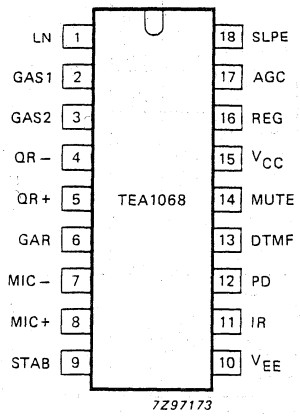


Fig. 2 (a) Pinning diagram for TEA1068 18-lead DIL version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

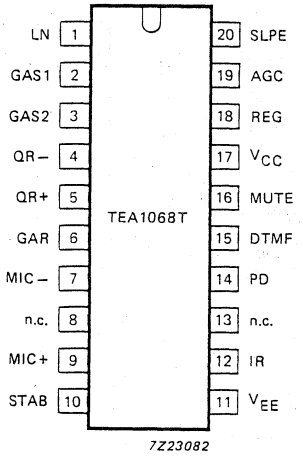


Fig. 2 (b) Pinning diagram for TEA1068T 20-lead mini-pack version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	n.c.	not connected
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	IR	receiving amplifier input
13	n.c.	not connected
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply; V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1068 and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

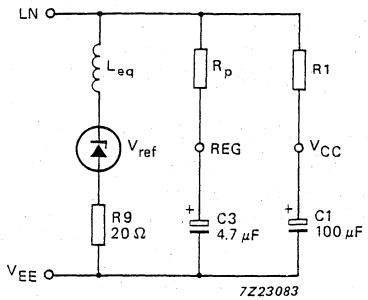
The TEA 1068 has an internal current stabilizer operating at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig. 8). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.
The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9; \text{ or } V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^{-3}) - I_p] \times R9$$

Where V_{ref} is an internally generated temperature compensated reference voltage of 4.2 V and R9 is an external resistor connected between SLPE and V_{EE}. In normal use the value of R9 would be 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics side-tone level and maximum output swing on LN, and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} \gg I_{CC} + 0.5\ mA + I_p$, the static behaviour of the circuit is that of a 4.2 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig. 3 shows the equivalent impedance of the circuit.

The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor connected between LN and REG will decrease the internal reference voltage, connected between REG and SLPE it will increase the internal reference voltage.
Current (I_p) available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Figure 9 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} \geq 3$ V (being the minimum supply voltage for most CMOS circuits including voltage drop for an enable diode).
If MUTE is LOW when the receiving amplifier is driven available current is further reduced.



$R_p = 17.5\ k\Omega$
$L_{eq} = C3 \times R9 \times R_p$

Fig. 3 Equivalent impedance circuit.

Microphone inputs (MIC+ and MIC−) and gain adjustment pins (GAS1 and GAS2)

The TEA1068 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Fig. 13). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are shown in Fig. 10.

The gain of the microphone amplifier can be adjusted between 44 dB and 60 dB. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by the external capacitor C6 which is connected between GAS1 and SLPE. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The cut-off frequency corresponds to the time constant R7 x C6.

Mute input (MUTE)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligable clicking on the earpiece outputs and the line.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the telephone earpiece at a low level (confidence tone).

Receiving amplifier (IR, QR+, QR− and GAR)

The receiving amplifier has one input (IR), one non-inverting complementary output (QR+) and an inverting complementary output (QR−). These outputs may be used for single-ended or differential drive depending on the sensitivity and type of earpiece used (see Fig. 11). IR to QR + gain is typically 25 dB (when R4 = 100 kΩ), this is sufficient for low-impedance magnetic or dynamic microphones which are suited for single end drive. Using both outputs for differential drive gives an additional gain of 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω, (high-impedance dynamic or piezoelectric types).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

FUNCTIONAL DESCRIPTION (continued)

Receiving amplifier (IR, QR+, QR− and GAR) (continued)

The receiving amplifier gain can be adjusted between 17 and 33 dB with single-ended drive and between 26 and 39 dB with differential drive to match the sensitivity of the transducer in use. The gain is set by the external resistor R4 connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by subracting the anti-sidetone network attenuation, (32 dB), from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 x the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 x C4.

Automatic gain control input (AGC)

Automatic line loss compensation is acieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 12 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Power-down input (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted. During these interruptions the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input which reduces the typical supply current from 1 mA to 55 μA and switches off the voltage regulator preventing discharge through LN. When PD is HIGH the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit.

Side-tone suppression

The anti-sidetone network, ($R1//Z_{line}$, R2, R3 and Z_{bal}), (see Fig. 4) suppresses transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

(a) $R9 \times R2 = R1\ (R3 + [R8//Z_{bal}])$;

(b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3, and R9 then condition (a) will always be fulfilled when $|R8//Z_{bal}| \ll R3$. To obtain optimum side-tone suppression condition (b) has to be fulfilled resulting in;

$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$ where k is a scale factor, $k = (R8/R1)$.

The scale factor (k), dependent on the value of R8, is chosen to meet the following criteria:

(a) Compatability with a standard capacitor from the E6 or E12 range for Z_{bal}

(b) $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensuring correct anti-sidetone bridge operation

(c) $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmitter gain

In practice Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The balanced line impedance (Z_{bal}) at which the optimum suppression is present can be calculated by: suppose Z_{line} = 210 Ω + (1265 Ω/140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

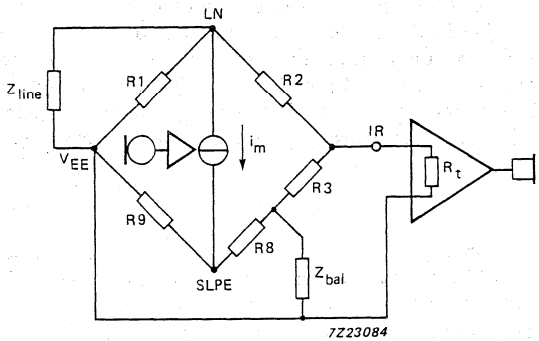


Fig. 4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

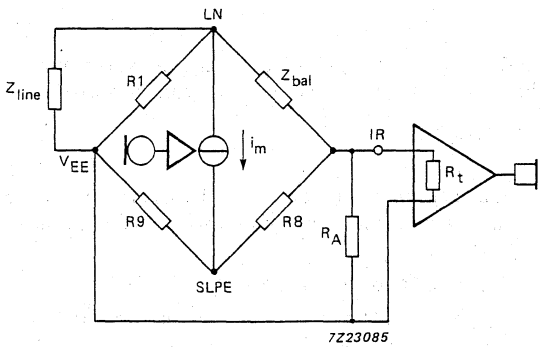


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

More information can be found in the designer guide; 9398 341 10011

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 15)	V_{LN}	–	28	V
Line current TEA1068 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1068T (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		V_i	–	−0.7	V
Total power dissipation (2)	R9 = 20 Ω				
TEA1068		P_{tot}	–	769	mW
TEA1068T		P_{tot}	–	555	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

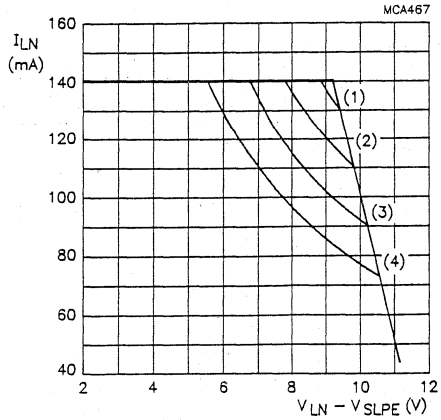
(1) Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 6 and 7 to determine the current as a function of the required voltage and the temperature.

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

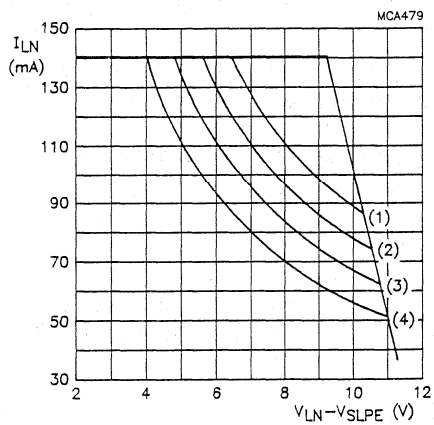
From junction to ambient in free air

TEA1068	$R_{th\ j\text{-}a}$	typ.	65	K/W
TEA1068T mounted on glass epoxy board 41 x 19 x 1.5 mm	$R_{th\ j\text{-}a}$	typ.	90	K/W



	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

Fig. 6 TEA1068 safe operating area.



	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

Fig. 7 TEA1068T safe operating area.

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz, T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply, LN and V_{CC}						
Voltage drop over circuit, between LN and V_{EE}	microphone inputs open					
	I_{line} = 5 mA	V_{LN}	3.95	4.25	4.55	V
	I_{line} = 15 mA	V_{LN}	4.2	4.45	4.7	V
	I_{line} = 100 mA	V_{LN}	5.4	6.1	6.7	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA; R_{VA} (LN to REG) = 68 kΩ		3.45	3.8	4.1	V
	I_{line} = 15 mA; R_{VA} (REG to SLPE) = 39 kΩ		4.65	5.0	5.35	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	0.96	1.3	mA
Supply current	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH					
	I_p = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_p = 0 mA	V_{CC}	3.5	3.75	–	V
Microphone inputs MIC+ and MIC−						
Input impedance (differential) between MIC− and MIC+		$\|Z_i\|$	51	64	77	kΩ
Input impedance (single-ended) MIC− or MIC+ to V_{EE}		$\|Z_i\|$	25.5	32	38.5	kΩ
Common mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain MIC+/MIC− to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	± 0.2	+0.5	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Microphone inputs MIC+ and MIC– (continued)						
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C; without R6; I_{line} = 50 mA	ΔG_{vT}	–	± 0.2	–	dB
Dual-tone multi-frequency input DTMF						
Input impedance		$\lvert Z_i \rvert$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF ro LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t 800 Hz	ΔG_{vf}	–0.5	± 0.2	+ 0.5	dB
Gain variation with temperature at – 25 °C and + 75 °C	w.r.t 25 °C I_{line} = 50 mA	ΔG_{vT}	–	± 0.5	–	dB
Gain adjustement GAS1 and GAS2						
Gain variation of the transmitting amplifier by varying R7 between GAS1 and GAS2		ΔG_v	–8	–	+8	dB
Sending amplifier output LN						
Output voltage	I_{line} = 15 mA THD = 2%	$V_{LN(rms)}$	1.9	2.3	–	V
	THD = 10%	$V_{LN(rms)}$	–	2.6	–	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp
Receiving amplifier input IR						
Input impedance		$\lvert Z_i \rvert$	17	21	25	kΩ

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier outputs QR+ and QR−						
Output impedance (single-ended)		$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR+ or QR−	I_{line} = 15 mA					
single-ended	R_L (from QR+ or QR−) = 300 Ω	G_v	24	25	26	dB
differential	R_L (from QR+ or QR−) = 600 Ω	G_v	30	31	32	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	−0.2	0	dB
Gain variation with temperature at −25 °C and +75 °C	w.r.t. 25 °C; I_{line} = 50 mA; without R6	ΔG_{vT}	–	± 0.2	–	dB
Output voltage	sinewave drive; I_{line} = 15 mA; I_p = 0 mA; THD = 2%; R4 = 100 kΩ					
single-ended	RL = 150 Ω	$V_{o(rms)}$	0.3	0.38	–	V
	RL = 450 Ω	$V_{o(rms)}$	0.4	0.52	–	V
differential	f = 3400 Hz; series R = 100 Ω; C_L = 47 nF	$V_{o(rms)}$	0.8	1.0	–	V
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted; (P53 curve)					
single-ended	RL = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	RL = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR						
Gain variation of receiving amplifier achievable by varying R4 between GAR and QR		ΔG_v	−8	–	+8	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Mute input						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Gain reduction MIC+ or MIC– to LN	MUTE = HIGH	G_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR–	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	G_v	–21	–19	–17	dB
Power-down input PD						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC						
Controlling the gain from IR to QR+/QR– and the gain from MIC+/MIC– to LN; R6 between AGC and V_{EE}	R6 = 110 kΩ					
Gain control range	I_{line} = 70 mA	ΔG_v	–5.5	–5.9	–6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Minimum line current for minimum gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		ΔG_v	–1.0	–1.5	–2.0	dB

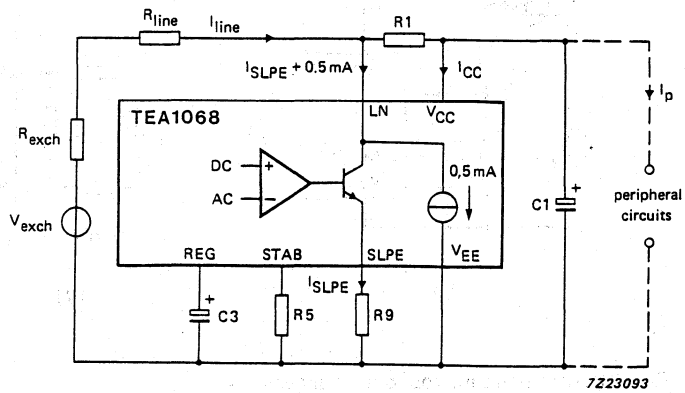


Fig. 8 Supply arrangement.

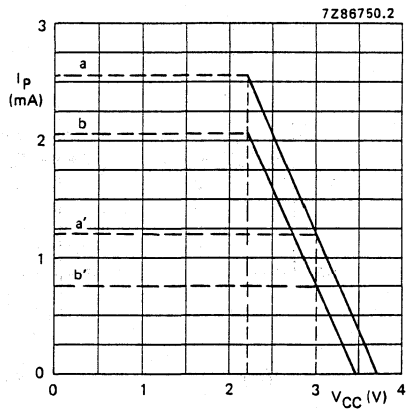


Fig. 9 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} >= 2.2$ V. Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)} = 150$ mV, $R_L = 150\ \Omega$ asymmetrical. The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

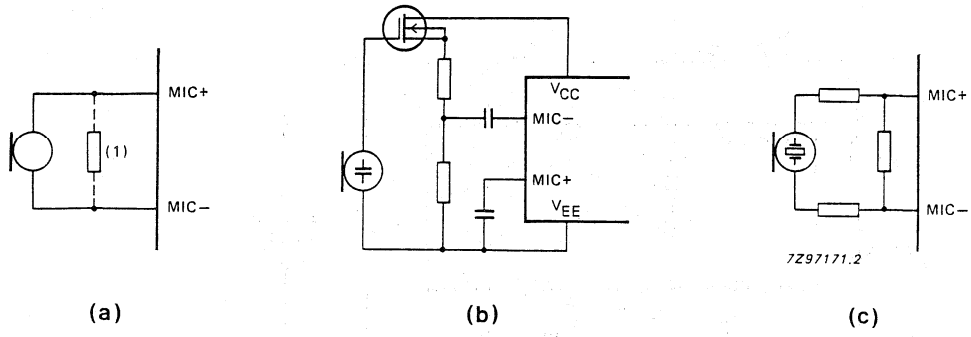


Fig. 10 Alternative microphone arrangements.

(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.
(b) Electret microphone.
(c) Piezoelectric microphone.

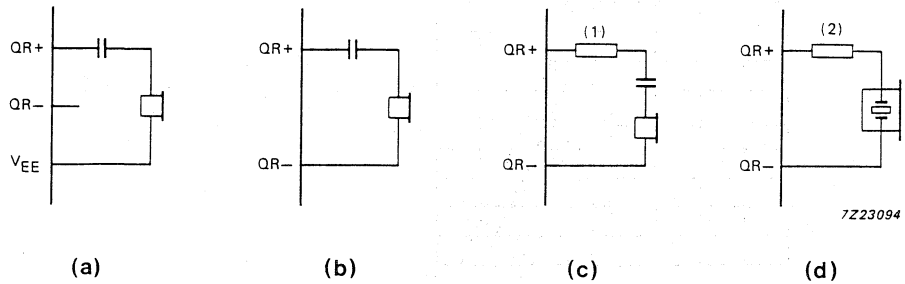


Fig. 11 Alternative receiver arrangements.

(a) Dynamic earpiece with less than 450 Ω impedance.
(b) Dynamic earpiece with more than 450 Ω impedance.
(c) Magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load).
(d) Piezoelectric telephone. The resistor marked (2) is required to increase the phase margin (capacitive load).

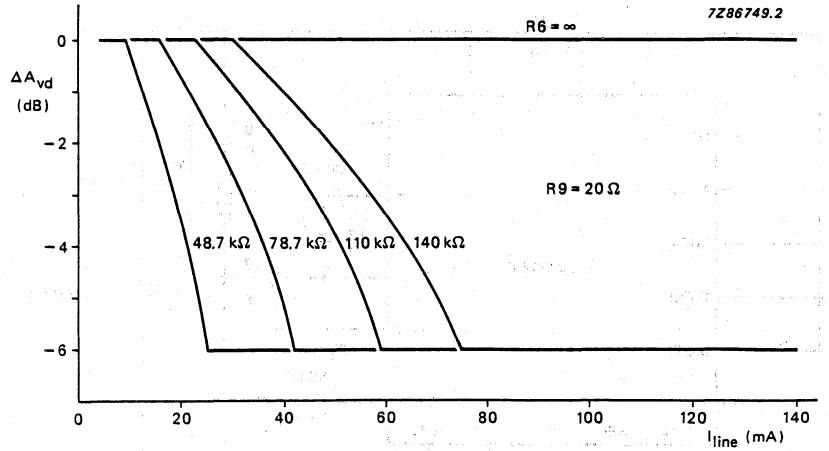


Fig. 12 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (KΩ)			
V_{exch} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

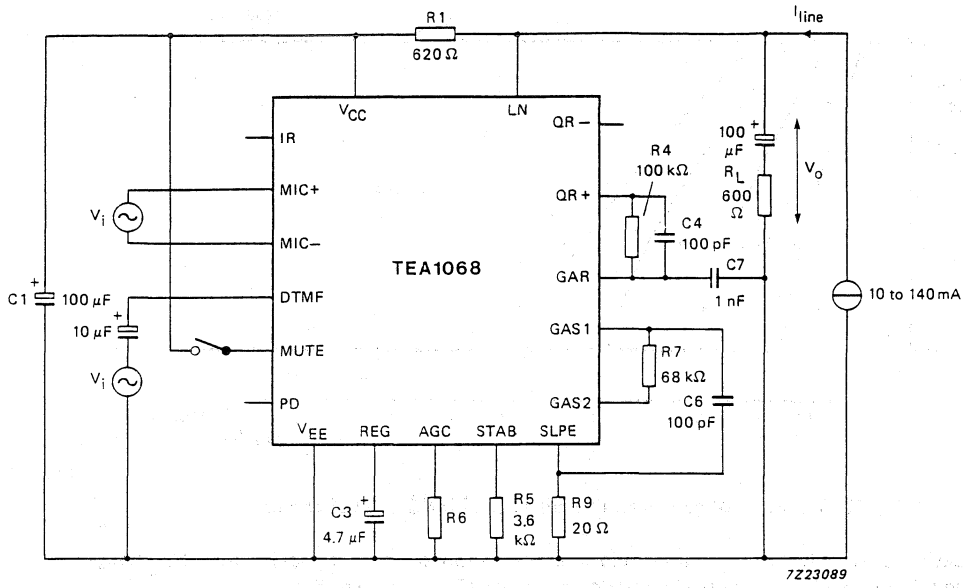


Fig. 13 Test circuit for defining voltage gain of MIC+, MIC− and DTMF inputs. Voltage gain is defined as; $G_V = 20 \log |V_O/V_i|$. For measuring the gain from MIC+ and MIC− the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

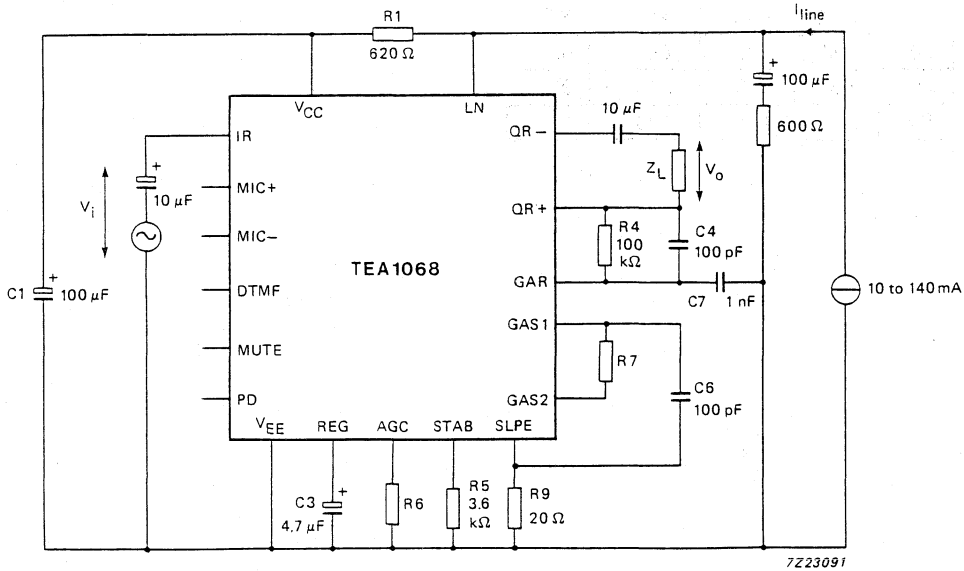


Fig. 14 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_V = 20 \log |V_O/V_i|$.

APPLICATION INFORMATION

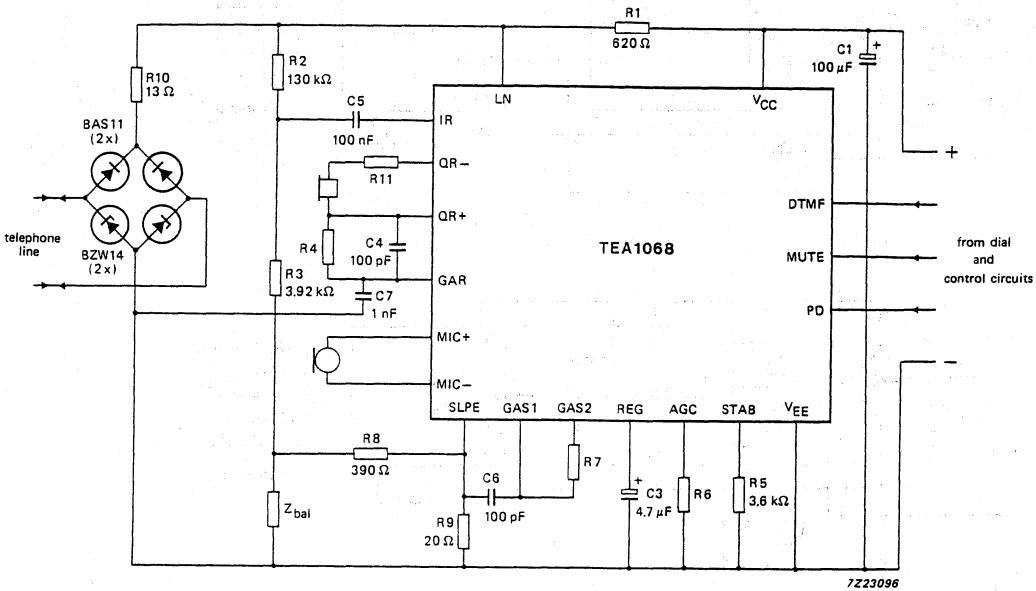
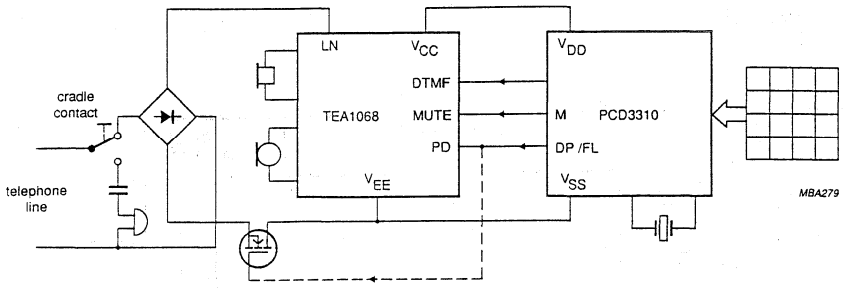
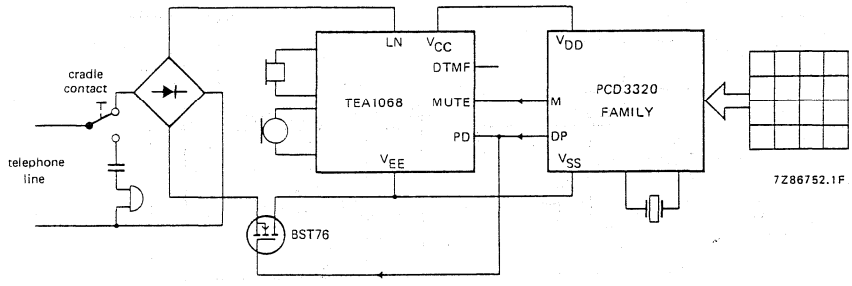


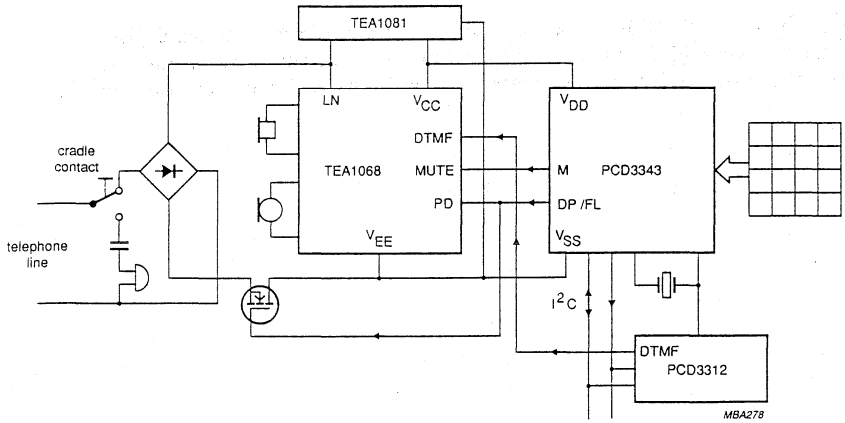
Fig. 15 Typical application of the TEA1068, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.



(a)



(b)



(c)

Fig. 16 Typical applications of the TEA1068 (simplified).

(a) DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by times loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C-bus. The supply is provided by TEA1081 supply circuit.

Supply circuit with power-down for telephone set peripherals

TEA1081

FEATURES

- High input impedance for audio signals
- Low DC series resistance
- High output current
- Large audio signal handling capability
- Low distortion
- Two modes of operation:
  - output voltage that follows the DC line voltage
  - regulated output voltage
- Power-down input
- Low number of external components.

GENERAL DESCRIPTION

The TEA1081 is an integrated circuit for use in line-powered telephone sets to supply peripheral circuits for extended dialling and/or loudspeaker facilities.

The IC uses a part of the surplus line current normally drawn by the voltage regulator of the speech/transmission circuit. A power-down function isolates the IC from its load and reduces the input current.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	operating DC line voltage		2.5	–	12.0	V
V_O	DC output voltage		2.0	–	10.0	V
ΔV_{LN-O}	voltage drop from line to output	I_O = 0 mA	–	0.5	–	V
R_S	internal series resistance		–	20	–	Ω
I_O	output current (pin 7)	V_{LN} = 4 V				
	TEA1081		–	–	30	mA
	TEA1081T		–	–	20	mA
$V_{LN(rms)}$	AC line voltage (RMS value)	V_{LN} = 4 V; I_O = 15 mA; THD = 2%	–	1.5	–	V
I_{INT}	internal supply current	V_{LN} = 4 V; I_O = 0 mA; PD = LOW; $V_{SP} = V_O$	–	0.8	1.4	mA
T_{amb}	operating ambient temperature		−25	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1081	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TEA1081T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Supply circuit with power-down for telephone set peripherals

TEA1081

BLOCK DIAGRAM

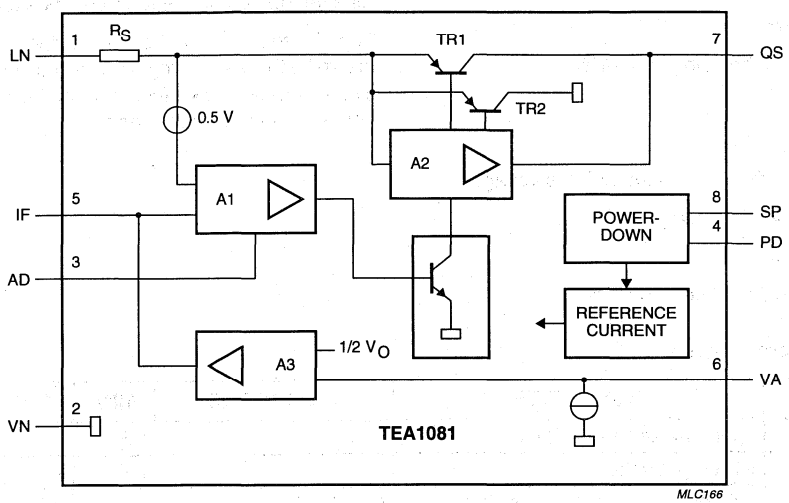


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
VN	2	negative line terminal
AD	3	amplifier decoupling
PD	4	power-down input
IF	5	low-pass filter input
VA	6	output voltage adjustment
QS	7	power supply output
SP	8	supply input; power-down circuit

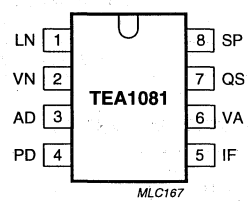


Fig.2 Pin configuration.

Supply circuit with power-down for telephone set peripherals

TEA1081

FUNCTIONAL DESCRIPTION

The TEA1081 is a supply interface between telephone line and peripheral devices in the telephone set. The high input impedance of the circuit allows direct connection to the telephone line (via a diode bridge). An inductor function is obtained by amplifier A1, resistor R_S (see Fig.1) and an external low-pass RC filter.

Under the control of amplifier A2, transistor TR1 supplies peripheral devices and transistor TR2 minimizes line signal distortion by momentarily diverting input current to ground whenever the instantaneous value of the line voltage drops below the output voltage.

Internal circuits are biased by a temperature and line voltage compensated reference current source.

The power-down circuit isolates the supply circuit from external circuitry.

Line terminals: LN and VN (pins 1 and 2)

The input terminals LN and VN can be connected directly to the line. The minimum DC line voltage required at the input is expressed by formula (1); see also Table 1.

$$V_{LN} = I_1 \times R_S + V_{LNmin} + V_{LN(P)} \text{ (V)} \quad (1)$$

Table 1 Explanation of formula (1).

SYMBOL	DESCRIPTION
I_1	input current
R_S	internal series resistance
V_{LNmin}	minimum instantaneous line voltage (1.4 V at I_O = 5 mA)
$V_{LN(P)}$	required peak level of AC line voltage

The internal current (I_{INT}) at I_O = 0 mA is typically 0.8 mA at V_{LN} = 4 V and reaches a maximum of 1.4 mA at V_{LN} = 12 V.

Supply terminals: QS and VA (pins 7 and 6)

Peripheral devices are supplied from QS (pin 7). Two modes of output voltage regulation are available.

OUTPUT VOLTAGE FOLLOWS LINE VOLTAGE (SEE FIG.3)

The TEA1081 operates in this mode when there is no external resistor (R_V) between QS and VA (see Fig.6).

The output voltage follows the line voltage and is expressed by formula (2); see also Table 2.

$$V_O = V_{LN} - (I_1 \times R_S + 0.5) \text{ (V)} \quad (2)$$

Table 2 Explanation of formula (2).

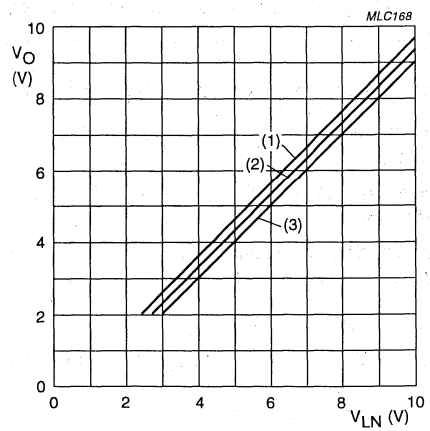
SYMBOL	DESCRIPTION
V_{LN}	line voltage
I_1	input current
R_S	internal series resistance

REGULATED OUTPUT VOLTAGE (SEE FIG.4)

The circuit operates in this mode when an external resistor (R_V) is connected between QS and VA (see Fig.6).

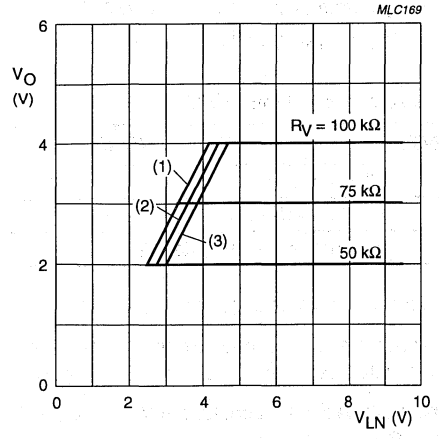
The output voltage is held constant at $V_O = 2 \times I_6 \times R_V$ (V) as soon as the line voltage
$V_{LN} > (2 \times I_6 \times R_V + I_1 \times R_S + 0.5)$ (V)

The control current I6 is typically 20 μA.



Application without R_V.
(1) I_1 = 5 mA.
(2) I_1 = 20 mA.
(3) I_1 = 30 mA; not valid for TEA1081T.

Fig.3 Output voltage as a function of line voltage.



R_V connected between QS and VA.
(1) I_1 = 5 mA.
(2) I_1 = 20 mA.
(3) I_1 = 30 mA; not valid for TEA1081T.

Fig.4 Output voltage as a function of line voltage.

Input and output currents I_1 and I_O (pins 1 and 7)

The maximum available current into pin 1 (I_1) is determined by:

- The minimum line current ($I_{LINEmin}$) that is available for the telephone set
- The specified minimum input current (I_{LNmin}) for the speech/transmission circuit.

That is $I_{1max} = I_{LINEmin} - I_{LNmin}$.

At $V_{LN(rms)} < 150$ mV, the input current I_1 is approximately:

$I_1 = I_{INT} + k \times I_O$ (mA)

Where:

I_{INT} = internal supply current (0.8 mA at V_{LN} = 4 V);

k = correction factor (k < 1.1 for the specified output current range).

With large line signals the instantaneous line voltage may drop below V_O + 0.4 V. Normally (when $V_{LN} > V_O$ + 0.4 V), instantaneous current flows from LN to QS (pin 1 to pin 7) to the output load.

When $V_{LN} < V_O$ + 0.4 V, the instantaneous current is diverted to pin 2 to prevent distortion of the line signal.

Input current at $V_{LN(rms)}$ = 1 V and without R_V approximates to:

$I_1 = I_{INT} + 2 \times I_O$ (mA)

The maximum supply current (within the specified output current limits) available for peripheral devices is shown by:

$$I_{Omax} = \frac{I_{LINEmin} - I_{LNmin} - I_{INT}}{2}$$

Where:

$I_{LINEmin}$ is the minimum line current of the telephone set;

I_{LNmin} is the specified minimum input current of the speech/transmission circuit.

Input low-pass filter: IF (pin 5)

The input impedance between LN and VN at audio frequencies is determined by the filter elements C_L (between pins 1 and 5), R_L (between pins 5 and 7) and the internal resistor R_S (typical value 20 Ω).

At audio frequencies the TEA1081 behaves as an inductor of the value $L_I = C_L \times R_L \times R_S$ (H). The typical value of L_I at C_L = 2.2 µF and R_L = 100 kΩ is 4.4 H.

Amplifier decoupling: AD (pin 3)

To ensure stability, a 68 pF decoupling capacitor is required between AD (pin 3) and LN (pin 1).
If $I_{Omin} < 1.5$ mA, a 47 pF capacitor has to be added between AD (pin 3) and VA (pin 6).

Power-down inputs: PD and SP (pins 4 and 8)

During pulse dialling or register recall, or if the input current to pin 1 is insufficient to maintain the output current, the supply to peripheral devices can be switched off by activating the PD input at pin 4. With PD = HIGH, the input current is reduced to 40 µA (typ.) at V_{LN} = 4 V and the internal circuits are isolated from the load at QS (pin 7).

The power-down circuit is supplied via the SP input (pin 8). SP can be wired to QS in conditions where $V_O > V_{SPmin}$ during line interruptions. When $V_O < V_{SPmin}$, SP should be wired to an external supply point (e.g. to V_{CC} of the TEA1060 family circuit).

When power-down is not required, the PD and SP inputs can be left open-circuit.

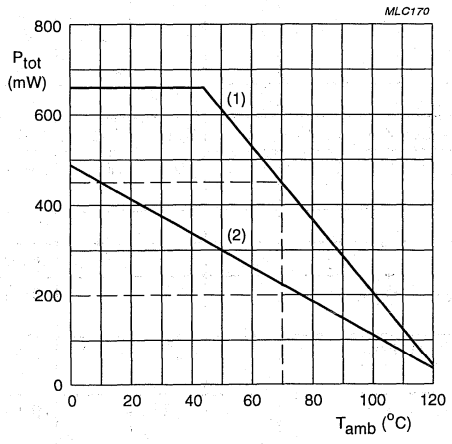
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage	continuous	–	12	V
		during switch-on or line interruptions	–	12.5	V
$V_{LN(RM)}$	repetitive peak line voltage for a 1 ms pulse per 5 s	12 Ω resistor in series with pin 1	–	28	V
V_I	input voltage (all other terminals)		V_{VN} – 0.5	V_{LN} + 0.5	V
I_1	DC input current				
	TEA1081		–	120	mA
	TEA1081T		–	80	mA
I_I	input current (all other terminals)		–1	+1	mA
P_{tot}	total power dissipation		see Fig.5		
T_{amb}	operating ambient temperature		–25	+70	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		–	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1081	120	K/W
	TEA1081T (mounted on a printed-circuit board of 50 × 50 × 1.5 mm)	260	K/W



(1) TEA1081.
(2) TEA1081T.

Fig.5 Power derating curves.

CHARACTERISTICS

V_{LN} = 4 V; $V_{LN(rms)}$ = 100 mV; I_O = 5 mA; f = 300 to 3400 Hz; R_L = 100 kΩ; C_L = 2.2 µF; R_V = 75 kΩ; T_{amb} = 25 °C; unless otherwise specified; see Fig.6.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	operating DC line voltage		2.5	–	12.0	V
V_{LNmin}	minimum instantaneous line voltage		–	–	1.4	V
V_{LNmax}	maximum instantaneous line voltage		12.0	–	–	V
Characteristics with R_V = 75 kΩ connected between pins 6 and 7 and C_L = 10 µF						
I_1	input current (pin 1)	$V_{LN(rms)}$ = 0 V	–	5.8	–	mA
		$V_{LN(rms)}$ = 1.5 V; I_O = 15 mA	–	30	–	mA
V_O	output voltage (pin 7)		–	3.0	–	V
ΔV_O	variation of output voltage over the ranges of:					
	line voltage	V_{LN} = 4 to 6 V	–	100	–	mV
	temperature	T_{amb} = +25 to −25 °C	–	−100	–	mV
	temperature	T_{amb} = +25 to +75 °C	–	−100	–	mV
	output current	I_O = 5 to 20 mA	–	−100	–	mV
I_6	control current (pin 6)		–	20	–	µA
Characteristics without R_V						
I_1	input current (pin 1)	$V_{LN(rms)}$ = 0 V	–	6.0	–	mA
		$V_{LN(rms)}$ = 1.5 V; I_O = 15 mA	–	31	–	mA
ΔV_{LN-O}	voltage drop from line to output	I_O = 0 mA	–	0.5	–	V
		I_O = 15 mA; $V_{LN(rms)}$ = 1.5 V	–	1.1	–	V
I_O	output current (pin 7)					
	TEA1081		–	–	30	mA
	TEA1081T		–	–	20	mA
R_S	internal series resistance		–	20	–	Ω
I_{INT}	internal supply current	I_O = 0 mA; PD = LOW; V_{SP} = V_O	–	0.8	1.4	mA
		I_O = 0 mA; PD = HIGH (note 1); V_{SP} > 2 V	–	40	60	µA
THD	total harmonic distortion	$V_{LN(rms)}$ = 1.5 V	–	–	2	%
BRL	balance return loss	600 Ω reference	25	–	–	dB
$V_{LN(2H)}$	second harmonic level of line voltage	f = 500 Hz; V_{LN} = 0 dBm; Z_{line} = 600 Ω	–	−58	–	dBm
$V_{LN(3H)}$	third harmonic level of line voltage	f = 500 Hz; V_{LN} = 0 dBm; Z_{line} = 600 Ω	–	−60	–	dBm
$V_{ni(rms)}$	noise voltage on input terminal (RMS value)	$V_{LN(rms)}$ = 0 V; R_L = 600 Ω; P53 curve	–	−83	–	dBmp
Power-down input (pin 4)						
V_{IL}	LOW level input voltage		–	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{SP}	V
I_4	input current		–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-down input (pin 8)						
V_8	supply voltage for power-down		2	–	V_{LN}	V
I_8	supply current to power-down circuit	V_8 = 3 V	–	–	70	µA

Note

1. Power-down circuit supplied via external source.

APPLICATION INFORMATION

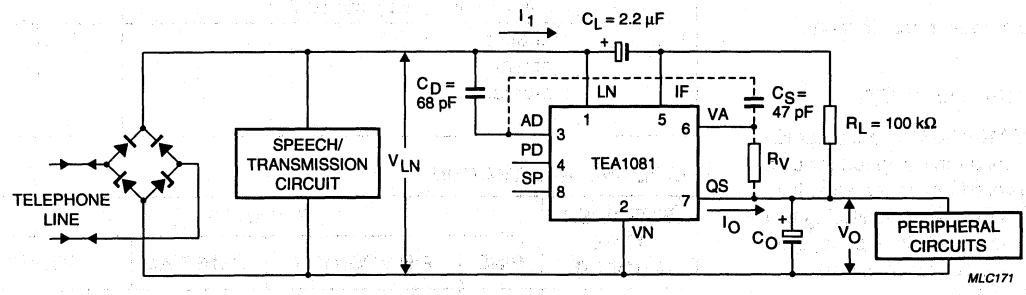


Fig.6 Application diagram.

Call progress monitor for line powered telephone sets

TEA1083/TEA1083A

FEATURES

- Internal supply
  - Optimum current split-up
  . Low constant current (adjustable) in transmission IC
  . Nearly all line current available for monitoring
  - Stabilized supply voltage
- Loudspeaker amplifier with a fixed gain of 35 dB
- Volume controled by potentiometer
- Power-down input (TEA1083A only)
- Loudspeaker enable input.

GENERAL DESCRIPTION

The TEA1083/83A is a bipolar IC which has been designed for use in line powered telephone sets. It is intended to offer a monitoring facility of the line signal via a loudspeaker during on-hook dialling. The TEA1083/83A is intended for use in conjunction with a transmission circuit of the TEA1060 family.
The device uses a part of the available line current via the internal supply circuit.
The loudspeaker amplifier, which consists of a preamplifier and a power amplifier, amplifies the received line signals from the transmission circuit when enabled via the LSE input. The loudspeaker amplifier can also be used to amplify dialling tones from the dialler IC.
The power amplifier contains a push-pull output stage to drive the loudspeaker in a Single Ended Load (SEL) configuration.
The internal voltage stabilizer can be used to supply external devices.
By activating the power-down (PD) input of the TEA1083A, the current consumption of the circuit will be reduced, this enables pulse dialling or flash (register recall).
An internal start circuit ensures normal start-up of the transmission IC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	input current range		3.0	–	120	mA
V_{BB}	stabilized supply current		–	2.95	–	V
I_{SUP}	current consumption	PD = HIGH; TEA1083A only	–	50	–	µA
G_v	voltage gain of loudspeaker amplifier		–	35	–	dB
I_{SUP}	minimum input current	P_O = 10 mW (typ) into 50 Ω	–	10	–	mA
T_{amb}	operating ambient temperature range		–25	–	+75	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1083	8	DIL	plastic	SOT97D
TEA1083A	16	DIL	plastic	SOT38
TEA1083AT	16	SOL	plastic	SOT162AG

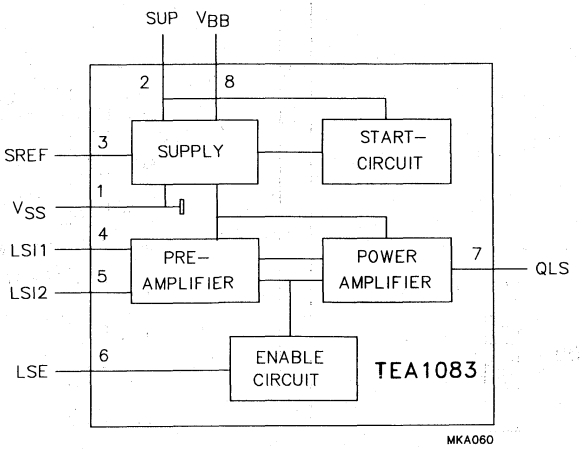


Fig.1 Block diagram (TEA1083).

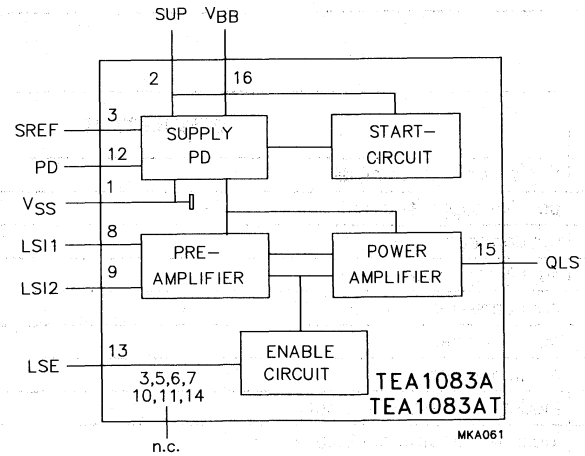


Fig.2 Block diagram (TEA1083A/AT).

Call progress monitor for line powered telephone sets

TEA1083/TEA1083A

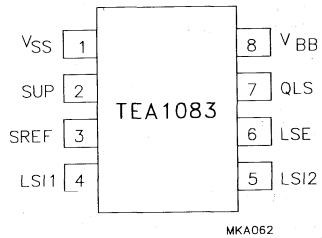


Fig.3 Pin configuration (TEA1083).

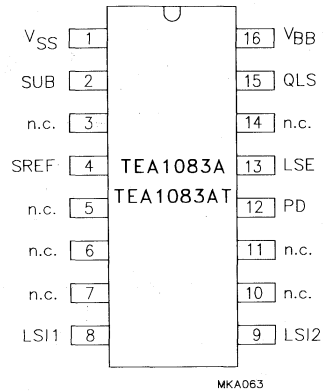


Fig.4 Pin configuration (TEA1083A/AT).

PINNING

SYMBOL	PIN DIL16	PIN DIL8	DESCRIPTION
V_{SS}	1	1	negative supply terminal
SUP	2	2	positive supply terminal
n.c.	3	–	not connected
SREF	4	3	supply reference input
n.c.	5	–	not connected
n.c.	6	–	not connected
n.c.	7	–	not connected
LSI1	8	4	loudspeaker amplifier input 1
LSI2	9	5	loudspeaker amplifier input 2
n.c.	10	–	not connected
n.c.	11	–	not connected
PD	12	–	power-down input
LSE	13	6	loudspeaker enable input
n.c.	14	–	not connected
QLS	15	7	loudspeaker amplifier output
V_{BB}	16	8	stabilized supply voltage

Table 1 Comparison of the TEA108X family.

PRODUCT	CONDITIONS	TEA1083	TEA1083A	TEA1085/85A
Application area	note 1	call progress monitoring		listening-in
PD facility		–	X	X
MUTE or LSE facility	note 2	X	X	X
Dynamic limiter		–	–	X
Howling limiter		–	–	X
V_{BB} setting		–	–	X
SEL	note 3	X	X	X
BTL	note 3	–	–	X
Number of pins	note 4	8	16	24

Notes to Table 1

1. A call progress monitor is recommended by the European Telecommunications Standards Institute (ETSI) for telephone sets with automatic on-hook dialling facilities so that audible, or visual, progress of a call attempt can be monitored. In accordance with the ETSI (at a frequency of 440 Hz and a line level of 20 dBm (600 Ω)), a minimum level of 50 dBA shall be guaranteed at a distance of 50 cm from the set. This corresponds to a minimum level of approximately 100 mV (RMS) ($P_O \geq 0.2$ mW) across a loudspeaker; Philips type AD2071/Z50.

   A listening-in set has to offer the user more facilities e.g. howling limiting to reduce annoying loudspeaker and line signals. Dynamic limiting of the loudspeaker signal, with respect to supply conditions, can also be required. Acoustic output levels for listening-in sets are approximately 70 to 75 dBA. This corresponds to a loudspeaker level of approximately 1 mV (RMS) ($P_O \approx 20$ mW).
2. The MUTE function of the TEA1085A has a logic input; the MUTE function of the TEA1085 has a toggle input.
3. SEL: loudspeaker connected in a single-ended-load configuration

   BTL: loudspeaker connected in a bridge-tied-load configuration
4. Consult the product specification for the package outline/s.

FUNCTIONAL DESCRIPTION

The TEA1083/83A is normally used in conjunction with a transmission circuit of the TEA1060 family. The circuit must be connected between the positive line terminal (pin 2) and pin SLPE of the transmission IC. The transmission characteristics (impedance, gain settings etc) are not affected.
An interconnection between the TEA1083/83A and a member of the TEA1060 family is illustrated in Fig.5.

Supplies SUP, SREF, V_{BB} and V_{SS}

In Fig.6 the line current is divided into I_{TR} for the transmission IC and I_{SUP} for the monitoring circuit TEA1083/83A.

I_{TR} is constant:

$I_{TR} = V_{int}/R20$

$I_{SUP} = I_{line} - I_{CC} - I_{TR}$

Where:

- V_{int} is an internal temperature compensated reference voltage of 500 mV(typ) between pins SUP and SREF
- R20 is a resistor connected between SUP and SREF
- I_{CC} is the internal current consumption of the TEA106X (approximately 1 mA).

A practical value for resistor R20 is 150 Ω; this produces a current of approximately 3.3 mA(typ) for I_{TR} and I_{SUP} is approximately equal to $I_{line} - 4.3$ mA.

The circuit stabilizes its own supply voltage at V_{BB}. Transistor TR1 provides the supplies for the internal circuits. Transistor TR2 is used to minimize signal distortion on the line by momentarily diverting the input current to V_{SS} whenever the instantaneous value of the voltage at V_{SUP} drops below the supply voltage V_{BB}. V_{BB} is fixed to a typical value of 2.95 V.
The supply at V_{BB} is decoupled with respect to V_{SS} by a 220 µF capacitor (C20).

The DC voltage ($V_{SUP} - V_{SS}$) is determined by the transmission IC and V_{int}; thus $V_{SUP} - V_{SS} = V_{LN-SLPE} + V_{int}$. The reference voltage of the transmission IC has to be adjusted to a level where $V_{SUP} - V_{BB(max)}$ is greater than 400 mV. The minimum voltage space between SUP and V_{BB} (400 mV) is required to maintain a 'high' efficiency of the internal supply for mean speech levels. $V_{BB(max)}$ is the specified maximum level.

The internal current consumption of the TEA1083/83A (I_{SUP0}) is typically 2.5 mA (where $V_{SUP} - V_{SS} = 3.6$ V). The current I_{SUP0} consists of currents I_{BIAS} (approximately 0.4 mA) for the circuitry connected to SUP and I_{BB0} (approximately 2.1 mA) for the internal circuitry connected to V_{BB} (see Fig.6).

LOUDSPEAKER AMPLIFIER (LSI1/LSI2 and QLS)

The TEA1083/83A has symmetrical inputs at LSI1 and LSI2. The input signal is normally taken from the earpiece output of the transmission circuit (see Fig.5) and/or from the signal output of the DTMF generator via a resistive attenuator.
The attenuation factor must be chosen in accordance with the output levels from the transmission IC and/or DTMF generator and, in accordance with the required output power and permitted signal distortion from the loudspeaker signal.

The output QLS drives the loudspeaker as a single-ended load. The output stage has been optimised for use with a 50 Ω loudspeaker (e.g. Philips type AD2071). The loudspeaker amplifier is enabled when the LSE input goes HIGH. The gain of the amplifier is fixed at 35 dB.

Volume control of the loudspeaker signal can be obtained by using a level control at the input (see Fig.5).

The maximum voltage swing at the QLS output is $V_{O(p-p)} = 2.5$ V (typical with 50 Ω load). The input level V_{LSI} is approximately 16 mV(rms) and the supply current $I_{SUP} > 11$ mA. In this condition the signal is limited by the available voltage space (V_{BB}). Higher input levels and/or lower supply currents will result in an increase of the harmonic distortion due to signal clipping.

With a limit of 2.5 V(p-p), the maximum output swing is dependent on the supply current and loudspeaker impedance. It can be approximated, for low distortions, by the following equation:

$$V_{O(p-p)} = 2 \times (I_{SUP} - I_{SUPO}) \times \pi \times R_{LS}$$

Where;

- $V_{O(p-p)}$ = the peak-to-peak level of the loudspeaker
- R_{LS} = the loudspeaker impedance
- I_{SUPO} = 2.5 mA (typ.)

POWER-DOWN INPUT (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, thereby breaking the supply current to the transmission IC. The capacitor connected to V_{BB} provides the supply for the TEA1083/83A during the supply breaks.

By making the PD input HIGH during the loop break, the requirement on the capacitor is eased and, consequently, the internal current consumption I_{BB0} (see Fig.5) is reduced from 2.1 mA to 400 µA typically. Transistors TR1 and TR2 are inhibited during power-down and the bias current is reduced from approximately 400 µA to approximately 50 µA with V_{SUP} =3.6 V in the following equation:

$$I_{SUP(PD)} = I_{BIAS(PD)} = (V_{SUP} - 2V_d)/Ra$$

Where $3.6 < V_{SUP} < V_{BB} + 3$ V

$2V_d$ is the voltage drop across 2 internal diodes (approximately 1.3 V)

Ra is an internal resistor (typical 50 kΩ)

LOUDSPEAKER ENABLE INPUT (LSE)

The LSE input has a pull-down structure. It switches the loudspeaker amplifier, in the monitoring condition, by applying a HIGH level at the input. The amplifier is in the standby condition when LSE is LOW (input open-circuit or connected to V_{SS}.

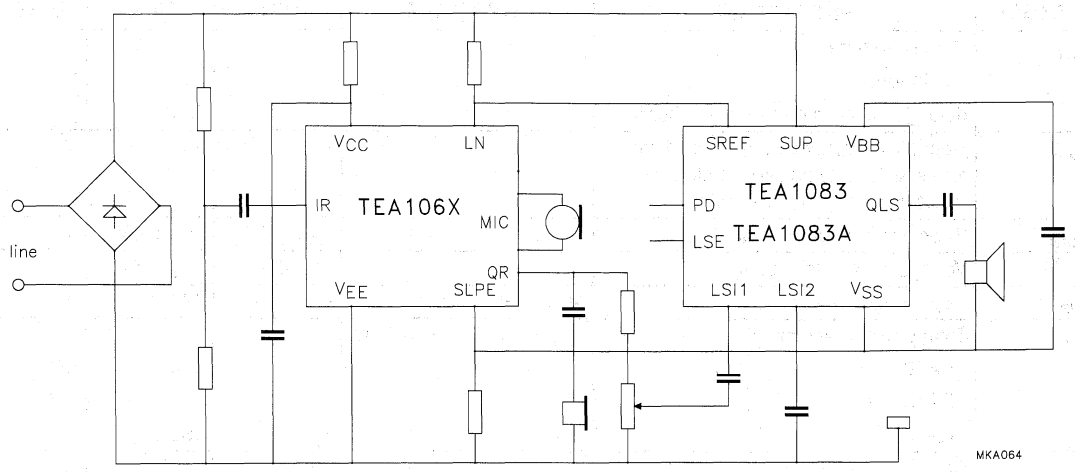


Fig.5 Interconnection with a transmission IC of the TEA106X family.

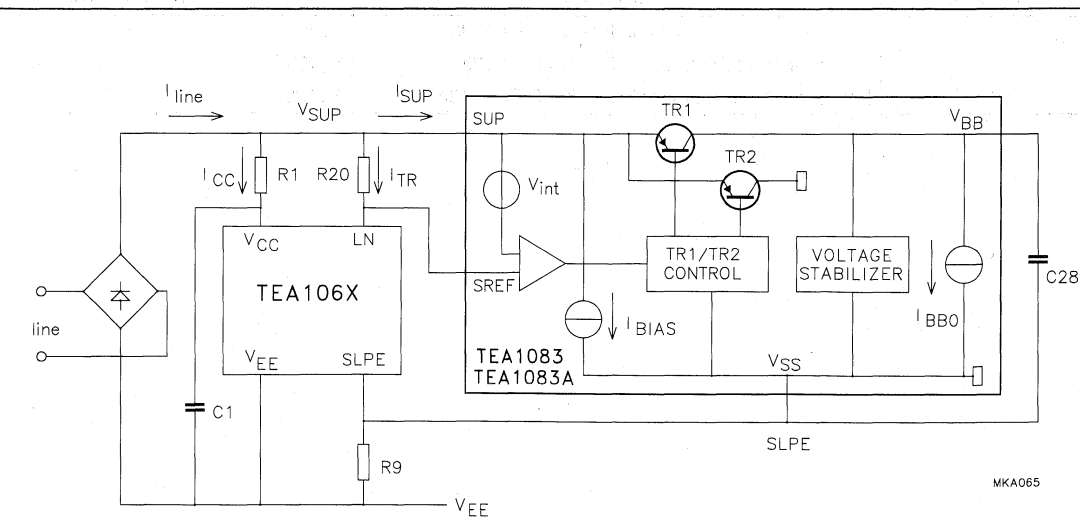


Fig.6 Supply arrangement.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SUP}	Supply voltage				
	continuous		–	12	V
	during switch-on or line interruption		–	13.2	V
V_{SUP}	Repetitive supply voltage from 1 ms to 5 s with 12 Ω current limiting resistor in series with supply		–	28	V
V_{SREF}	Supply reference voltage		V_{SS}–0.5	V_{SUP}+0.5	V
V	Voltage on all other pins		V_{SS}–0.5	V_{BB}+0.5	V
I_{SUP}	Supply current	see Fig.6	–	120	mA
P_{tot}	Total power dissipation	T_{amb} = 75 °C; T_j = 125 °C			
	TEA1083		–	500	mW
	TEA1083A		–	769	mW
	TEA1083AT		–	555	mW
T_{stg}	Storage temperature range		–40	+125	°C
T_{amb}	Operating ambient temperature range		–25	+75	°C
T_j	Junction temperature		–	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (TEA1083)	100 K/W
	from junction to ambient in free air (TEA1083A)	65 K/W
	from junction to ambient in free air (TEA1083AT)	90 K/W

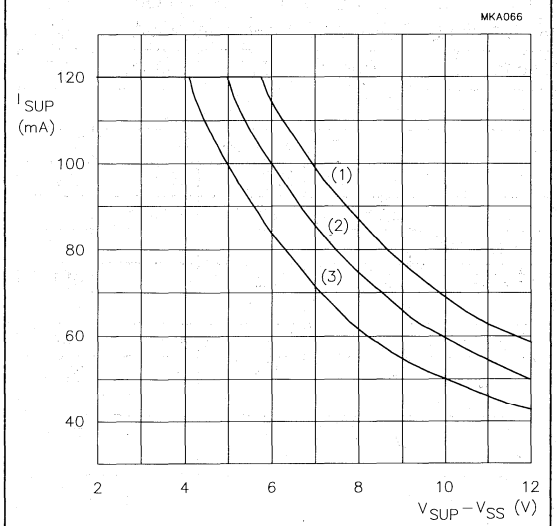


Fig.7 Safe operating area; see Table 2 (TEA1083).

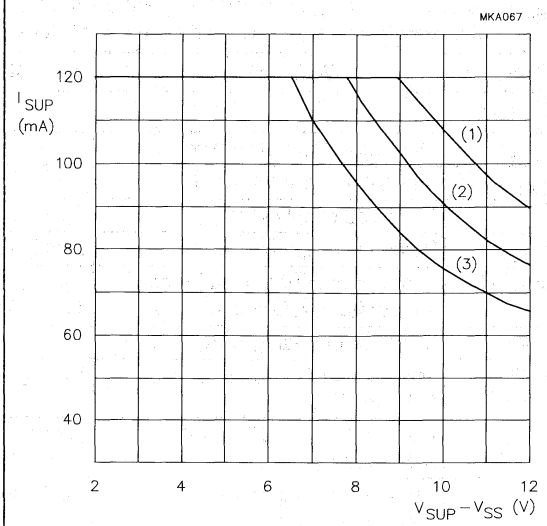


Fig.8 Safe operating area; see Table 3 (TEA1083A).

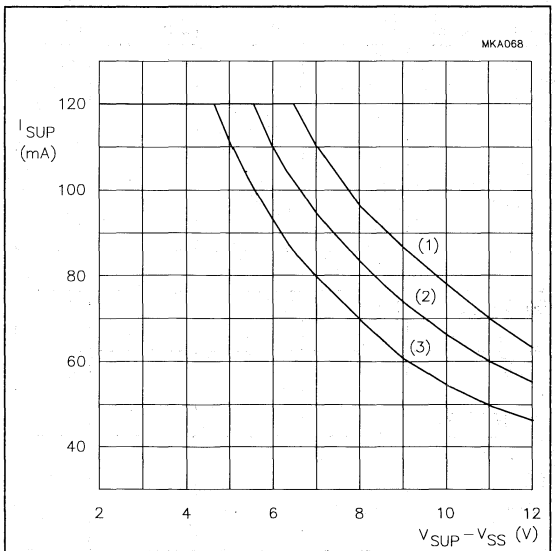


Fig.9 Safe operating area; see Table 4 (TEA1083AT).

Table 2

CURVE	T_{amb}	P_{tot}
1	55 °C	700 mW
2	65 °C	600 mW
3	75 °C	500 mW

Table 3

CURVE	T_{amb}	P_{tot}
1	55 °C	1077 mW
2	65 °C	923 mW
3	75 °C	769 mW

Table 4

CURVE	T_{amb}	P_{tot}
1	55 °C	777 mW
2	65 °C	666 mW
3	75 °C	555 mW

CHARACTERISTICS

V_{SUP} = 3.6 V; V_{SS} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V (RMS); f = 800 Hz; T_{amb} = 25 °C; PD = LOW; LSE = HIGH; loudspeaker amplifier load = 50 Ω; all measurements taken in test circuit Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SUP}	Minimum DC input voltage		–	V_{BB}+0.6	–	V
$V_{SUP-SREF}$	Internal reference voltage		400	500	600	mV
V_{BB}	Stabilized supply voltage	I_{SUP} = 15 mA	2.75	2.95	3.15	V
ΔV_{BB}	Variation of supply voltage	from I_{SUP} = 15 to 120 mA	–	15	–	mV
$\Delta V_{BB}/\Delta T$	Variation of supply voltage with temperature, referred to 25 °C	T_{amb} = –25 to +75 °C; I_{sup} = 15 mA	–	±0.2	–	mV/K
I_{SUP}	Minimum operating current		–	2.5	4.0	mA
THD	Distortion of AC signal between SUP and V_{EE}	$V_{SUP(RMS)}$ = 1 V	–	0.3	–	%
$V_{no(RMS)}$	Noise between SUP and V_{EE} (RMS value)	psophometrically weighted (P53 curve)	–	–71	–	dBmp
	Current consumption in power-down condition	PD = HIGH				
I_{SUP}	V_{SUP} = 3.6 V		–	50	75	µA
I_{BB}	V_{BB} = 2.95 V		–	400	550	µA
Loudspeaker amplifier inputs LSI1 and LSI2						
Z_i	input impedance (LSI1 and LSI2)	single ended	7.5	9.5	11.5	kΩ
		differential (LSI1 to LSI2)	15	19	23	kΩ
G_v	Voltage gain from LSI1/2 to QLS	I_{SUP} = 15 mA; V_i = 2 mV(RMS)	34	35	36	dB
ΔG_v	Total gain variation with input signal from 2 mV(RMS) to 10 mV(RMS)		–	0.2	–	dB
$\Delta G/\Delta T$	Total gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.4	–	dB
Output capabilities						
$V_{O(p-p)}$	Maximum output voltage (peak-to-peak value)	THD = 3 %; 50 Ω load	2.0	2.5	–	V
$V_{O(p-p)}$	Output voltage (peak-to-peak value)	V_i = 10 mV(RMS); I_{SUP} = 15 mA; V_{SUP}–V_{EE} = 1 V(RMS)	–	1.6	–	V
$V_{no(RMS)}$	Noise output voltage (RMS value)	1 kΩ between inputs LSI1 and LSI2; psophometrically weighted (P53 curve)	–	250	–	µV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-down input (PD) (TEA1083A only)						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}	V
I_{PD}	Input current	PD = HIGH	–	2.3	2.8	μA
LSE input						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}	V
I_I	Input current	LSE = HIGH	–	5	10	μA
ΔG	Reduction of gain from LSI1/LSI2 to QLS	LSE = LOW	60	80	–	dB

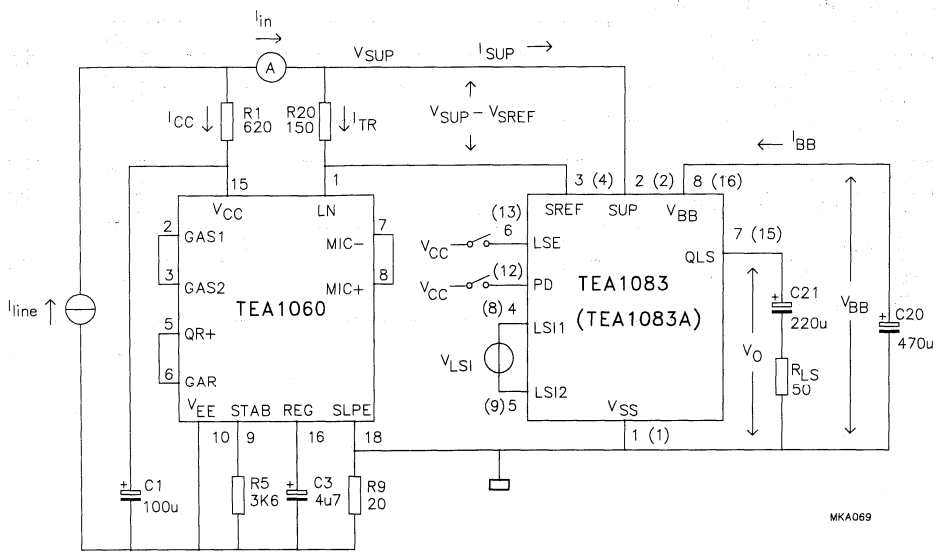


Fig.10 Test circuit.

Notes to figure 10

1. $I_{SUP} = I_{IN} - I_{TR}$
2. $G_v = 20 \log \left| \frac{V_O}{V_{LSI}} \right|$
3. $I_{TR} = \frac{V_{SUP-SREF}}{R20}$
4. The pin numbers in parenthesis refer to the TEA1083
5. LSE has to be HIGH to measure the voltage gain
6. PD has to be HIGH to measure in PD conditions
7. The pins not shown in the TEA1060 are left open-circuit
8. An impedance in series with pin SUP (e.g. an ammeter) should be avoided as it interferes with the values of I_{TR} and I_{SUP}.

Call progress monitor for line powered telephone sets

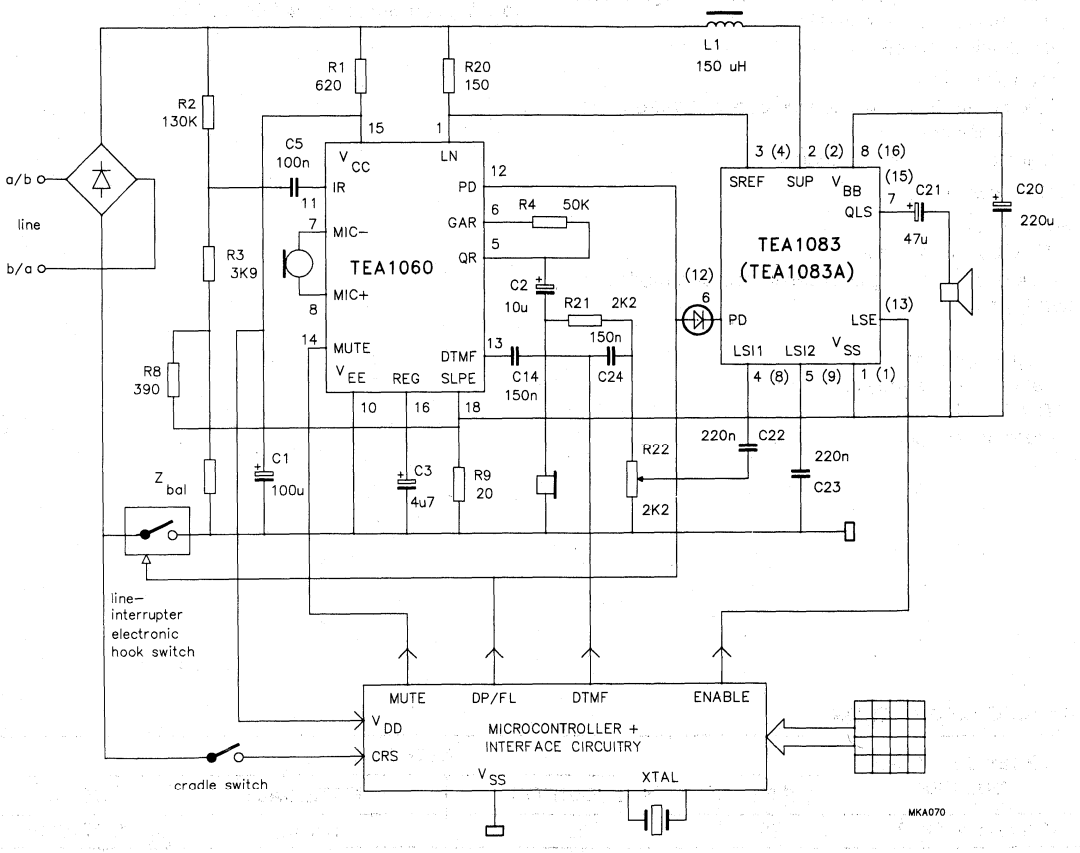
TEA1083/TEA1083A

APPLICATION INFORMATION

An application of the TEA1083/83A, in conjunction with a member of the TEA1060 family, is illustrated in figure 11. The TEA1083/83A is used for call progress monitoring during on-hook dialling. The dialling facilities are performed by a microcontroller (e.g. PCD3344, PCD3349).

Only the most important components have been shown. For detailed information refer to a data sheet of the TEA1060 family.

The electronic hook switch can be replaced by a mechanical system (hook switch) with a hold/release function which is intended for on-hook dialling.



Pin numbers in parenthesis refer to the TEA1083.

Fig.11 Application example when the TEA1083/83A is used in conjunction with the TEA1060.

Listening-in circuit for line-powered telephone sets

TEA1085/TEA1085A

FEATURES

- Internal supply
  optimum current split-up
  - low constant current (adjustable) in transmission IC
  - nearly all line current available for listening-in
  adjustable supply voltage
- Loudspeaker amplifier
  dynamic limiter providing low distortion and the highest possible output power
  SE or BTL drive for loudspeaker
  volume control by potentiometer and/or logic inputs (e.g. microcontroller drive)
  fixed gain of 35 dB
- Larsen level limiter
  low sensitivity for own speech due to 3rd-order filter and attack delay
  adjustable voltage thresholds
- Power down input
- MUTE input
  TEA1085/TEA1085A
  - clickfree switching between listening-in mode and standby mode
  TEA1085
  - toggle function
  - start-up in standby condition
  TEA1085A
  - logic level input

GENERERAL DESCRIPTION

The TEA1085 and TEA1085A are bipolar ICs which have been designed for use in line-powered telephone sets and provide a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.
The circuits incorporate a supply circuit, loudspeaker amplifier dynamic limiter, MUTE circuit, power-down facility and logic inputs for gain setting. The devices also incorporate a Larsen Level Limiter to reduce howling effects.
The ICs are intended for use in conjunction with a transmission circuit of the TEA1060 family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1085/TEA1085A	24	DIL	plastic	SOT101B
TEA1085T/TEA1085AT	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	input current range		4	–	120	mA
V_{BB}	stabilized supply voltage		–	3.6	–	V
I_{SUP}	current consumption	PD = HIGH	–	55	–	µA
G_v	voltage gain loudspeaker amplifier					
		SE	–	35	–	dB
		BTL	–	41	–	dB
ΔG_v	maximum gain reduction with logic inputs (3 steps)		–	18	–	dB
I_{SUP}	minimum input current					
		P_{OUT} = 20 mW typ. into 50 Ω SE	–	15	17	mA
		P_{OUT} = 40 mW typ. into 50 Ω BTL	–	–	32	mA
$t_{ad(RMS)}$	Larsen limiter attack delay time V_{DTI} jumps from 0 to ≥ 100 mV (RMS value)		100	–	200	ms
$V_{DTI(RMS)}$	Larsen limiter threshold level	Larsen mode	–	7	–	mV
G_v	Larsen limiter preamplifier gain setting range		30	–	52	dB
T_{amb}	operating ambient temperature range		−25	–	+75	°C

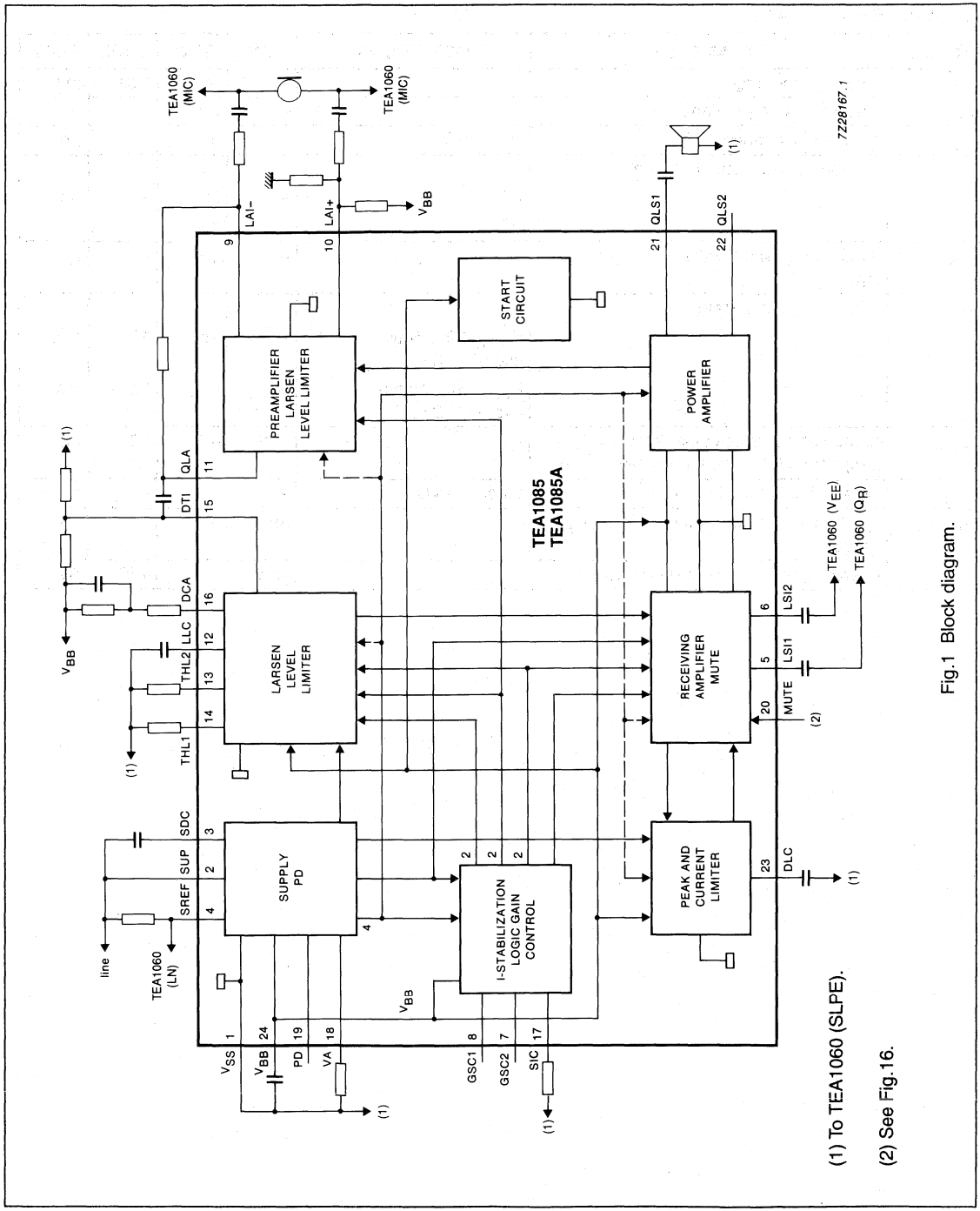


Fig.1 Block diagram.

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	negative supply
SUP	2	positive supply
SDC	3	supply amplifier decoupling
SREF	4	supply reference input
LSI1	5	loudspeaker amplifier input 1
LSI2	6	loudspeaker amplifier input 2
GSC2	7	logic input 2 for gain select
GSC1	8	logic input 1 for gain select
LAI−	9	Larsen limiter preamplifier inverting input
LAI+	10	Larsen limiter preamplifier non-inverting input
QLA	11	Larsen limiter preamplifier output
LLC	12	Larsen limiter capacitor
THL2	13	Larsen limiter residual threshold level
THL1	14	Larsen limiter attack delay threshold level
DTI	15	Larsen limiter detector input
DCA	16	Larsen limiter detector current adjustment
SIC	17	Larsen limiter current stabilizer
VA	18	V_{BB} voltage adjustment
PD	19	power-down input
MUTE	20	MUTE input
QLS1	21	loudspeaker amplifier output 1
QLS2	22	loudspeaker amplifier output 2
DLC	23	dynamic limiter capacitor
V_{BB}	24	stabilized supply decoupling

PIN CONFIGURATION

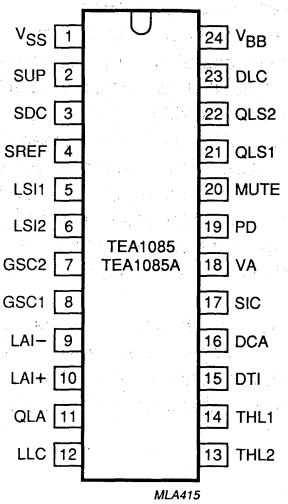


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 illustrates a block diagram of the TEA1085/TEA1085A with external components and connections to the transmission IC.

The TEA1085/TEA1085A are bipolar ICs which have been designed for use in line-powered telephone sets and provide a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.

The loudspeaker amplifier consists of a preamplifier, to amplify the earpiece signal from the transmission circuit and, a double push-pull output stage to drive the loudspeaker in the BTL (bridge tied load) or SE (single ended) configuration. The gain of the preamplifier is controlled by a dynamic limiter which prevents high distortion of the loudspeaker signal. This is achieved by preventing clipping of the loudspeaker signal, with respect to the supply voltage, and at too low supply current. Two logic inputs can be used to reduce the gain in 3 steps.

Because of acoustic feedback from the loudspeaker to the microphone, howling signals (Larsen effect) can occur on the telephone line and in the loudspeaker. When the Larsen signal exceeds a voltage and time duration threshold the Larsen level limiter (LLL) will reduce the Larsen signal to a low level within a short period of time by reducing the gain of the receiving preamplifier. This is achieved by using the microphone signal as an input signal which is processed in the LLL via a preamplifier and 3rd-order filter.

The MUTE input can be used to enable or disable the loudspeaker amplifier.

The MUTE function of the TEA1085 has a toggle input to permit the use of a simple push-button switch.

The MUTE function of the TEA1085A has a logic input to operate with a microcontroller.

By activating the power-down input the current consumption of the circuit will be reduced, this enables pulse dialling or flash (register recall).

An internal start circuit ensures normal start-up of the transmission IC and start-up of the listening-in IC in the standby mode.

The TEA1085/TEA1085A are intended for use in conjunction with a member of the TEA1060 family and should be connected between LINE and SLPE of the transmission IC. The transmission characteristics (impedance, gain settings, for example) are not affected. The interconnection between the two ICs is illustrated in Fig.3.

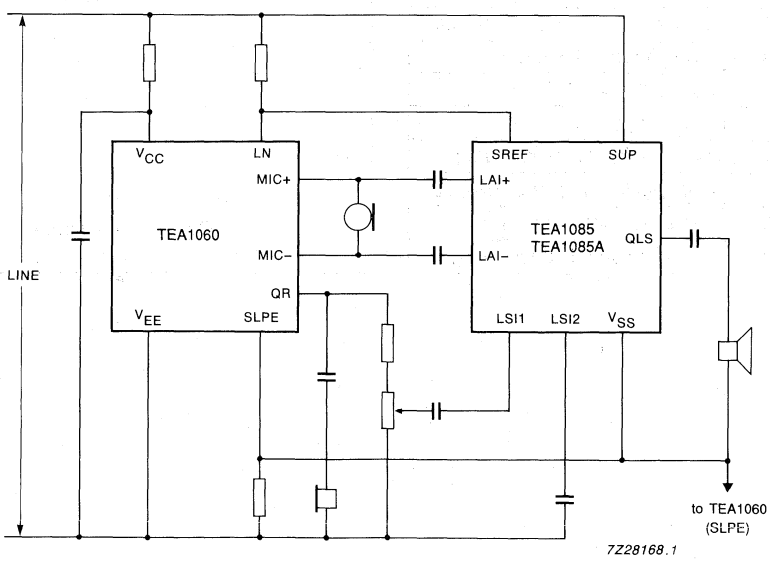
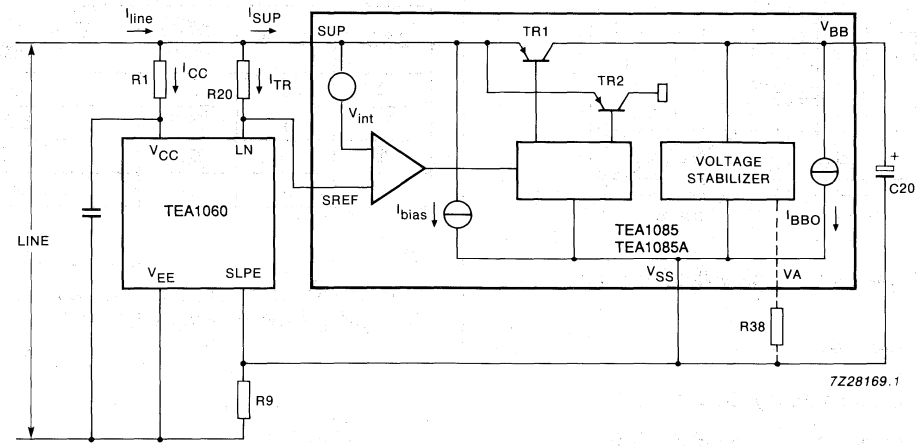


Fig.3 Interconnection of the TEA1085/TEA1085A with the TEA1060.

Supply; SUP, SREF, V_{BB}, V_{SS} and VA

The line current is divided into I_{TR} for the TEA1060 and I_{SUP} for the TEA1085/TEA1085A. The supply arrangement is illustrated in Fig.4.



I_{TR} is constant: $I_{TR} = V_{int}/R20$; $I_{SUP} = I_{line} - I_{CC} - I_{TR}$

Fig.4 Supply arrangement.

Where:

V_{int} is an internal temperature compensated reference voltage with a typical value of 315 mV between SUP and SREF

R20 is a resistor between SUP and SREF

I_{CC} is the internal current consumption of the TEA106X (≈ 1 mA)

A practical value for R20 is 150 Ω. This value of resistance produces a value for I_{TR} = 2 mA and $I_{SUP} = I_{line} - 3$ mA.

The TEA1085/TEA1085A stabilizes its own supply voltage at V_{BB}. Transistor TR1 provides the supplies for the internal circuits. TR2 is used to minimize the signal distortion on the line by momentarily diverting the input current to V_{SS} whenever the instantaneous value of the voltage V_{SUP} drops below the supply voltage V_{BB}. V_{BB} is fixed to a typical value of 3.6 V but can be increased by means of an external resistor (R38) connected between VA and V_{SS} or decreased by connecting this resistor between VA and V_{BB}. The minimum level on V_{BB} is restricted to 3.0 V; the level of the V_{BB} limiter is also affected (see application report for further information). The supply at V_{BB} is decoupled by a 470 µF capacitor.

The DC voltage ($V_{SUP} - V_{SS}$) is determined by the transmission IC ($V_{LN-SLPE}$); thus $V_{SUP} - V_{SS} = V_{LN-SLPE} + V_{int}$. The minimum DC voltage that can be applied to this input is $V_{BB(max)}$ + 0.4 V.

Where: $V_{BB(max)}$ is the worst case supply voltage (this depends on the setting of R38, which is connected between VA and V_{SS}).

The internal current consumption of the TEA1085/TEA1085A (I_{SUP0}) is typically 4.2 mA (where $V_{SUP} - V_{SS}$ = 4.5 V, MUTE off). Thus the current available for powering the loudspeaker is $I_{SUP} - I_{SUP0}$.
The current I_{SUP0} consists of a bias current of ≈ 0.4 mA for the circuitry connected to SUP and current I_{BB0} of ≈ 3.8 mA which is used for the circuitry connected to V_{BB} (see Fig.4).

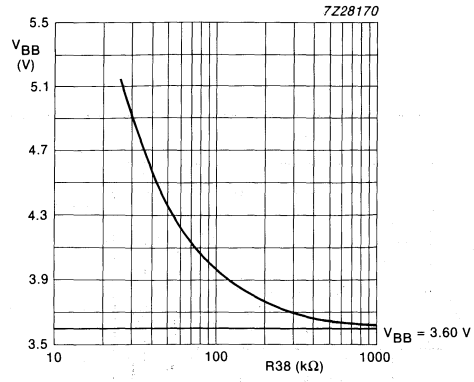


Fig.5 Stabilized supply voltage as a function of R38.

Supply amplifier stability (SDC) pin 3

To ensure stability of the TEA1085/TEA1085A, in combination with a transmission IC of the TEA1060 family, a 47 pF capacitor connected between SDC and SUP and a 150 µH coil connected between SUP and the positive line terminal (Fig.16) is required.

Loudspeaker amplifier (LSI1/LSI2 and QLS1/QLS2) pins 5/6, 21/22

The TEA1085/TEA1085A have symetrical inputs at LSI1 and LSI2. The input signal is normally taken from the earpiece output of the transmission circuit via a resistive attenuator (see Fig.3). The amount of attenuation must be chosen in accordance with the receive gain of the transmission IC (which depends on the sensitivity of the earpiece transducer). The maximum input signal level is 450 mV(RMS) at T_{amb} = +25 °C.
The outputs QLS1 and QLS2 can be used for single ended drive (SE) or bridge tied load drive (BTL). The output stages have been optimized for use with a 50 Ω loudspeaker (eg Philips type AD2071).
The gain of the amplifier is fixed to ≈ 35 dB for the SE drive and ≈ 41 dB for the BTL drive (when the inputs for logic control are left open-circuit or are connected to V_{SS}). The volume control can be obtained by using a potentiometer at the input and/or by the logic control function.

Logic gain control (GSC1 and GSC2) pins 7 and 8

The logic inputs GSC1 and GSC2 can be used to reduce the gain of the loudspeaker amplifier by means of the logic gain control function in 3 steps of 6 dB.

Table 1 Data for microcontroller drive of logic inputs

GSC2	GSC1	gain (dB)	gain reduction (dB)
0	0	35	0
0	1	28.7	6.3
1	0	22.2	12.2
1	1	17	18

Where:

0 = connection to V_{SS} or left open-circuit
1 = applying a voltage ≥ V_{SS} + 1.5 V

Dynamic limiter (DLC) pin 23

To prevent distortion of the signal at the loudspeaker outputs the gain of the amplifier is reduced rapidly when:

- the peaks of the signal at the loudspeaker outputs exceed an internaly determined threshold (voltage limiter)
- the DC current into SUP is insufficient (current limiter)
- the voltage at V_{BB} decreases below an internally determined threshold, typically 2.9 V (V_{BB} limiter)

The time in which the gain reduction is effected is the 'attack time'; this is very short in the first and third instance and relatively long in the second instance. The circuit will remain in the gain-reduced condition until the peaks of the output signal remain below the threshold level. The gain will then return to a nominal level after a time determined by the capacitor connected to DLC (release time).

MUTE input (MUTE) pin 20; TEA1085A

This MUTE is provided with a logic input to operate with a microcontroller for instance.
The loudspeaker amplifier is disabled when the MUTE input is LOW (connected to V_{SS} or open input). A HIGH level at the MUTE input enables the amplifier in the listening-in mode.

MUTE input (MUTE) pin 20; TEA1085

The MUTE function is provided with a toggle input and is designed to switch between the standby condition and the listening-in condition on the rising edge of the input MUTE signal (see Fig.6).
In the basic application the MUTE input must be LOW (connected to V_{SS}). A simple push-button can be used to operate the MUTE toggle (see Fig.7). Debouncing can be realized by means of a small capacitor connected between MUTE and V_{SS}.
An internal start circuit ensures that the circuit always starts up in the standby condition.

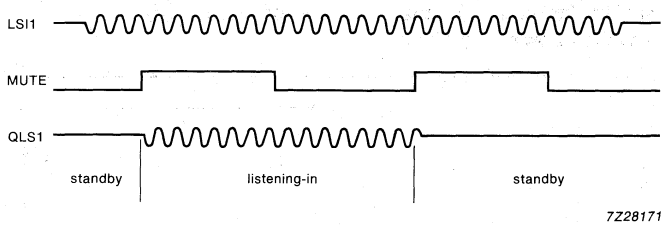
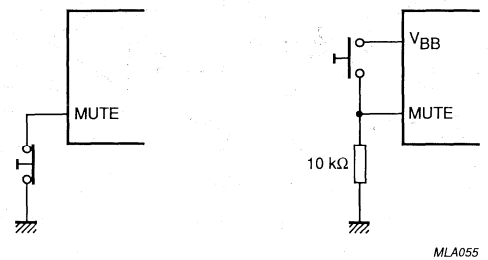


Fig.6 Mute toggle function of the TEA1085.



(a) Break contact. (b) Make contact.

Fig.7 Mute switch alternatives with the TEA1085.

Power down input (PD) pin 19

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, thereby breaking the supply to the transmission and listening-in circuits. The capacitor connected to V_{BB} provides the supply for the listening-in circuit during the supply breaks.
By making the PD input HIGH during the loop break the requirement on the capacitor is eased and, consequently, the internal (standby) current consumption I_{BBO} (Fig.4) at V_{BB} is reduced from 3.8 mA to 400 µA typical. So that the transmission circuit is not affected transistors TR1 and TR2 are inhibited and the bias current is reduced from ≈ 0.4 mA to ≈ 55 µA with V_{SUP} = 4.5 V in the following equation:

$I_{SUP(PD)} = I_{BIAS(PD)} = (V_{SUP} - 2V_d)/Ra$

(where $4.2\ V < V_{SUP} < V_{BB} + 3\ V$)

$2V_d$ = the voltage drop across 2 internal diodes (≈ 1.3 V)
Ra = an internal resistor of typical 60 kΩ

Larsen limiter current stabilizer (SIC) pin 17

A current reference is set by resistor R36 between SIC and V_{SS}. The preferred value is 120 kΩ. The internal reference current is given by the following equation:

$I_{SIC} = 1.25/R36$; when R36 = 120 kΩ, I_{SIC} = 10.5 µA

Changing the value of R36 will affect the timing of the Larsen level limiter system.

Larsen limiter preamplifier (LAI1/LAI2 and QLA) pins 9/10 and 11

This circuit amplifies the microphone signal to a level suitable for the Larsen limiter detector. The gain is set by external components (see Fig.8).
Normally the gain is set to the same level as the microphone amplifier of the transmission circuit, this ensures that the output signal level at output QLA is equal to the line signal level.

The gain between QLA and the microphone input is given by the following equation (the high-pass filter is not taken into account):

$A_{pre} = V_{QLA}/V_M = R29/R26$; in the basic application R25 = R26 = 10 kΩ

The gain can be adjusted between 30 dB (R29 = 316 kΩ) and 52 dB (R29 = 4 MΩ). The impedance result of R28 and R27 in parallel must be equal to R29 (e.g. R27 = R28 = 2 x R29)

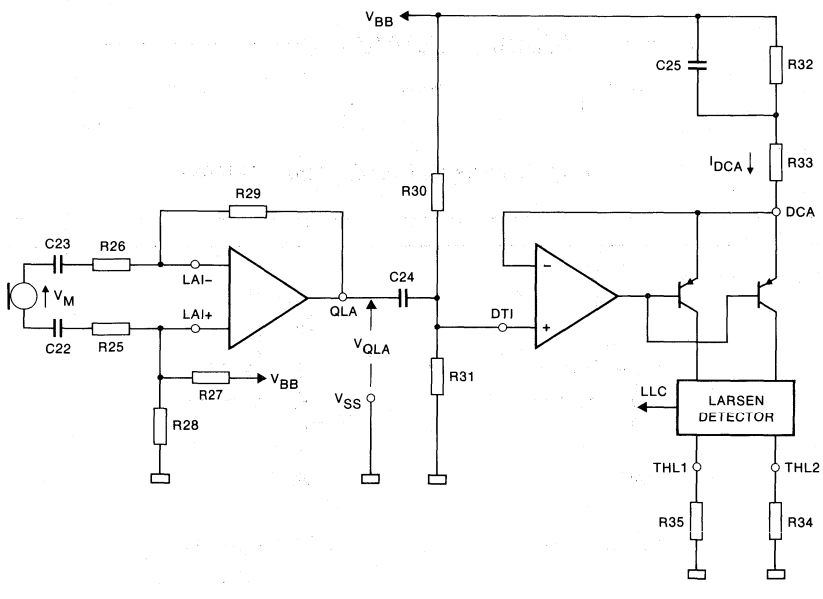


Fig.8 Larsen limiter preamplifier and voltage/current converter. 7Z28173

Larsen limiter detector (DTI and DCA) pins 15 and 16

The QLA output signal is AC coupled to the detector input DTI. DTI is biased by potential divider R30 and R31. The voltage applied to DTI of the Larsen level limiter is converted into a current for further processing in this circuit. Current adjustment is achieved using the network connected between DCA and V_{BB} (see Fig.8).

The equation for DC current is:

$$I_{DCA} = \frac{R30}{R30 + R31} \times V_{BB} \times \frac{1}{R32 + R33}$$

The equation for AC current is:

$$i_{DCA} = \frac{V_{DTI}}{R33} \text{ for } f > 1/2\pi R33C25$$

In the basic application:

R30 = 100 kΩ, R31 = 220 kΩ, R33 = 500 Ω, R32 = 100 kΩ and C25 = 330 nF

This results in I_{DCA} = 11 μA and the equation:

$$\frac{i_{DCA}}{V_{DTI}} + 2 \text{ (mA/V)}$$

High-pass filter

A third order high-pass filter is created between the microphone input voltage and the current flowing into DCA. The cut-off frequencies (see Fig.9) of the three sections are:

$$f1 = \frac{1}{2\pi R_{eg} C24} \text{ where } R_{eq} = \frac{R30 \times R31}{R30 + R31}$$

$$f2 = \frac{1}{2\pi R33 C24} \qquad f3 = \frac{1}{2\pi R26 C23} = 1/(2\pi R25C22)$$

Where: R25 = R26 and C22 = C23

The filter reduces the sensitivity of the system to own speech.
Normal speech is in the frequency range 300 Hz to 3400 Hz, however, the Larsen signal normally occurs at a frequency > 3 kHz.
With the component values as used in the basic application (see Fig.16); f1 = 500 Hz, f2 = 1 kHz and f3 = 3 kHz

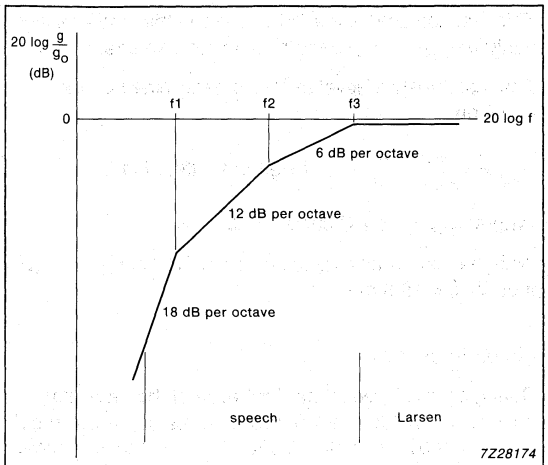


Fig.9 Third-order high-pass filter.

Where:

$$g = \frac{i_{DCA}}{V_m} \qquad g_O = \frac{A_{pre}}{R33}$$

Larsen limiter capacitor (LLC) pin 12

A 1 μF capacitor (C26) is connected externally between V_{SS} and LLC to determine the attack and release timing of the Larsen level limiter in the listen-in and Larsen mode. The timing is also dependent on the value of the resistor connected between SIC and V_{SS}.

Larsen level limiter threshold (THL1 and THL2) pins 13 and 14

When the signal at DTI exceeds the first threshold level the capacitor connected to LLC will start to discharge. The first threshold level is determined by the value of the resistor, R35, connected to THL1 and V_{SS}. The amount of discharge of C26 depends on how much the level of the signal at DTI exceeds the first threshold level (for normal speech the discharge is small).
The Larsen effect is generally defined as a signal level of ≥ 100 mV(RMS),on line, for a period of more than 100 ms. The Larsen signal must be reduced to a low level within 200 ms. For Larsen signal levels (f > f3 in Fig.9) of ≥ 100 mV(RMS) at DTI and, with the component values of Fig.16, the system will switch from the listen-in mode to the Larsen mode in a time period of 100 ms to 200 ms; consequently, the initial Larsen effect will last only for a short period of time.

This reaction time is the 'attack delay time' and ensures minimum sensitivity of the system for own speech.

The first threshold level at DTI is determined by the equation:

$$V_{DTI1} = (\frac{1.25}{R25} - \frac{I_{DCA}}{2}) \times 2 \times R33 \text{ (if f > f3 in Fig.9)}$$

Where: I_{DCA} = the DC current into DCA

With the component values given in Fig.16, I_{DCA} = 11 µA thus V_{DTI1} = 18.8 mV.

Listen-in mode

During normal speech the discharge of the capacitor connected to LLC is not sufficient to reach the threshold level whereby the system switches to the Larsen mode. This is because normal speech is not continuous, the discharge of C26 is slow (attack delay) and the charge is fast.
The slope of V_{LLC} during charge is given in the equation:

$$S_{1i} = \frac{\Delta V_{LLC}}{\Delta_t} = \frac{1.25}{C26 \times R36} \text{ (V/s)}$$

With C26 = 1 µF and R36 = 120 kΩ this results in S_{1i} = 10 V/s.

Discharge of the capacitor at LLC occurs when the signal at DTI exceeds V_{DTI1}, thus for a continuous signal at DTI the attack delay time t_{ad} (see Fig.10) is determined by the equation:

$$t_{ad} = \frac{C26 \times R36}{2 \times (3 \times k - 1)}$$

Where k = t1/T

The duty cycle is determined by the time in which the first threshold level (V_{DTI1}) is exceeded by the signal level at DTI (see Fig.11) thus for large signals; k ≤ 0.5.
With the component values given in Fig.16; k ≥ 0.457 for signals ≥ 100 mV(RMS).
Consequently 120 ms ≤ t_{ad} ≤ 160 ms, for V_{DTI} ≥ 100 mV(RMS)

Larsen mode

After the 'attack delay time' the circuit switches from the listen-in mode to the Larsen mode. The gain of the loudspeaker amplifier is reduced quickly to a value (t_{LAa} = Larsen attack time see Fig.10) whereby the residual Larsen signal is determined by a second threshold level. This level can be set by resistor R34 connected between THL2 and V_{SS}. The second threshold level must always be selected at a lower level than the first threshold level thus R34 > R35.
The time taken to effect gain reduction is very short. In the Larsen mode the circuit acts as a dynamic limiter with peak detector and regulates the gain so that the signal level at DTI is determined by the second threshold level V_{DTI2}.
The second threshold level at DTI is determined by the equation:

$$V_{DTI2} = (\frac{1.25}{R34} - \frac{I_{DCA}}{2}) \times 2 \times R33 \text{ (if f > f3 in Fig.9)}$$

Where: I_{DCA} = the DC current into DCA

With the component values given in Fig.16, V_{DTI2} = 6.9 mV.

The charge current in the Larsen mode is reduced to half the charge current in the listen-in mode.

The slope of V_{LLC} during charge (see Fig.10) is given in the equation:

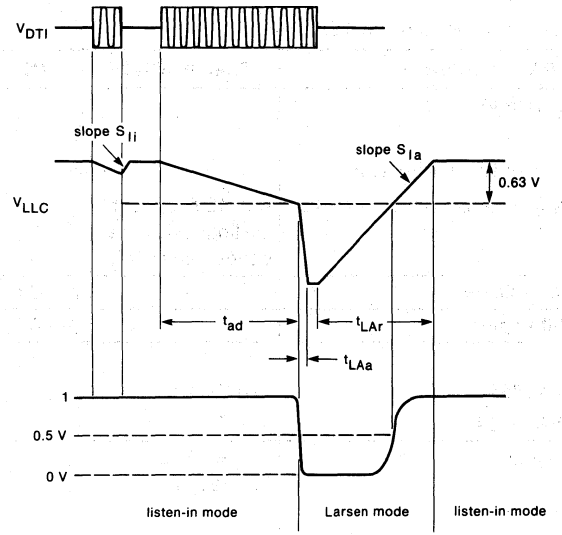
$$S_{la} = \frac{\Delta V_{LLC}}{\Delta_t} = \frac{1.25}{2 \times C26 \times R34} \text{ (V/s)}$$

Where: C26 = 1 µF and R36 = 100 kΩ, S_{la} = 5 V/s

When the Larsen effect stops (total open-loop gain < 1) the gain of the loudspeaker amplifier will return to its normal value in a time period known as the 'Larsen release time' (t_{LAr}). This time period is determined by capacitor C26 connected to LLC and resistor R36 connected to SIC.

Where: C26 = 1 µF and R36 = 120 kΩ, t_{LAr} = 250 ms

In practice the choice of the threshold levels (determined by R35 and R34) depends on the sensitivity of the microphone and loudspeaker, the send and receive gains, sidetone suppression and the acoustical properties which are determined by the cabinet of the telephone set.

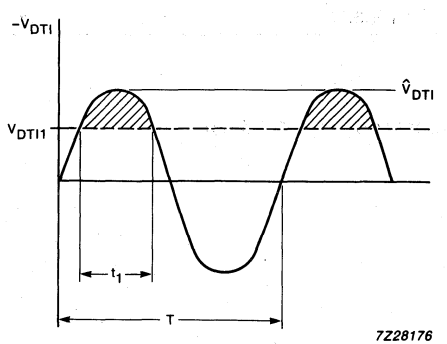


Where:

Change of receive gain = $\frac{G_v}{G_{vo}}$

Nominal receive gain = 20 log G_{vo} = 35 dB

Fig.10 Dynamic behaviour of Larsen limiter (in open-loop condition).



Where:

$k = \frac{t_1}{T}$

$k = 0.5 - \frac{\arcsin\left(\frac{V_{DTI1}}{\hat{V}_{DTI}}\right)}{\pi}$

Fig.11 Definition of duty cycle k.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

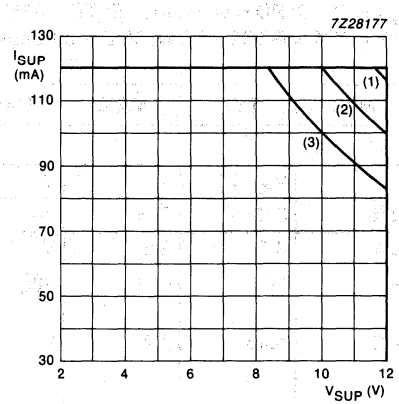
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SUP}	positive supply voltage				
	continous		–	12	V
	during switch-on or line interruption		–	13.2	V
	repetitive supply voltage from 1 ms to 5 s	with 12 Ω current limiting resistor in series with supply	–	28	V
V_{SREF}	supply reference voltage		V_{SS}–0.5	V_{SUP}+0.5	V
V_n	voltage on all other pins		V_{SS}–0.5	V_{BB}+0.5	V
I_{SUP}	supply current				
	TEA1085/TEA1085A	see Fig.12	–	120	mA
	TEA1085T/TEA1085AT	see Fig.13	–	120	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; T_j = 125 °C			
	TEA1085/TEA1085A		–	1	W
	TEA1085T/TEA1085AT		–	666	mW
T_{amb}	operating ambient temperature range		–25	+75	°C
T_{stg}	storage temperature range		–40	+125	°C
T_j	junction temperature		–	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air		
	TEA1085/TEA1085A		50 K/W
	TEA1085T/TEA1085AT	note 1	75 K/W

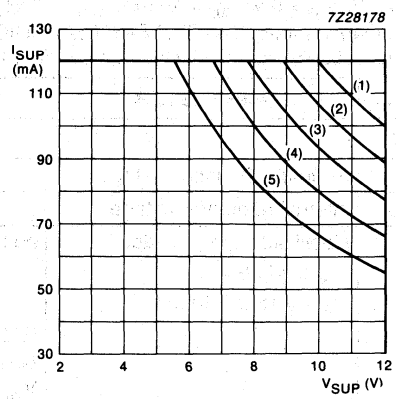
Note

1. Device mounted on a glass epoxy board 40.1 x 19.1 1.5 mm.



(1) T_{amb} = 55 °C; P_{tot} = 1.4 W.
(2) T_{amb} = 65 °C; P_{tot} = 1.2 W.
(3) T_{amb} = 75 °C; P_{tot} = 1.0 W.

Fig.12 TEA1085/TEA1085A safe operating area.



(1) T_{amb} = 35 °C; P_{tot} = 1.2 W.
(2) T_{amb} = 45 °C; P_{tot} = 1.07 W.
(3) T_{amb} = 55 °C; P_{tot} = 0.93 W.
(4) T_{amb} = 65 °C; P_{tot} = 0.8 W.
(5) T_{amb} = 75 °C; P_{tot} = 0.666 W.

Fig.13 TEA1085T/TEA1085AT safe operating area.

CHARACTERISTICS

V_{SREF} = 4.2 V; V_{SS} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V(RMS); f = 800 Hz; T_{amb} = 25 °C; PD = LOW; MUTE (TEA1085) = OFF (listening-in mode); MUTE (TEA1085A) = HIGH (listening-in mode); GSC1 = GSC2 = LOW; 50 Ω loudspeaker; no R38; test circuit Fig.14; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{SUP}	minimum DC input voltage		–	V_{BB}+0.7	–	V
$V_{SUP-SREF}$	internal reference voltage		275	315	355	mV
V_{BB}	stabilized supply voltage	no R38; I_{SUP} = 15 mA	3.4	3.6	3.8	V
ΔV_{BB}	variation from I_{SUP} = 15 to 120 mA		–	10	–	mV
		R38 = 39.2 kΩ between pins V_{SS} and VA; V_{SREF} = 5.2 V; I_{SUP} = 15 mA	4.2	4.45	4.7	V
$\Delta V_{BB}/\Delta T$	variation with temperature	no R38; I_{SUP} = 15 mA	tbf	–0.2	tbf	V
I_{SUP}	minimum operating current		–	4.2	5.5	mA
THD	distortion of AC signal on SUP	$V_{SUP(RMS)}$ = 1 V	–	0.3	–	%
$V_{no(RMS)}$	noise between SUP and V_{EE}		–	–72	–	dBmp
	current consumption in power-down condition	PD = HIGH				
I_{SUP}		V_{SUP} = 4.5 V	–	55	75	μA
I_{BB}		V_{BB} = 3.6 V	–	400	550	μA
Loudspeaker amplifier inputs LSI1 and LSI2						
$\lvert Z_i \rvert$	input impedance					
		single ended	7.5	9.5	11.5	kΩ
		differential	15	19	23	kΩ
G_v	voltage gain with 50 Ω load	I_{SUP} = 15 mA; V_i = 1.8 mV(RMS)				
		single ended	34	35	36	dB
		BTL output	39.9	40.9	41.9	dB
ΔG_v	variation with signal level	I_{SUP} = 50 mA; V_i = 1.8 mV(RMS) and 14 mV(RMS)				
		single ended	–	+0.1	0.4	dB
		BTL output	–	+0.2	0.6	dB
ΔG_v	variation with frequency referred to 1 kHz	f = 300 Hz and 3400 Hz; V_i = 1.8 mV(RMS)				
		single ended	–	± 0.1	–	dB
		BTL output	–	± 0.1	–	dB

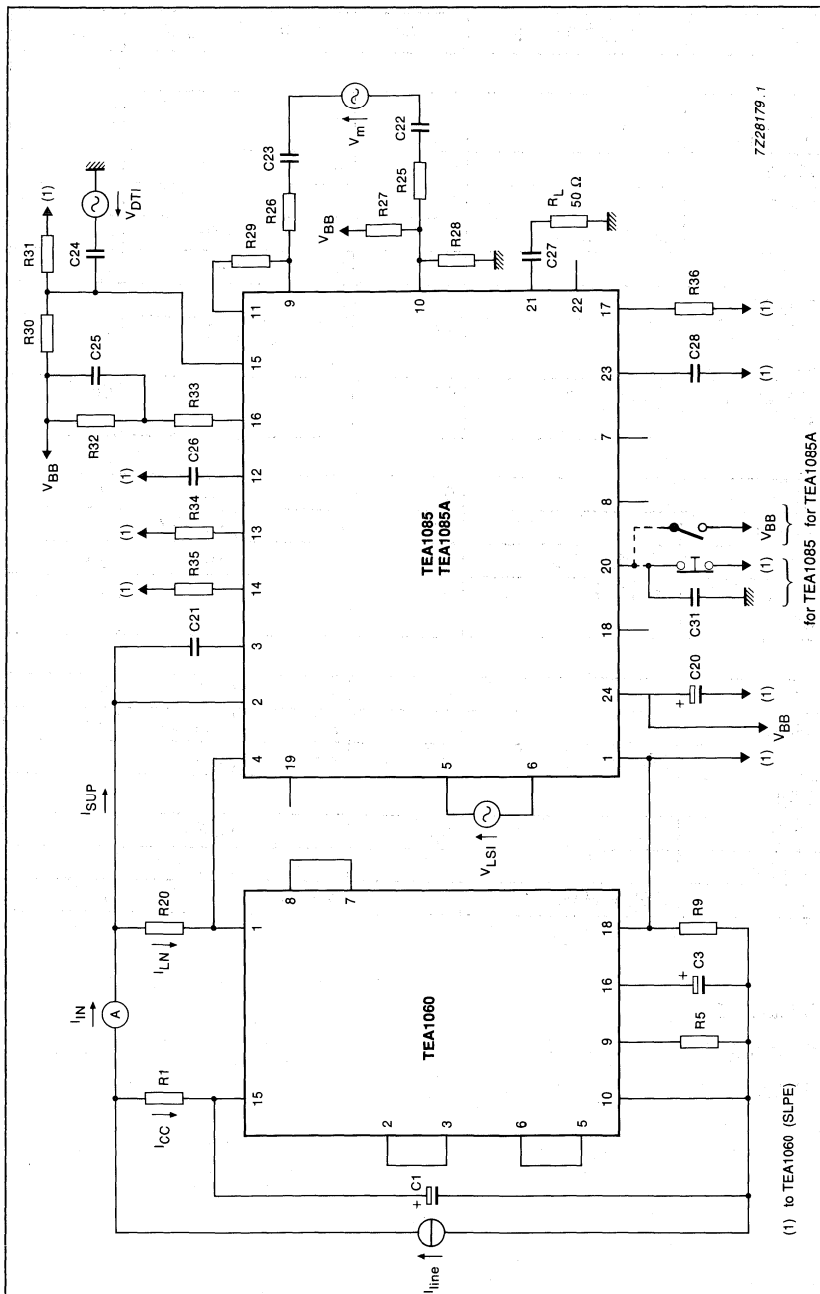
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_v	variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C				
		single ended	–	± 0.4	–	dB
		BTL output	–	± 0.5	–	dB
Loudspeaker outputs QLS1 and QLS2						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 9 mA; note 1	1.2	1.45	–	V
		I_{SUP} = 17 mA; note 2	2.5	2.9	–	V
	bridge-tied load	I_{SUP} = 23.5 mA; note 2	2.5	2.9	–	V
		I_{SUP} = 32 mA; note 3	3.5	4.0	–	V
THD	total harmonic distortion	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 9 mA	–	0.4	2	%
		I_{SUP} = 17 mA	–	0.7	2	%
	bridge tied load	I_{SUP} = 23.5 mA	–	0.4	2	%
$V_{o(p-p)}$	output voltage (peak-to-peak value)	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 17 mA; V_{SUP}-V_{EE} = 1 V(RMS)	1.75	2.15	–	V
Dynamic limiter						
THD	total harmonic distortion	V_i = 22 mV(RMS) +10 dB				
	single ended	I_{SUP} = 9 mA	–	0.5	10	%
		I_{SUP} = 17 mA	–	1.2	10	%
	bridge tied load	I_{SUP} = 23.5 mA	–	0.6	10	%
	dynamic behaviour of limiter	single ended load				
t_{att}	attack time; V_i jumps from 10 mV(RMS) to 65 mV(RMS)					
	voltage limiter	I_{SUP} = 17 mA	–	2	5	ms
	current limiter	I_{SUP} = 12 mA	–	500	tbf	ms
	V_{BB} limiter	I_{SUP} = 9 mA	–	10	–	ms
t_{rel}	release time; V_i jumps from 65 mV(RMS) to 10 mV(RMS)	I_{SUP} = 17 mA	tbf	75	tbf	ms
V_{BBO}	threshold V_{BB} limiter below which gain reduction starts	I_{SUP} = 9 mA	tbf	2.95	tbf	V
$V_{no(RMS)}$	noise output voltage	1 kΩ between inputs LSI1, LSI2; psophometrically weighted (P53 curve)				
	single ended		–	170	–	µV
	bridge tied load		–	350	–	µV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic gain control						
ΔG_v	reduction of voltage gain	V_i = 1.8 mV(RMS)				
	GSC2 = 0, GSC1 = 1		5.8	6.3	6.8	dB
	GSC2 = 1, GSC1 = 0		11.7	12.2	12.7	dB
	GSC2 = 1, GSC1 = 1		17	18	19	dB
Larsen limiter preamplifier						
	operational amplifier					
G_{v0}	open-loop gain		–	92	–	dB
f_{p1}	1st pole		–	120	–	Hz
f_{p2}	2nd pole		–	3.3	–	MHz
G_B	unity gain bandwidth		–	4	–	MHz
G_v	voltage gain	f = 3 kHz; R26 = 10 kΩ; R29 = 4 MΩ	51	52	53	dB
G_v	gain adjustment range		30	–	52	dB
Larsen limiter detector						
	voltage to current convertor					
V_{DCA}-V_{DTI}	DC offset voltage	V_{BB}-V_{DTI} = 1 V	–25	1	+25	mV
G_v	voltage gain from DTI to DCA	V_{DTI} = 100 mV(RMS); f = 3 kHz	tbf	–0.8	tbf	dB
V_{THL1}	DC voltage at THL1	R35 = 51 kΩ	1.8	1.25	1.33	V
V_{THL2}	DC voltage at THL2	R34 = 100 kΩ	1.8	1.25	1.33	V
	dynamic behaviour with a burst at DTI	f = 3 kHz; see Fig.15				
t_{LIr}	listen-in release time	see Fig.15(a)	tbf	40	tbf	ms
t_{ad}	attack delay time	see Fig.15(b)				
	V_{DTI} jumps from 0 to 100 mV (RMS value)		–	160	200	ms
	V_{DTI} jumps from 0 to 1 V (RMS value)		100	120	–	ms
t_{LAa}	Larsen attack time	see Fig.15(b); V_{DTI} = 100 mV(RMS)	–	20	tbf	ms
t_{LAr}	Larsen release time	see Fig.15(b)				
	V_{DTI} jumps from 100 mV to 0 mV (RMS value)		tbf	250	tbf	ms
V_{LLC}	DC voltage at LLC	V_{DTI} = 0 V	1.75	1.9	2.0	V
$-\Delta V_{LLC}$	reduction of V_{LLC} to attack Larsen mode		0.59	0.63	0.68	V
ΔG_v	gain reduction	V_{LLC} = 0.7 V	60	tbf	tbf	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE INPUT; TEA1085						
	(toggle function, positive edge triggered set-reset flip-flop)					
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{MUTE}	input current	MUTE = LOW	–	–22	–28	μA
t_W	minimum input pulse width		–	50	–	μs
P_R	minimum pulse repetition time		–	2	–	ms
$V_{BB(MUTE)}$	supply voltage below which MUTE toggle is reset		tbf	2	tbf	V
ΔG_v	reduction of gain from LSI1, LSI2 to QLS1, QLS2	MUTE = ON	60	100	–	dB
MUTE INPUT; TEA1085A						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{MUTE}	input current	MUTE = HIGH	–	10	20	μA
ΔG_v	reduction of gain from LSI1, LSI2 to QLS1, QLS2	MUTE = HIGH	60	100	–	dB
POWER DOWN INPUT						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{PD}	input current	PD = HIGH	–	2.3	2.8	μA
LOGIC INPUTS GSC1 and GSC2						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{GSC}	input current	GSC = HIGH	–	6	8	μA

Notes to the characteristics

1. Typical output power is 5 mW into 50 Ω
2. Typical output power is 20 mW into 50 Ω
3. Typical output power is 40 mW into 50 Ω



The DC current is divided as follows:

$$I_{SUP} = I_N - \frac{V_{SUP-SREF}}{R20}$$

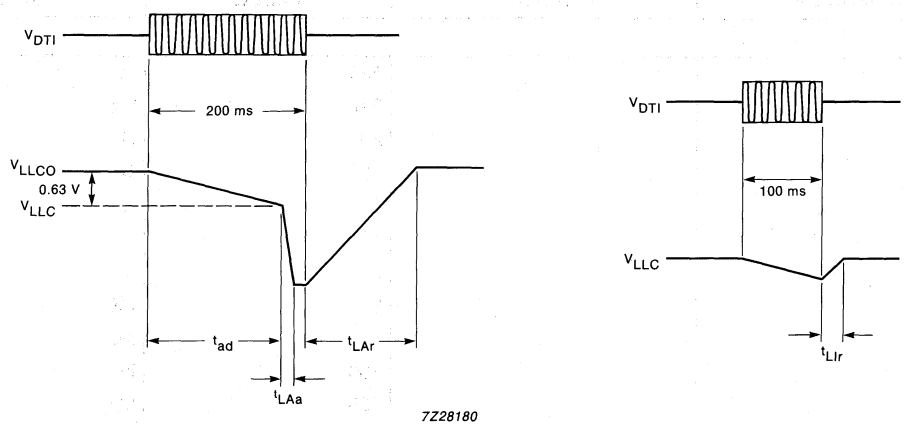
$$I_{LN} = \frac{V_{SUP-SREF}}{R20}$$

The pins not shown in the TEA1060 are left open. An impedance in series with pin SUP (e.g. an ammeter) should be avoided as it interferes with the value of I_{LN}.

Fig.14 Test circuit.

Table 2 Component values in test circuit Fig.14

COMPONENT	CONDITION	VALUE	UNIT
Resistor			
R1		620	Ω
R5		3.6	kΩ
R9		20	Ω
R20		150	Ω
R25		10	kΩ
R26		10	kΩ
R27		8	MΩ
R28		8	MΩ
R29		4	MΩ
R30		100	kΩ
R31		220	kΩ
R32		100	kΩ
R33		500	Ω
R34		100	kΩ
R35		51	kΩ
R36		120	kΩ
Capacitor			
C1		100	µF
C3		4.7	µF
C20		470	µF
C21		68	pF
C22		2.2	µF
C23		2.2	µF
C24		100	nF
C25		330	nF
C26		1	µF
C27		220	µF
C28		330	nF
C31	TEA1085 only	10	nF



(a) Listen-in release time (t_{LIr}); V_{DTI} = 100 mV(RMS); f = 3 kHz.

(b) Attack delay (t_{ad}), Larsen attack time (t_{LAa}), Larsen release time (t_{LAr}); V_{DTI} = 100 mV(RMS) and 1 V(RMS); f = 3 kHz.

Fig.15 Test signals for Larsen level limiter.

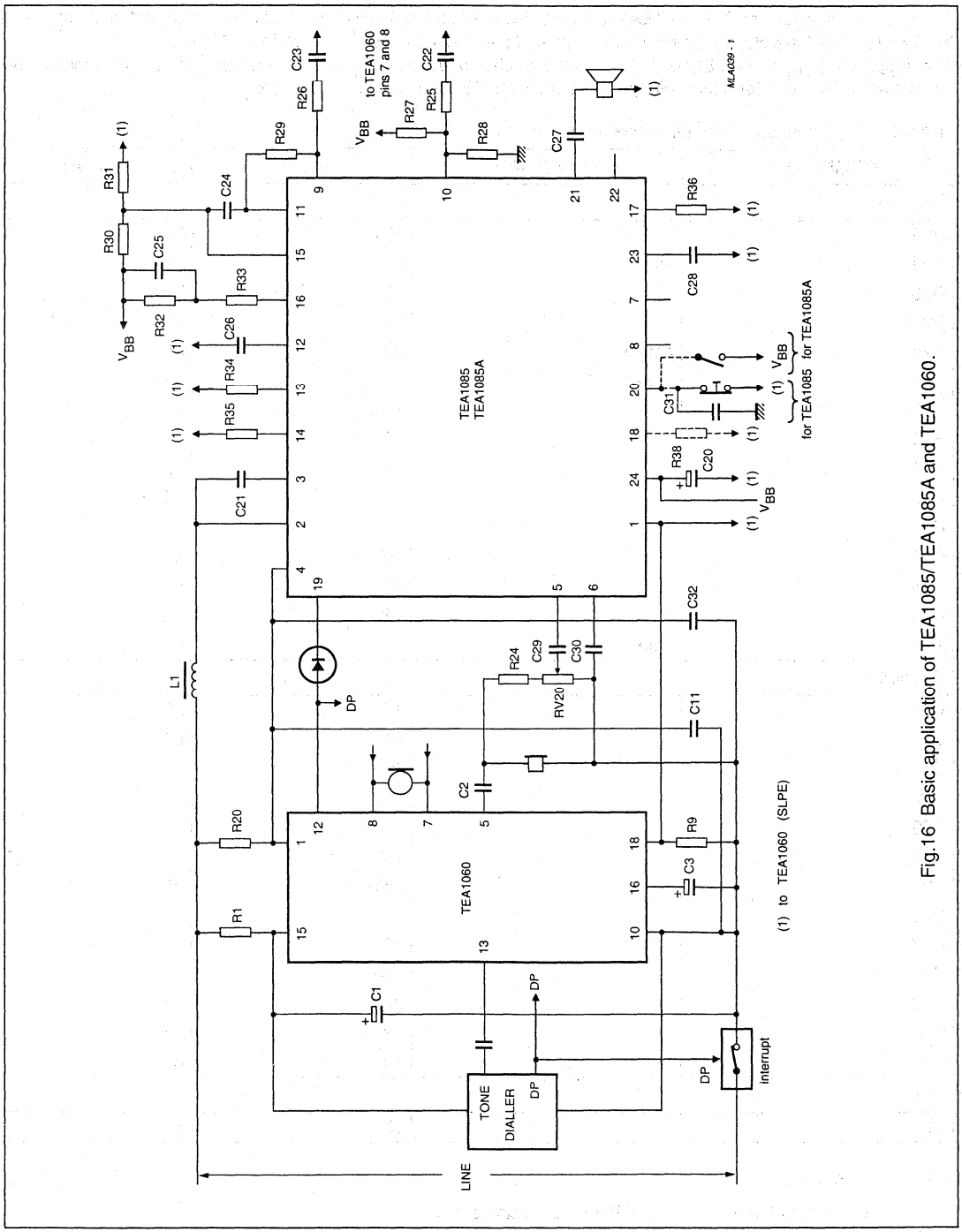


Fig.16 Basic application of TEA1085/TEA1085A and TEA1060.

APPLICATION INFORMATION

The basic application circuit of the TEA1085/TEA1085A is illustrated in Fig.16. Only the most important components of the TEA1060 part are shown, other components and their values are given in the TEA1060 Data sheet.
The supply pin (V_{BB}) of the TEA1085/TEA1085A can also be used to supply peripheral circuits (e.g. microcontrollers, diallers etc.). Further information will be published in the TEA1085 application report.

Table 3 Component values in application circuit Fig.16

COMPONENT	CONDITION	VALUE	UNIT
Resistor			
R20		150	Ω
R24	note 1	1	kΩ
R25		10	kΩ
R26		10	kΩ
R27	note 1	3.3	MΩ
R28	note 1	3.3	MΩ
R29	note 1	1.65	MΩ
R30		100	kΩ
R31		220	kΩ
R32		100	kΩ
R33		500	Ω
R34		100	kΩ
R35		51	kΩ
R36		120	kΩ
RV20	note 1	1	kΩ
Capacitor			
C11		4.7	nF
C20		470	µF
C21		47	pF
C22		4.7	nF
C23		4.7	nF
C24		4.7	nF
C25		330	nF
C26		1	µF
C27		47	µF
C28		330	nF
C29		220	nF
C30		220	nF
C31	TEA1085 only	10	nF
Coil			
L1		150	µH

Note to Table 3

1. Value depends on the gain setting of the transmission circuit.

SMPS battery charger control circuit TEA1088T

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

FEATURES

- SMPS control circuit
  fixed frequency/duty factor regulation
  emitter drive for power switch
  current mode control
  dynamic primary current limiting
- Charge control circuit
  accurate output current setting
  fast, two stages, charge mode
  two hours fast charge protection limit
  trickle charge mode for full batteries
- Voltage control circuit
  voltage regulation for connected mains and load
- Battery monitor circuit
  accurate fully charged detection (−dV phenomenon)
  LOW-level detection and indication
  protection against faulty batteries, short or open-circuit
  data output for condition of charge processing
  very LOW stand-by current, < 10 μA

GENERAL DESCRIPTION

The TEA1088T is a control circuit which has been designed for use in a battery charger and/or monitor system. The device incorporates all the control and protection functions that are required in a switched-mode power supply used to deliver charge current. The circuit also achieves direct drive to the emitter of the SMPS power transistor.
The battery monitor circuit includes a reliable battery-full detector which controls the switch-over from fast charge to trickle charge mode and, in the discharge mode, a battery-LOW detector with two outputs for an LED or buzzer warning indicator.
Protections are provided against open-circuit, short-circuit or faulty batteries.
The device is primarily designed to control two batteries in series. The number of cells can be extended by using a tap.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1088T	16	SO16	plastic	SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_6	supply voltage	charge	5.5	-	31.0	V
I_6	supply current	charge	-	-	19	mA
I_{10}	supply current	discharge	-	-	12	mA
I_{10}	stand by current		-	-	10	µA
I_1	SMPS transistor bias current		-	–2	-	mA
V_2-V_3	saturation voltage emitter switch	I_2 = 350 mA	0.9	-	1.4	V
V_{10}	battery voltage range	2 cells	1.8	-	4.0	V
V_{11}	threshold battery LOW indication		1.17	-	1.33	V
$I_{13,14}$	LED output currents	$V_{13,14}$ = 0.5 V	21	30	39	mA
V_{10}	voltage range of battery full detection		2.3	-	4.3	V
V_{10}	threshold for full indication		-	–22	-	mV

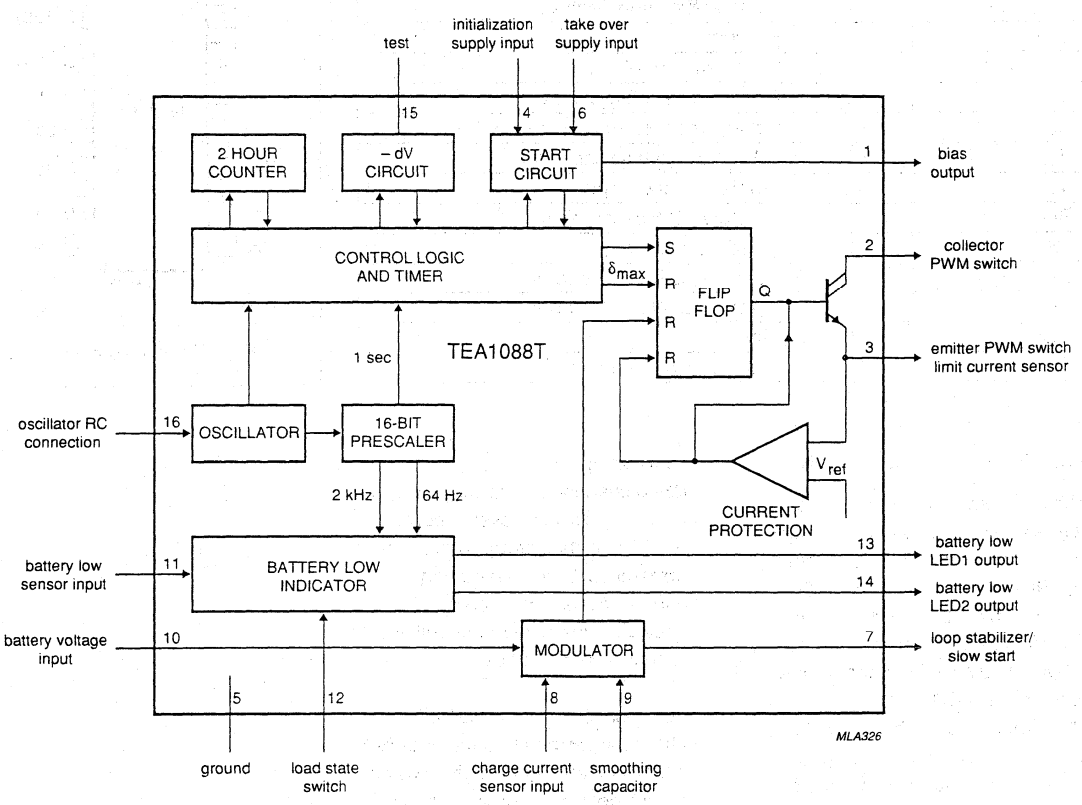


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
O2	1	bias output
O1	2	collector PWM switch
IT	3	emitter PWM switch/limit current sensor
V_{IC}	4	initialization supply input
GND	5	ground
V_{AT}	6	take over supply input
MI	7	loop stabilizer/slow start
I_{IN}	8	charge current sense input
V_{IN}	9	"V_{AC}" smoothing capacitor
V_{AC}	10	battery voltage input
BLI	11	battery LOW sense input
LS	12	load state switch
L1	13	battery LOW LED1 output
L2	14	battery LOW LED2 output
TEST	15	test pin
OSC	16	oscillator RC connection

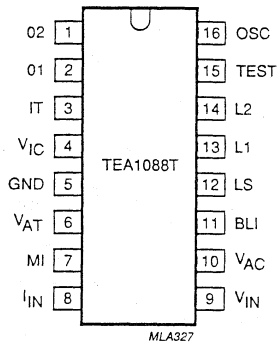


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The pin description of the device refers to external components as illustrated in the test circuit diagram (Fig.9). In this circuit the TEA1088T directly drives the emitter of the SMPS Darlington power transistor to provide fast switching and a wide reverse bias SOAR.
The supply output characteristics are shown in Fig.4 and the operational cycles of the charger system are shown in Fig.5.

The battery monitor circuit includes a reliable battery-full detector which controls switch-over from the fast charge to the trickle charge mode. The battery-full detector employs the phenomenon of an increase in battery voltage during charge due to the conversion of charge current into stored energy and, when the battery is full, a slight decrease in voltage due to a negative temperature coefficient when the charge current is only dissipative.
During charging the battery voltage is carefully sampled every second, the SMPS is then stopped to prevent interference. When a reducing voltage, –dV, is measured in succession the detector circuit sets the trickle charge mode.

In the discharge mode the battery LOW detector monitors the battery voltage and an output is given when the voltage drops below a set value. The output signals on the L1 and L2 pins are given in Figure 6. The device can also be employed purely as a monitor, this is because the monitor circuit is separate from the charge circuit. Figure 8 gives an application example.

Hands-free IC TEA1093

FEATURES

- Line powered supply with:
  - adjustable stabilized supply voltage
  - power down function.
- Microphone channel with:
  - externally adjustable gain
  - microphone mute function
- Loudspeaker channel with:
  - externally adjustable gain
  - dynamic limiter to prevent distortion
  - rail-to-rail output stages for single-ended or bridge-tied load drive
  - logarithmic volume control via linear potentiometer
  - loudspeaker mute function
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:
    - externally adjustable sensitivity
    - externally adjustable signal envelope time constant
    - externally adjustable noise envelope time constant
  - decision logic with:
    - externally adjustable switch-over timing
    - externally adjustable idle mode timing
    - externally adjustable dial tone detector in receive channel
  - voice switch control with:
    - adjustable switching range
    - constant sum of gain during switching
    - constant sum of gain at different volume settings.

APPLICATIONS

- Line-powered telephone sets with hands-free/listening-in functions.

GENERAL DESCRIPTION

The TEA1093 is a bipolar circuit intended for use in line-powered telephone sets. In conjunction with a member of the TEA1060 family or PCA1070 transmission circuits, the device offers a hands-free function for line powered telephone sets. It incorporates a supply, a microphone channel, a loudspeaker channel and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1093	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1093T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	operating supply current (pin SUP)		6.8	–	140	mA
V_{BB}	stabilized supply voltage		3.45	3.6	3.75	V
$I_{BB(pd)}$	current consumption from pin V_{BB} in power-down condition	PD = HIGH; V_{BB} = 3.6 V	–	400	550	µA
$I_{SUP(pd)}$	current consumption from pin SUP in power-down condition	PD = HIGH; V_{sup} = 4.5 V	–	55	75	µA
G_{vtx}	voltage gain from pin MIC to pin MOUT in transmit mode	V_{MIC} = 1 mV (RMS); R_{GAT} = 30.1 kΩ	13	15	17	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−10	–	+10	dB
G_{vrx}	voltage gain in receive mode	V_{RIN} = 20 mV (RMS); R_{GAR} = 66.5 kΩ; R_L = 50 Ω				
	the difference between RIN1 and RIN2 to LSP1 or LSP2 single-ended load		16	18	20	dB
	the difference between RIN1 and RIN2 to the difference between LSP1 and LSP2 bridge-tied load		22	24	26	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−15	–	+15	dB
$V_{O(p-p)}$	bridge-tied load (peak-to-peak value)	V_{RIN} = 150 mV (RMS); R_L = 33 Ω; note 1	–	5.15	–	V
SWRA	switching range		36.5	40	43.5	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to R_{SWR} = 365 kΩ		−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

Note

1. Corresponds to 100 mW output power.

BLOCK DIAGRAM

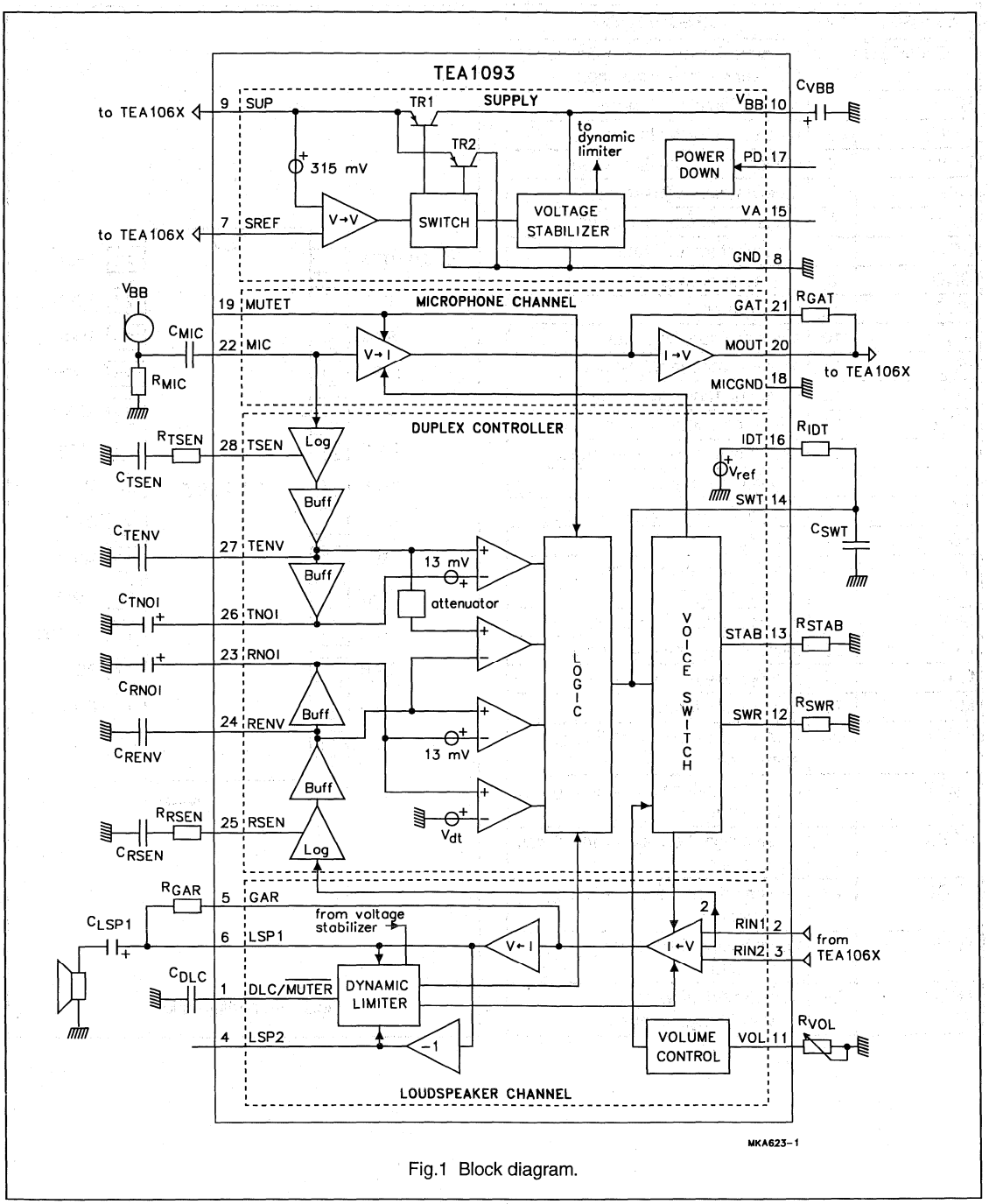


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DLC/$\overline{\text{MUTER}}$	1	dynamic limiter timing adjustment, receiver channel mute input
RIN1	2	receiver amplifier input 1
RIN2	3	receiver amplifier input 2
LSP2	4	loudspeaker amplifier output 2
GAR	5	receiver gain adjustment
LSP1	6	loudspeaker amplifier output 1
SREF	7	supply reference input
GND	8	ground reference
SUP	9	supply input
V_{BB}	10	stabilized supply output
VOL	11	receiver volume adjustment
SWR	12	switching range adjustment
STAB	13	reference current adjustment
SWT	14	switch-over timing adjustment
VA	15	V_{BB} voltage adjustment
IDT	16	idle mode timing adjustment
PD	17	power-down input
MICGND	18	ground reference for the microphone amplifier
MUTET	19	transmit channel mute input
MOUT	20	microphone amplifier output
GAT	21	microphone gain adjustment
MIC	22	microphone input
RNOI	23	receive noise envelope timing adjustment
RENV	24	receive signal envelope timing adjustment
RSEN	25	receive signal envelope sensitivity adjustment
TNOI	26	transmit noise envelope timing adjustment
TENV	27	transmit signal envelope timing adjustment
TSEN	28	transmit signal envelope sensitivity adjustment

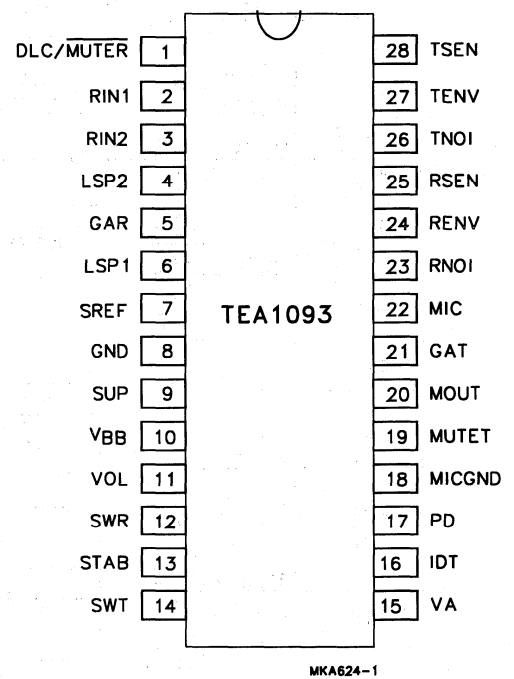


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The values given in the functional description are typical values except when otherwise specified.

A principle diagram of the TEA106X is shown on the left side of Fig.3. The TEA106X is a transmission circuit of the TEA1060 family intended for hand-set operation. It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone and a hybrid. For more details on the TEA1060 family, please refer to *"Data Handbook IC03"*. The right side of Fig.3 shows a principle diagram of the TEA1093, a hands-free add-on circuit with a microphone amplifier, a loudspeaker amplifier and a duplex controller.

As can be seen from Fig.3, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller.The duplex controller of the TEA1093 detects which channel has the 'largest' signal and then controls the gain of the microphone amplifier and the loudspeaker amplifier so that the sum of the gains remains constant. As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode): the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.
2. Receive mode (Rx mode): the gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.
3. Idle mode: the gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

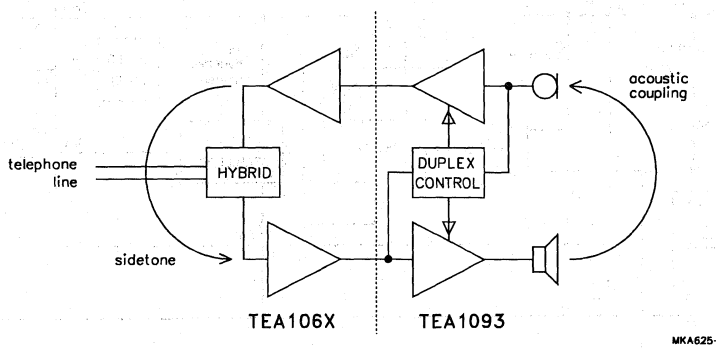


Fig.3 Hands-free telephone set principles.

Supply: pins SUP, SREF, V_{BB}, GND, VA and PD

As can be seen from Fig.4, the line current is divided between the speech-transmission circuit ($I_{TR} + I_{CC}$) and the TEA1093 circuit (I_{SUP}). It can be shown that:

$I_{SUP} = I_{line} - I_{TR} - I_{CC}$

Where:

$I_{TR} = V_{SUP} - V_{SREF}/R_{SREF}$

$V_{SUP} - V_{SREF} = 315$ mV

$R_{SREF} = 100\ \Omega$

$I_{CC} \approx 1$ mA

It follows that $I_{SUP} \approx I_{LINE} - 4$ mA.

The TEA1093 stabilizes its own supply voltage of 3.6 V at V_{BB}. The voltage on V_{BB} can be adjusted by means of an external resistor R_{VA}. When R_{VA} is connected between pin V_A and GND, the voltage on V_{BB} is increased, when connected between pin V_A and V_{BB}, it is decreased. This is shown in Fig.5. A capacitor of 4.7 nF (C_{SREF}) is required to ensure stability of the supply block. When V_{SUP} is greater than $V_{BB} + 0.4$ V, the current I_{SUP} is supplied to V_{BB} via TR1. When V_{SUP} is less, the current is shunted to GND via TR2, which prevents distortion on the line.

To reduce current consumption during pulse dialling or register recall (flash), the TEA1093 is provided with a power-down (PD) input. When the voltage on PD is HIGH, the current consumption from SUP is 55 µA and from V_{BB} 400 µA. Therefore a capacitor of 470 µF (C_{VBB}) is sufficient to power the TEA1093 during pulse dialling.

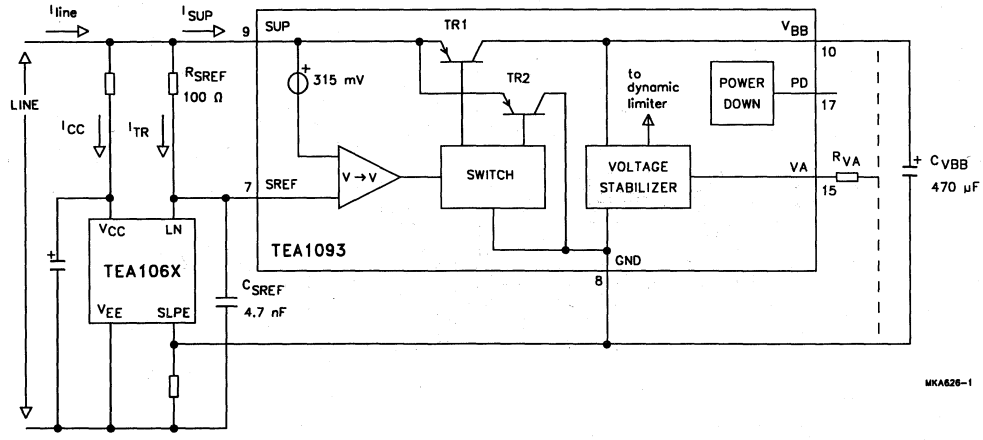


Fig.4 Supply arrangement.

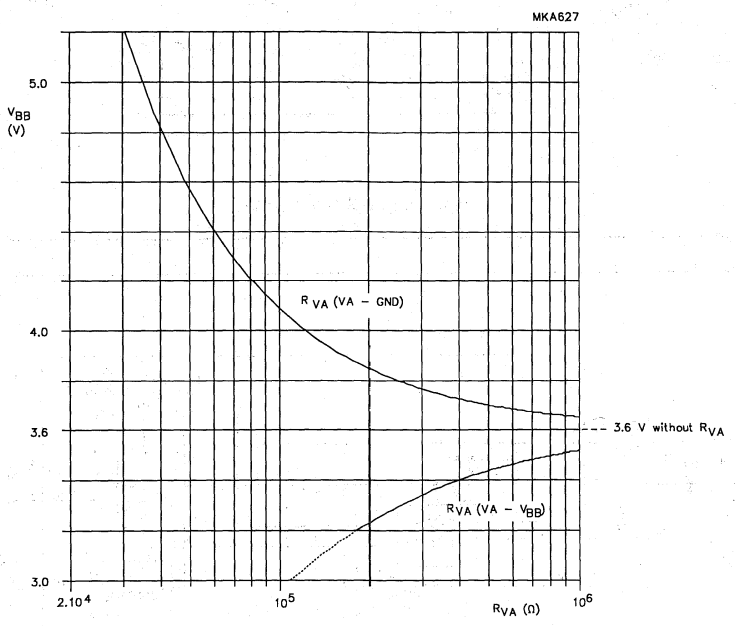


Fig.5 V_{BB} as a function of R_{VA}.

Microphone channel: pin MIC, GAT, MOUT, MICGND and MUTET

The TEA1093 has an asymmetrical microphone input MIC with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1093. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The output capability at pin MOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the microphone amplifier (from pin MIC to MOUT) can be adjusted from 5 dB up to 25 dB to suit specific application requirements. The gain is proportional to the value of R_{GAT} and equals 15 dB typical with R_{GAT} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GAT} to ensure stability of the microphone amplifier. Together with R_{GAT}, it also provides a first-order low-pass filter.

By applying a HIGH level on pin MUTET, the microphone amplifier is muted and the TEA1093 is automatically forced into the receive mode.

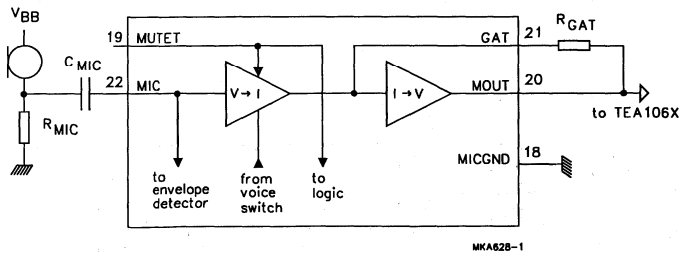


Fig.6 Microphone channel.

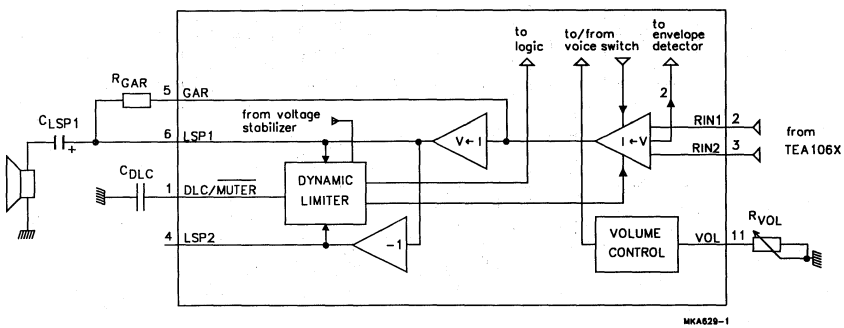


Fig.7 Loudspeaker channel.

Loudspeaker channel

LOUDSPEAKER AMPLIFIER: PINS RIN1, RIN2, GAR, LSP1 AND LSP2

The TEA1093 has symmetrical inputs for the loudspeaker amplifier with an input resistance of 40 kΩ between RIN1 and RIN2 (2 x 20 kΩ). The input stage can accommodate signals up to 390 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The gain of the input stage varies according to the mode of the TEA1093. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker which is connected as a single-ended load (between LSP1 and GND) or as a bridge-tied load (between LSP1 and LSP2).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 3 dB up to 39 dB to suit specific application requirements. The gain from RIN1 or RIN2 to LSP1 is proportional to the value of R_{GAR} and equals 18 dB with R_{GAR} = 66.5 kΩ. The second output LSP2 is in opposite phase with LSP1. Therefore, in the basic application, the gain difference between RIN1 and RIN2 to LSP1 or LSP2 equals 24 dB typical with R_{GAR} = 66.5 kΩ.

A capacitor connected in parallel with R_{GAR} can be used to provide a first-order low-pass filter.

VOLUME CONTROL: PIN VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

DYNAMIC LIMITER: PIN DLC/$\overline{\text{MUTER}}$

The dynamic limiter of the TEA1093 prevents clipping of the loudspeaker output stages and protects the operation of the circuit when the supply condition falls below a certain level.

Hard clipping of the loudspeaker output stages is prevented by rapidly reducing the gain when the output stages start to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typical 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stages, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{RIN} is below 390 mV (RMS)].

When the supply conditions drop below the required level, the gain of the loudspeaker amplifier is reduced in order to prevent the TEA1093 from malfunctioning. Only the gain of the loudspeaker amplifier is affected since it is considered to be the major power consuming part of the TEA1093.

When the TEA1093 experiences a loss of current, the supply voltage V_{BB} decreases. In this event, the gain of the loudspeaker amplifiers is slowly reduced (approximately a few seconds). When the supply voltage continues to decrease and drops below an internal voltage threshold of 2.75 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When normal supply conditions are resumed, the gain of the loudspeaker amplifier is increased again. This system ensures that in the event of large continuous signals, all current is used to power the loudspeaker while the voltage on pin V_{BB} remains at its nominal value.

By forcing a level lower than 0.2 V on pin DLC/$\overline{\text{MUTER}}$, the loudspeaker amplifier is muted and the TEA1093 is automatically forced into the transmit mode.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelope detectors are shown in Fig.8.

For the transmit channel, the input signal at MIC is 40 dB, amplified to TSEN. For the receive channel, the differential signal between RIN1 and RIN2 is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first-order high-pass filter. In the basic application, see Fig.16, it is assumed that V_{MIC} = 1 mV (RMS) and V_{RIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is sufficient to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is sufficient for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

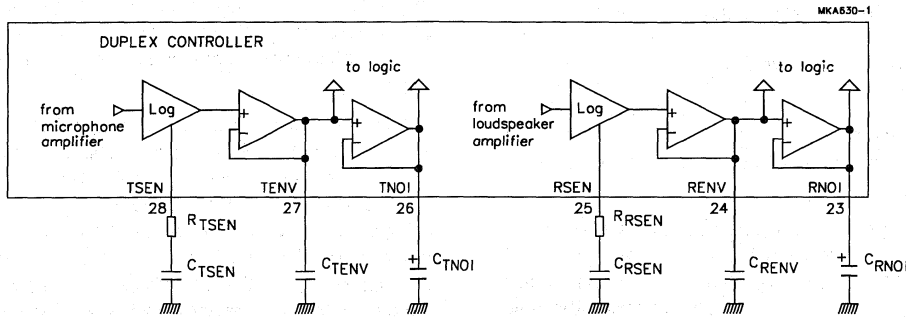


Fig.8 Signal and noise envelope detectors.

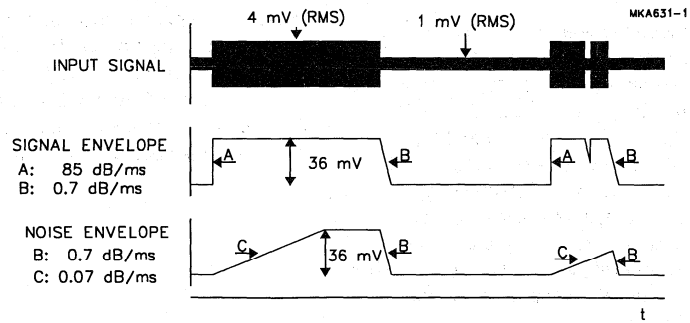
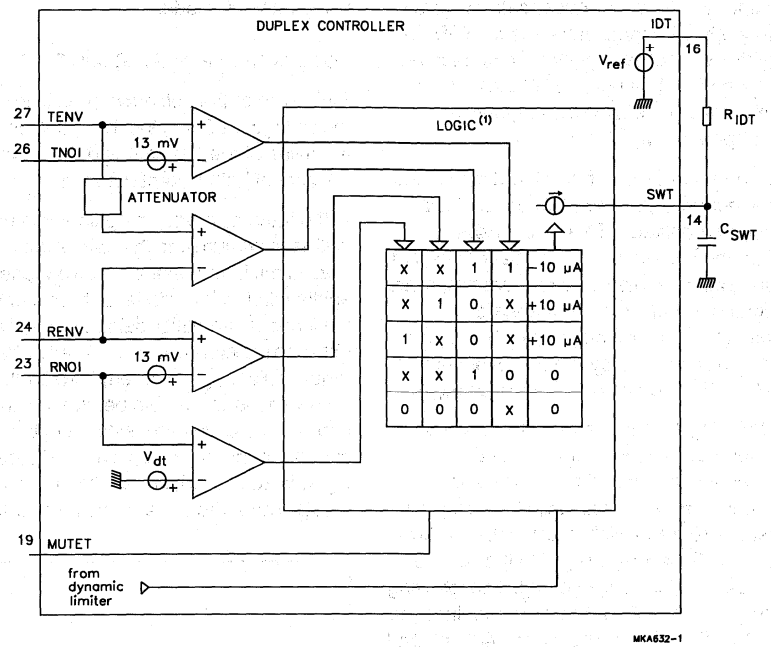


Fig.9 Signal and noise envelope waveforms.



(1) When MUTET = HIGH, +10 µA is forced.
When DLC/MUTER < 0.2 V, −10 µA is forced.

Fig.10 Decision logic.

To determine the noise level, the signal on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 µA and a maximum sink current of 120 µA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.16, the value of both capacitors is 4.7 µF. At room temperature, the 1 µA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms. This is small enough to track background noise and not to be influenced by speech bursts. The 120 µA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.9.

Decision logic: pins IDT and SWT

The TEA1093 selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference V_{ENV}–V_{NOI} = 13 mV. This so called speech/noise threshold is implemented in both channels.

The signal on MIC contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1093 to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard applications, does not consider input signals between RIN1 and RIN2 as noise when they have a level greater than 127 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.10, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1093 and can vary between −400 mV and +400 mV.

Table 1 Modes of TEA1093.

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
> 80	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.16, C_{SWT} is 220 nF and R_{IDT} is 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch over, from receive mode or transmit mode to idle mode, is equal to $4 \times R_{IDT} \times C_{SWT}$ and is approximately 2 seconds (idle mode time).

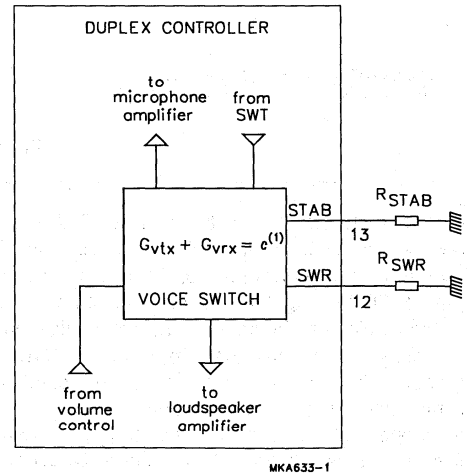
The inputs MUTET and DLC/$\overline{\text{MUTER}}$ overrule the decision logic. When MUTET goes HIGH, the capacitor C_{SWT} is charged with 10 μA thus resulting in the receive mode.

When the voltage on pin DLC/$\overline{\text{MUTER}}$ goes lower than 0.2 V, the capacitor is discharged with 10 μA thus resulting in the transmit mode.

VOICE-SWITCH: PINS STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.11. With the voltage on SWT, the TEA1093 voice-switch regulates the gains of the transmit and the receive channel so that the sum of both is kept constant.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gains are halfway. The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.16, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.12.



(1) c - constant.

Fig.11 Voice switch.

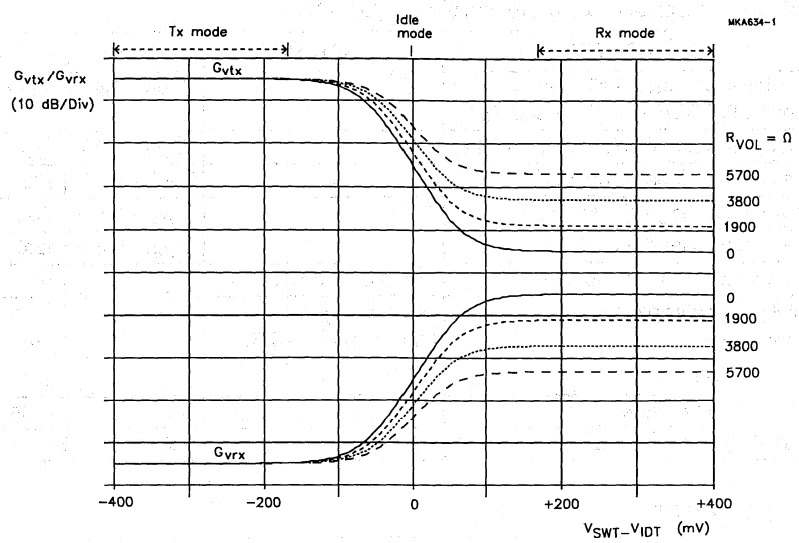


Fig.12 Switch-over behaviour.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.12). In the transmit mode, however, the volume control has no influence on the gain of the microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.

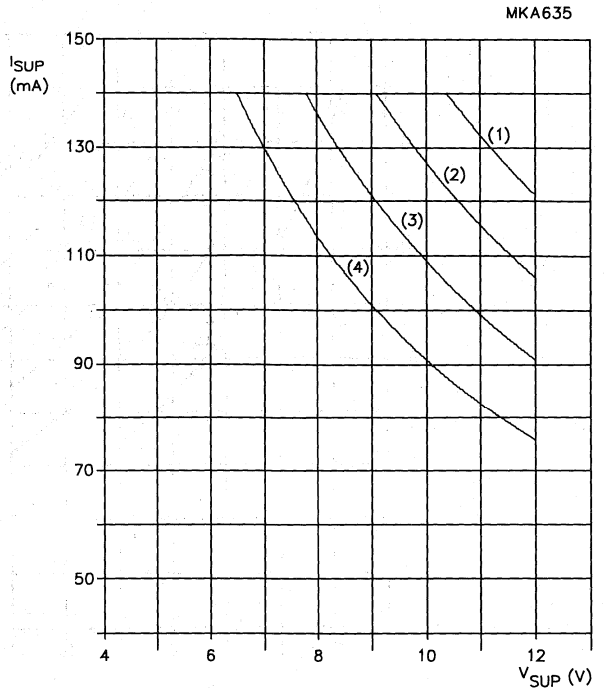
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins SUP, SREF, V_{BB}, RIN1 and RIN2		V_{GND} – 0.4 V	V_{BB} + 0.4 V	V
V_{RINmax}	maximum voltage on pin RIN1 or RIN2		V_{GND} – 1.2 V	V_{BB} + 0.4 V	V
V_{BBmax}	maximum voltage on pin V_{BB}		V_{GND} – 0.4 V	12.0	V
$V_{SREFmax}$	maximum voltage on pin SREF		V_{GND} – 0.4 V	V_{SUP} + 0.4 V	V
V_{SUPmax}	maximum voltage on pin SUP		V_{GND} – 0.4 V	12.0	V
I_{SUPmax}	maximum current on pin SUP	see also Figs 13 and 14	–	140	mA
P_{tot}	total power dissipation	see also Figs 13 and 14; T_{amb} = 75 °C			
	TEA1093		–	910	mW
	TEA1093T		–	670	mW
T_{stg}	storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

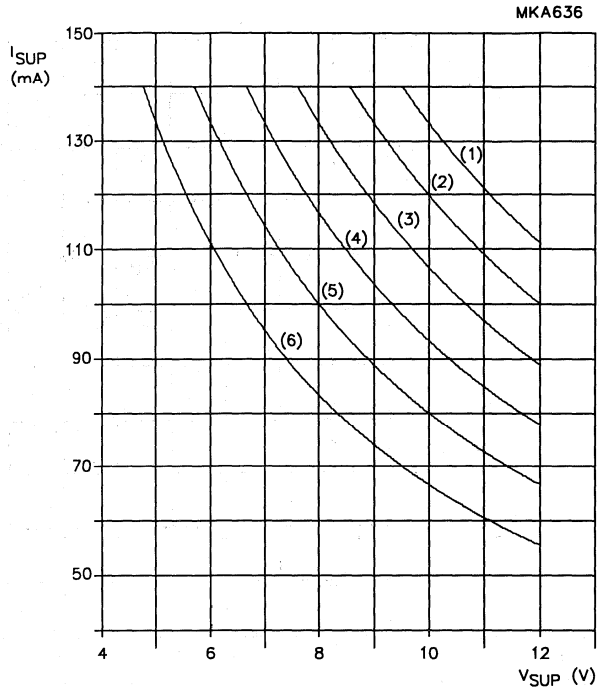
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1093	55	K/W
	TEA1093T	75	K/W



(1) T_{amb} = 45 °C; P_{tot} = 1.45 W.
(2) T_{amb} = 55 °C; P_{tot} = 1.27 W.
(3) T_{amb} = 65 °C; P_{tot} = 1.09 W.
(4) T_{amb} = 75 °C; P_{tot} = 0.91 W.

Fig.13 TEA1093 safe operating area.



(1) T_{amb} = 25 °C; P_{tot} = 1.33 W.
(2) T_{amb} = 35 °C; P_{tot} = 1.20 W.
(3) T_{amb} = 45 °C; P_{tot} = 1.07 W.
(4) T_{amb} = 55 °C; P_{tot} = 0.93 W.
(5) T_{amb} = 65 °C; P_{tot} = 0.80 W.
(6) T_{amb} = 75 °C; P_{tot} = 0.67 W.

Fig.14 TEA1093T safe operating area.

CHARACTERISTICS

V_{SREF} = 4.2 V; V_{GND} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V (RMS); f = 1 kHz; T_{amb} = 25 °C; PD = LOW; MUTET = LOW; R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.15; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (VA, SREF, SUP, V_{BB}, GND and PD)						
V_{BB}	stabilized supply voltage		3.45	3.6	3.75	V
$\Delta V_{BB(ISUP)}$	V_{BB} variation with I_{SUP}	I_{SUP} = 15 to 140 mA	–	20	–	mV
$\Delta V_{BB(T)}$	V_{BB} variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±20	–	mV
$\Delta V_{BB(RVA)}$	V_{BB} adjustment with R_{VA}	between VA and V_{BB}; R_{VA} = 180 kΩ	3.0	3.2	3.4	V
		between VA and GND; V_{SREF} = 4.9 V; R_{VA} = 56 kΩ,	4.25	4.5	4.75	V
$I_{SUP(min)}$	minimum operating current		–	5.5	6.8	mA
V_{SUP}–V_{BB}	minimum DC voltage drop between pin SUP and V_{BB}		0.4	–	–	V
$V_{SUP-SREF}$	internal reference voltage		275	315	355	mV
THD	total harmonic distortion of AC signal on SUP	V_{SUP} = 1 V (RMS)	–	0.5	–	%
Power-Down input PD						
V_{IL}	LOW level input voltage		V_{GND} – 0.4 V	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4 V	V
I_{PD}	input current in power-down condition	PD = HIGH	–	2.5	5.0	µA
$I_{SUP(PD)}$	current consumption from pin SUP in power-down condition	PD = HIGH; V_{SUP} = 4.5 V	–	55	75	µA
$I_{BB(PD)}$	current consumption from pin V_{BB} in power-down condition	PD = HIGH; V_{BB} = 3.6 V	–	400	550	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microphone channel (MIC, GAT, MOUT, MUTET and MICGND)						
MICROPHONE AMPLIFIER						
$\|Z_i\|$	input impedance between pin MIC and MICGND		17	20	23	kΩ
G_{vtx}	voltage gain from pin MIC to MOUT in transmit mode	V_{MIC} = 1 mV (RMS)	13	15	17	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−10	–	+10	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{MIC} = 1 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.3	–	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{MIC} = 1 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
V_{notx}	noise output voltage at pin MOUT	pin MIC connected to MICGND through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	−100	–	dBmp
TRANSMIT MUTE INPUT MUTET						
V_{IL}	LOW level input voltage		V_{GND} − 0.4 V	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4 V	V
I_{MUTET}	input current	MUTET = HIGH	–	2.5	5	µA
ΔG_{vtxm}	voltage gain reduction with MUTET active	MUTET = HIGH	–	80	–	dB
Loudspeaker channel (RIN1, RIN2, GAR, LSP1, LSP2 and DLC/$\overline{\text{MUTER}}$)						
LOUDSPEAKER AMPLIFIER						
$\|Z_i\|$	input impedance	between pins RIN1 or RIN2 and GND	17	20	23	kΩ
		between pins RIN1 and RIN2	34	40	46	kΩ
G_{vrx}	voltage gain in receive mode	V_{RIN} = 20 mV (RMS)				
	the difference between RIN1 and RIN2 to the difference between LSP1 and LSP2, bridge-tied load		22	24	26	dB
	the difference between RIN1 and RIN2 to LSP1 or LSP2, single-ended load		16	18	20	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−15	–	+15	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RIN} = 20 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RIN} = 20 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
$V_{RIN(rms)}$	maximum input voltage between RIN1 and RIN2 (RMS value)	for 2% THD in input stage; R_{GAR} = 11.8 kΩ	–	390	–	mV
$V_{norx(rms)}$	noise output voltage at pin LSP1 or LSP2 (RMS value)	inputs RIN1 and RIN2 short-circuited through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	80	–	µV
CMRR	common mode rejection ratio		–	50	–	dB
ΔG_{vrxv}	voltage gain variation related to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	–	3	–	dB
OUTPUT CAPABILITY						
$V_{OSE(p-p)}$	single-ended load (peak-to-peak value)	V_{RIN} = 150 mV (RMS); I_{SUP} = 11 mA; note 1	1.2	1.45	–	V
		V_{RIN} = 150 mV (RMS); I_{SUP} = 16.5 mA; note 2	2.5	2.9	–	V
$V_{OBTL(p-p)}$	bridge-tied load (peak-to-peak value)	V_{RIN} = 150 mV (RMS); I_{SUP} = 27 mA; note 2	2.5	2.9	–	V
		V_{RIN} = 150 mV (RMS); I_{SUP} = 35 mA; note 3	3.5	4.0	–	V
		V_{RIN} = 150 mV (RMS); I_{SUP} = 62 mA; R_L = 33 Ω; note 4	–	5.15	–	V
DYNAMIC LIMITER						
t_{att}	attack time when V_{RIN} jumps from 20 mV to 20 mV + 10 dB	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA	–	–	5	ms
t_{rel}	release time when V_{RIN} jumps from 20 mV + 10 dB to 20 mV	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA	–	250	–	ms
THD	total harmonic distortion at V_{RIN} = 20 mV + 10 dB	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA; $t > t_{att}$	–	0.9	5	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.75	–	V
t_{att}	attack time when V_{BB} jumps below $V_{BB(th)}$		–	1	–	ms
MUTE RECEIVE						
$V_{DLC(th)}$	threshold voltage required on pin DLC/$\overline{\text{MUTER}}$ to obtain mute receive condition		V_{GND} – 0.4 V	–	0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC/$\overline{\text{MUTER}}$ in mute receive condition	V_{DLC} = 0.2 V	–	80	–	µA
ΔG_{vrxm}	voltage gain reduction in mute receive condition	V_{DLC} < 0.2 V	–	80	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Envelope and noise detectors (TSEN, TENV, RSEN and RENV)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from MIC to TSEN		38.3	40	41.7	dB
$G_{v(RSEN)}$	voltage gain between RIN1 and RIN2 to RSEN.		−1.7	0	+1.7	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\Delta V_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 µA	–	18	–	mV
$\Delta V_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 µA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	µA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	µA
ΔV_{ENV}	voltage difference between pin RENV and TENV	when 10 µA is sourced from both RSEN and TSEN; envelope detectors tracking; note 5	–	±3	–	mV
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pin TNOI or RNOI		0.75	1	1.25	µA
$I_{sink(NOI)}$	maximum current sunk by pin TNOI or RNOI		–	120	–	µA
ΔV_{NOI}	voltage difference between pin RNOI and TNOI	when 5 µA is sourced from both RSEN and TSEN; noise detectors tracking; note 5	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pin RIN1 and RIN2 (RMS value)		–	127	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pin RENV and RNOI to switch-over from receive to idle mode	$V_{RIN} < V_{RINDT}$; note 6	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pin TENV and TNOI to switch-over from transmit to idle mode	note 6	–	13	–	mV
SWITCH-OVER						
$I_{sourceSWT}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	µA
$I_{sinkSWT}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	µA
$I_{idleSWT}$	current sourced from pin SWT in idle mode		–	0	–	µA
Voice switch (STAB and SWR)						
SWRA	switching range		36.5	40	43.5	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to 365 kΩ		–40	–	12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		17.5	20	22.5	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to 5 mW output power.
2. Corresponds to 20 mW output power.
3. Corresponds to 40 mW output power.
4. Corresponds to 100 mW output power.
5. Corresponds to ±1 dB tracking.
6. Corresponds to 4.3 dB noise/speech recognition level.

HANDLING

ESD in accordance with MIL STD883C; Method 3015 (HBM 1500 Ω, 100 pF); 3 pulses positive and 3 pulses negative on each pin referenced to ground. Class 2: 2000 to 3999 V.

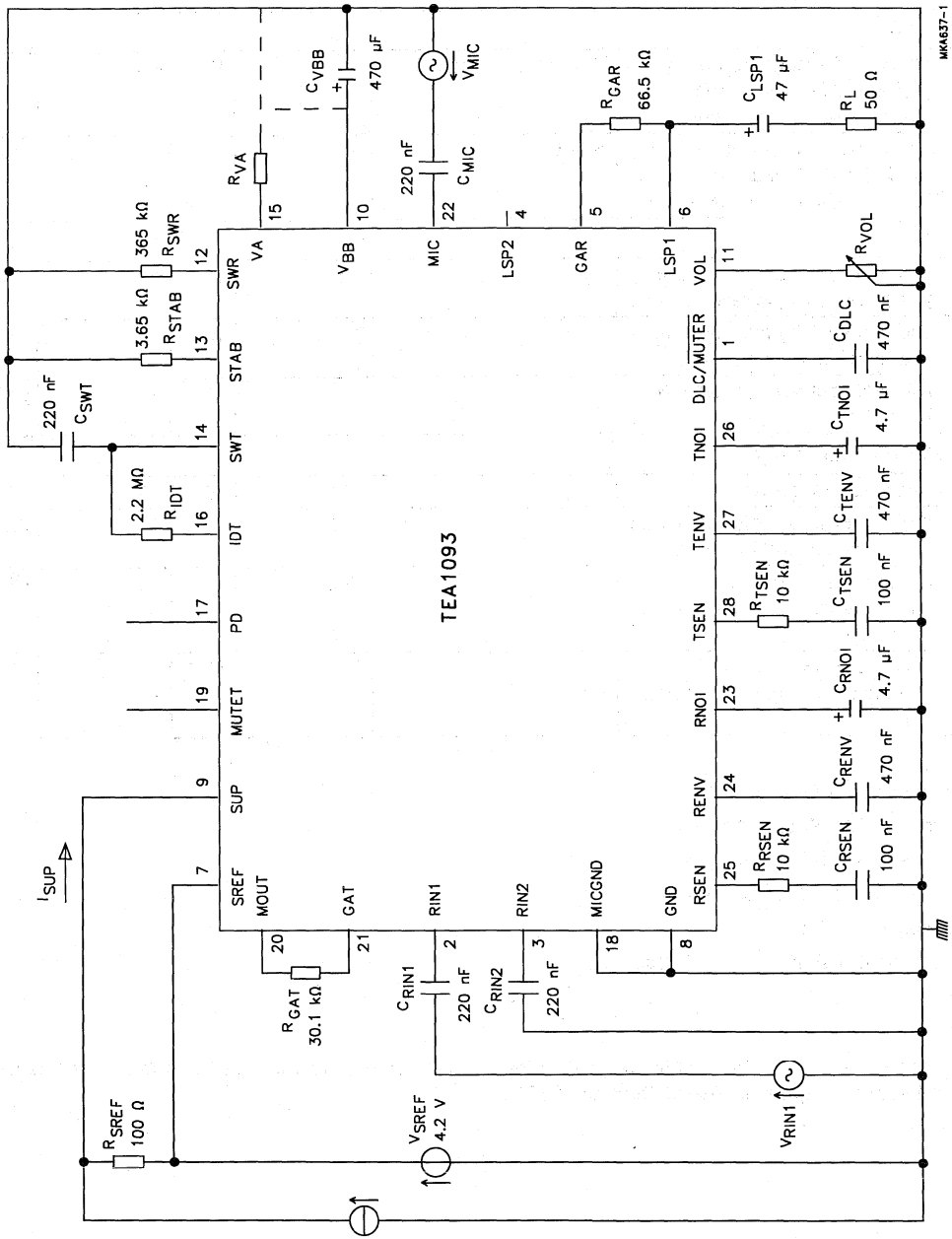


Fig.15 Test circuit.

APPLICATION INFORMATION

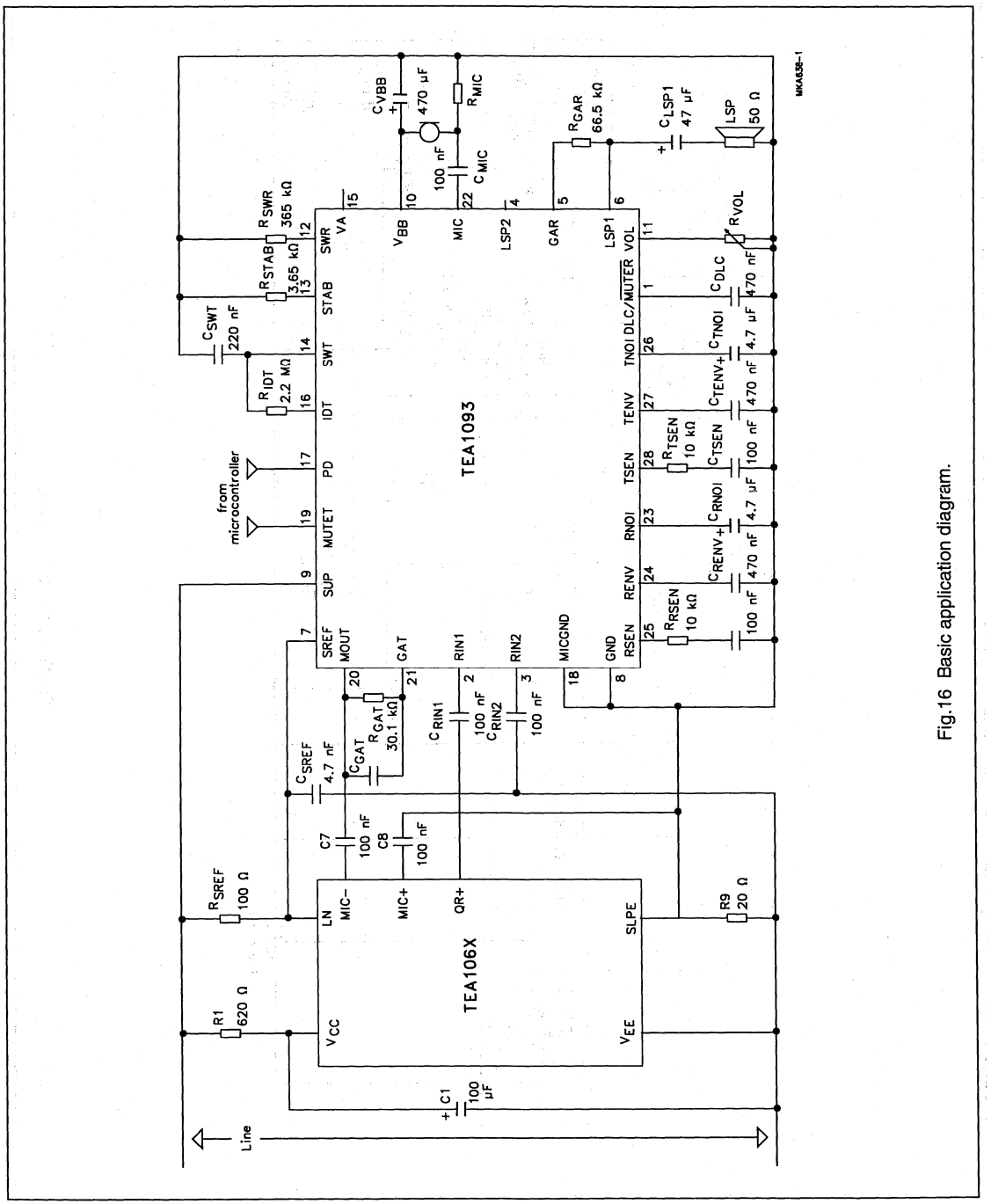


Fig.16 Basic application diagram.

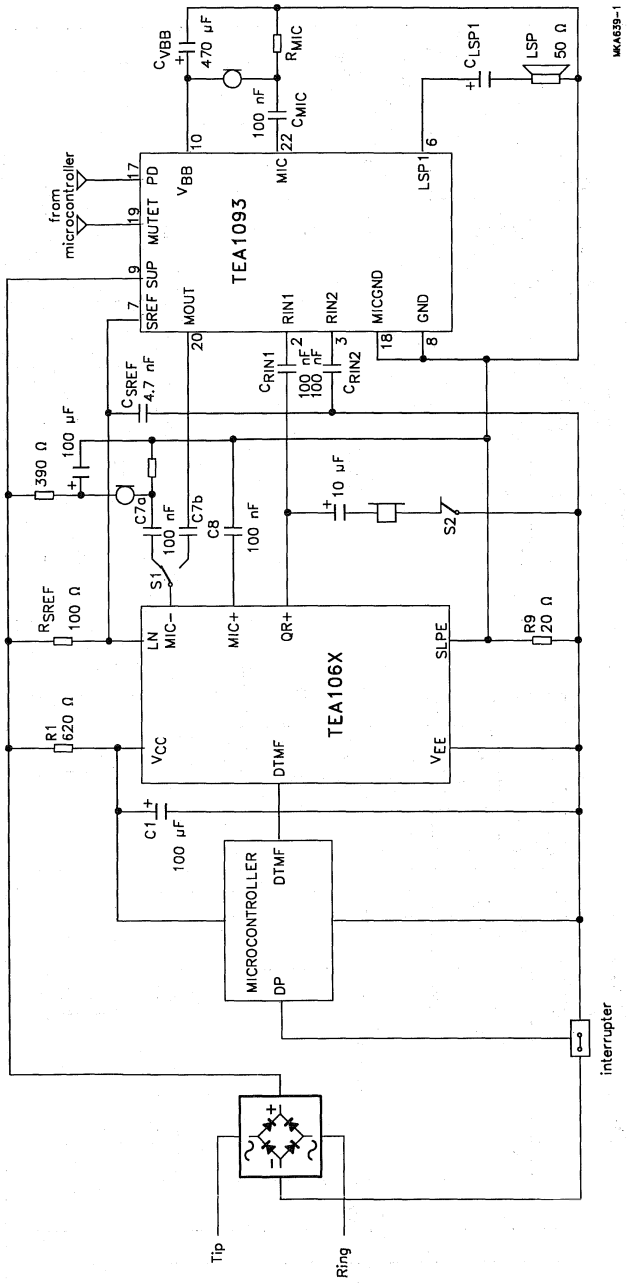


Fig.17 Application proposal.

Hands-free IC TEA1094

FEATURES

- Low power consumption
- Microphone channel with:
  - externally adjustable gain
  - microphone mute function
- Loudspeaker channel with:
  - externally adjustable gain
  - dynamic limiter to prevent distortion
  - rail-to-rail output stage for single-ended load drive
  - logarithmic volume control via linear potentiometer
  - loudspeaker mute function
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:
    - externally adjustable sensitivity
    - externally adjustable signal envelope time constant
    - externally adjustable noise envelope time constant
  - decision logic with:
    - externally adjustable switch-over timing
    - externally adjustable idle mode timing
    - externally adjustable dial tone detector in receive channel
  - voice switch control with:
    - adjustable switching range
    - constant sum of gain during switching
    - constant sum of gain at different volume settings.

APPLICATIONS

- Mains-powered telephone sets and cordless telephones with hands-free/listening-in functions
- Answering machines with hands-free/listening-in.

GENERAL DESCRIPTION

The TEA1094 is a bipolar circuit intended for use in mains-powered telephone sets, cordless telephones and answering machines. In conjunction with a member of the TEA1060 family (or PCA1070) transmission circuits, the device offers a hands-free function. It incorporates a microphone amplifier, a loudspeaker amplifier and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1094	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1094T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTET = LOW; R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.11; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BB}	supply voltage		3.3	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	3.6	5.0	mA
G_{vtx}	voltage gain from pin MIC to pin MOUT in transmit mode	V_{MIC} = 1 mV (RMS); R_{GAT} = 30.1 kΩ	13	15.5	18	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−15.5	–	+15.5	dB
G_{vrx}	voltage gain in receive mode; the difference between RIN1 and RIN2 to LSP	V_{RIN} = 20 mV (RMS); R_{GAR} = 66.5 kΩ; R_L = 50 Ω	16	18.5	21	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−18.5	–	+14.5	dB
$V_{O(p-p)}$	output voltage (peak-to-peak value)	V_{RIN} = 150 mV (RMS); R_{GAR} = 374 kΩ; R_L = 33 Ω; V_{BB} = 9.0 V; note 1	–	7.5	–	V
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to R_{SWR} = 365 kΩ		−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

Note

1. Corresponds to 200 mW output power.

BLOCK DIAGRAM

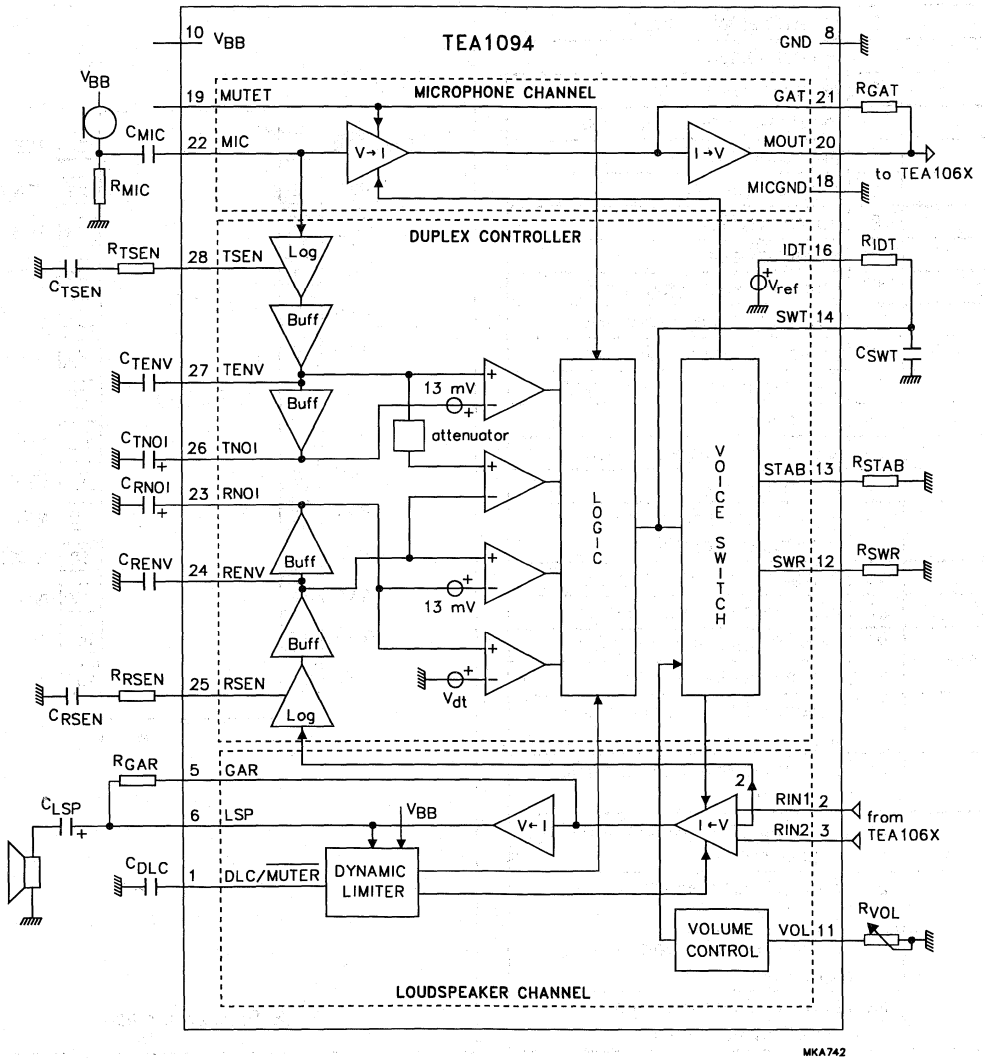


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DLC/$\overline{\text{MUTER}}$	1	dynamic limiter timing adjustment; receiver channel mute input
RIN1	2	receiver amplifier input 1
RIN2	3	receiver amplifier input 2
n.c.	4	not connected
GAR	5	receiver gain adjustment
LSP	6	loudspeaker amplifier output
n.c.	7	not connected
GND	8	ground reference
n.c.	9	not connected
V_{BB}	10	supply voltage
VOL	11	receiver volume adjustment
SWR	12	switching range adjustment
STAB	13	reference current adjustment
SWT	14	switch-over timing adjustment
n.c.	15	not connected
IDT	16	idle mode timing adjustment
n.c.	17	not connected
MICGND	18	ground reference for the microphone amplifier
MUTET	19	transmit channel mute input
MOUT	20	microphone amplifier output
GAT	21	microphone gain adjustment
MIC	22	microphone input
RNOI	23	receive noise envelope timing adjustment
RENV	24	receive signal envelope timing adjustment
RSEN	25	receive signal envelope sensitivity adjustment
TNOI	26	transmit noise envelope timing adjustment
TENV	27	transmit signal envelope timing adjustment
TSEN	28	transmit signal envelope sensitivity adjustment

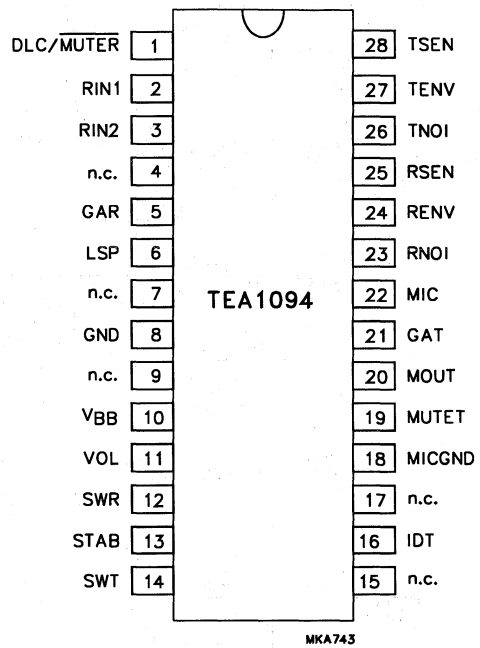


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The values given in the functional description are typical values unless otherwise specified.

A principle diagram of the TEA106X is shown on the left side of Fig.3. The TEA106X is a transmission circuit of the TEA1060 family intended for hand-set operation. It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone and a hybrid. For more details on the TEA1060 family, please refer to *"data Handbook IC03"*. The right side of Fig.3 shows a principle diagram of the TEA1094, a hands-free add-on circuit with a microphone amplifier, a loudspeaker amplifier and a duplex controller.

As can be seen from Fig.3, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1094 detects which channel has the 'largest' signal and then controls the gain of the microphone amplifier and the loudspeaker amplifier so that the sum of the gains remains constant. As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode).

   The gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.

2. Receive mode (Rx mode).

   The gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.

3. Idle mode.

   The gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

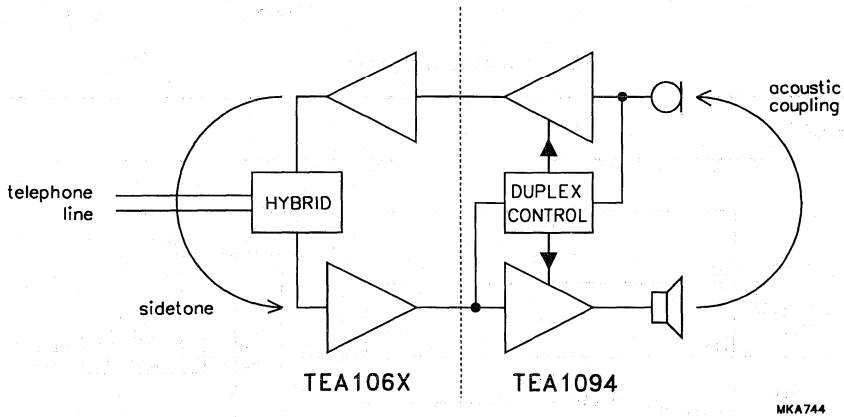


Fig.3 Hands-free telephone set principles.

Supply: pins V_{BB} and GND

The TEA1094 must be supplied with an external stabilized voltage source between pins V_{BB} and GND. In idle mode, without any signal, the internal supply current is 3.6 mA at V_{BB} = 5 V.

Microphone channel: pins MIC, GAT, MOUT, MICGND and MUTET (see Fig.4)

The TEA1094 has an asymmetrical microphone input MIC with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1094. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The output capability at pin MOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the microphone amplifier (from pins MIC to MOUT) can be adjusted from 0 dB up to 31 dB to suit specific application requirements. The gain is proportional to the value of R_{GAT} and equals 15.5 dB with R_{GAT} = 30.1 kΩ.

A capacitor connected in parallel with R_{GAT} can be used to provide a first-order low-pass filter.

By applying a HIGH level on pin MUTET, the microphone amplifier is muted and the TEA1094 is automatically forced into the receive mode.

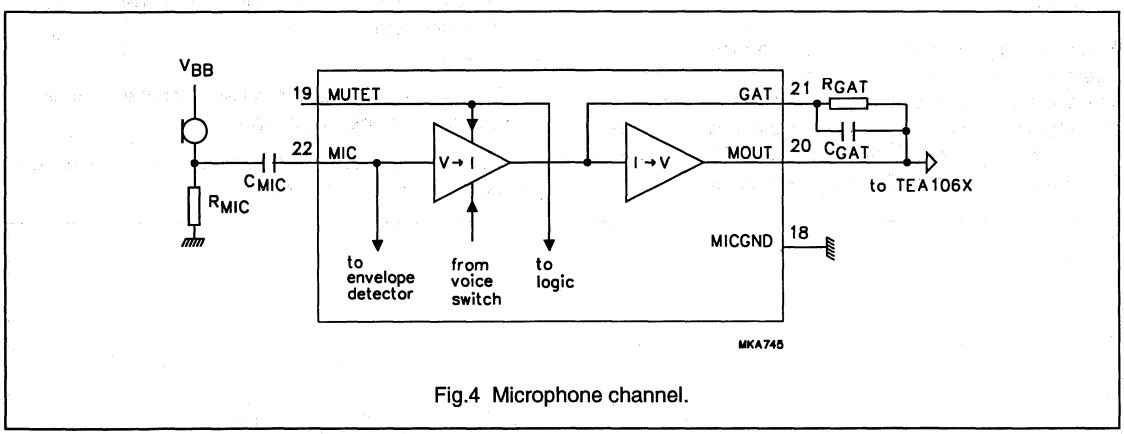


Fig.4 Microphone channel.

Loudspeaker channel

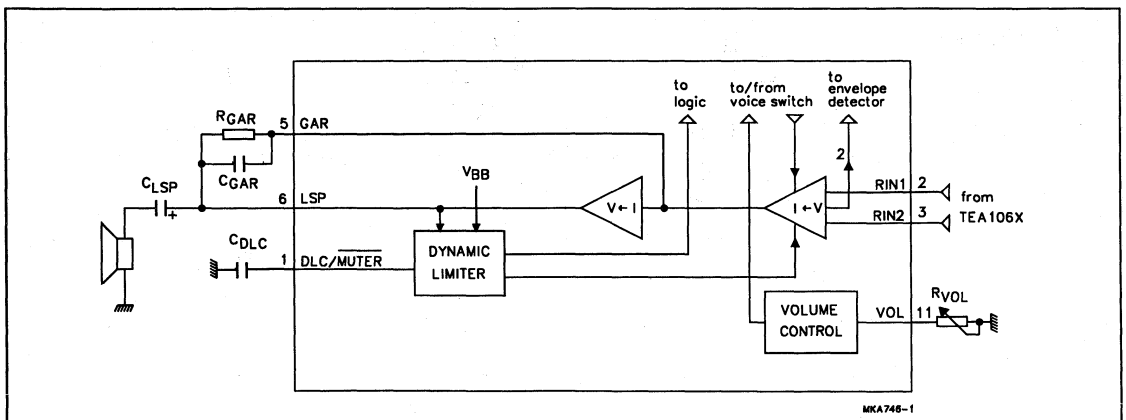


Fig.5 Loudspeaker channel.

LOUDSPEAKER AMPLIFIER: PINS RIN1, RIN2, GAR AND LSP

The TEA1094 has symmetrical inputs for the loudspeaker amplifier with an input resistance of 40 kΩ between RIN1 and RIN2 (2 × 20 kΩ). The input stage can accommodate signals up to 390 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The gain of the input stage varies according to the mode of the TEA1094. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker connected as a single-ended load (between LSP and GND).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 0 dB up to 33 dB to suit specific application requirements. The gain from RIN1 and RIN2 to LSP is proportional to the value of R_{GAR} and equals 18.5 dB with R_{GAR} = 66.5 kΩ. A capacitor connected in parallel with R_{GAR} can be used to provide a first-order low-pass filter.

VOLUME CONTROL: PIN VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

DYNAMIC LIMITER: PIN DLC/$\overline{\text{MUTER}}$

The dynamic limiter of the TEA1094 prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{BB} falls below 2.9 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{RIN} is below 390 mV (RMS)].

When the supply voltage drops below an internal threshold voltage of 2.9 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.9 V, the gain of the loudspeaker amplifier is increased again.

By forcing a level lower than 0.2 V on pin DLC/$\overline{\text{MUTER}}$, the loudspeaker amplifier is muted and the TEA1094 is automatically forced into the transmit mode.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelope detectors are shown in Fig.6.

For the transmit channel, the input signal at MIC is 40 dB, amplified to TSEN. For the receive channel, the differential signal between RIN1 and RIN2 is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first-order high-pass filter. In the basic application, see Fig.12, it is assumed that V_{MIC} = 1 mV (RMS) and V_{RIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is sufficient to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is sufficient for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

To determine the noise level, the signals on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and

C_{RNOI}, the timing can be set. In the basic application of Fig.12 the value of both capacitors is 4.7 µF. At room temperature, the 1 µA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms. This is small enough to track background noise and not to be influenced by speech bursts. The 120 µA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.7.

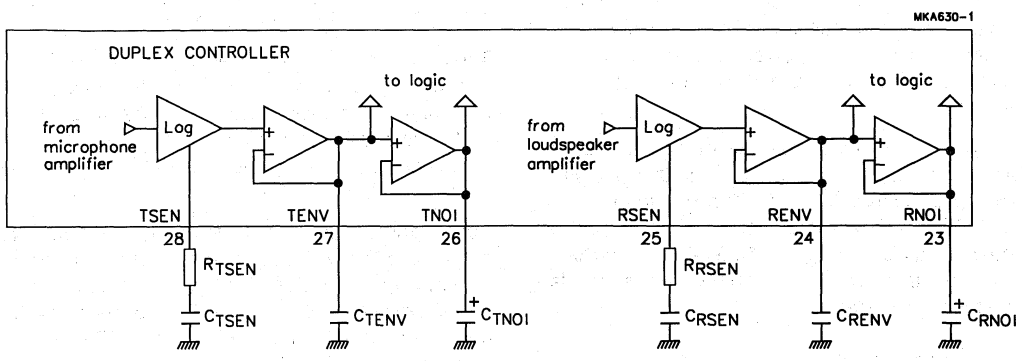


Fig.6 Signal and noise envelope detectors.

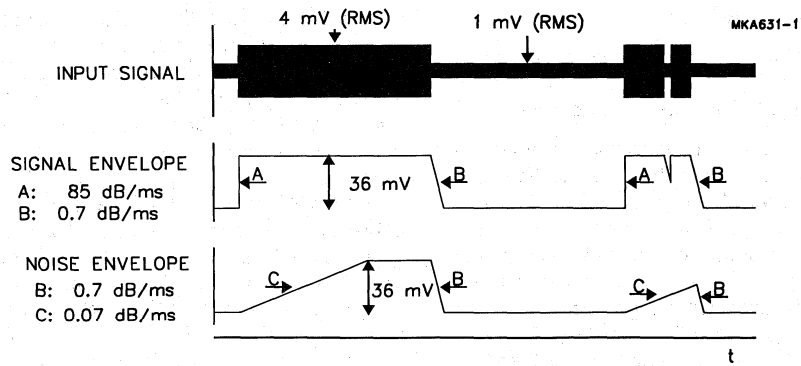
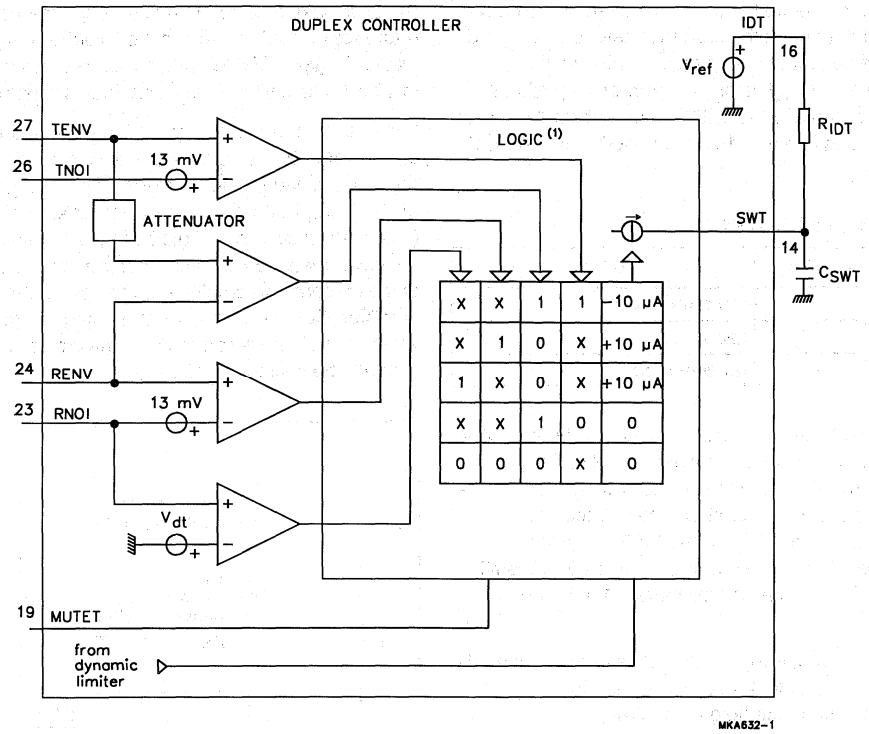


Fig.7 Signal and noise envelope waveforms.

DECISION LOGIC: PINS IDT AND SWT



(1) When MUTET = HIGH, +10 µA is forced.
When DLC/$\overline{\text{MUTER}}$ < 0.2 V, −10 µA is forced.

Fig.8 Decision logic.

The TEA1094 selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV} - V_{NOI} = 13$ mV. This so called speech/noise threshold is implemented in both channels.

The signal on MIC contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1094 to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard applications, does not consider input signals between RIN1 and RIN2 as noise when they have a level greater than 127 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.8, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1094 and can vary between –400 and +400 mV (see Table 1).

Table 1 Modes of TEA1094.

$V_{SWT} - V_{IDT}$ (mV)	MODE
<–180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.12, C_{SWT} is 220 nF and R_{IDT} is 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time, from receive mode or transmit mode to idle mode, is equal to $4 \times R_{IDT}C_{SWT}$ and is approximately 2 seconds (idle mode time).

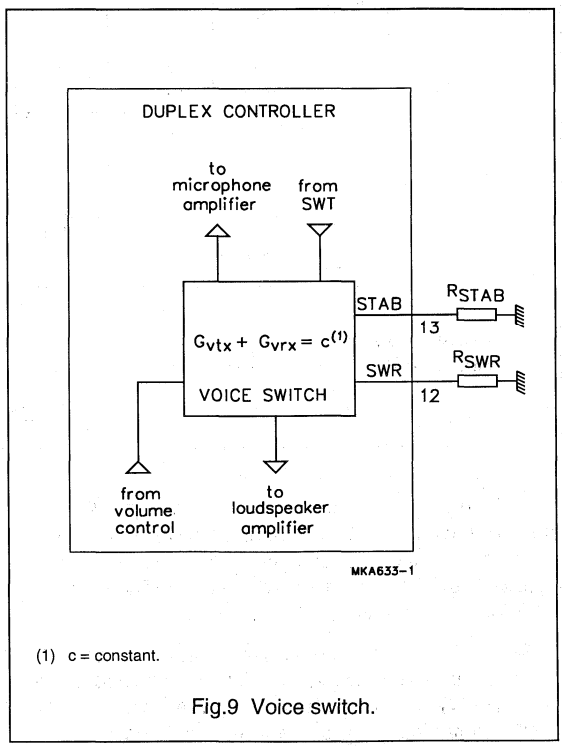
The inputs MUTET and DLC/$\overline{\text{MUTER}}$ overrule the decision logic. When MUTET goes HIGH, the capacitor C_{SWT} is charged with 10 μA thus resulting in the receive mode. When the voltage on pin DLC/$\overline{\text{MUTER}}$ goes lower than 0.2 V, the capacitor C_{SWT} is discharged with 10 μA thus resulting in the transmit mode.

VOICE-SWITCH: PINS STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.9. With the voltage on SWT, the TEA1094 voice-switch regulates the gains of the transmit and the receive channel so that the sum of both is kept constant.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gains are halfway. The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.12, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.10.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.10). In the transmit mode, however, the volume control has no influence on the gain of the microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.



(1) c = constant.

Fig.9 Voice switch.

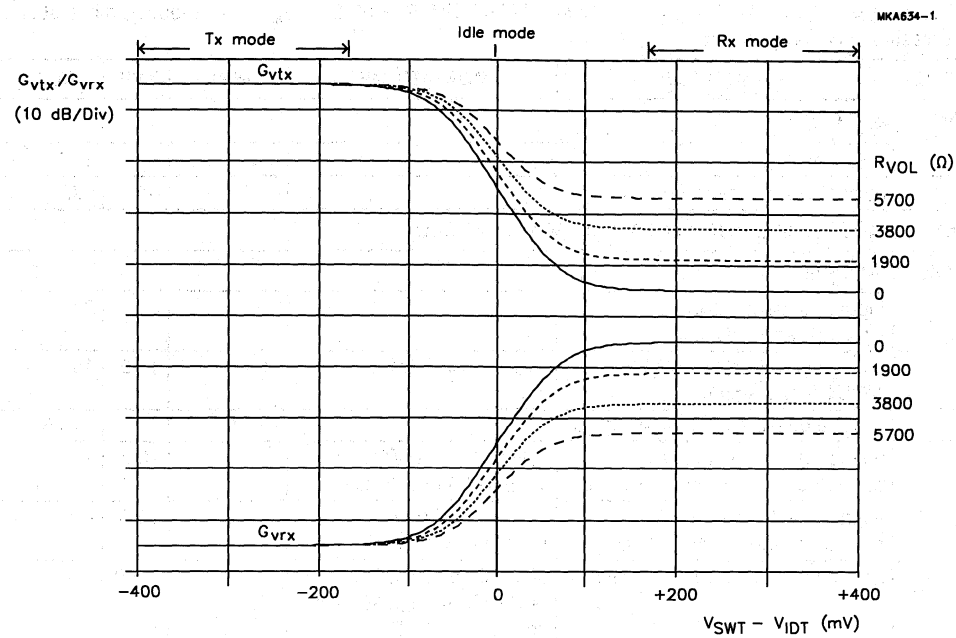


Fig.10 Switch-over behaviour.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins V_{BB}, RIN1 and RIN2		$V_{GND} - 0.4$	$V_{BB} + 0.4$	V
$V_{RIN(max)}$	maximum voltage on pins RIN1 and RIN2		$V_{GND} - 1.2$	$V_{BB} + 0.4$	V
$V_{BB(max)}$	maximum voltage on pin V_{BB}		$V_{GND} - 0.4$	12.0	V
P_{tot}	total power dissipation	T_{amb} = 75 °C			
	TEA1094		–	910	mW
	TEA1094T		–	670	mW
T_{stg}	storage temperature		−40	+125	°C
T_{amb}	operating ambient temperature		−25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	TEA1094	55	K/W
	TEA1094T	75	K/W

CHARACTERISTICS

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTET = LOW; R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.11; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_{BB} and GND)						
V_{BB}	supply voltage		3.3	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	3.6	5.0	mA
Microphone channel (MIC, GAT, MOUT, MUTET and MICGND)						
MICROPHONE AMPLIFIER						
$\|Z_i\|$	input impedance between pins MIC and MICGND		17	20	23	kΩ
G_{vtx}	voltage gain from pin MIC to MOUT in transmit mode	V_{MIC} = 1 mV (RMS)	13	15.5	18	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−15.5	–	+15.5	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{MIC} = 1 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.3	–	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{MIC} = 1 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
V_{notx}	noise output voltage at pin MOUT	pin MIC connected to MICGND through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	−100	–	dBmp
TRANSMIT MUTE INPUT MUTET						
V_{IL}	LOW level input voltage		V_{GND} − 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{MUTET}	input current	MUTET = HIGH	–	2.5	5	μA
ΔG_{vtxm}	voltage gain reduction with MUTET active	MUTET = HIGH	–	80	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Loudspeaker channel (RIN1, RIN2, GAR, LSP and DLC/$\overline{\text{MUTER}}$)						
LOUDSPEAKER AMPLIFIER						
$\lvert Z_i \rvert$	input impedance	between pins RIN1 or RIN2 and GND	17	20	23	kΩ
		between pins RIN1 and RIN2	34	40	46	kΩ
G_{vrx}	voltage gain in receive mode; between RIN1 and RIN2 to LSP	V_{RIN} = 20 mV (RMS)	16	18.5	21	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−18.5	–	+14.5	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RIN} = 20 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RIN} = 20 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
$V_{RIN(rms)}$	maximum input voltage between RIN1 and RIN2 (RMS value)	R_{GAR} = 11.8 kΩ; for 2% THD in input stage	–	390	–	mV
$V_{norx(rms)}$	noise output voltage at pin LSP (RMS value)	inputs RIN1 and RIN2 short-circuited through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	80	–	μV
CMRR	common mode rejection ratio		–	50	–	dB
ΔG_{vrxv}	voltage gain variation related to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	–	3	–	dB
OUTPUT CAPABILITY						
$V_{OSE(p-p)}$	output voltage (peak-to-peak value)	V_{RIN} = 300 mV (RMS); note 1	3.5	4.5	–	V
		V_{RIN} = 150 mV (RMS); R_{GAR} = 374 kΩ; R_L = 33 Ω; V_{BB} = 9.0 V; note 2	–	7.5	–	V
I_{OM}	maximum output current at LSP (peak value)		150	500	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DYNAMIC LIMITER						
t_{att}	attack time when V_{RIN} jumps from 20 mV to 20 mV + 10 dB	R_{GAR} = 374 kΩ	–	–	5	ms
t_{rel}	release time when V_{RIN} jumps from 20 mV + 10 dB to 20 mV	R_{GAR} = 374 kΩ	–	250	–	ms
THD	total harmonic distortion at V_{RIN} = 20 mV + 10 dB	R_{GAR} = 374 kΩ; $t > t_{att}$	–	0.9	5	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.9	–	V
t_{att}	attack time when V_{BB} jumps below $V_{BB(th)}$		–	1	–	ms
MUTE RECEIVE						
$V_{DLC(th)}$	threshold voltage required on pin DLC/$\overline{\text{MUTER}}$ to obtain mute receive condition		V_{GND} – 0.4	–	0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC/$\overline{\text{MUTER}}$ in mute receive condition	V_{DLC} = 0.2 V	–	100	–	µA
ΔG_{vrxm}	voltage gain reduction in mute receive condition	V_{DLC} < 0.2 V	–	80	–	dB
Envelope and noise detectors (TSEN, TENV, RSEN and RENV)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from MIC to TSEN		37.5	40	42.5	dB
$G_{v(RSEN)}$	voltage gain between RIN1 and RIN2 to RSEN		–2.5	0	+2.5	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\Delta V_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 µA	–	18	–	mV
$\Delta V_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 µA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	µA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	µA
ΔV_{ENV}	voltage difference between pins RENV and TENV	when 10 µA is sourced from both RSEN and TSEN; envelope detectors tracking; note 3	–	±3	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pins TNOI or RNOI		0.75	1	1.25	µA
$I_{sink(NOI)}$	maximum current sunk by pins TNOI or RNOI		–	120	–	µA
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	when 5 µA is sourced from both RSEN and TSEN; noise detectors tracking; note 3	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pins RIN1 and RIN2 (RMS value)		–	127	–	mV
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	$V_{RIN} < V_{RINDT}$; note 4	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 4	–	13	–	mV
SWITCH-OVER						
$I_{sourceSWT}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	µA
$I_{sinkSWT}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	µA
$I_{idleSWT}$	current sourced from pin SWT in idle mode		–	0	–	µA
Voice switch (STAB and SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to 365 kΩ	–40	–	12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to 50 mW output power.
2. Corresponds to 200 mW output power.
3. Corresponds to ±1 dB tracking.
4. Corresponds to 4.3 dB noise/speech recognition level.

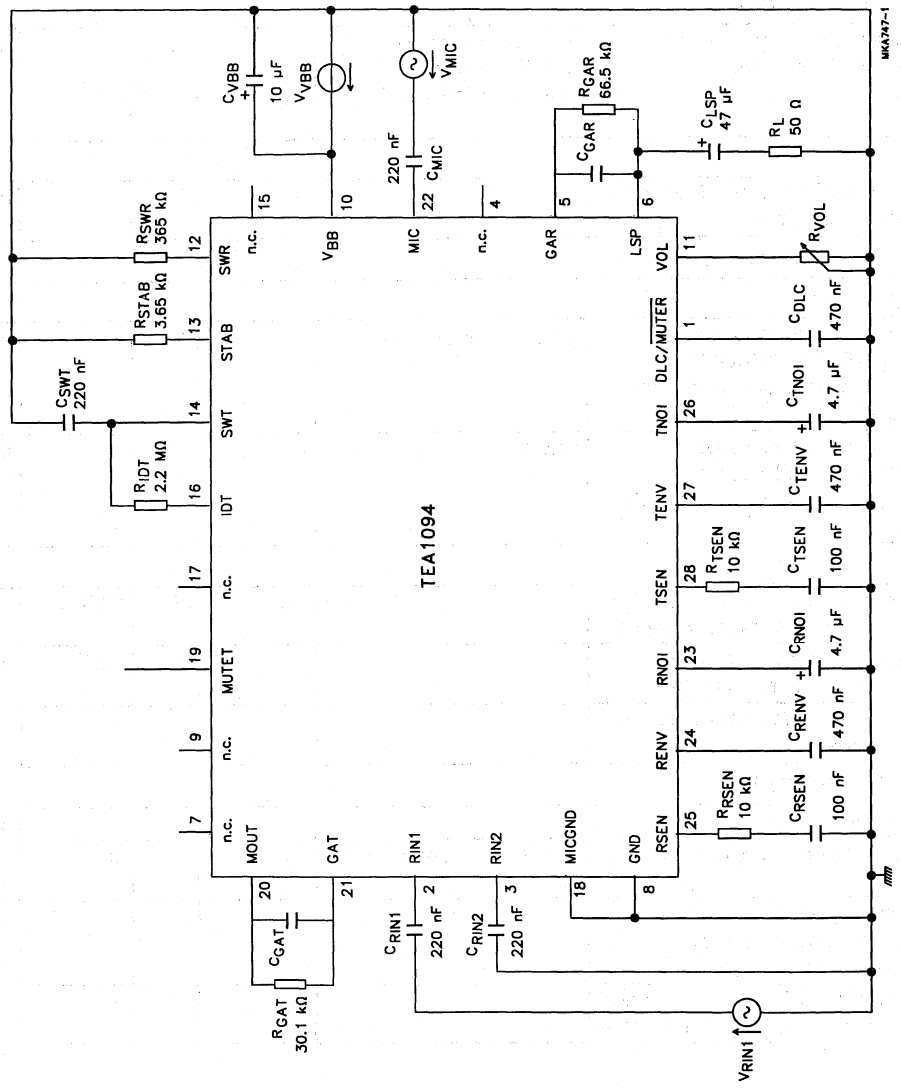


Fig.11 Test circuit.

APPLICATION INFORMATION

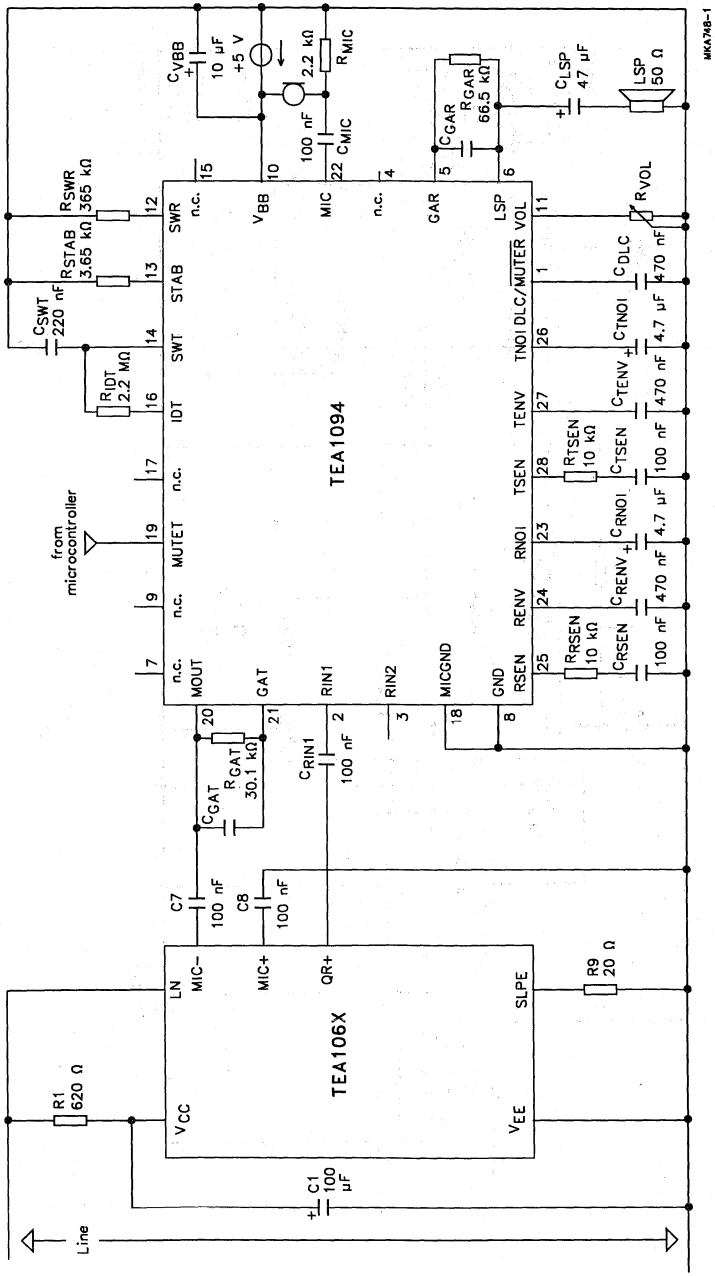


Fig.12 Basic application diagram.

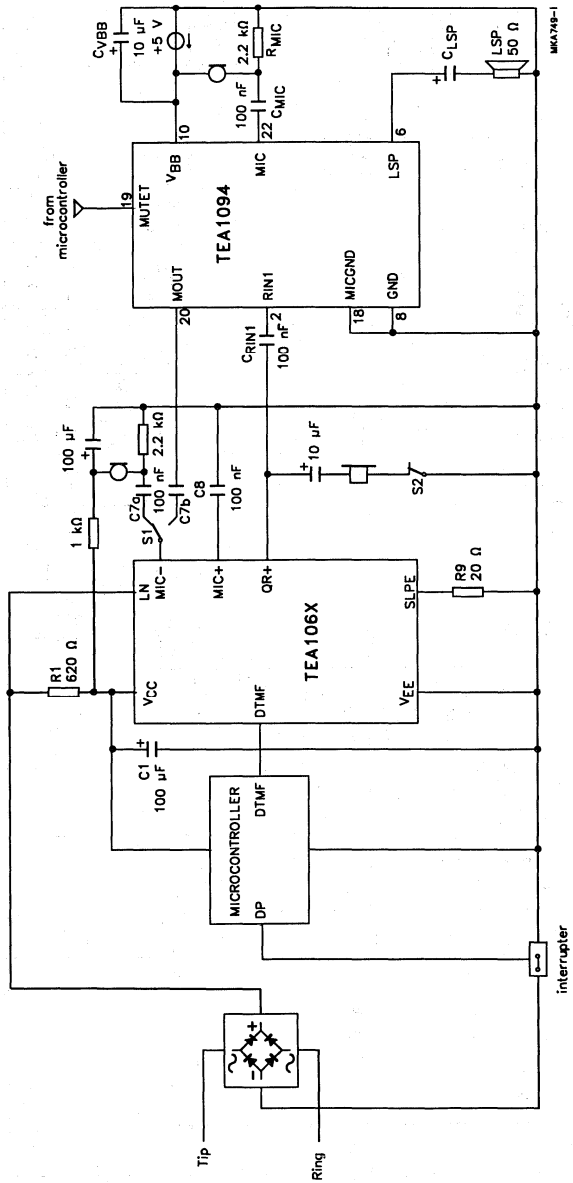


Fig.13 Application example.

Speech and listening-in IC TEA1096; TEA1096A

FEATURES

- Line Interface with:
  - active set impedance (adjustable)
  - voltage regulator with adjustable DC voltage
  - low voltage circuit for parallel operation
- Interface to peripheral circuits with:
  - supply V_{DD} for microcontroller
  - stabilized supply voltage (V_{BB}) which is:
    available for peripheral circuits
    adjustable (TEA1096 only)
  - Dual-Tone MultiFrequency (DTMF) signal input
  - power-down function for pulse dialling/flash
  - mute function to disable speech during dialling
- Microphone amplifier with:
  - symmetrical high impedance inputs
  - externally adjustable gain
  - AGC; line-loss compensation
  - dynamic limiter
  - microphone mute function
- Receiving amplifier with:
  - externally adjustable gain
  - confidence tone during dialling
  - double anti-sidetone circuit for long and short lines
  - AGC; line-loss compensation
  - earpiece protection by soft clipping.
- Listening-in circuit with:
  - loudspeaker amplifier
  - dynamic limiter to prevent distortion at any supply condition
  - volume control via a potentiometer
  - fixed gain of 35.5 dB
  - disable function
  - gain control input (TEA1096A only).

APPLICATIONS

- Line-powered telephone sets with listening-in/line monitoring function.

DIFFERENCES BETWEEN TEA1096 AND TEA1096A

The TEA1096 offers via input VBA an adjustable stabilized supply voltage V_{BB}, whereas the TEA1096A offers a fixed stabilized voltage V_{BB}.

The TEA1096A offers a DC gain control input VCI to set the loudspeaker volume, whereas the TEA1096 offers volume control via a potentiometer.

GENERAL DESCRIPTION

The TEA1096 and TEA1096A are bipolar ICs intended for use in line powered telephone sets. They offer a speech/transmission function, listening-in and line monitoring facilities of the received line signal via the loudspeaker.

The devices incorporate a line interface block, a microphone and DTMF amplifier, a receiving amplifier, a supply function, a loudspeaker amplifier, and a dynamic limiter in the transmission channel and the listening-in channel.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1096	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1096A	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1096T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TEA1096AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current	normal condition	15	–	140	mA
		with reduced performance	–	–	15	mA
I_{DD}	current consumption from pin V_{DD} during normal operation	PD = LOW	–	2.4	2.9	mA
$I_{DD(PD)}$	current consumption from capacitor C_{VDD} during power-down	PD = HIGH	–	100	150	µA
$I_{BB(PD)}$	current consumption from capacitor C_{VBB} during power-down	PD = HIGH	–	350	500	µA
V_{SLPE}	stabilized voltage (line interface)		4.2	4.45	4.7	V
V_{DD}	supply voltage for microcontroller	R_{DD} = 390 Ω; I_P = 0 mA	–	3.5	–	V
		R_{DD} = 390 Ω; I_P = 1 mA	–	3.1	–	V
V_{BB}	stabilized supply voltage		3.4	3.6	3.8	V
G_{vtx}	voltage gain from pin MICP or MICM to LN	V_{MIC} = 2 mV (RMS); R_{GAS} = 90.9 kΩ; I_{line} = 20 mA	51	52	53	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAS}		–19	–	0	dB
G_{vrx}	voltage gain from pin LN to QRP or QRM	V_{line} = 50 mV (RMS); R_{GAR} = 90.9 kΩ; I_{line} = 20 mA	–3.5	–2.5	–1.5	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		–12	–	8	dB
ΔG_{trx}	line-loss compensation	R_{AGC} = 100 kΩ	5	6	7	dB
G_{vlx}	voltage gain from pin LSI to QLS	V_{LSI} = 10 mV (RMS)	34	35.5	37	dB
$V_{LN(p-p)}$	maximum output voltage swing on pin LN (peak-to-peak value)		–	3.65	4.3	V
$V_{QLS(p-p)}$	output voltage between pins QLS and V_{EE} (peak-to-peak value)	V_{LSI} = 18 mV; I_{line} = 20 mA	2.5	2.9	–	mA
T_{amb}	operating ambient temperature		–25	–	+75	°C

BLOCK DIAGRAMS

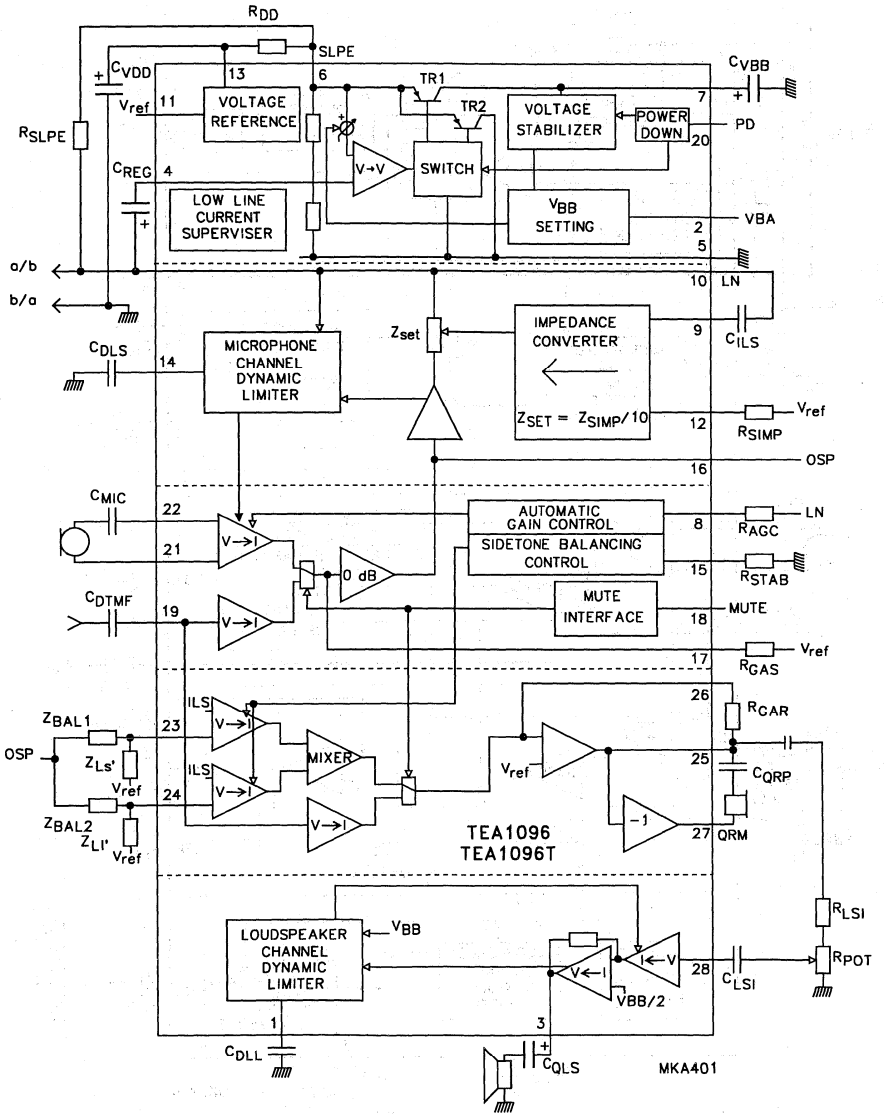


Fig.1 Block diagram (TEA1096).

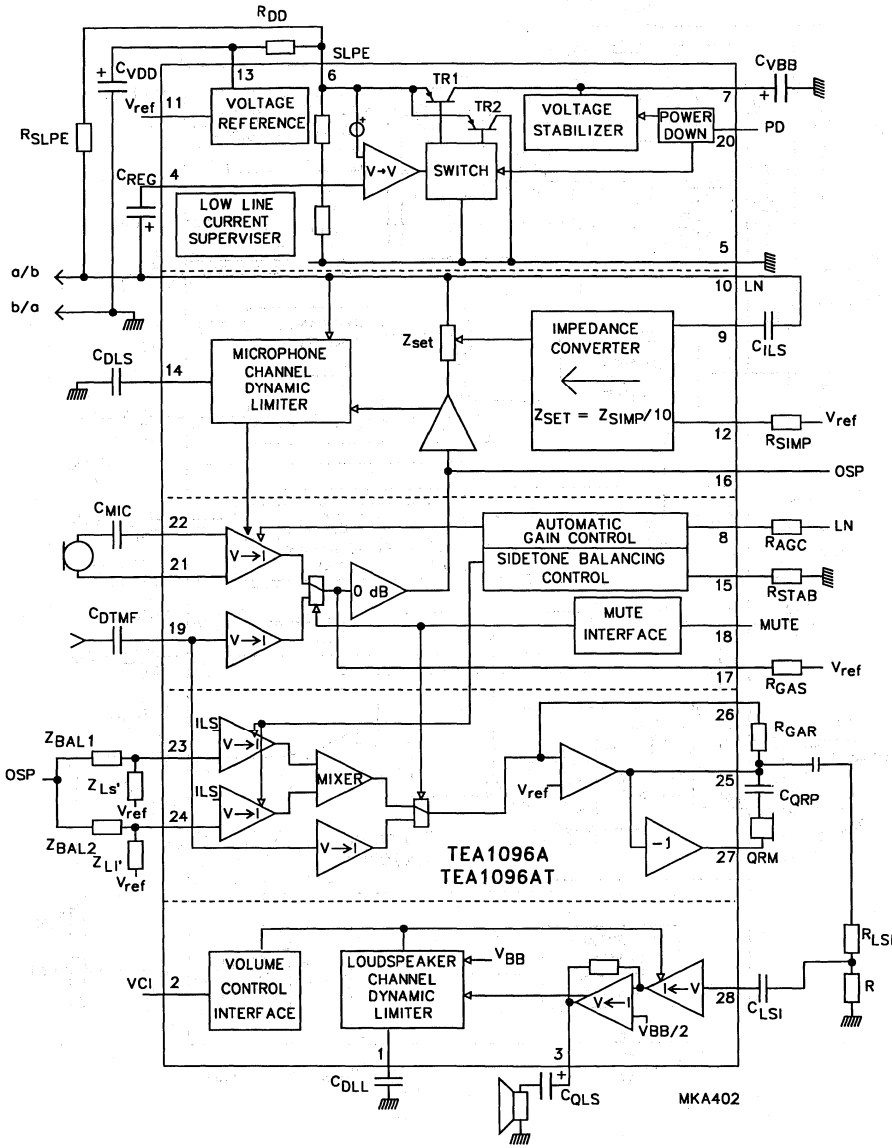


Fig.2 Block diagram (TEA1096A).

PINNING

SYMBOL	PINS		DESCRIPTION
	TEA1096	TEA1096A	
DLL/DIL	1	1	dynamic limiter and disable input for loudspeaker amplifier
VBA	2	–	V_{BB} voltage adjustment
VCI	–	2	volume control input for loudspeaker amplifier
QLS	3	3	loudspeaker amplifier output
REG	4	4	decoupling line voltage stabilizer
V_{EE}	5	5	negative line terminal (ground reference)
SLPE	6	6	stabilized voltage, connection for slope resistor
V_{BB}	7	7	stabilized supply voltage for listening-in circuitry
AGC	8	8	automatic gain control
ILS	9	9	input line signal
LN	10	10	positive line terminal
V_{ref}	11	11	reference voltage output
SIMP	12	12	set impedance input
V_{DD}	13	13	supply voltage for speech circuitry/peripherals
DLS/$\overline{\text{MMUTE}}$	14	14	dynamic limiter for sending and microphone mute
STAB	15	15	reference current adjustment
OSP	16	16	sending preamplifier output
GAS	17	17	sending gain adjustment
MUTE	18	18	mute input to select speech or DTMF dialling
DTMF	19	19	dual-tone multi-frequency (DTMF) input
PD	20	20	power-down input
MICM	21	21	inverting microphone amplifier input
MICP	22	22	non-inverting microphone amplifier input
BAL1	23	23	connection for balance network 1
BAL2	24	24	connection for balance network 2
QRP	25	25	non-inverting receiving amplifier output
GAR	26	26	receiving gain adjustment
QRM	27	27	inverting receiving amplifier output
LSI	28	28	loudspeaker amplifier input

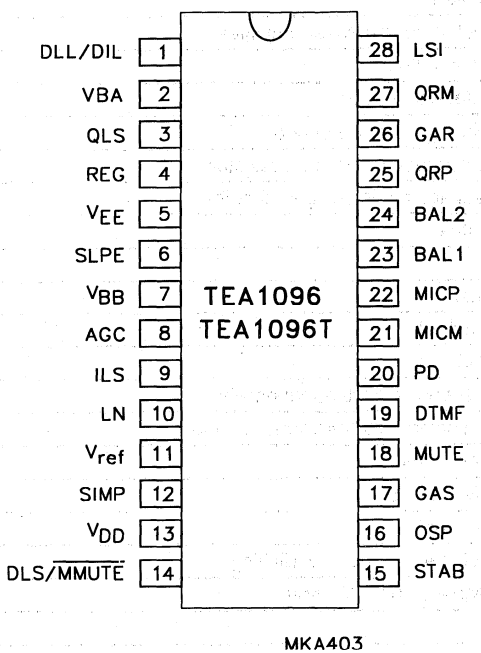


Fig.3 Pin configuration (TEA1096).

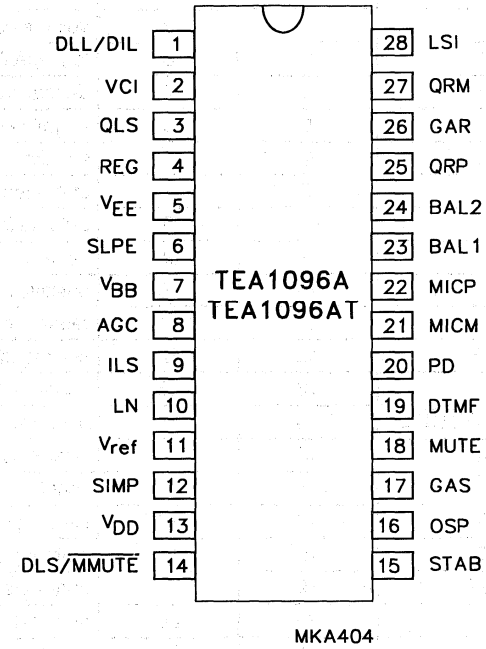


Fig.4 Pin configuration (TEA1096A).

FUNCTIONAL DESCRIPTION

Remark: all data given in this chapter are typical values except when otherwise specified.

Supply pins SLPE, LN, V_{EE}, V_{BB}, V_{DD}, REG and PD

The supply for the TEA1096/TEA1096A and its peripherals is obtained from the telephone line. The circuits regulate the line voltage and generate their own supply voltages V_{DD} and V_{BB} to power the transmission part and the loudspeaker amplifier respectively.

As can be seen from Fig.5, the line current (I_{line}) is split between the sending output stage (I_{ln}), the circuitry connected to SLPE (I_{sl}), the transmission circuit (I_{DD}), the peripheral circuits (I_p) and the current switch (I_{SUP}). It can be shown that:

$$I_{SUP} = I_{line} - (I_{ln} + I_{sl} + I_{DD} + I_P)$$

With nominal conditions where:

I_{ln} = 5 mA, I_{sl} = 0.3 mA and I_{DD} = 2.4 mA

it therefore follows that $I_{SUP} \approx I_{line} - 7.7\ mA - I_P$.

The remaining current I_{SUP} is available for the listening-in part. The current consumption I_{BB0} of the listening-in circuitry is 2.5 mA. To power the loudspeaker, the line current has to be more than 10 mA.

The voltage at SLPE is stabilized at 4.45 V nominal. The DC line voltage is regulated at:
$V_{LN} = V_{SLPE} + R_{SLPE} \times (I_{line} - I_{ln})$.

The supply voltage for the transmission part and peripheral circuits (V_{DD}) is generated from V_{SLPE} and is equal to $V_{DD} = V_{SLPE} - R_{DD} \times (I_{DD} + I_p)$.

V_{BB} supplies the listening-in circuitry and is stabilized at 3.6 V nominal.

A resistor connected between pin REG and V_{EE} can be used to decrease the SLPE voltage while maintaining V_{BB} at its nominal value, whereas a resistor connected between pin REG and pin SLPE will increase the SLPE voltage while maintaining V_{BB} at its nominal value. When adjusting the SLPE voltage to a lower value, care should be taken that the V_{SLPE} is at least 0.4 V higher than V_{BB} (V_{BB} supply efficiency).

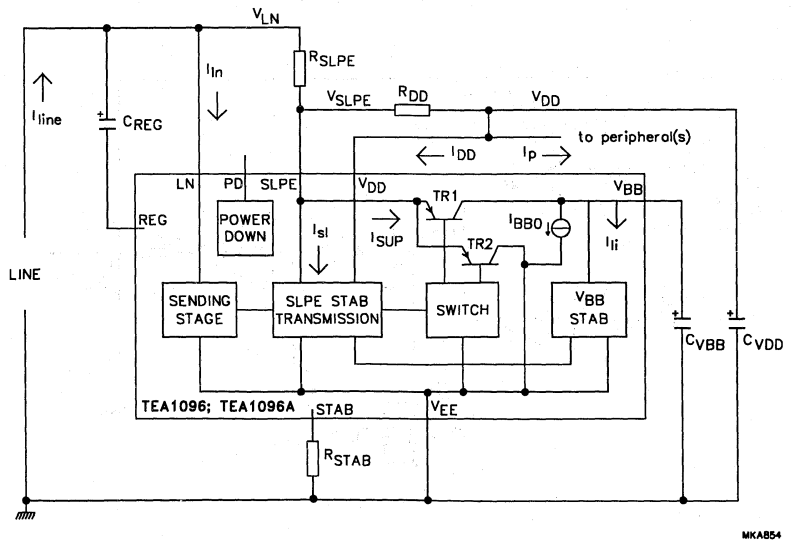


Fig.5 Supply arrangement.

The function of the current switch TR1-TR2 is to reduce distortion of large line signals. Current I_{SUP} is supplied to V_{BB} via TR1, when V_{SLPE} is higher than V_{BB} + 0.4 V. When V_{SLPE} is lower, this current is shunted to V_{EE} via TR2. All excess line current, not used for internal supply is consumed in the V_{BB} stabilizer or directly shunted to V_{EE}.

To reduce the current consumption during pulse dialling, the TEA1096/TEA1096A are provided with a power-down (PD) input. The PD input has a pull-down structure. When the voltage on PD is HIGH, the current consumption from V_{DD} capacitor C_{VDD} is 100 μA and from the V_{BB} supply point 350 μA. The capacitors C_{VDD} (100 μF) and C_{VBB} (470 μF) are sufficient to power theTEA1096/TEA1096A during pulse dialling/flash.

V_{BB} voltage adjustment: pin VBA (TEA1096 only)

A resistor connected between pins VBA and V_{EE} can be used to increase the V_{BB} voltage, whereas a resistor connected between pins VBA and V_{BB} will decrease the V_{BB} voltage. When adjusting the V_{BB} voltage to a higher value, care should be taken that V_{SLPE} is at least 0.4 V higher than V_{BB} (V_{BB} supply efficiency).

Sending channel: pins MICP, MICM, DTMF, GAS, OSP, LN, MUTE, DLS and AGC

The TEA1096/TEA1096A has symmetrical microphone inputs MICP, MICM with an input resistance of 64 kΩ between MICP and MICM (2 × 32 kΩ). In the speech mode (MUTE = LOW), the overall gain from MICP-MICM to LN can be adjusted from 33 dB to 52 dB to suit specific requirements. The gain is proportional to the value of R_{GAS} and equals 52 dB with R_{GAS} = 90.9 kΩ and I_{line} = 20 mA. A capacitor C_{GAS} connected in parallel with R_{GAS} can be used to provide a first-order low-pass filter.

Automatic gain control (AGC) is provided for line-loss compensation as well as dynamic limitation for reduction of the distortion of the transmitted signal on the line. The microphone amplifier can be disabled by short-circuiting pin DLS to V_{EE} (secret function) and can be muted into DTMF mode by applying a HIGH level on pin MUTE.

The TEA1096/TEA1096A has an asymmetrical DTMF input with an input resistance of 20 kΩ. In the DTMF mode, the overall gain from DTMF to LN is proportional to R_{GAS}, and is 26.5 dB less than the microphone amplifier gain. Switch-over from one mode to the other is click-free.

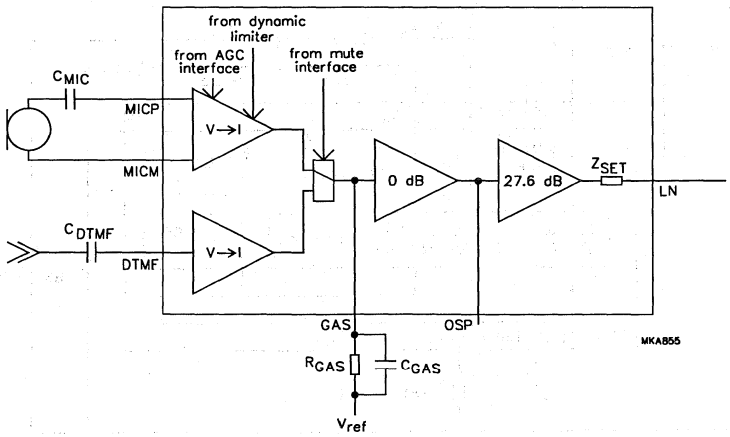


Fig.6 Sending channel.

It can be calculated from Fig.7 that the AC modulator gain can be written:

- $\frac{V_{LN}}{V_{OSP}} = \frac{Z_{line}}{(Z_{line} + Z_{SET}) \times 24} = 12$ providing $Z_{SET} = Z_{line}$
- G_v (LN to OSP) = 21.6 dB.

The frequency response for audio frequencies of the sending channel is flat in this case for a complex line termination.

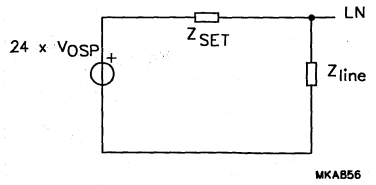


Fig.7 AC modulator equivalent model.

Set impedance: pins ILS, SIMP and LN

The TEA1096/TEA1096A provides an active set impedance in both the receiving and sending conditions, thus allowing a flat frequency response for a complex line impedance, without the need for any extra compensation network.

As can be derived from Fig.8 the set impedance Z_{SET} is 10 times lower than Z_{SIMP}.

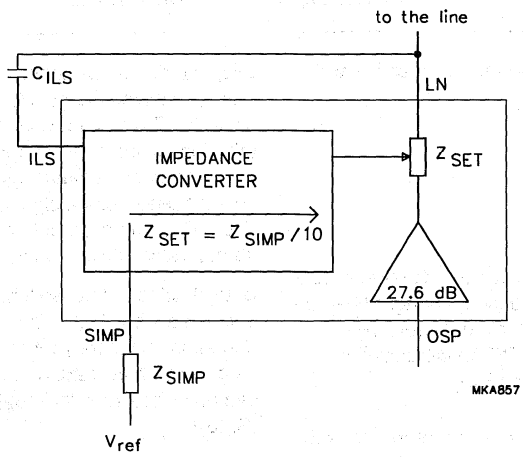


Fig.8 Set impedance.

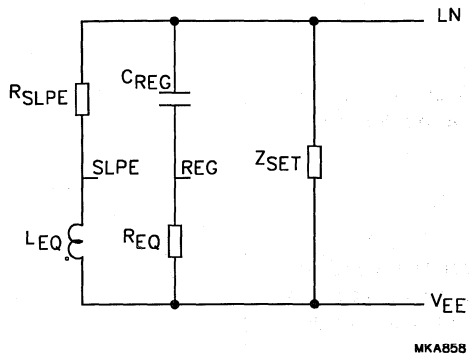


Fig.9 Equivalent AC impedance between LN and V_{EE}.

The equivalent impedance connected between LN and V_{EE} is illustrated in Fig.9.

Where:

- $L_{EQ} = R_{EQ} \times C_{REG} \times R_{SLPE}$
- $R_{EQ} = 40\ k\Omega$
- $Z_{SET} = {}^{1}/_{10} Z_{SIMP}$.

Remark: a resistor R (REG-V_{EE}) connected between REG and V_{EE} (to lower the regulated voltage) changes R_{EQ} into R_{EQ} // R (REG-V_{EE}), whereas a resistor $R_{REG\text{-}SLPE}$ connected between REG and SLPE (to increase the regulated voltage) has no effect on R_{EQ}.

Dynamic limiter of the microphone channel: pin DLS

The dynamic limiter in the microphone channel of the TEA1096/TEA1096A prevents clipping of the microphone signal, and limits the transmitted signal on LN to a maximum value of typically 3.65 V (4.4 dBm).

Clipping on the microphone channel is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which the gain reduction is effected (clipping attack time) is approximately a few milliseconds. The microphone channel stays in the reduced gain mode until the peaks of the signal no longer cause saturation. The gain of the microphone channel then returns to its normal value within the clipping release time.

Both attack and release time are proportional to the value of the capacitor C_{DLS}. The THD (Total Harmonic Distortion) of the microphone amplifier in the reduced gain mode stays below 2% up to 10 dB of input voltage overdrive [provided that V_{MICP}, V_{MICM} is below 10 mV (RMS)].

The dynamic limiter of the TEA1096/TEA1096A also provides a microphone mute (secret function) when pin DLS is short-circuited to V_{EE}. The microphone gain is then 80 dB lower. The release time after a microphone mute is approximately 10 ms.

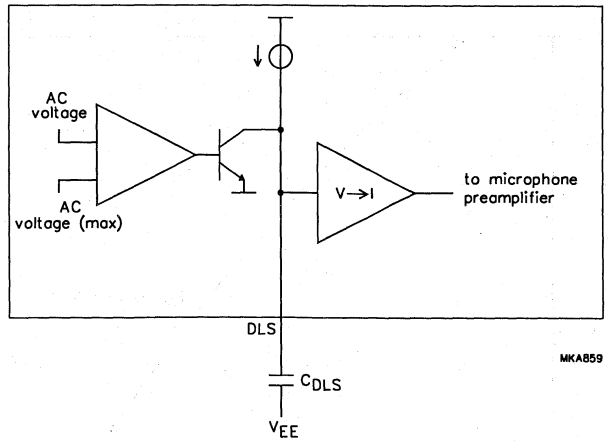


Fig.10 Dynamic limiter of the microphone channel.

Receiving amplifier: pins LN, GAR, QRP and QRM

The receiver gain is defined between the line connection LN and the earpiece complementary outputs QRP (non-inverting) and QRM (inverting). With R_{GAR} equal to 90.9 kΩ the gain from LN to QRP is –2.5 dB. The outputs may be used to connect a dynamic, magnetic or piezoelectric earpiece. When the earpiece impedance exceeds 450 Ω, differential drive (BTL connection) can be used. As both outputs are in opposite phase, the gain from LN to QRP or QRM is 3.5 dB.

By means of the R_{GAR} resistor, the gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer which is used. The permitted range is between –14 dB and +6 dB for single-ended drive (SE), and between –8 dB and +12 dB for bridge-tied load (BTL) drive.

Two external capacitors, C_{GAR} (100 pF) and C_{GARS} (1 nF), ensure stability. The C_{GAR} capacitor is also used to obtain a first-order low-pass filter. The cut-off frequency (corresponding to the time constant $R_{GAR} \times C_{GAR}$) can be adjusted by the C_{GAR} capacitor, but the relationship $C_{GARS} = C_{GAR} \times 10$ must be maintained.

During DTMF dialling, the dialling tones can be heard in the earpiece at a very low level. This is called confidence tone.

Automatic gain control: pin AGC

Automatic compensation of line-loss is obtained by connecting a resistor R_{AGC} between pin LN and pin AGC. This automatic gain control changes the gain of the microphone and receiving amplifiers in accordance with the DC line current.

The control range is 6 dB; This corresponds to a 5 km line of 0.5 mm diameter copper twisted-pair cable:

DC resistance = 176 Ω /km

average attenuation = 1.2 dB/km.

The value of R_{AGC} must be chosen with reference to the exchange supply voltage and its feeding bridge resistance and has no influence on the ratio (I_{start}/I_{stop}) which remains constant. Figure11 illustrates the gain attenuation when R_{AGC} = 100 kΩ. If automatic line-loss compensation is not required, the AGC pin can be left open circuit, the amplifiers then give their maximum gain and the double sidetone principle is no longer active. Only one network is used. Pins BAL1 and BAL2 must then be short-circuited together.

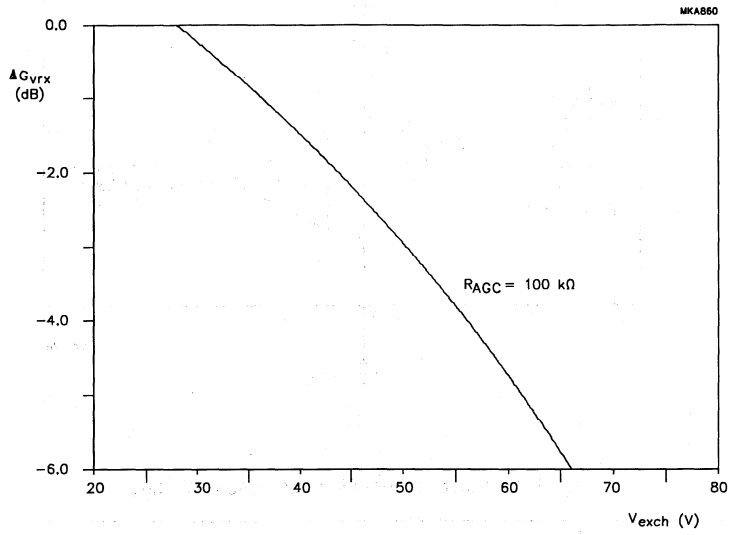


Fig.11 Variation of microphone and receiver gain as a function of the exchange supply voltage with R_{AGC} as a parameter.

Sidetone suppression: pins BAL1, BAL2, OSP and ILS

Suppression of the microphone signal in the earpiece is obtained by subtracting a part of this signal to a fraction of the line signal (see Fig.12). For optimum suppression, the voltage at the BAL inputs (BAL1 and BAL2) should be equal to:

$$V_{BAL} = 0.5 \times \frac{Z_{line}}{Z_{SET} \times Z_{line}} \times V_{SOP}$$

To reach this requirement, an anti-sidetone network using two impedances Z_{BAL} and $Z_{LI'}$ is needed.

In the event of real impedances, the anti-sidetone network is composed of resistors connected as shown in Fig.13.

Where: $R_{LI'} = \alpha \times R_{line}$ and $R_{BAL} = \alpha \times R_{SET}$;

where α is a scale factor allowing to have $R_{LI'}$ in the order of 10 kΩ (DC biasing to V_{ref} has to be ensured on BAL1 and BAL2).

In the event of complex impedances, the equivalent network Z_s, representing Z_{line}, has to be transformed into Z_p in accordance with Fig.14.

The components of Z_p, scaled by a factor α, are applied in anti-sidetone network $Z_{LI'}$. The complete anti-sidetone network is shown in Fig.15.

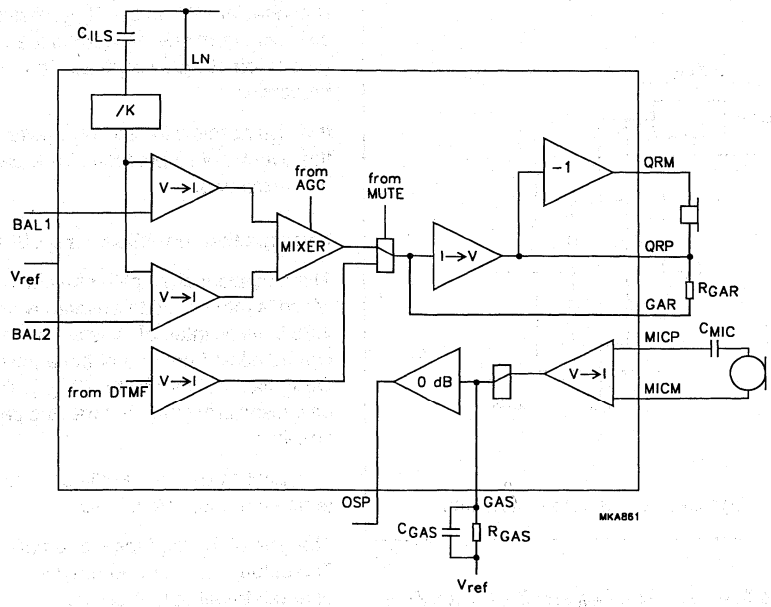


Fig.12 Balance networks connection.

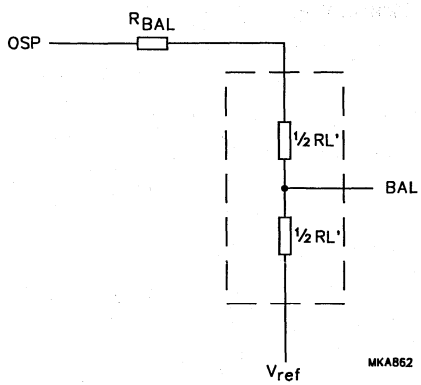
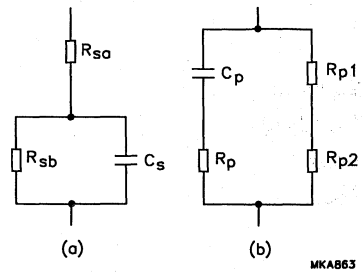


Fig.13 Anti-sidetone network.



(a) Series impedance (Z_s).
(b) Parallel impedance (Z_p).

Fig.14 Equivalent network.

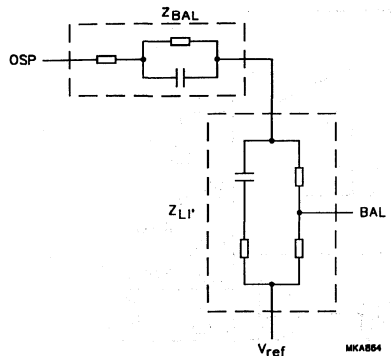


Fig.15 Complete anti-sidetone network.

Again, it means that: $Z_{LI'} = \alpha \times Z_{line}$ and $Z_{BAL} = \alpha \times Z_{SET}$

Where α is a scale factor allowing $Z_{LI'}$ to be in the order of 10 kΩ (DC biasing to V_{ref} has to be ensured on BAL1 and BAL2).

As the line impedance Z_{line} varies considerably with the line length, two anti-sidetone networks can be used. One of them $Z_{LI'}$, connected to BAL2 is optimized for long lines, the other one $Z_{LS'}$, connected to BAL1 is optimized for short lines:

Where:

$Z_{LI'} = \alpha \times Z_{line}$ (long)

$Z_{LS'} = \alpha \times Z_{line}$ (short)

$Z_{BAL1} = \alpha \times Z_{SET}$

$Z_{BAL2} = \alpha \times Z_{SET}$.

Switching from one network to the other is carried out continuously with the line current, when the R_{AGC} resistor is connected. When the R_{AGC} resistor is not connected, switching from one network to the other is not possible (see automatic gain control). Only one network has then to be applied.

It is also possible to use only one anti-sidetone network. In this event, both inputs BAL1 and BAL2 must be short-circuited.

Loudspeaker amplifier: pins LSI and QLS

The loudspeaker amplifier has an asymmetrical input LSI which is referenced to an internal voltage reference of 1.25 V via an internal resistance of 10 kΩ. The input signal can be taken from one of the earpiece outputs QRP or QRM via a potentiometer (R_{POT}). The attenuation has to be chosen in accordance with the gain G_{vrx} of the receiving amplifier.

The input stage can handle up to 200 mV (RMS) at room temperature for 3% of THD.

The gain of the loudspeaker amplifier is fixed at 35.5 dB. The output QLS is referenced to a DC level of $\frac{1}{2}V_{BB}$ to offer rail-to-rail output swing.

The maximum voltage gain from line to loudspeaker has to be fixed in relation to the side-tone transfer of the telephone set. An enlarged listening-in gain improves the listening-in behaviour but can introduce audible instabilities in the form of howling during normal use of the set. The loudspeaker can be disabled by short-circuiting DLL/DIL input to V_{EE}.

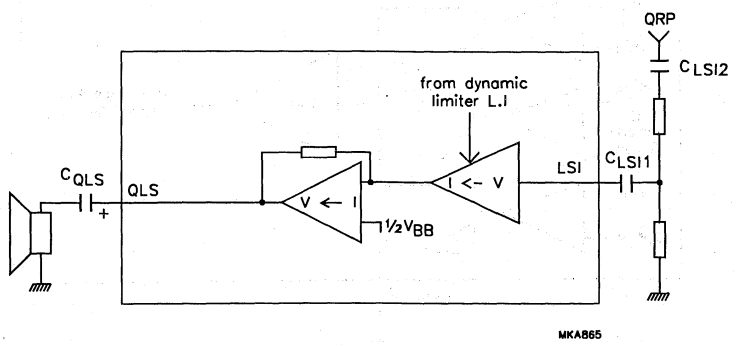


Fig.16 Loudspeaker amplifier channel.

Dynamic limiter/loudspeaker amplifier disabling; pin DLL/DIL

The dynamic limiter in the loudspeaker channel of the TEA1096/TEA1096A prevents clipping of the loudspeaker output stage and protects the functioning of the circuit when low supply conditions are detected.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which the gain reduction is effected (clipping attack time) is approximately a few milliseconds. The loudspeaker amplifier stays in the reduced gain mode until the peaks of the loudspeaker signals no longer start to cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time. Both attack and release time are proportional to the value of the capacitor C_{DLL}. The THD of the loudspeaker amplifier in the reduced gain mode stays below 5% up to 10 dB of input voltage overdrive.

When the supply conditions drop below the required level, the gain of the loudspeaker amplifier is reduced in order to prevent the device from malfunctioning. When the supply current drops below the required level, the supply voltage V_{BB} decreases. In this condition, the gain of the loudspeaker amplifier is reduced slowly (approximately a few seconds). When the supply voltage continues to decrease and drops below an internal threshold of 2.8 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). After returning to normal supply conditions, the gain of the loudspeaker amplifier is raised again.

The dynamic limiter also provides a loudspeaker disable when pin DLL/DIL is short-circuited to V_{EE}. The loudspeaker gain is then typically 80 dB lower. The release time is approximately 10 ms.

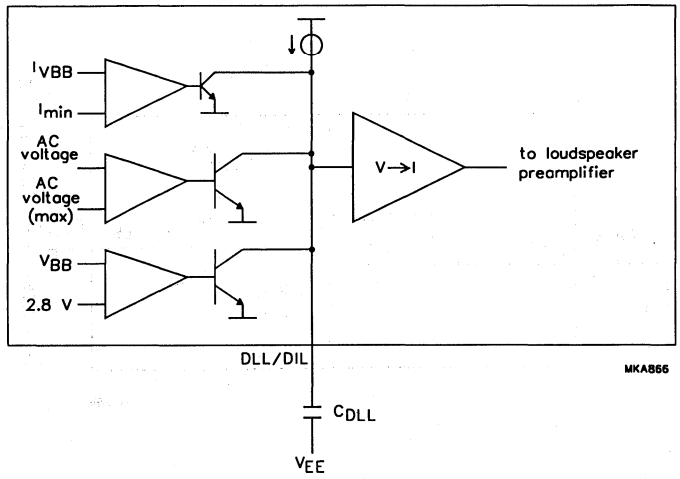


Fig.17 Dynamic limiter of the listening-in part.

Volume control: pin VCI (TEA1096A only)

The TEA1096A is provided with a volume control input VCI, to adjust the gain of the loudspeaker channel by means of a controlled DC voltage. A typical application is illustrated in Fig.18. A pulse width modulation on a microcontroller open drain output imposes a DC voltage on the VCI capacitor:

Where $V_{VCI} = \frac{\delta \times K \times V_{BB}}{1 - \delta \times (1 - K)}$

with δ = duty cycle and $K = \frac{R1}{R1 + R2}$

A typical response is given in Fig.19.

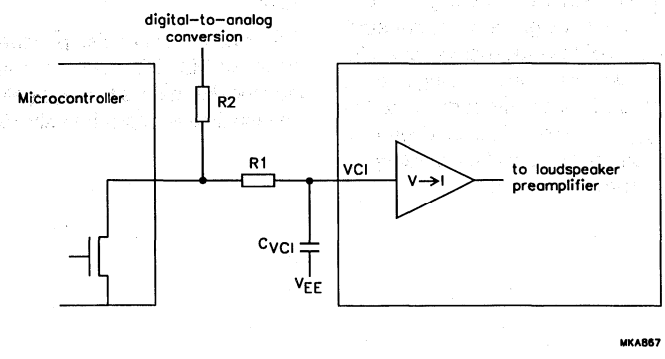


Fig.18 Digital volume control application.

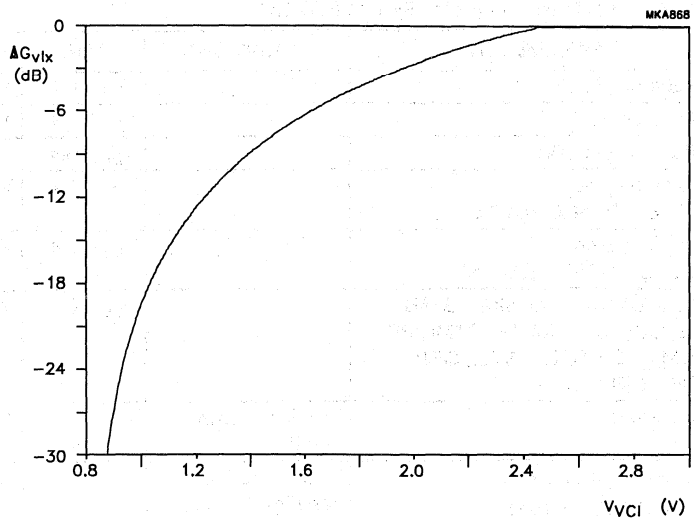


Fig.19 Change of loudspeaker gain as a function of the voltage at VCI.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

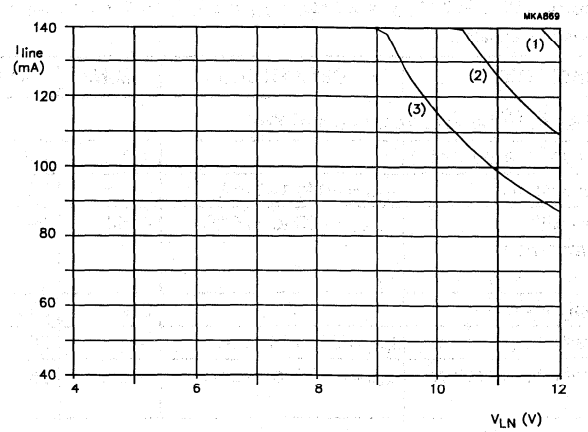
SYMBOLS	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	voltage on pin LN		V_{EE} – 0.4	12.0	V
V_{DD}	voltage on pin VDD		V_{EE} – 0.4	12.0	V
V_{BB}	voltage on pin VBB		V_{EE} – 0.4	12.0	V
V_{n1}	voltage on pins: REG, SLPE, AGC and ILS		V_{EE} – 0.4	V_{LN} + 0.4	V
V_{n2}	voltage on pins: DLL, VBA or VCI, QLS, LSI		V_{EE} – 0.4	V_{BB} + 0.4	V
V_{n3}	voltage on pins: V_{ref}, SIMP, STAB, DLS, OSP, GAS, MUTE, DTMF, PD, MICM, MICP, BAL1, BAL2, QRP, QRM, GAR		V_{EE} – 0.4	V_{DD} + 0.4	V
I_{line}	line current	see also Figs 20 and 21	–	140	mA
P_{tot}	total power dissipation:	T_{amb} = +75 °C; see Figs 20 and 21			
	TEA1096/TEA1096A		–	0.91	W
	TEA1096T/TEA1096AT		–	0.66	W
T_{stg}	storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOLS	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air:		
	TEA1096; TEA1096A	55	K/W
	TEA1096T; TEA1096AT (note 1)	75	K/W

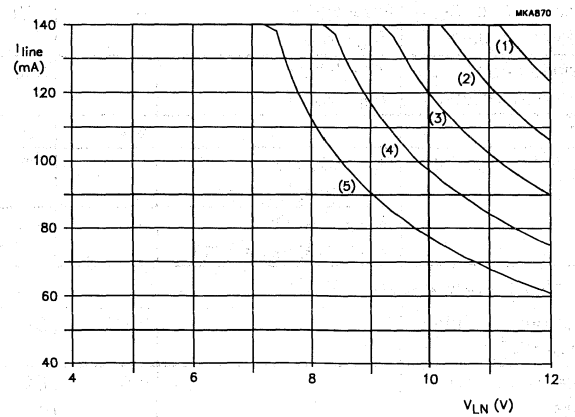
Note

1. Mounted on epoxy board 40.1 × 19.1 × 1.5 mm.



(1) T_{amb} = 55 °C; P_{tot} = 1272 mW.
(2) T_{amb} = 65 °C; P_{tot} = 1091 mW.
(3) T_{amb} = 75 °C; P_{tot} = 910 mW.

Fig.20 TEA1096; TEA1096A safe operating area.



(1) T_{amb} = 35 °C; P_{tot} = 1199 mW.
(2) T_{amb} = 45 °C; P_{tot} = 1066 mW.
(3) T_{amb} = 55 °C; P_{tot} = 933 mW.
(4) T_{amb} = 65 °C; P_{tot} = 800 mW.
(5) T_{amb} = 75 °C; P_{tot} = 667 mW.

Fig.21 TEA1096T; TEA1096AT safe operating area.

CHARACTERISTICS

I_{line} = 20 mA; I_P = 0 mA; V_{EE} = 0 V; PD = LOW; MUTE = LOW; Z_{line} = 600 Ω; Z_{SIMP} = 6 kΩ; Z_{BAL1} = 18 kΩ; $Z_{LI'}$ = 6 kΩ; R_{SLPE} = 20 Ω; R_{DD} = 390 Ω; R_{GAS} = 90.9 kΩ; R_{GAR} = 0.9 kΩ; R_{QLS} = 50 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig.22; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Line interface/supply (LN, SLPE, REG, V_{EE}, V_{DD}, V_{BB} and V_{ref})						
V_{SLPE}	stabilized voltage (line interface)		4.2	4.45	4.7	V
$\Delta V_{SLPE(Iline)}$	V_{SLPE} variation with I_{line}	I_{line} = 20 to 140 mA	–	30	–	mV
$\Delta V_{SLPE(T)}$	V_{SLPE} variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	−150	±60	+150	mV
V_{BB}	stabilized supply voltage		3.4	3.6	3.8	V
$\Delta V_{BB(Iline)}$	V_{BB} variation with I_{line}	I_{line} = 20 to 140 mA	–	30	–	mV
$\Delta V_{BB(T)}$	V_{BB} variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	−150	±50	+150	mV
I_{sink}	current sunk by V_{BB} shunt regulator when a line current equal to 20 mA is available	I_P = 0 mA; note 1	–	9.0	–	mA
I_{DD}	internal current consumption from pin V_{DD}	I_P = 0 mA; R_{DD} = 390 Ω	–	2.4	2.9	mA
V_{DD}	supply voltage for speech and microcontroller	R_{DD} = 390 Ω; I_P = 0 mA	–	3.5	–	V
		R_{DD} = 390 Ω; I_P = 1 mA	–	3.1	–	V
V_{ref}	reference output voltage		–	$0.5V_{DD}$	–	V
$I_{DD(PD)}$	current consumption from C_{VDD} during power-down condition	PD = HIGH; V_{DD} = 4.3 V	–	100	150	µA
$I_{BB(PD)}$	current consumption from C_{VBB} during power-down condition	PD = HIGH; V_{BB} = 3.5 V	–	350	500	µA
V_{LN}	DC line voltage		4.4	4.7	5.0	V
V_{LN}	DC line voltage in low current conditions	R_{DD} = 390 Ω; I_P = 0 mA; I_{line} = 4 mA	–	2.5	–	V
		R_{DD} = 390 Ω; I_P = 0 mA; I_{line} = 6 mA	–	3.3	–	V
Microphone amplifier (MICP, MICM, GAS, LN, and MUTE)						
$\lvert Z_{i1} \rvert$	input impedance between pins MICP or MICM and V_{EE}		25.5	32	38.5	kΩ
$\lvert Z_{i2} \rvert$	input impedance between pins MICP and MICM		51	64	77	kΩ
G_{vtx}	voltage gain from pin MICP or MICM to LN	V_{MIC} = 2 mV (RMS); R_{GAS} = 90.9 kΩ	51	52	53	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C.	V_{MIC} = 2 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.5	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{MIC} = 2 mV (RMS); f = 300 to 3400 Hz	–	±0.5	–	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAS}	note 2	–19	–	0	dB
ΔG_{txm}	gain reduction with MUTE = HIGH		60	80	–	dB
ΔG_{txd}	gain reduction when DLS/$\overline{\text{MMUTE}}$ is short-circuited to V_{EE}		60	80	–	dB
$V_{LN(p-p)}$	maximum output voltage swing at pin LN (peak-to-peak value)	R_{GAS} = 90.9 kΩ	–	3.65	4.3	V
V_{notx}	noise output voltage at pin LN	pins MICP and MICM short-circuited through 200 Ω; Psophometrically weighted (P53 curve)	–	–72	–	dBmp
CMRR	common mode rejection ratio		–	80	–	dB
Dynamic limiter for sending (DLS/$\overline{\text{MMUTE}}$); related to the microphone amplifier clipping detector						
t_{att}	attack time when V_{MIC} jumps from 3.2 mV to 3.2 mV + 10 dB	R_{GAS} = 90.9 kΩ; C_{DLS} = 470 nF	–	1.5	5	ms
t_{rel}	release time when V_{MIC} drops from 3.2 mV + 10 dB to 3.2 mV	R_{GAS} = 90.9 kΩ; C_{DLS} = 470 nF	40	120	–	ms
THD	total harmonic distortion	V_{MIC} = 3.2 mV + 10 dB; R_{GAS} = 90.9 kΩ; C_{DLS} = 470 nF	–	2	3	%
		V_{MIC} = 3.2 mV + 15 dB; R_{GAS} = 90.9 kΩ; C_{DLS} = 470 nF	–	3	10	%
Receiving amplifier (ILS, BAL1, BAL2, OSP, GAR, QRP, QRM and MUTE)						
G_{vrx}	voltage gain from pin LN to QRP or QRM	R_{GAR} = 90.9 kΩ; V_{line} = 50 mV (RMS); single-ended load; R_{QRP} = 150 Ω	–3.5	–2.5	–1.5	dB
		R_{GAR} = 90.9 kΩ; V_{line} = 50 mV (RMS); bridge tied load; R_{QRM} = 450 Ω	2.5	3.5	4.5	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C.	T_{amb} = –25 to +75 °C	–	±0.5	–	dB
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.5	–	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		–12	–	8	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{QR(rms)}$	maximum output voltage for THD = 2% (RMS value)	R_{GAR} = 90.9 kΩ; single-ended load; R_{QRP} = 150 Ω	0.3	0.375	–	V
		R_{GAR} = 90.9 kΩ; bridge-tied load; R_{QRM} = 450 Ω	0.6	0.72	–	V
		R_{GAR} = 90.9 kΩ; bridge-tied load with 300 Ω series resistor; C_{QRM} = 60 nF; f = 3400 Hz	0.75	0.95	–	V
$V_{norx(rms)}$	noise output voltage (RMS value)	Psophometrically weighted (P53 curve); single-ended load; R_{QRP} = 150 Ω	–	90	–	μV
		Psophometrically weighted (P53 curve); bridge-tied load; R_{QRM} = 450 Ω	–	180	–	μV
DTMF amplifier (DTMF, LN, MUTE)						
$\|Z_i\|$	input impedance between pins DTMF and V_{EE}		16	20	24	kΩ
G_{vtx}	voltage gain from pin DTMF to LN	V_{DTMF} = 4 mV (RMS); R_{GAS} = 90.9 kΩ	24.5	25.5	26.5	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{DTMF} = 4 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.5	–	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{DTMF} = 4 mV (RMS); f = 300 to 3400 Hz	–	±0.5	–	dB
G_{vtx}	voltage gain from pin DTMF to QRP	MUTE = HIGH; V_{line} = 80 mV (RMS); R_{GAR} = 90.9 kΩ; R_{QRP} = 150 Ω	–	−19	–	dB
Automatic gain control (AGC); controlling the gain from LN to QRP, QRM and the gain from MICP, MICM to LN						
ΔG_{trx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 20 mA	I_{line} = 85 mA; R_{AGC} = 100 kΩ	5	6	7	dB
$I_{line(h)}$	highest line current for maximum gain	R_{AGC} = 100 kΩ	–	28	–	mA
$I_{line(l)}$	lowest line current for minimum gain	R_{AGC} = 100 kΩ	–	66	–	mA
ΔG_{trx}	change of gain when varying I_{line} from 20 mA to 40 mA	R_{AGC} = 100 kΩ	1	1.5	2	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Loudspeaker amplifier (LSI and QLS)						
$\|Z_i\|$	input impedance between pins LSI and V_{EE}		8	10	12	kΩ
G_{vlx}	voltage gain from pin LSI to QLS	V_{LSI} = 10 mV (RMS)	34	35.5	37	dB
ΔG_{vlxT}	voltage gain variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	±0.5	–	dB
ΔG_{vlxf}	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.5	–	dB
$V_{QLS(p-p)}$	output voltage between pins QLS and V_{EE} (peak-to-peak value)	V_{LSI} = 18 mV; I_{line} = 16 mA	1.2	1.45	–	V
		V_{LSI} = 18 mV; I_{line} = 20 mA	2.5	2.9	–	V
$V_{nolx(rms)}$	noise output voltage at pin LN (RMS value)	pin LSI open-circuit; Psophometrically weighted (P53 curve)	–	200	–	μV
Dynamic limiter for the loudspeaker amplifier (DLL/DIL); related to the loudspeaker amplifier clipping detector						
THD	total harmonic distortion	V_{LSI} = 18 mV + 0 dB; I_{line} = 30 mA	–	2	5	%
t_{att}	attack time when V_{LSI} jumps from 18 mV to 18 mV + 0 dB	I_{line} = 30 mA; C_{DLL} = 470 nF	–	1.5	5	ms
t_{rel}	release time when V_{LSI} drops from 18 mV + 0 dB to 18 mV	I_{line} = 30 mA; C_{DLL} = 470 nF	30	60	–	ms
Dynamic limiter for the loudspeaker amplifier (DLL/DIL); related to the V_{BB} threshold detector						
$V_{BB(th)}$	V_{BB} limiter threshold detector level		–	2.8	–	V
t_{att}	attack time when V_{BB} jumps below $V_{BB(th)}$	C_{DLL} = 470 nF	–	1	–	ms
Volume control for the loudspeaker amplifier (VCI) (TEA1096A only); related to the loudspeaker amplifier volume control						
$\|Z_i\|$	input impedance		–	1	–	MΩ
V_{VCImin}	minimum DC level on pin VCI for 0 dB control on loudspeaker amplifier	I_{line} = 30 mA; V_{LSI} = 10 mV (RMS)	–	2.8	–	V
V_{VCI}	DC level on pin VCI for −6 dB control on loudspeaker amplifier	I_{line} = 30 mA; v_{LSI} = 10 mV (RMS)	–	1.63	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-down input (PD)						
V_{IL}	LOW level input voltage		–	–	0.5	V
V_{IH}	HIGH level input voltage		1.5	–	V_{DD} +0.4	V
I_{PD}	input current in power-down condition	PD = HIGH	–	6	10	μA
Mute input (MUTE)						
V_{IL}	LOW level input voltage		–	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{DD} +0.4	V
I_{MUTE}	input current	MUTE = HIGH	–	15	20	μA
Microphone mute input (DLS/$\overline{\text{MMUTE}}$)						
V_{IL}	LOW level input voltage		–	–	0.3	V
$I_{sink(DLS)}$	sink current	DLS/$\overline{\text{MMUTE}}$ = LOW	–	60	100	μA
t_{rel}	release time after a LOW level on pin DLS/$\overline{\text{MMUTE}}$	C_{DLS} = 470 nF	–	15	–	ms
ΔG_{txm}	gain reduction when DLS/$\overline{\text{MMUTE}}$ is short-circuited to V_{EE}	DLS/$\overline{\text{MMUTE}}$ = LOW	60	80	–	dB
Disable input for loudspeaker amplifier (DLL/DIL)						
V_{IL}	LOW level input voltage		–	–	0.25	V
$I_{sink(DLL/DIL)}$	sink current	DLL/DIL = LOW	–	75	120	μA
t_{rel}	release time after a LOW level on pin DLL/DIL	I_{line} = 30 mA; C_{DDL} = 470 nF	–	10	–	ms
ΔG_{lm}	gain reduction when DLL is short-circuited to V_{EE}	DLL/DIL = LOW	60	80	–	dB

Notes

1. This gives the current available for receiving, listening-in and peripherals at this line current.
2. Both gains, microphone and sending DTMF, are determined in the same way by the resistor R_{GAS}.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

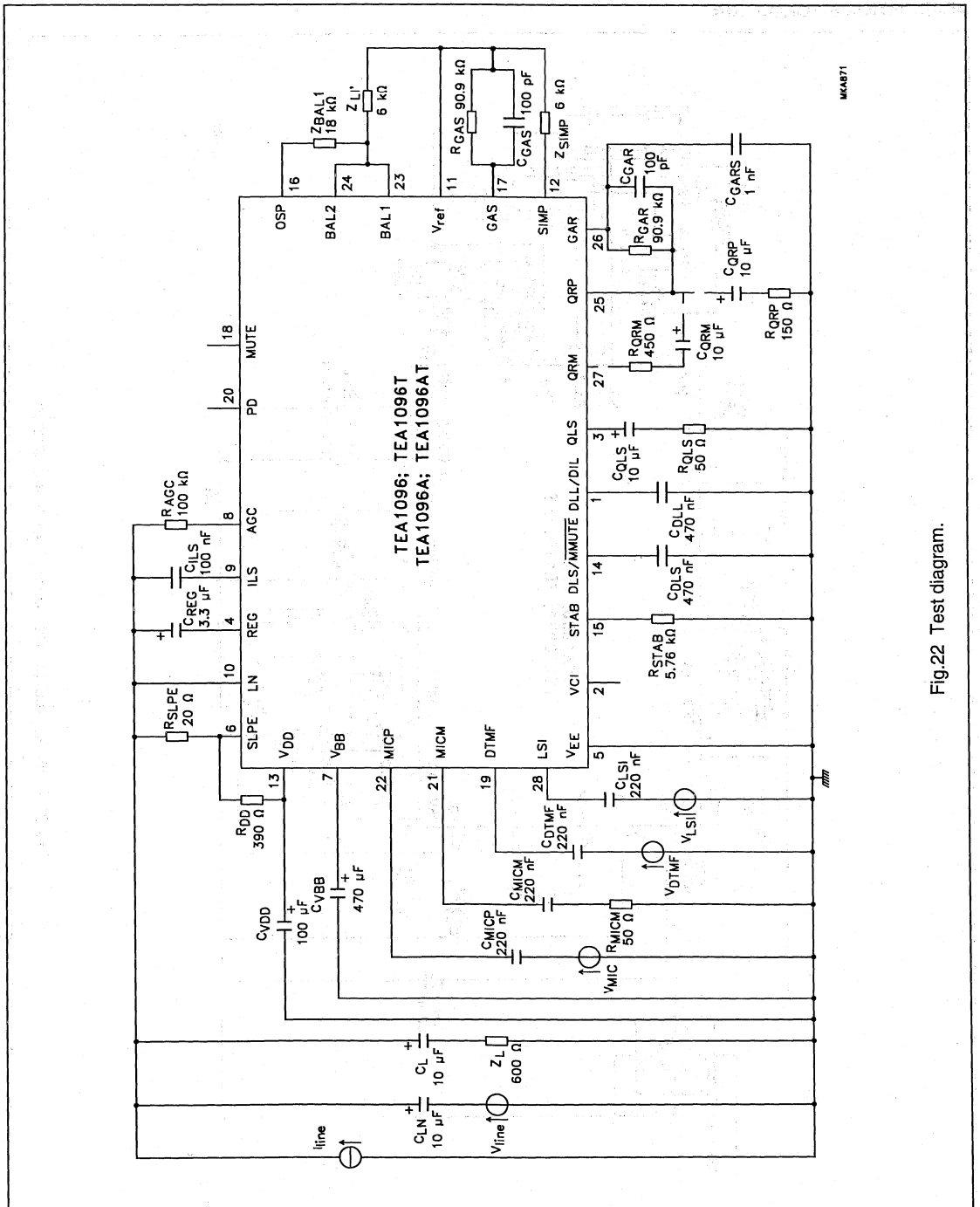


Fig.22 Test diagram.

APPLICATION INFORMATION

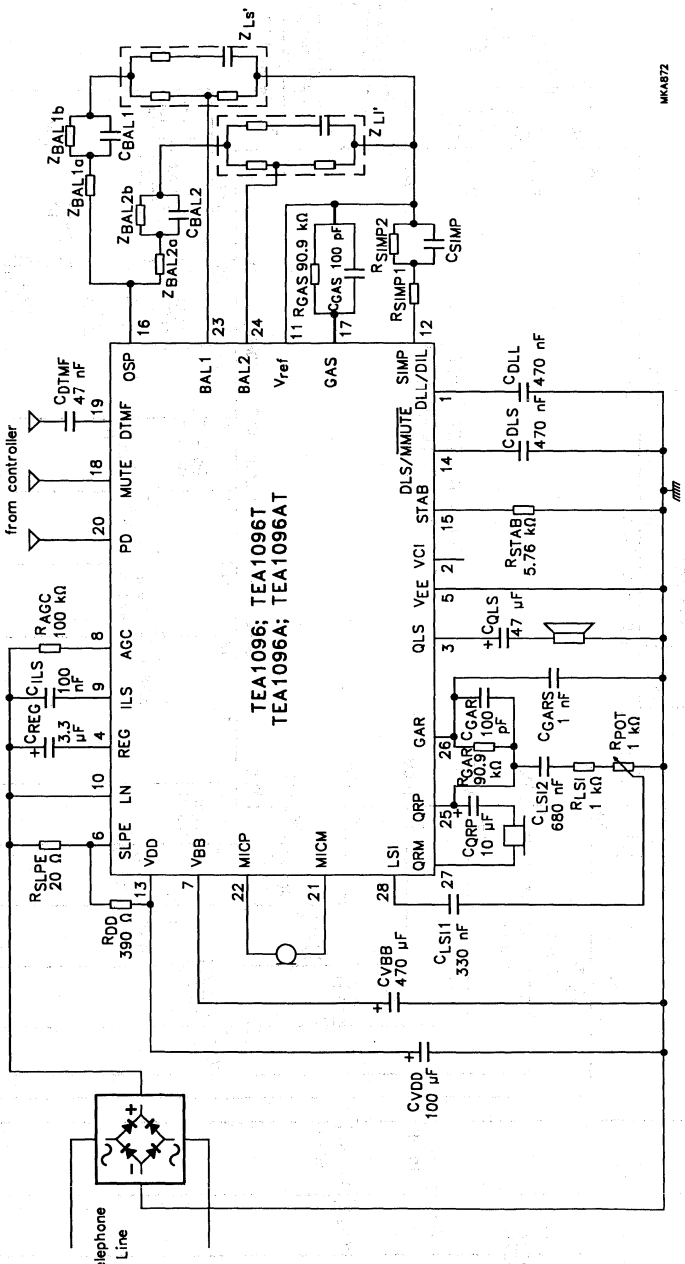


Fig.23 Basic application with a complex line impedance.

Battery monitor for NiCd and NiMH chargers

TEA1100; TEA1100T

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

FEATURES

- Accurate regulation of charge current settings in co-operation with a switched mode power supply
- Accurate detection of fully charged batteries by currentless battery voltage sensing
- Switch over from fast to normal charging when batteries are fully charged
- Adjustable fast charging level (1 C to 5 C)
- Adjustable normal charging level (0.05 C to 0.25 C)
- Temperature guarding by means of an NTC resistor
- Tracking of maximum fast charging time with fast charging current level
- Protections against short-circuited and open batteries
- Large battery voltage range
- Both DC and PWM outputs with polarity switch

APPLICATIONS

- Charge systems for NiCd and NiMH batteries

GENERAL DESCRIPTION

The TEA1100 is manufactured in a BICMOS process intended to be used as a battery monitor circuit in charge systems for NiCd and NiMH batteries.

The circuit has to be situated on the secondary side in mains-isolated systems where it monitors the battery voltage and the charge current. The circuit drives, by means of an opto-coupler or a pulse transformer interface, an SMPS circuit, situated on the primary side of the system, thus controlling the charge current of the batteries. The circuit can drive the external power transistor in switched mode systems, which have a DC power source, via a driver stage.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1100	16	DIL	plastic	SOT38G
TEA1100T	16	SO16L	plastic	SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		5.65	–	11.5	V
I_P	supply current	outputs off	–	–	4.1	mA
V_{VAC}	voltage range of battery-full detection		0.385	–	3.85	V
dV_{VAC}/V_{VAC}	–dV detection level w.r.t. top value	note 1	–	1	–	%
I_{VAC}	input current battery monitor		–	–	1	nA
V_{VAC}	voltage protection battery low battery high		 – –	 0.3 4.25	 – –	 V V
 I_{ref} I_n	charging level fast normal	$I_{charge} = R1/R_s \times I$; see Fig. 3 $I = I_{ref}$ $I = 1/p \times 0.1 \times I_n$ (p = prescale factor)	 20 10	 – –	 100 50	 µA µA
f_{OSC}	oscillator frequency		10	–	100	kHz

Note to the quick reference data

1. The –dV detection level can be adjusted by use of an external voltage regulator diode to increase the sensitivity.

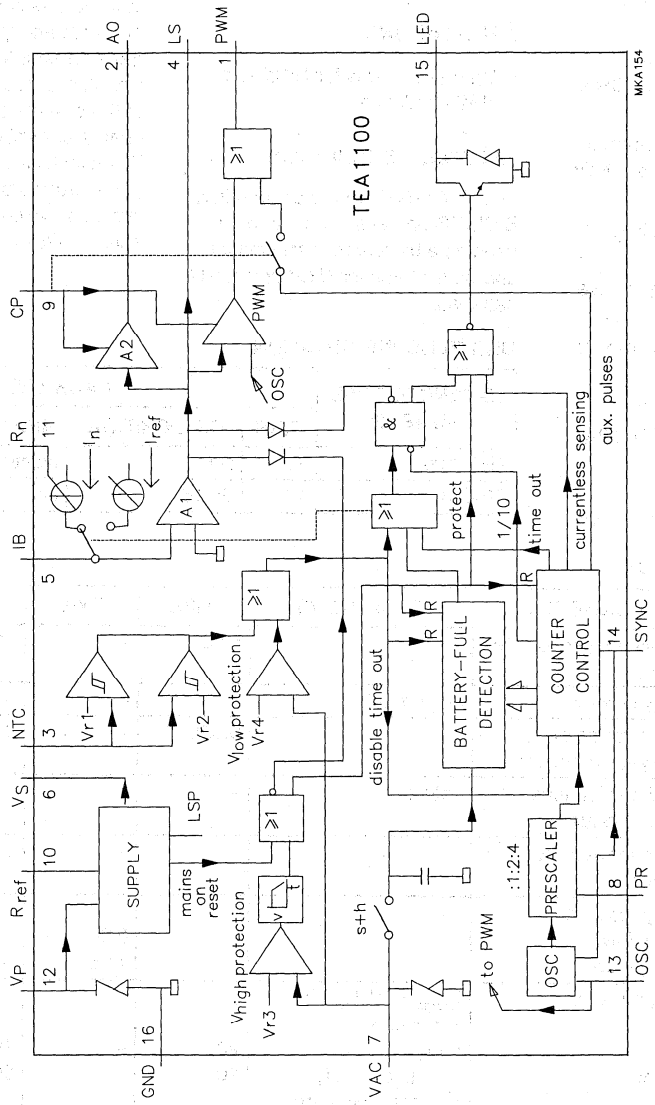


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
PWM	1	pulse width modulator
AO	2	analog output
NTC	3	temperature sensor input
LS	4	loop stability
IB	5	charge current
V_S	6	stabilized supply voltage
VAC	7	battery voltage
PR	8	prescaler
CP	9	change polarity
R_{ref}	10	reference resistor
R_n	11	normal charge reference resistor
V_P	12	positive supply voltage
OSC	13	oscillator input
SYNC	14	synchronization input
LED	15	LED output
GND	16	ground

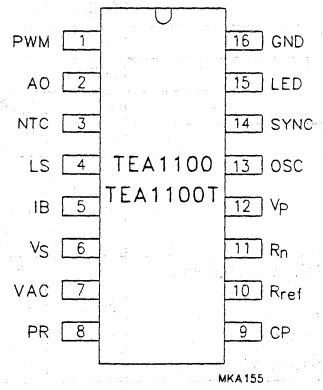


Fig.2 Pin configuration.

Battery monitor for NiCd and NiMH chargers

TEA1101; TEA1101T

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

FEATURES

- Accurate detection of fully charged batteries by currentless –dV sensing
- Digital filtering of the battery voltage to avoid false –dV triggering
- Minimum and maximum temperature guarding by means of an NTC resistor
- Battery checking to protect against short-circuit and open batteries
- Battery monitor allows recharging different battery-pack voltages
- Tracking of maximum fast charging time with fast charging current level
- Accurate regulation of charge current settings in co-operation with a switched mode power supply or DC current source
- Both DC and PWM outputs with polarity switch
- Adjustable fast charge level (1 C to 5 C)
- Adjustable pulsating trickle charge level (0.05 C to 0.25 C)
- Large operating temperature range.

APPLICATIONS

- Charge systems for NiCd and NiMH batteries.

GENERAL DESCRIPTION

The TEA1101 is manufactured in a BICMOS process intended to be used as a battery monitor circuit in charge systems for NiCd and NiMH batteries.

The circuit has to be situated on the secondary side in mains-isolated systems where it monitors the battery voltage and the charge current. The circuit drives, by means of an opto-coupler or a pulse transformer interface, an SMPS circuit, situated on the primary side of the system, thus controlling the charge current of the batteries.

The circuit can drive the external power transistor in switched mode systems, which have a DC power source, via a driver stage.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		5.65	–	11.5	V
I_P	supply current	outputs off	–	–	4.3	mA
V_{VAC}	voltage range of battery-full detection		0.385	–	3.85	V
dV_{VAC}/V_{VAC}	–dV detection level w.r.t. top value	note 1	–	0.25	–	%
I_{VAC}	input current battery monitor		–	–	1	nA
V_{VAC}	voltage protection					
	battery low		–	0.3	–	V
	battery high		–	4.25	–	V
	charging level	$I_{charge} = R1/R_s \times I$; see Fig.3				
I_{ref}	fast	$I = I_{ref}$	20	–	100	µA
I_n	normal	$I = 1/p \times 0.1 \times I_n$ (p = prescale factor)	10	–	50	µA
f_{OSC}	oscillator frequency		10	–	100	kHz

Note

1. The –dV detection level can be adjusted by use of an external voltage regulator diode to increase the sensitivity.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1101	16	DIL	plastic	SOT38G
TEA1101T	16	SO16L	plastic	SOT162A

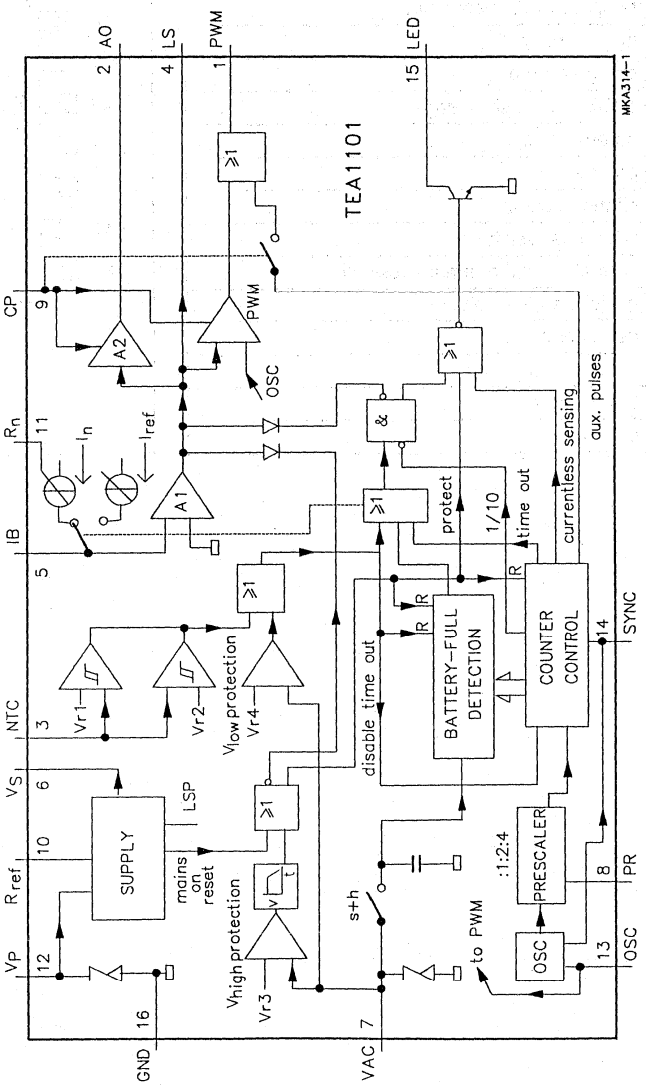


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
PWM	1	pulse width modulator
AO	2	analog output
NTC	3	temperature sensor input
LS	4	loop stability
IB	5	charge current
V_S	6	stabilized supply voltage
VAC	7	battery voltage
PR	8	prescaler
CP	9	change polarity
R_{ref}	10	reference resistor
R_n	11	normal charge reference resistor
V_P	12	positive supply voltage
OSC	13	oscillator input
SYNC	14	synchronization input
LED	15	LED output
GND	16	ground

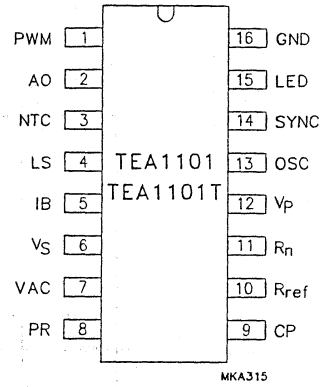


Fig.2 Pin configuration.

Low power digital UHF paging receiver UAA2050T

GENERAL DESCRIPTION

The UAA2050T is a very low power UHF and VHF radio receiver circuit, primarily intended for use in paging receivers (27 MHz to 470 MHz) for wide-area digital paging systems employing direct FM non-return-to-zero (NRZ) frequency-shift keying (FSK) modulation.

Used in conjunction with the PCA5000T decoder for POCSAG paging systems, it offers an extremely advanced radio paging concept.

The radio receiver design is based on the offset receiver principle. The receiver provides fully filtered and squared data to drive the decoder and can be turned off completely by external inputs.

Features

- Low noise preamplifier ensuring high RF sensitivity
- Few external components required
- Low current consumption
- Wide operating supply voltage range
- Power on/off mode selectable via the enable input (RE)
- Low battery voltage detector
- Crystal controlled receiver frequency (AFC)
- Fully compatible with all FSK modulated systems (512 and 1200 bits/s)
- Uses low cost crystal

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage range		$V_P = V_{7-15}$	1.9	–	3.5	V
Supply voltage for preamplifier		$V_{23,24-15}$	1.0	–	3.5	V
Total supply current		I_{tot}	2.25	–	3.76	mA
Supply current OFF		$-I_{OFF}$	–	–	1.0	µA
RF sensitivity (RMS value)	1 x 10^{-2} bit error rate	EMF/2	–	0.18	0.25	µV
Preamplifier noise figure	note 1; f = 470 MHz	NF	–	4.5	–	dB
Operating ambient temperature range		T_{amb}	−10	–	+70	°C

Note to the Quick reference data

. Including the transforming network.

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO28; SOT136A).

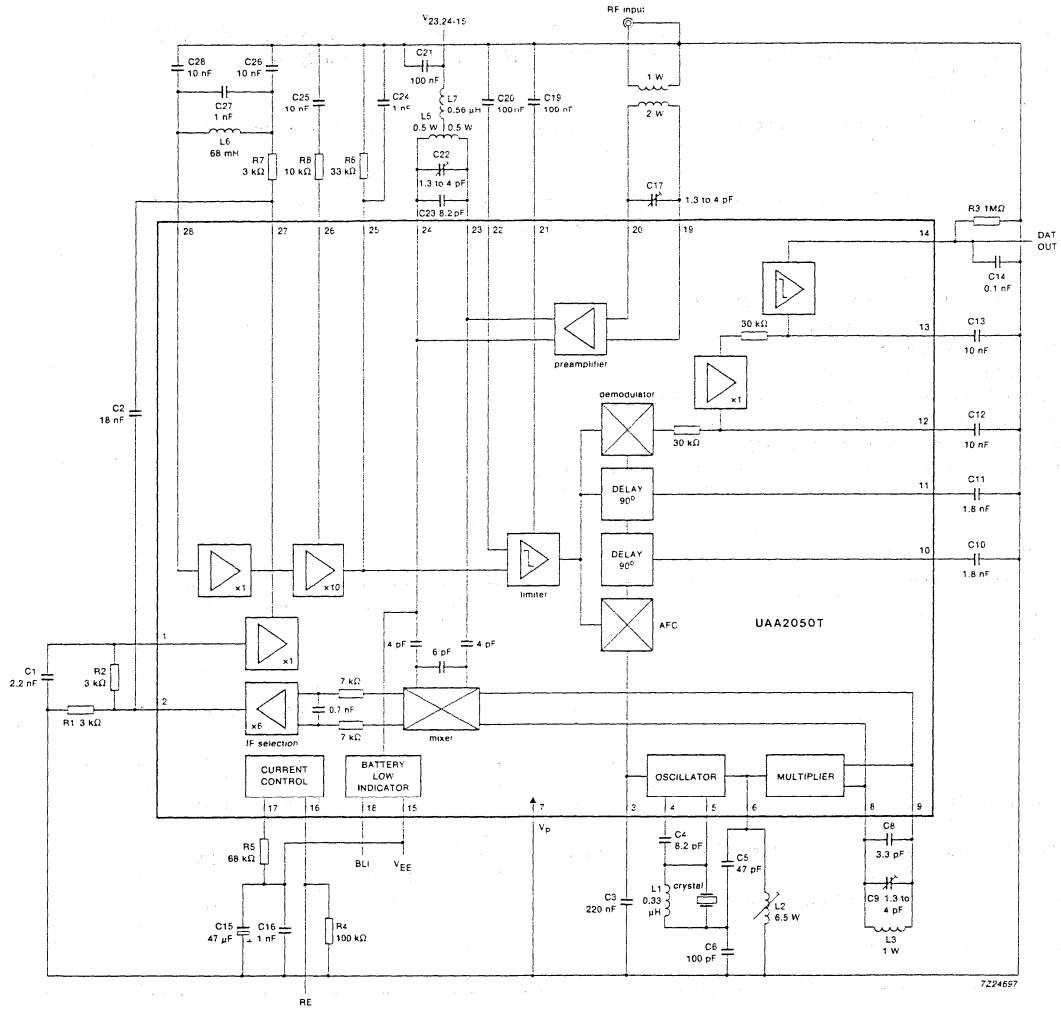


Fig.1 Block diagram (showing UHF external components).

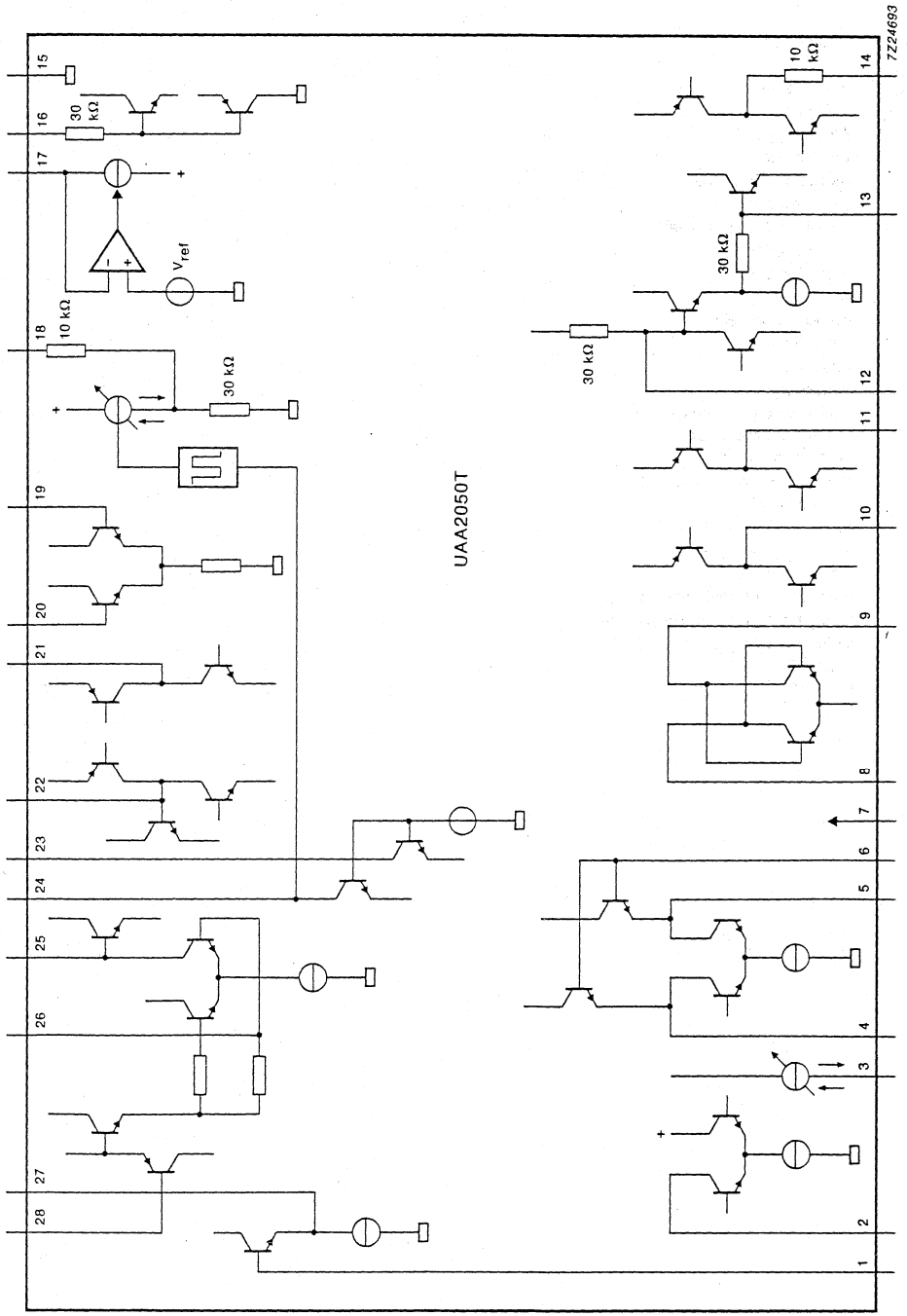


Fig.2 Pinning diagram and equivalent circuits.

PINNING

pin	mnemonic	description
1	IFF2	IF filter 2
2	IFF1	IF filter 1
3	AFC	AFC (test point 1)
4	OSC IN	oscillator input
5	OSC AFC	oscillator AFC range
6	OSC OUT	oscillator output
7	V_P	supply voltage (positive)
8	MC1	multiplier coil
9	MC2	multiplier coil
10	AFCD	AFC delay
11	DEMODD	demodulator delay
12	DAT F1	data filter 1
13	DAT F2	data filter 2
14	DAT OUT	data output
15	V_{EE}	supply voltage (negative)
16	RE	receiver enable input
17	CC	current control input
18	BLI	battery low indicator output
19	PREAMP1	preamplifier input 1
20	PREAMP2	preamplifier input 2
21	LC2	limiter decoupling 2
22	LC1	limiter decoupling 1
23	MIX1	mixer input 1 (preamplifier output)
24	MIX2	mixer input 2 (preamplifier output)
25	LIM IN	limiter input (test point 2)
26	IFF5	IF filter 5
27	IFF3	IF filter 3
28	IFF4	IF filter 4

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

parameter	condition	symbol	min.	max.	unit
Supply voltage		$V_P = V_{7-15}$	−0.3	+5.0	V
Supply voltage for preamplifier		$V_{23,24-15}$	−0.3	+5.0	V
Operating ambient temperature range		T_{amb}	−10	+70	°C
Storage temperature range		T_{stg}	−55	+125	°C
Electrostatic handling; human body model*	except pins 19 and 20	V_{ESD}	−1000	+1000	V
	only pins 19 and 20	V_{ESD}	−500	+1000	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

V_P = 2.0 V; $V_{23,24-15}$ = 1.1 V; all voltages referenced to V_{EE}; T_{amb} = −10 to +55 °C; typical values measured at T_{amb} = 25 °C; test circuit as Fig.4; L2 and L3 short-circuited; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{7-15}$	1.9	2.0	3.5	V
Supply voltage for preamplifier	$V_{23,24-15} \leqslant V_P$	$V_{23,24-15}$	1.0	1.1	3.5	V
Supply current	$V_{RE} \geqslant V_P - 0.6$ V	I_7	1.9	2.5	3.2	mA
Supply current for preamplifier	$V_{RE} \geqslant V_P - 0.6$ V	$I_{23,24}$	0.35	0.45	0.56	mA
Supply current OFF	$V_{RE} \leqslant 0.4$ V	I_{OFF}	–	–	1.0	µA
Receiver enable (RE)						
POWER-OFF MODE:						
input voltage		$V_{RE} = V_{16-15}$	–	–	0.4	V
input current	V_{RE} = 0.4 V	I_{16}	–	–	1.0	µA
POWER-ON MODE:						
input voltage		$V_{RE} = V_{16-15}$	$V_P - 0.6$ V	–	–	V
input current	V_{RE} = 1.4 V	I_{16}	–	1.0	5.0	µA
Data output (DAT OUT)						
Output voltage HIGH	$I_{14} = \pm 10$ µA	V_{14-15}	$V_P - 0.7$ V	–	–	V
Output voltage LOW	$I_{14} = \pm 10$ µA	V_{14-15}	–	–	0.5	V
Battery voltage low indicator						
Detection voltage	see Fig.3	V_{DET} V_{DET}	1.10 1.90	1.17 2.00	1.24 2.10	V V
Output voltage HIGH	1.0 V ⩽ V_{24-15} ⩽ 1.10 V; 1.85 V ⩽ V_{24-15} ⩽ 1.90 V; $I_{18} = \pm 7$ µA	V_{OH}	$V_P - 0.5$ V	–	–	V
Output voltage LOW	1.24 V ⩽ V_{24-15} ⩽ 1.65 V; 2.10 V ⩽ V_{24-15}; $I_{18} = \pm 7$ µA	V_{OL}	–	–	0.5	V

Note to the DC characteristics

1. V_{18-15} goes HIGH if V_{24-15} is less than V_{DET}.

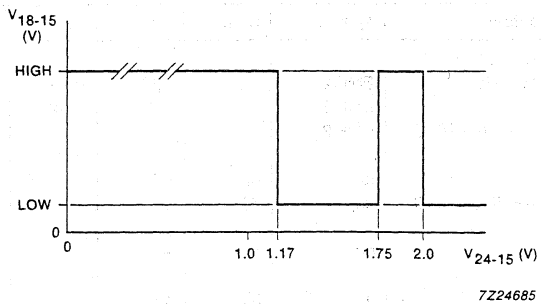


Fig.3 Typical battery low indicator thresholds.

AC CHARACTERISTICS (UHF)

For AC test procedures refer to section 'TEST INFORMATION'. V_P = 2.0 V; $V_{23,24-15}$ = 1.1 V; all voltages referenced to V_{EE}; T_{amb} = −10 to +55 °C; typical values measured at T_{amb} = 25 °C; test circuit as Fig.4 and printed-circuit board layout as Fig.7; test signal: f = 469.200 MHz: deviation = ±4.5 kHz: modulation = 256 Hz rectangular; channel spacing = 25 kHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
UHF sensitivity range (RMS value)	note 1; 1 x 10^{-2} bit error rate	EMF/2	–	0.18	0.25	µV
		EMF/2	–	−122	−119	dBm
	T_{amb} = −10 to +70 °C	EMF/2	–	–	−116	dBm
Adjacent channel selectivity		αa	60	67	–	dB
	T_{amb} = −10 to +70 °C	αa	50	–	–	dB
Co-channel selectivity		αc	8	–	–	dB
Spurious response rejection		αs	55	58	–	dB
Intermodulation response		IM	50	60	–	dB
Blocking	Δf ≥ ±4 MHz	EMF	80	83	–	dBµV
AFC lock-in range		±Δf	3	–	–	kHz
Preamplifier	see Fig.9					
Noise Figure	note 2	NF	–	4.5	–	dB
Third order intercept point		IP3	–	−20	–	dBm
Available power gain		G_p	–	6	–	dB
1 dB compression point (RMS value)		EMF/2	–	10	–	mV
VHF RF sensitivity range (RMS value)	see Fig.10; f = 173.95 MHz; 1 x 10^{-2} bit error rate	EMF/2	–	0.14	–	µV
		EMF/2	–	−124	–	dBm

Notes to the AC characteristics

1. A simple digital method of performing an approximate bit error rate (BER) measurement with a counter is shown in Fig.5. At high signal levels (10 µV) the counter should read the exact frequency of the data input to the signal generator (256 Hz). As the signal level is reduced, errors occur at the receiver output and effectively changes the output frequency read by the counter (error duration is nearly always less than one bit length).
   The input signal level (V_{ref}) is reduced until the bit error rate is ≤ 1 x 10^{-2} (5 bit errors for 512 bit/s system). The frequency from the data output signal will change from 256 Hz (512 bit/s system) to 261 Hz. This RF-level is the reference for the following tests (V_{ref}).

2. Including the transforming network.

TEST INFORMATION

Tuning procedure for AC tests

1. After performing the DC tests, prepare the device for AC testing (as shown in Fig. 4).

2. Connect pin 3 to a voltage source of $V_{3-7} = -0.5$ V. Measure the multiplier frequency with a counter or spectrum analyzer connected to the link winding of L3. Tune L2 to set the crystal oscillator to a frequency of:

   $$\frac{\text{Received frequency} + 2.2\ \text{kHz}}{5} \quad (\pm 100\ \text{Hz})$$

   For a received frequency of f = 469.200 MHz, the oscillator frequency (f_{OSC}) = 93.840 MHz.

3. Remove the test voltage source and turn on the signal generator (f = 469.200 MHz; deviation = ±4.5 kHz; rectangular 256 Hz modulation; RF input level = 1 mV).

   Note During the following tests the RF signal generator level should be reduced as the receiver is tuned, to ensure the peak-to-peak output voltage at pin 25 lies between 20 mV and 100 mV.

4. Tune C9 (multiplier) to obtain a peak audio output voltage on pin 25.

5. Tune C22 (Mixer input) to obtain a peak audio output voltage on pin 25.

6. Disconnect the frequency counter from the multiplier output. Measure the voltage at pin 3 and check if it is within the range of −0.48 V to −0.52 V. If it is outside this range then adjust L2 (oscillator) until it is within the limits.

7. Check with an oscilloscope that clean data is appearing on the data output (pin 14) and proceed with the AC tests.

Test conditions

The data output signal corresponds to the sensitivity definition.

Where:

f_1 is the modulated test signal
f_2 is the unmodulated test signal
f_{cs} is the channel spacing (25 kHz)
V_1 is the signal generator 1 output
V_2 is the signal generator 2 output
V_{ref} is defined in 'Notes to the AC characteristics'.

1. Adjacent channel selectivity (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3dB$
   - generator 2: unmodulated test signal; $V_2 = V_1 + 60$ dB ($f_2 = f_1 \pm \Delta f_{cs}$).

2. Co-channel selectivity (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB
   - generator 2: unmodulated test signal; $V_2 = V_1 - 8$ dB ($f_2 = f_1 \pm 3$ kHz maximum).

3. Spurious response rejection (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB
   - generator 2: unmodulated test signal; $V_2 = V_1 + 55$ dB (f_2 =100 kHz to 1 GHz; $|f_2 - f_1| \geq 2\Delta f_{cs}$).

4. Intermodulation response (see Fig.6);
   - generator 1: modulated test signal; $f_1 = 469.2$ MHz $\pm 2 \times n \times \Delta f_{cs}$) n = 1 to 4 .
   - generator 2: unmodulated test signal; $f_2 = 469.2$ MHz $\pm n \times \Delta f_{cs}$). n = 1 to 4.

   Output voltages of both generators increase with the same level, until a data output signal corresponding to the sensitivity definition is reached. The level must be 50 dB above the V_{ref} + 3 dB level.

5. Blocking (see Fig.6);
   - generator 1: modulated test signal; V_1 (EMF) = 3 dBμV
   - generator 2: unmodulated test signal; V_2 (EMF) = 80 dBμV ($f_2 = f_1 \pm \Delta f$; $\Delta f \geq 4$ MHz)

6. AFC lock-in-range (see Fig.5);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB ($f_1 = 469.2$ MHz ± 3 kHz)

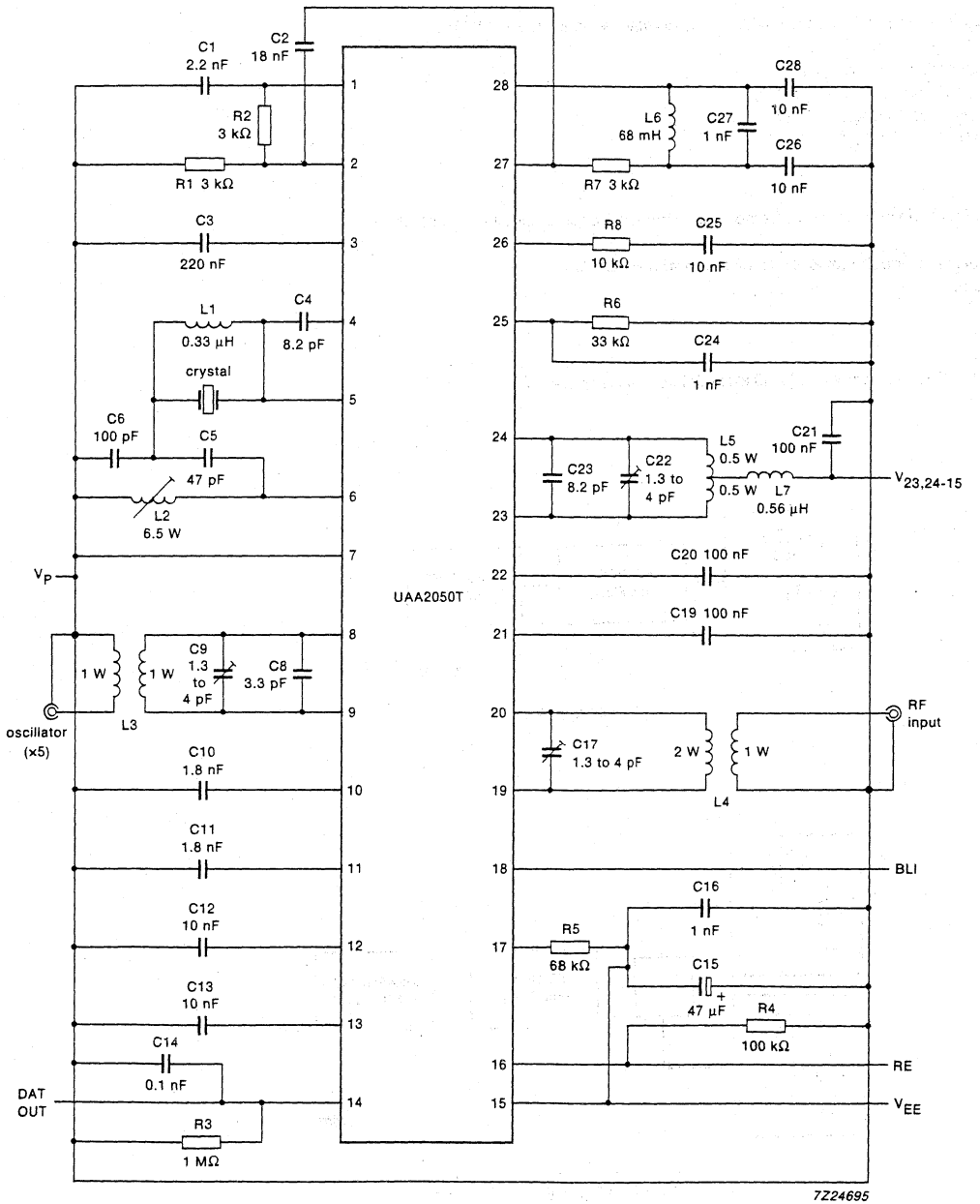


Fig.4 Test circuit (UHF).

Crystal data

Test frequency for the receiver chip is 469.2 MHz, crystal frequency is 93.838 MHz.

Static capacitance C0 (max.) = 4 pF
Dynamic capacitance C1 = 0.4 fF ±20%
Dynamic resistance R1 (max.) = 75 Ω
Temperature drift = $\pm 5 \times 10^{-6}$.

Inductors

L3, L4 and L5: wound with 0.9 mm silvered wire, without pot or core and diameter of 4.5 mm.

L1 = 0.33 µH chip inductor (at 25 MHz minimum value of Q = 12)
L2 = 6.5 turns
L3 = 1 turn
L4 = 2 turns
L5 = 1 turn
L6 = inductor, Philips microchoke (at 10 kHz minimum value of Q = 10)

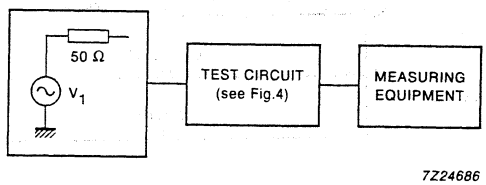


Fig.5 Test figure A.

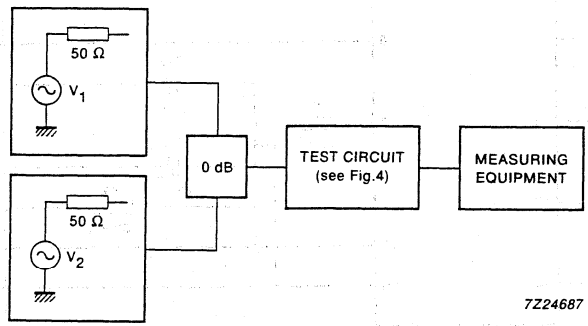
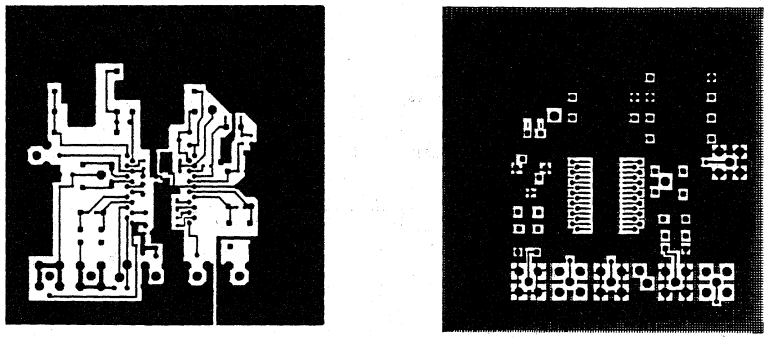


Fig.6 Test figure B.



7Z24689

(a) underside (b) top side

Fig. 7 Printed-circuit board for UHF range (see Fig.4).

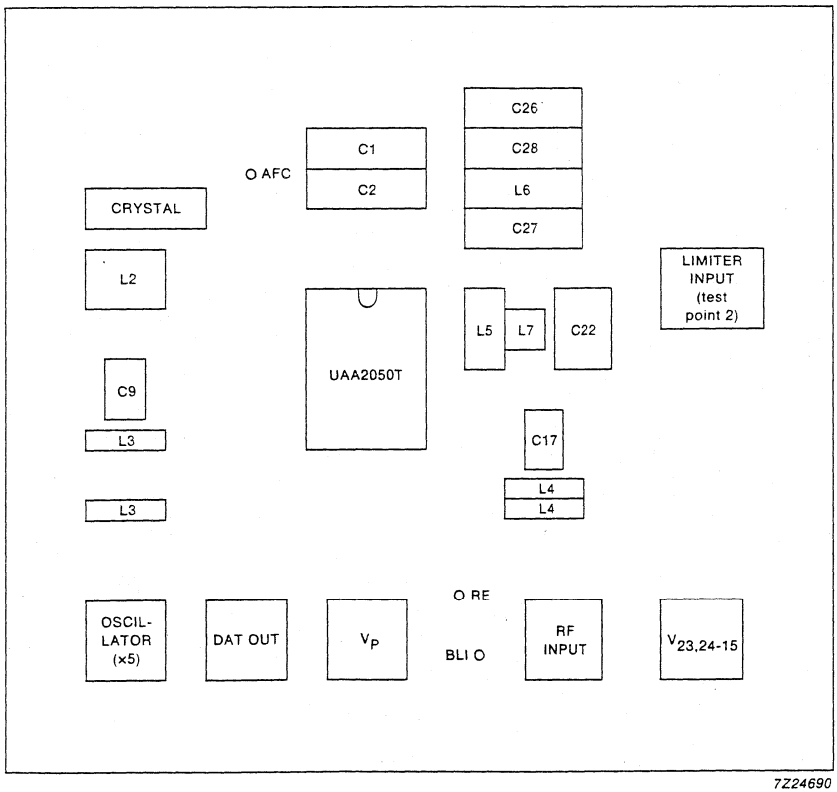


Fig. 8 Printed-circuit board for UHF range (component arrangement).

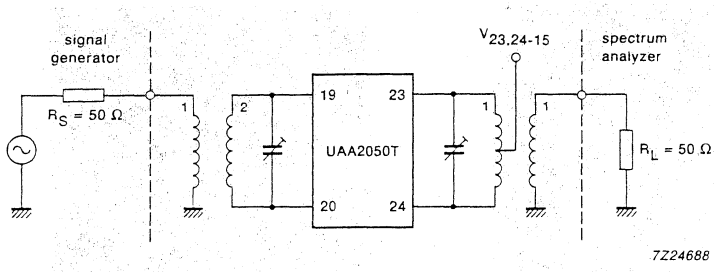


Fig.9 Test circuit for the preamplifier.

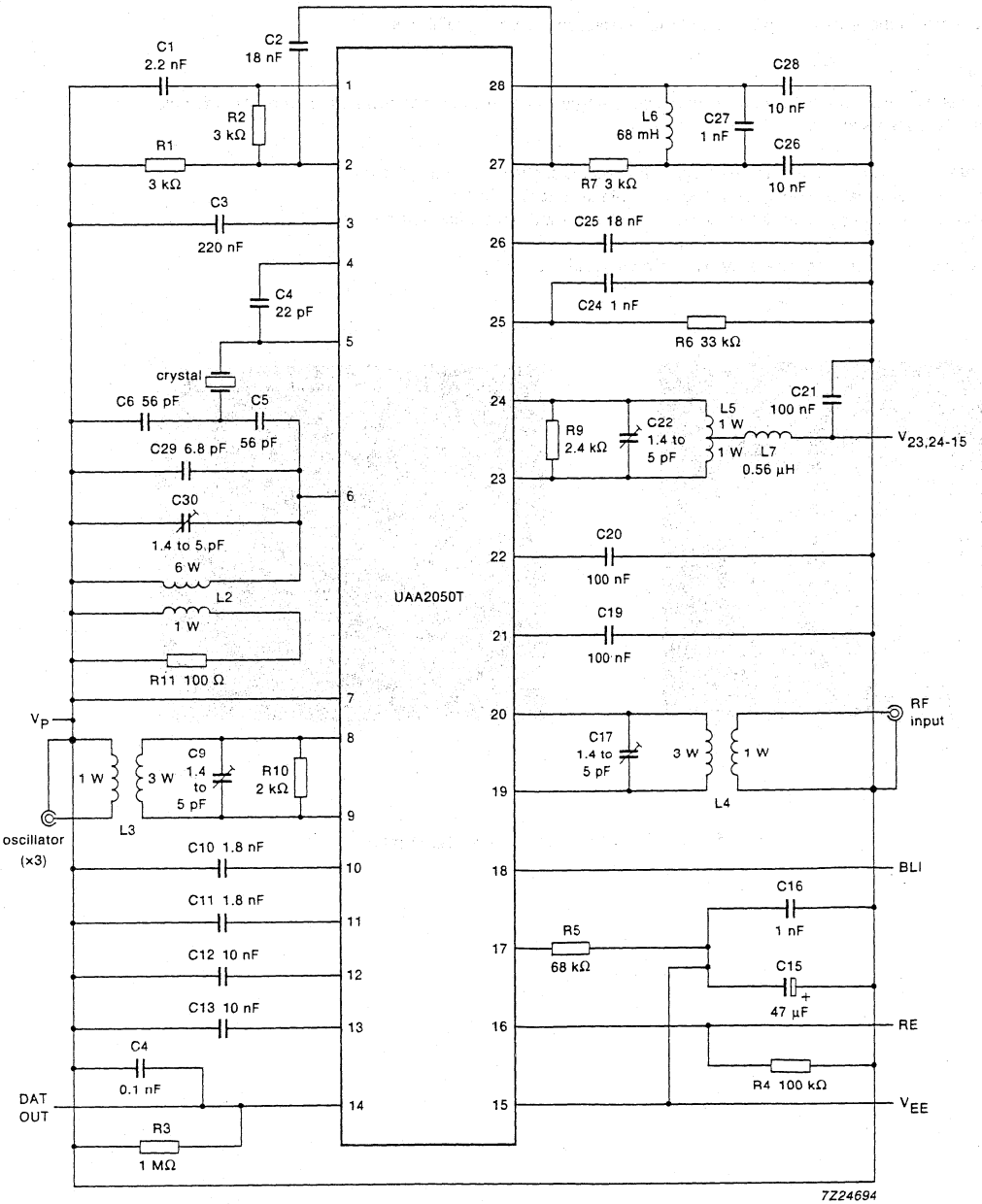


Fig.10 Test circuit (VHF).

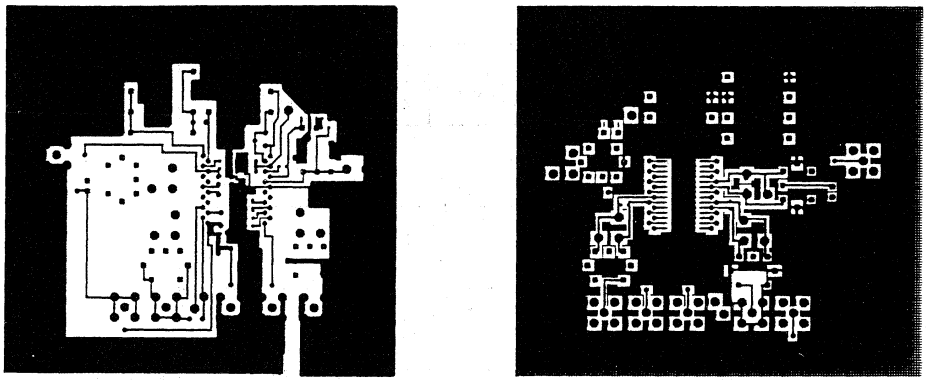
Crystal data

Test frequency for the receiver chip is 173.95 MHz, crystal frequency is 57.9859 MHz.

Inductors

L2, L3, L4 and L5: wound with 0.3 mm enamelled copper wire on Toko 4.5 mm diameter former, without pot or core. Screening cans are also used.

L2 = 6 turns, 2 turns per groove; link winding, 1 turn over the centre of the other winding
L3 = 3 turns, 1 turns per groove; link winding, 1 turn at the bottom of the former
L4 = 3 turns, 1 turns per groove; link winding, 1 turn at the centre of the other winding
L5 = 2 turns
L6 = inductor, Philips microchoke (at 10 kHz minimum value of Q = 10)



(a) underside (b) top side

7Z24691

Fig. 11 Printed-circuit board for VHF range (see Fig.10).

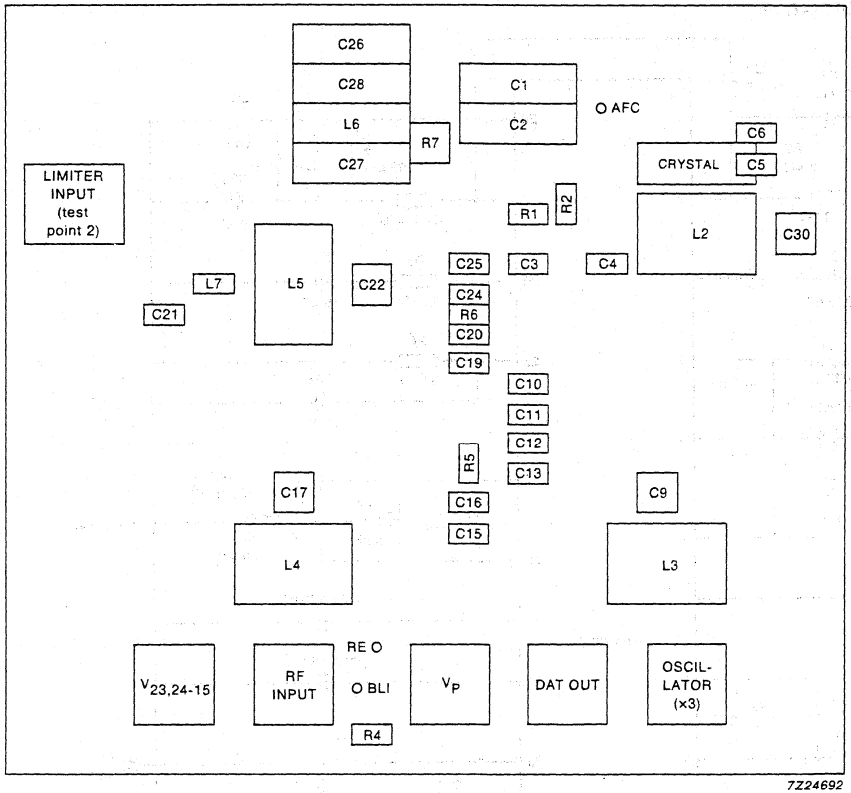


Fig. 12 Printed-circuit board for VHF range (component arrangement).

APPLICATION INFORMATION

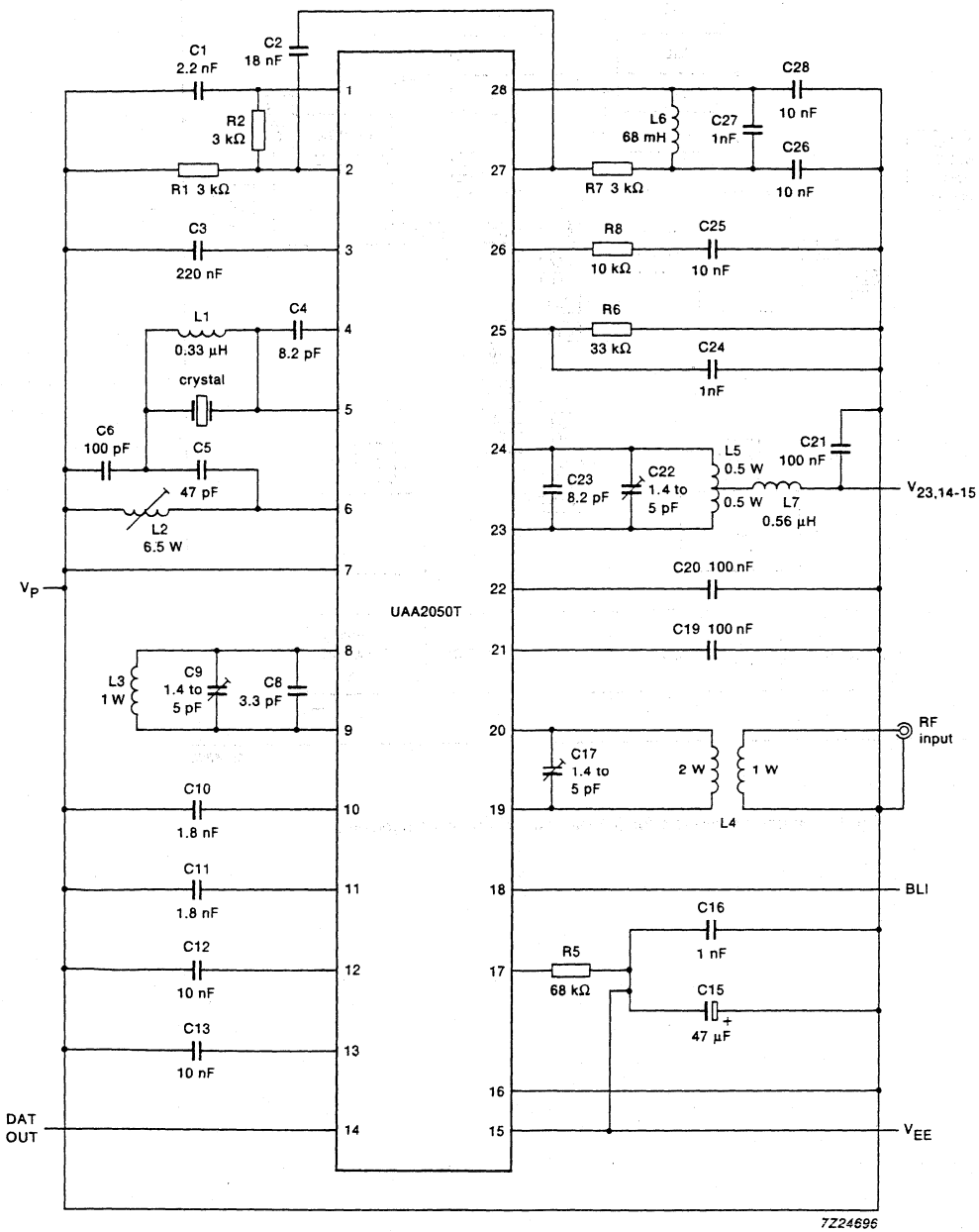


Fig.13 Application diagram (UHF).

Note to Fig.13

For information concerning the crystal oscillator and inductors, refer to Fig.4.

Image rejecting front-end for GSM applications

UAA2072M

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for up to 60 dB on-chip image rejection
- Programmable IF I/Q combiner
- On-chip programmable quadrature network
- Very fast 3-wire control bus
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2072M contains both a receiver front-end and a high frequency transmit mixer intended to be used in the GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2072M is its ability to provide at least 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne or supradyne reception. The precision needed for this signal processing is achieved by compensating for process spreads and trimming for the choosen IF frequency and the LO band centre frequency via a 3-wire serial bus interface.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The overall phase rotation is programmable for maximum image rejection at a given IF. The IF output drivers have differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced, and 200 Ω is used as standard RF impedance.

A 3-pin unidirectional serial interface is used to program the circuits, using 16-bit words. This data bus allows compensation of process spreads, and is used to adjust for maximum image rejection performance at a given IF. It also offers a selection to reject the upper or lower image frequency and control over the different power-down modes. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	4.5	4.8	5.3	V
I_{CCRX}	receive supply current	26	31.5	38	mA
I_{CCTX}	transmit supply current	10	12	14	mA
I_{CCPD}	supply current in power-down	–	–	50	µA
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2072M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

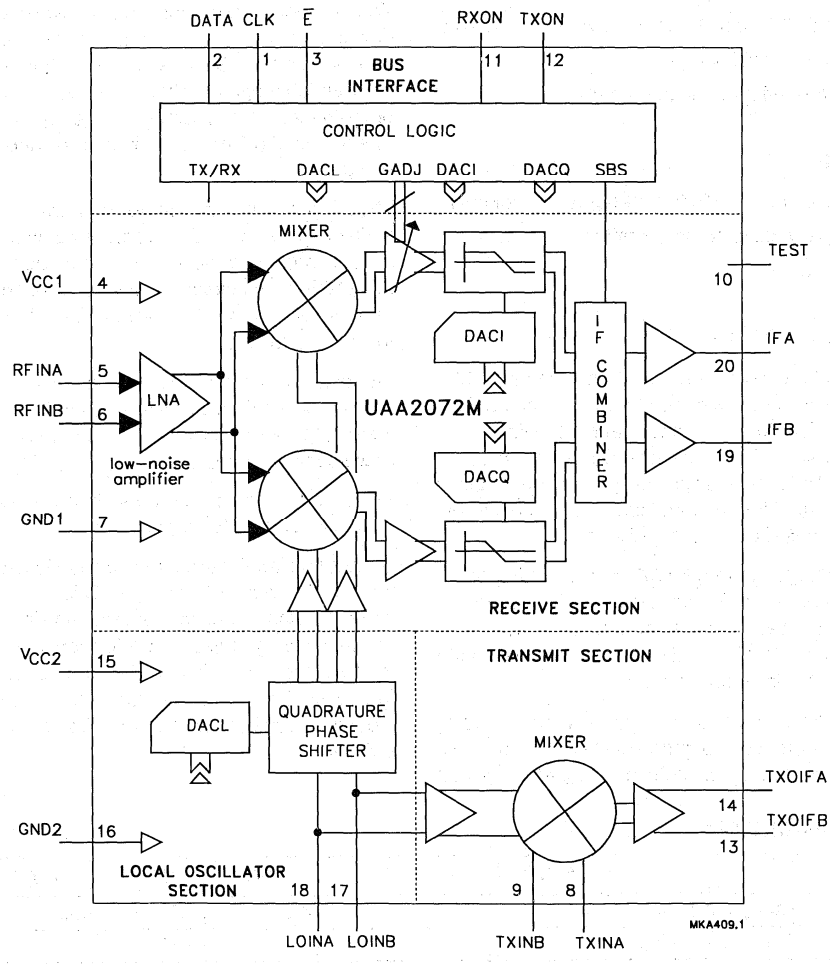


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	serial bus clock
DATA	2	serial bus data
$\overline{E}$	3	serial bus enable (active LOW)
V_{CC1}	4	supply voltage for LNA, IF parts and TX mixer
RFINA	5	RF balance input A
RFINB	6	RF balance input B
GND1	7	ground for synthesizer buffer and logic
TXINA	8	transmit mixer input A (balanced)
TXINB	9	transmit mixer input B (balanced)
TEST	10	reserved for test purposes, should be connected to ground
RXON	11	hardware power-on for receive parts
TXON	12	hardware power-on for transmit mixer
TXOIFB	13	transmit mixer IF output B (balanced)
TXOIFA	14	transmit mixer IF output A (balanced)
V_{CC2}	15	supply voltage for local oscillator parts
GND2	16	ground for LO parts
LOINB	17	LO input B (balanced)
LOINA	18	LO input A (balanced)
IFB	19	IF output (balanced)
IFA	20	IF output (balanced)

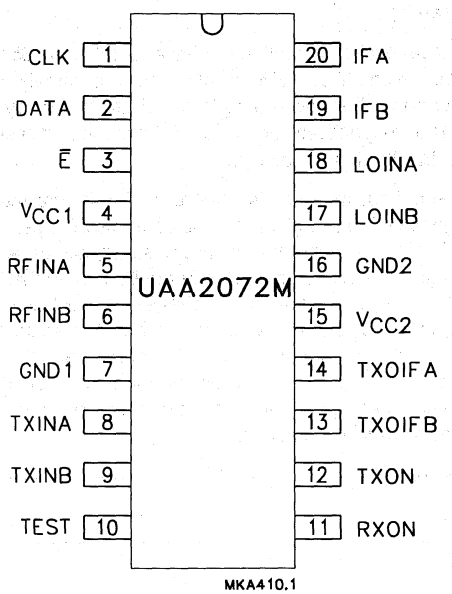


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

The serial bus interface is used for tuning to maximum image rejection at a given IF. The contents of registers ip5 to ip0 and qp5 to qp0 (named IF phase adjustment words) are digital-to-analog converted in the DACI and DACQ blocks. The obtained internal voltages control the phase shift in I and Q; thus allowing them to be trimmed precisely to 45° and 135° at any given IF between 30 and 90 MHz. The gain in the I channel is slightly adjustable using the four bits ga3 to ga0 to allow compensation of small gain mismatches between I and Q.

One bit (sbs) allows selection between infradyne or supradyne reception.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 200 Ω, choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; i.e. a 1 kΩ resistor load at each IF output, plus a 2 kΩ resistor to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

In the event of only one output being used, a 1 kΩ resistive load in parallel with a tuning inductor to V_{CC}, provides a matched 1 kΩ output to the external IF filter.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON or via the bus interface by changing the srx-bit in the internal register.

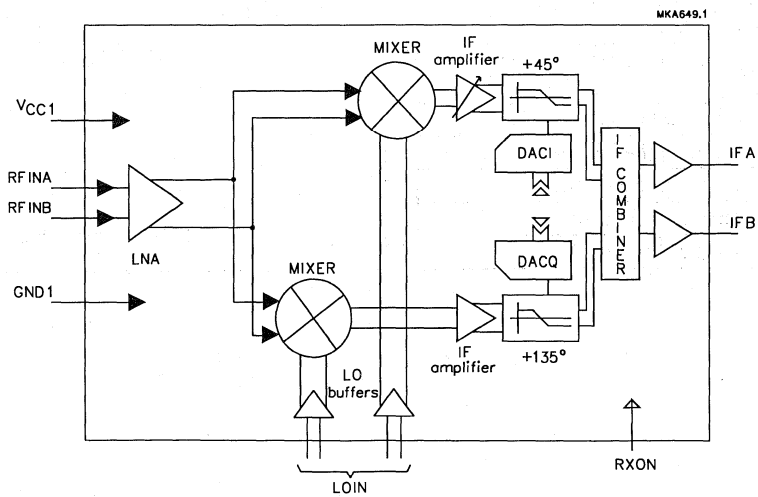


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by programming via the serial bus. The word 'lo5 to lo0' named LO Quad Centre Frequency Adjustment word is converted to an analog voltage in a digital-to-analog converter (DACL, see Fig.4). This voltage trims the all-pass network to the selected LO frequency range. To obtain the 30 dB specified image rejection the precision required on this trimming remains low.

The LO input impedance is 100 Ω differential. Switching from RX to TX or power-down mode has little influence on the LO input impedance.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 kΩ load. The IF outputs are low impedance (common collector type).

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON or via the serial bus interface by changing the stx-bit in the internal register.

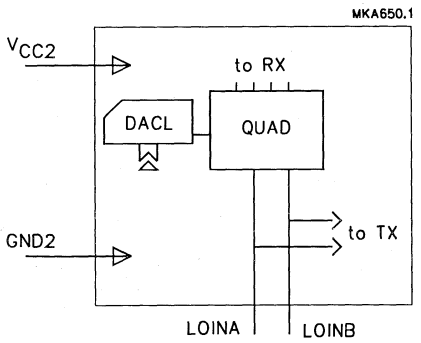


Fig.4 Block diagram, LO section.

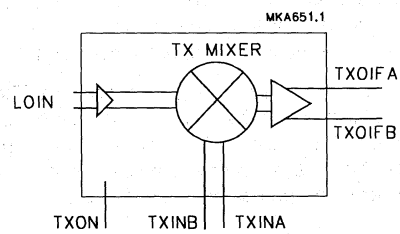


Fig.5 Block diagram, transmit mixer.

Serial bus interface

The 3-wire serial bus interface allows control over the selective power-up of the transmit, receive and LO buffer circuits, the tuning of the LO quadrature and IF quadrature circuits and the selection of sideband rejection. The interface consists of a 16-bit programming register, three working latches and three DACs which provide the tuning voltages for the image rejection of the receive quadrature circuits.

BUS FORMAT

A 3-wire unidirectional bus is used to program the circuit, the 3 wires being: DATA, CLOCK (CLK) AND ENABLE ($\overline{E}$). The timing diagram is illustrated in Fig.4. The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their corresponding data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed working latch when $\overline{E}$ returns HIGH.
Only the last 16 bits clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. If $\overline{E}$ returns HIGH while CLK is still LOW, the extra clock edge produced will cause data shift. The bus interface will not output any address recognition.

Data is entered with the most significant bit first. The leading 12 bits make up the data field, while the trailing 4 bits comprise the address. The first bit entered is p1, the last bit p16. The bits in the programming registers and addresses are arranged as shown in Table 1.

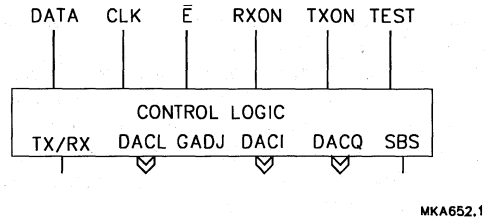


Fig.6 Block diagram, serial bus interface.

Table 1 Register bit allocation

REGISTER BIT ALLOCATION															
FIRST															**LAST**
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16
DATA FIELD												ADDRESS			
dt11	dt10	dt9	dt8	dt7	dt6	dt5	dt4	dt3	dt2	dt1	dt0	ad3	ad2	ad1	ad0
This register is reserved for test purposes and should not be programmed												0	0	0	0
X	X	X	X	sbs	X	X	X	X	hpn	srx	stx	0	0	0	1
ga3	ga2	ga1	ga0	X	X	lo5	lo4	lo3	lo2	lo1	lo0	0	0	1	0
ip5	ip4	ip3	ip2	ip1	ip0	qp5	qp4	qp3	qp2	qp1	qp0	0	0	1	1

Table 2 Bit allocation description

BIT	REMARKS	LOGIC		PRESET
stx	software transmit power-on	1 = power-up	0 = power-down	0
srx	software receive power-on	1 = power-up	0 = power-down	0
hpn	hardware priority not (selects if power status of blocks is controlled via hardware or software)	1 = soft priority	0 = hard priority	0
sbs	sideband select	1 = upper sideband selected	0 = lower sideband selected	0
ga3 to ga0	IF I channel gain adjustment			0111
lo5 to lo0	LO quadrature centre frequency adjustment			011111
ip5 to ip0	IF I channel phase adjustment			011111
qp5 to qp0	IF Q channel phase adjustment			011111
X	not used			

Table 3 details the different power-up modes of the circuit. Attention should be paid to the hpn-bit. This bit enables the RXON and TXON pins to take any logic position when software programming for power-up is used.

Table 3 Control of power status (note 1)

REGISTER BIT STATUS			EXTERNAL PIN LEVEL		CIRCUITS POWER STATUS	
hpn	**stx**	**srx**	**TXON**	**RXON**	**TRANSMIT**	**RECEIVE**
0	X	X	LOW	LOW	off	off
0	X	X	LOW	HIGH	off	on
0	X	X	HIGH	LOW	on	off
0	X	X	HIGH	HIGH	on (2)	on(2)
1	0	0	x	x	off	off
1	0	1	x	x	off	on
1	1	0	x	x	on	off
1	1	1	x	x	on(2)	on(2)

Notes

1. X = don't care; x = HIGH or LOW logic voltage level applied at designated pin.
2. Circuit is operative in this mode but specification is NOT guaranteed.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	v
ΔGND	difference in ground supply voltage applied between GND1 and GND2	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 4.8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CC1}, V_{CC2}, LOINA and LOINB						
V_{CC}	supply voltage	over full temperature range	4.5	4.8	5.3	V
I_{CCRX}	supply current	receive mode active; DC tested	26	31.5	38	mA
I_{CCTX}	supply current	transmit mode active; DC tested	10	12	14	mA
I_{CCPD}	supply current in power-down mode	DC tested	–	–	50	µA
Pins: CLK, DATA, $\overline{E}$, RXON, TXON and TEST						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	µA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	1.7	2.1	2.4	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	2.0	2.5	3.5	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	1.8	2.2	2.5	V
Pins: TXOIFA and TXOIFB						
V_O	DC output voltage level	transmit section enabled	2.5	2.9	3.4	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4.8 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RFI}	RF input impedance	balanced	–	200	–	Ω
f_{RFI}	RF input frequency		925	–	960	MHz
RL_{RF}	return loss on matched RF input impedance	note 1	15	20	–	dB
G_{CP}	conversion power gain	RF impedance to 1 IF output matched to 500 Ω	20	23	26	dB
		RF impedance to differential IF outputs matched to 1 kΩ differential	23	26	29	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.1	0.5	dB
ΔG/T	gain variation with temperature	note 2	–20	–15	–10	mdB/K
$CP1_{RX}$	1 dB input compression point	note 1	–26	–24.5	–	dBm
$IP2_{RX}$	2nd order intercept point referenced to the RF input	single-ended output; note 2	+15	+22	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF input differential	differential output; note 2	–	+32	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	–18	–15	–	dBm
F_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	4	5	dB
$Z_{L(IF)}$	typical application IF output load impedance	unbalanced	–	500	–	Ω
$C_{L(IF)}$	IF output load capacitance	unbalanced	–	–	2	pF
f_{IF}	IF frequency range	RF < LO	30	71	90	MHz
		RF > LO	30	45	50	MHz
f_{IR}	image frequency rejection	note 4	30	–	–	dB
f_{IRp}	image rejection at preset	superheterodyne; f_{IF} = 71 MHz; note 1	30	35	–	dB
Local oscillator section (receive section enabled)						
f_{LO}	LO input frequency		875	–	1050	MHz
Z_{LO}	LO input impedance	balanced	–	100	–	Ω
RL_{LO}	return loss on matched input (including standby mode)	note 2	10	15	–	dB
$P_{i(LO)}$	LO input power level		–7	–4	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section enabled)						
Z_O	TX IF output impedance		–	–	200	Ω
Z_L	TX IF load impedance		–	1000	–	Ω
C_L	maximum TX IF load capacitance		–	–	2	pF
$Z_{i(RF)}$	TX RF input impedance	balanced	–	200	–	Ω
f_{TXmix}	TX mixer input frequency		880	–	915	MHz
RL_{TX}	return loss on matched TX input	note 2	15	20	–	dB
G_{CP}	conversion power gain	from 200 Ω to 1 kΩ output	8	10	12	dB
$f_{o(TX)}$	TX mixer output frequency		40	–	200	MHz
$CP1_{TX}$	1 dB input compression point		–20	–15	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+20	–	dBm
$IP3_{TX}$	3rd order intercept point		–10	–7	–	dBm
F_{TX}	noise figure	double sideband; note 2	–	–	12	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2072M demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2072M demonstration board.
3. This value includes printed-circuit board and balun losses.
4. This value might be dependent upon control values sent by a microcontroller via the serial bus. This performance is maintained over the RF band for a fixed phase rotation control word.

TIMING CHARACTERISTICS

Typical values measured at V_{CC} = 4.8 V; T_{amb} = 25 °C; maximum value conditions under maximum clock speed; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial bus interface					
f_{clk}	clock frequency	–	–	13	MHz
Serial programming clock (pin CLK)					
t_r	rise time	–	10	40	ns
t_f	fall time	–	10	40	ns
T_{cy}	clock period	75	–	–	ns
Enable programming (pin $\overline{E}$)					
t_{START}	delay to rising edge of clock	30	–	–	ns
t_{END}	delay from last edge of clock	10	–	–	ns
t_W	minimum inactive pulse width	75	–	–	ns
t_{NEW}	delay from $\overline{E}$ inactive to new data	150	–	–	ns
Register serial input data (pin DATA)					
t_{su}	input data to CLK set-up time	20	–	–	ns
t_h	input data to CLK hold time	20	–	–	ns

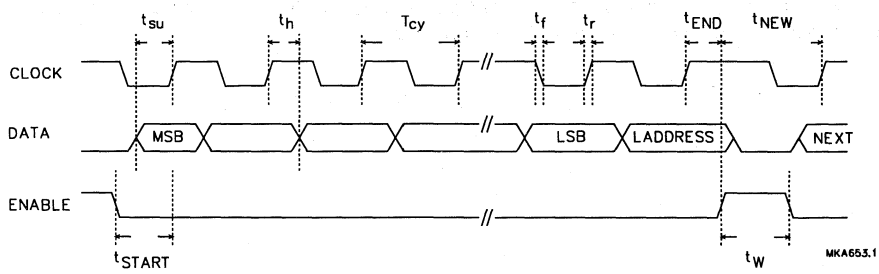


Fig.7 Serial bus timing diagram.

APPLICATION INFORMATION

Figure 8 illustrates the electrical diagram of the UAA2072M Philips demonstration board. All matching is to 50 Ω for measurement purposes. Different values will be used in a real application.

Component manufacturers

All surface mounted resistors and capacitors are manufactured by Philips Components. The small value capacitors are multi-layer ceramic with NPO dielectric.

The inductors are manufactured by Coilcraft UK.

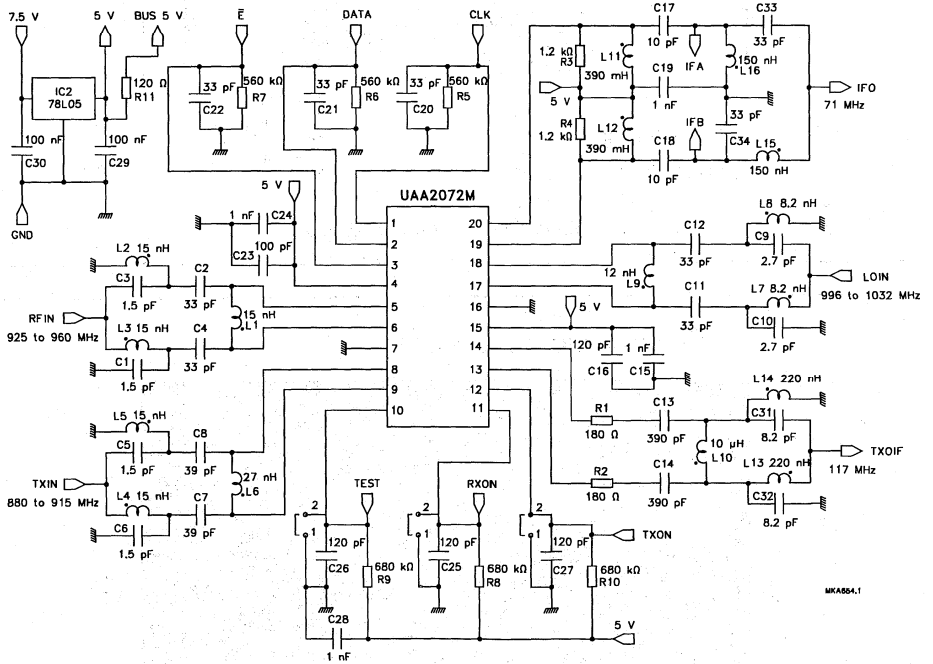


Fig.8 Application diagram.

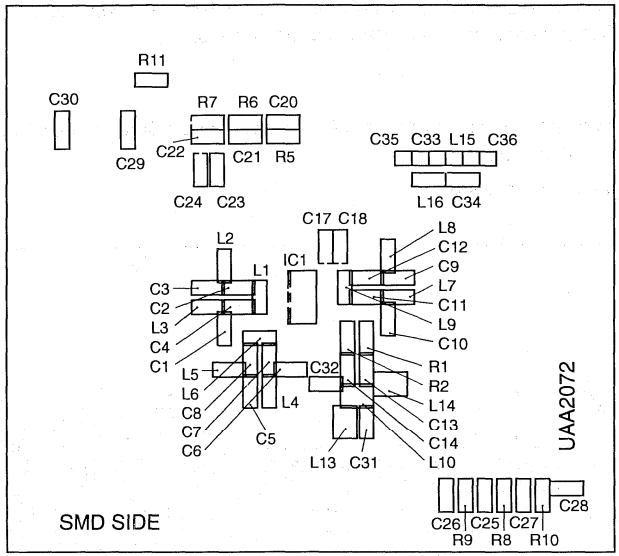


Fig.9 Printed-circuit board, SMD side.

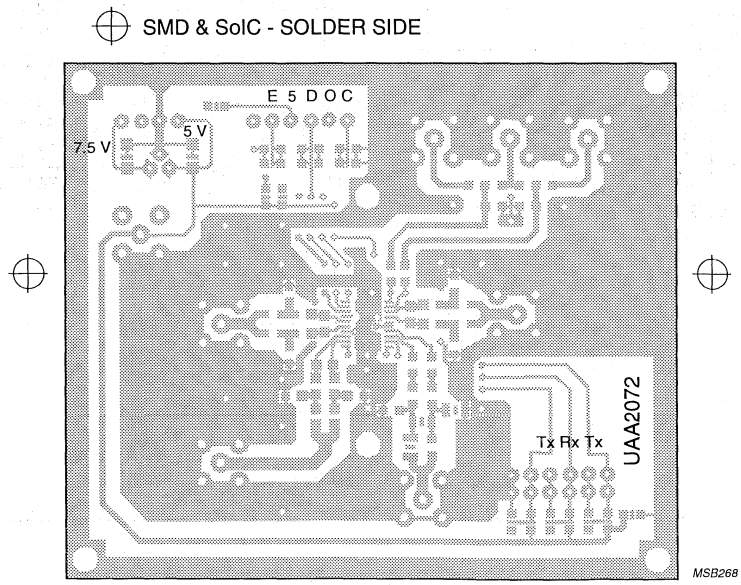


Fig.10 Printed-circuit board, SMD solder side.

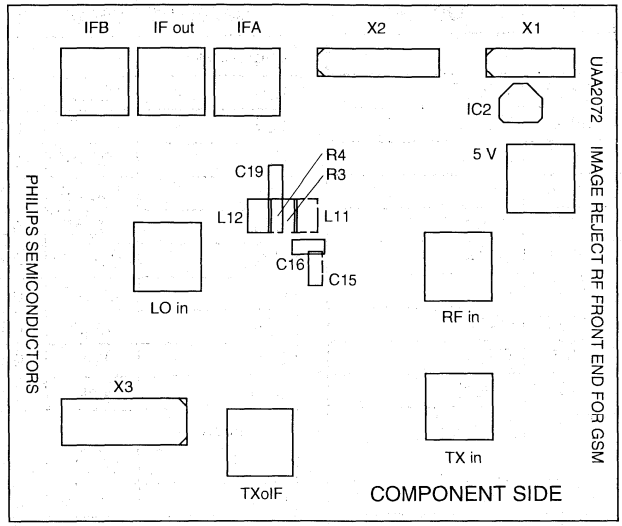


Fig.11 Printed-circuit board, component side for image reject RF front-end for GSM.

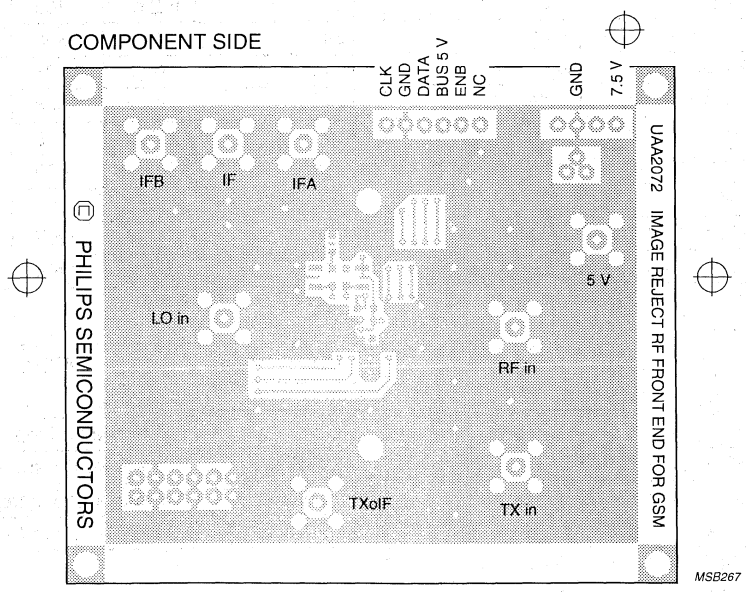


Fig.12 Printed-circuit board, component solder side for image reject RF front-end for GSM.

DEMONSTRATION BOARD - PARTS LIST

COMPONENT	VALUE	SIZE	LOCATION
Resistors			
R1	180 Ω	0805	TXOIF
R2	180 Ω	0805	TXOIF
R3	1.2 kΩ	0805	IF
R4	1.2 kΩ	0805	IF
R5	560 kΩ	0805	CLK
R6	560 kΩ	0805	DATA
R7	560 kΩ	0805	$\overline{E}$
R8	680 kΩ	0805	RXON
R9	680 kΩ	0805	TEST
R10	680 kΩ	0805	TXON
R11	120 Ω	0805	5 V BUS
Capacitors			
C1	1.5 pF	0805	RFIN
C2	33 pF	0805	RFIN
C3	1.5 pF	0805	RFIN
C4	33 pF	0805	RFIN
C5	1.5 pF	0805	TXIN
C6	1.5 pF	0805	TXIN
C7	39 pF	0805	TXIN
C8	39 pF	0805	TXIN
C9	2.7 pF	0805	LOIN
C10	2.7 pF	0805	LOIN
C11	33 pF	0805	LOIN
C12	33 pF	0805	LOIN
C13	390 pF	0805	TXOIF
C14	390 pF	0805	TXOIF
C15	1 nF	0805	V_{CC2}
C16	120 pF	0805	V_{CC2}
C17	10 pF	0805	IFO
C18	10 pF	0805	IFO
C19	1 nF	0805	IF / 5 V
C20	33 pF	0805	CLK
C21	33 pF	0805	DATA
C22	33 pF	0805	$\overline{E}$
C23	100 pF	0805	V_{CC1}
C24	1 nF	0805	V_{CC1}
C25	120 pF	0805	RXON
C26	120 pF	0805	TEST

COMPONENT	VALUE	SIZE	LOCATION
Capacitors			
C27	120 pF	0805	TXON
C28	1 nF	0805	5 V
C29	100 nF	1206	5 V regulator
C30	100 nF	1206	5 V regulator
C31	8.2 pF	0805	TXOIF
C32	8.2 pF	0805	TXOIF
C33	33 pF	0805	IFO
C34	33 pF	0805	IFO
C35	link	0805	IF/NOT USED
C36	link	0805	IF/NOT USED
Inductors			
L1	15 nH	0805	RFIN
L2	15 nH	0805	RFIN
L3	15 nH	0805	RFIN
L4	15 nH	0805	TXIN
L5	15 nH	0805	TXIN
L6	27 nH	0805	TXIN
L7	8.2 nH	0805	LOIN
L8	8.2 nH	0805	LOIN
L9	12 nH	0805	LOIN
L10	10 µH	1008	TXOIF/OPTIONAL
L11	390 nH	1008	IFO
L12	390 nH	1008	IFO
L13	220 nH	1008	TXOIF
L14	220 nH	1008	TXOIF
L15	150 nH	0805	IFO
L16	150 nH	0805	IFO

Other components

COMPONENT	DESCRIPTIONS
IC1	UAA2072M
IC2	5 V regulator; type 78L05
SMA/RIM	sockets for RF and IF inputs/outputs
SMB	5 V socket (optional, in place of IC2)
X1, X2 and X3	various 2.54 mm (0.1 inch) connectors

Image rejecting front-end for GSM applications

UAA2073M

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for at least 30 dB on-chip image rejection
- IF I/Q combination network for 50 to 90 MHz
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2073M contains both a receiver front-end and a high frequency transmit mixer intended to be used in the GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2073M is its ability to provide over 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne or supradyne reception. Image rejection is at an optimum when the IF is 71 MHz and local oscillator is above the wanted signal.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection.The IF driver has differential outputs of open-collector type.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The all-pass filters outputs are buffered before been fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced to reduce EMC issues.

Fast power-up switching is possible. A synthon mode enables LO buffers independent of the other circuits. When SYNTHON pin is high, all internal buffers on the LO path of the circuit are turned on, thus minimizing LO pulling when remainder of receive chain is powered-up.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	3.75	5.3	V
I_{CCRX}	receive supply current	–	26	–	mA
I_{CCTX}	transmit supply current	–	16	–	mA
I_{CCPD}	supply current in power-down	–	–	50	µA
T_{amb}	operating ambient temperature	−30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2073M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

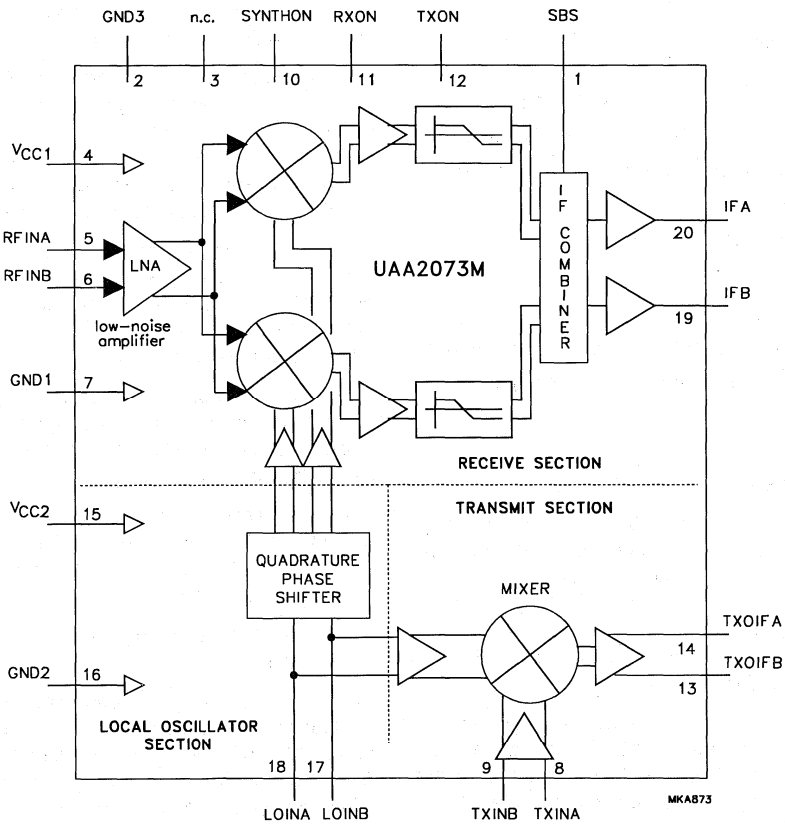


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SBS	1	sideband selection (LOW = LO > RF)
GND3	2	ground 3
n.c.	3	not connected
V_{CC1}	4	supply voltage for LNA, IF parts and TX mixer
RFINA	5	RF balance input A
RFINB	6	RF balance input B
GND1	7	ground 1 for receiver and transmitter mixer
TXINA	8	transmit mixer input A (balanced)
TXINB	9	transmit mixer input B (balanced)
SYNTHON	10	hardware power-on of internal LO buffer
RXON	11	hardware power-on for receive parts
TXON	12	hardware power-on for transmit mixer
TXOIFB	13	transmit mixer IF output B (balanced)
TXOIFA	14	transmit mixer IF output A (balanced)
V_{CC2}	15	supply voltage for LO parts
GND2	16	ground 2 for LO parts
LOINB	17	LO input B (balanced)
LOINA	18	LO input A (balanced)
IFB	19	IF output (balanced)
IFA	20	IF output (balanced)

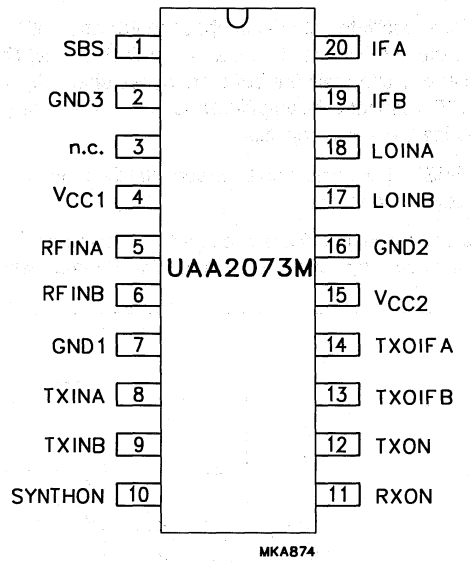


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin (SBS) allows selection between infradyne or supradyne reception.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 150 Ω, choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type, tuned for 71.3 MHz. Typical application will load the output with a differential 500 Ω load; i.e. a 500 Ω resistor load at each IF output, plus a 1 kΩ resistor to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

In the event of only one output being used, a 1 kΩ resistive load in parallel with a tuning inductor to V_{CC}, provides a matched 1 kΩ output to the external IF filter.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

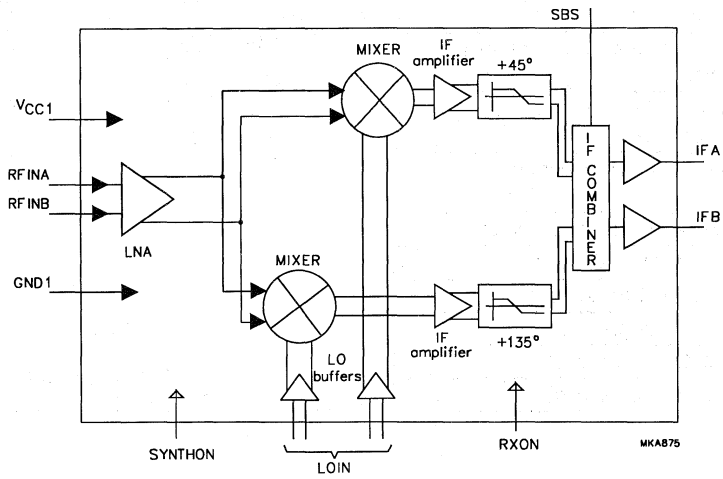


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The LO input impedance is 50 Ω differential.

A synthon mode is used to power-up the buffering on the LO inputs, minimizing the pulling effect on the external VCO when entering transmit or receive modes.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 kΩ load. The IF outputs are low impedance (common collector type).

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON.

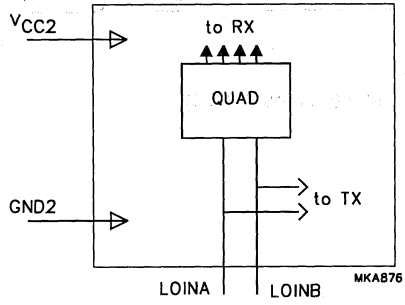


Fig.4 Block diagram, LO section.

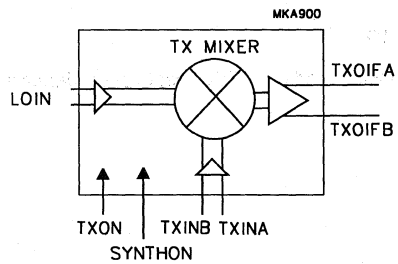


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SYNTHON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	receive section on
HIGH	LOW	LOW	transmit section on
LOW	LOW	HIGH	synthon on mode, transmit and receive LO buffers enabled
LOW	HIGH	HIGH	receive section on and synthon mode active
HIGH	LOW	HIGH	transmit section on and synthon mode active
HIGH	HIGH	LOW	receive and transmit sections on
HIGH	HIGH	HIGH	receive and transmit sections on

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between GND1 and GND2	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CC1}, V_{CC2}, LOINA and LOINB						
V_{CC}	supply voltage	over full temperature range	3.6	3.75	5.3	V
I_{CCRX}	supply current	receive mode active; DC tested	–	26	–	mA
I_{CCTX}	supply current	transmit mode active; DC tested	–	16	–	mA
I_{CCPD}	supply current in power-down mode	DC tested	–	–	50	µA
Pins: SYNTHON, RXON and TXON						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	µA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	1.7	2.1	2.4	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	2.0	2.5	3.5	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	1.8	2.2	2.5	V
Pins: TXOIFA and TXOIFB						
V_O	DC output voltage level	transmit section enabled	2.5	2.9	3.4	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RFI}	RF input impedance	balanced	–	150	–	Ω
f_{RFI}	RF input frequency		925	–	960	MHz
RL_{RF}	return loss on matched RF input impedance	note 1	15	20	–	dB
G_{CP}	conversion power gain	differential RF input to any IF output matched to 50 Ω	17	20	23	dB
		differential RF input to differential IF output matched to 1 kΩ differential	20	23	26	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.1	0.5	dB
ΔG/T	gain variation with temperature	note 2	−20	−15	−10	mdB/K
$CP1_{RX}$	1 dB input compression point	note 1	−24.5	−23.0	–	dBm
$IP2_{RX}$	2nd order intercept point referenced to the RF input	single-ended output; note 2	+22	–	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF input differential	differential output; note 2	–	+32	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	−18	−15	–	dBm
F_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	3.5	4.5	dB
$Z_{L(IF)}$	typical application IF output load impedance	unbalanced	–	250	–	Ω
$C_{L(IF)}$	IF output load capacitance	unbalanced	–	–	2	pF
f_{IF}	IF frequency range	RF < LO	50	71	90	MHz
		RF > LO	50	71	90	MHz
f_{IR}	image frequency rejection		30	–	–	dB
f_{IRp}	image rejection at preset	superheterodyne; f_{IF} = 71 MHz; note 1	30	35	–	dB
Local oscillator section (transmit and receive section enabled, SYNTHON = 1)						
f_{LO}	LO input frequency		850	–	1100	MHz
Z_{LO}	LO input impedance	balanced	–	50	–	Ω
RL_{LO}	return loss on matched input (including standby mode)	note 2	10	15	–	dB
$P_{i(LO)}$	LO input power level		−7	−4	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section enabled)						
Z_O	TX IF output impedance		–	–	200	Ω
Z_L	TX IF load impedance		–	100	–	Ω
C_L	maximum TX IF load capacitance		–	–	2	pF
$Z_{i(RF)}$	TX RF input impedance	balanced	–	200	–	Ω
f_{TXmix}	TX mixer input frequency		890	–	915	MHz
RL_{TX}	return loss on matched TX input	note 2	15	20	–	dB
G_{CP}	conversion power gain	from 200 Ω to 1 kΩ output	8	10	12	dB
$f_{o(TX)}$	TX mixer output frequency		40	–	200	MHz
$CP1_{TX}$	1 dB input compression point		–22	–17	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+20	–	dBm
$IP3_{TX}$	3rd order intercept point		–12	–9	–	dBm
F_{TX}	noise figure	double sideband; note 2	–	–	12	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2073M demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2073M demonstration board.
3. This value includes printed-circuit board and balun losses.

Image rejecting front-end for DECT applications

UAA2077AM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 30 dB on-chip image rejection
- IF I/Q combiner at 110 MHz
- On-chip quadrature network
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 1800 MHz front-end for DECT hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2077AM contains both a receiver front-end and a high frequency transmit mixer intended to be used in DECT mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077AM is its ability to provide over 25 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne or supradyne reception.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential outputs of open-collector type.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers.The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a low-noise amplifier, and a down-conversion mixer. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced.

Pins allow a selection of whether to reject the upper or lower image frequency and control of the different power-down modes. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.15	4.0	5.3	V
I_{CCRX}	receive supply current	22	27	33	mA
I_{CCTX}	transmit supply current	10	14	18	mA
I_{CCPD}	supply current in power-down	–	–	50	µA
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2077AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

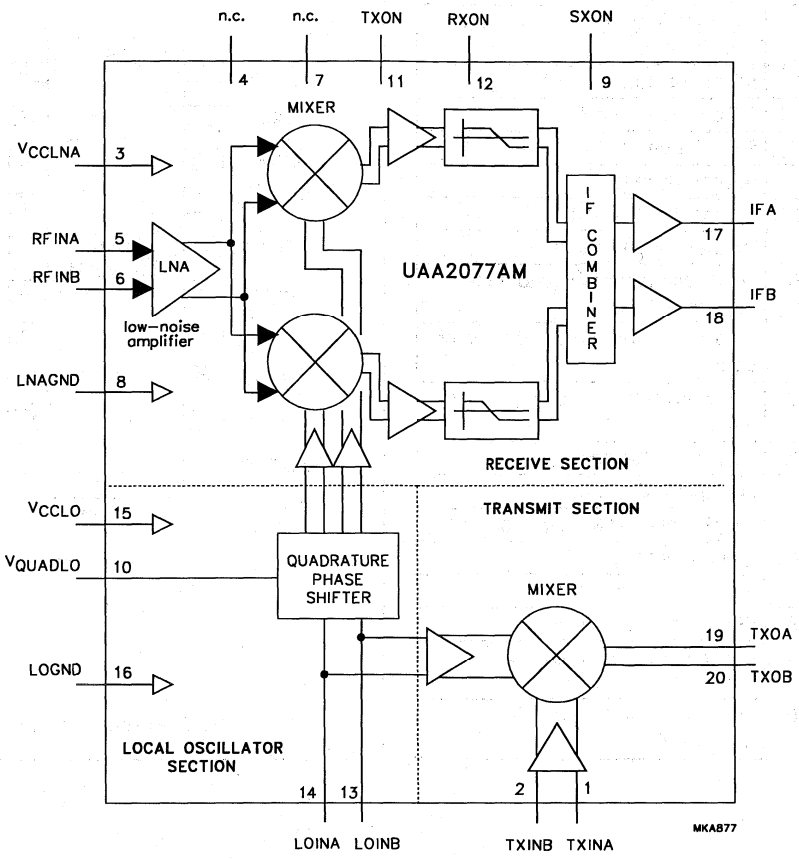


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXINA	1	transmit mixer input A (balanced)
TXINB	2	transmit mixer input B (balanced)
V_{CCLNA}	3	supply voltage for LNA, IF parts and TX mixer
n.c.	4	not connected
RFINA	5	RF balance input A
RFINB	6	RF balance input B
n.c.	7	not connected
LNAGND	8	ground for LNA parts
SXON	9	synthon mode enable
V_{QUADLO}	10	input voltage for LO quadrature trimming
TXON	11	hardware power-on of the transmit parts
RXON	12	hardware power-on of the receive parts
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
TXOIFA	19	transmit mixer IF output A (balanced)
TXOIFB	20	transmit mixer IF output B (balanced)

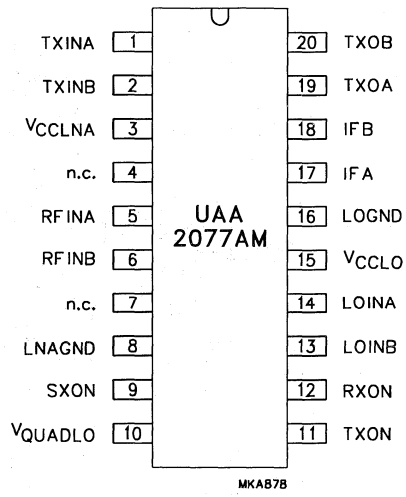


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 30 Ω, choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; i.e. a 1 kΩ resistor load at each IF output, plus a 2 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

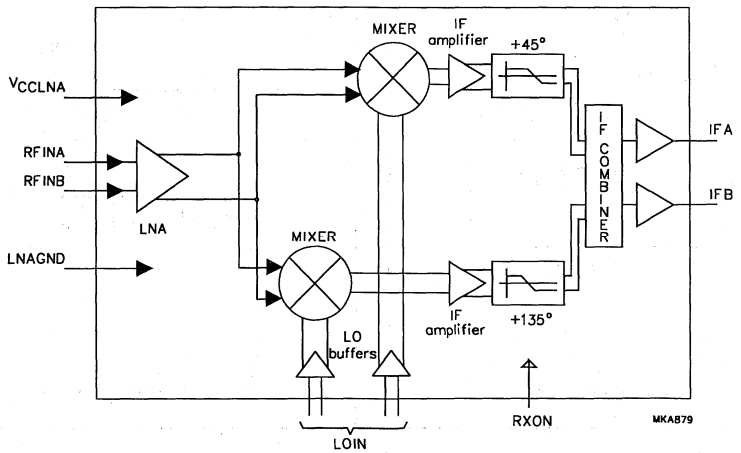


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by the voltage on pin V_{QUADLO}. This voltage trims the all-pass network to the selected LO frequency range. Over 30 dB of image rejection can be obtained by trimming at this point.

The LO input impedance is 35 Ω differential. A synthon mode is used to power-up all LO input buffers, thus minimizing the pulling effect on the external VCO when entering receive or transmit mode. This mode is active when SXON = 1.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF which is down-converted to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 30 Ω and a differential HIGH impedance output. The IF outputs are HIGH impedance (open-collector type); i.e. a 500 Ω resistor load at each IF output, plus a 1 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The mixer can also be used for frequency up-conversion.

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON.

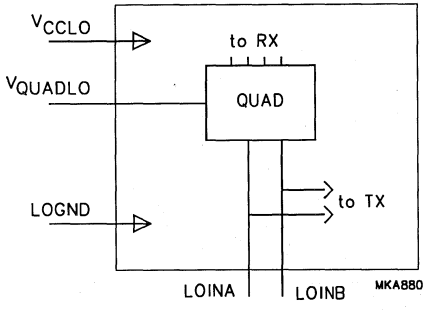


Fig.4 Block diagram, LO section.

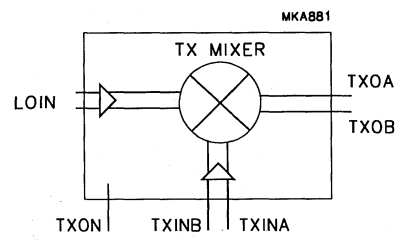


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SXON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	receive section on, infradyne reception
HIGH	LOW	LOW	transmit section on
LOW	LOW	HIGH	synthon on mode
LOW	HIGH	HIGH	receive section on and synthon mode active, infradyne reception
HIGH	LOW	HIGH	transmit section on and synthon mode active
HIGH	HIGH	LOW	receive section on supradyne reception
HIGH	HIGH	HIGH	receive section on and synthon mode active, supradyne reception

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	v
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CCLNA}, V_{CCLO}						
V_{CC}	supply voltage	over full temperature range	3.25	4.0	5.3	V
		T_{amb} between 5 and 50 °C	3.15	4.0	5.3	V
I_{CCRX}	supply current	receive mode active; DC tested	22	27	33	mA
I_{CCTX}	supply current	transmit mode active; DC tested	10	14	18	mA
I_{CCPD}	supply current in power-down mode	DC tested	–	–	50	µA
I_{CCSX}	supply current	synthon mode only	4	7	10	mA
I_{CCSRX}	supply current	receive and synthon mode active	–	29	–	mA
I_{CCSTX}	supply current	transmit and synthon mode active	–	18	–	mA
Pins: RXON, TXON and SXON						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	µA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	1.8	2.0	2.2	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	2.0	2.5	3.5	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	1.8	2.0	2.2	V
Pins: TXOIFA and TXOIFB						
I_O	DC output current	transmit section enabled	–	0.9	–	mA
Pins: LOINA and LOINB						
V_{LOIN}	DC input voltage level	RX, TX or SXON HIGH	–	3.3	–	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RFI}	RF input impedance	balanced at 1850 MHz	–	35	–	Ω
f_{RFI}	RF input frequency		1880	–	1900	MHz
RL_{RF}	return loss on matched RF input	balanced; note 1	11	15	–	dB
G_{CP}	conversion power gain	differential RF input to differential IF outputs loaded to 1 kΩ differential	17	20	23	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.1	–	dB
ΔG/T	gain variation with temperature	note 2	−20	−15	−10	mdB/K
$CP1_{RX}$	1 dB input compression point	note 1	−25	−22.5	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF input differential	differential output; note 2	–	tbf	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	−20	−17	–	dBm
F_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	4.3	5.0	dB
$Z_{L(IF)}$	typical application IF output load impedance	balanced	–	1	–	kΩ
RL_{IF}	return loss on matched IF output	balanced; note 1	11	15	–	dB
f_{IF}	IF frequency range	RF < LO	–	110	–	MHz
f_{IR}	image frequency rejection	V_{QUADLO} tuned	–	32	–	dB
IR	image rejection	infradyne; f_{IF} = 110 MHz; note 4	25	27	–	dB
Local oscillator section (receive section enabled)						
f_{LO}	LO input frequency		1770	–	2010	MHz
Z_{LO}	LO input impedance	balanced	–	35	–	Ω
RL_{LO}	return loss on matched input (including standby mode)	note 2	9	12	–	dB
$P_{i(LO)}$	LO input power level		−6	−3	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section enabled)						
Z_L	TX IF typical load impedance		–	500	–	Ω
RL_{TXIF}	return loss on matched transmitter IF output		11	15	–	dB
$Z_{i(RF)}$	TX RF input impedance	balanced	–	35	–	Ω
f_{TXmix}	TX mixer input frequency		1880	–	1900	MHz
RL_{TX}	return loss on matched TX input	note 2	10	15	–	dB
G_{CP}	conversion power gain	differential transmitter input to differential transmitter IF output loaded with 500 Ω differential	6	9	12	dB
$f_{o(TX)}$	TX mixer output frequency		50	–	150	MHz
$CP1_{TX}$	1 dB input compression point		–23	–20	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+22	–	dBm
$IP3_{TX}$	3rd order intercept point		–17	–14	–	dBm
F_{TX}	noise figure	double sideband; note 2	–	6	9	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	10	µs

Notes

1. Measured and guaranteed only on UAA2077AM demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2077AM demonstration board.
3. This value includes printed-circuit board and balun losses.
4. V_{QUADLO} open-circuit.

2 GHz image rejecting front-end UAA2077BM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 30 dB on-chip image rejection
- IF I/Q combiner at 188 MHz
- On-chip quadrature network
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 1800 MHz front-end for DCS1800 hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers e.g. PCS, RF-LANS.

GENERAL DESCRIPTION

UAA2077BM contains both a receiver front-end and a high frequency transmit mixer intended to be used in mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077BM is its ability to provide over 25 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne or supradyne reception.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers.The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a low-noise amplifier, and a down-conversion mixer. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced.

Pins allow a selection of whether to reject the upper or lower image frequency and control of the different power-down modes. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	4.0	5.3	V
I_{CCRX}	receive supply current	22	27	33	mA
I_{CCTX}	transmit supply current	10	14	18	mA
I_{CCPD}	supply current in power-down	–	–	50	µA
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2077BM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

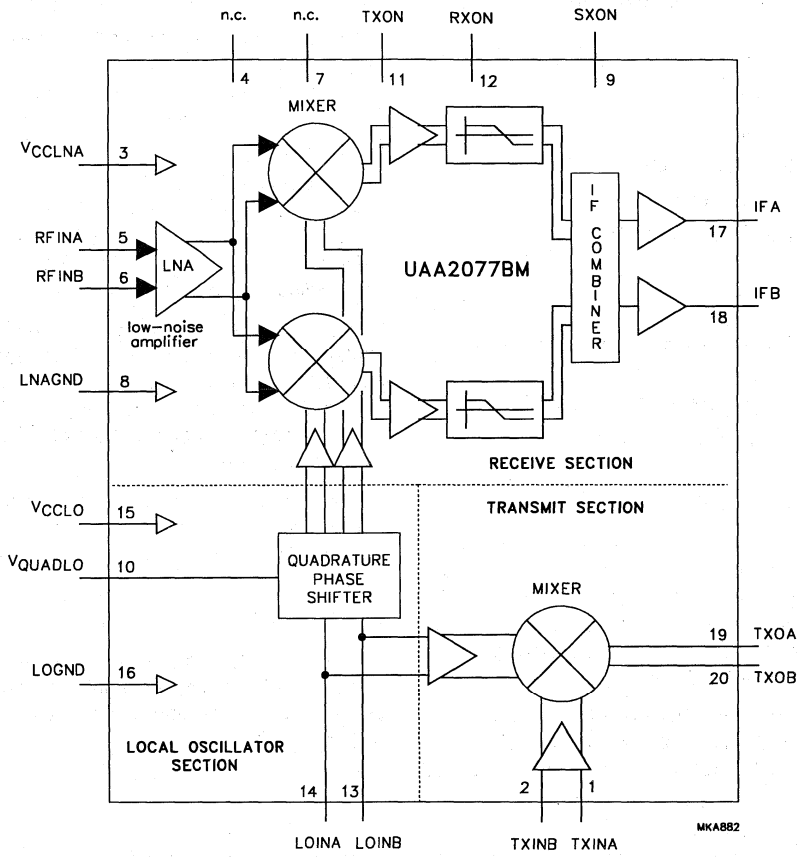


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXINA	1	transmit mixer input A (balanced)
TXINB	2	transmit mixer input B (balanced)
V_{CCLNA}	3	supply voltage for LNA, IF parts and TX mixer
n.c.	4	not connected
RFINA	5	RF balance input A
RFINB	6	RF balance input B
n.c.	7	not connected
LNAGND	8	ground for LNA parts
SXON	9	synthon mode enable
V_{QUADLO}	10	input voltage for LO quadrature trimming
TXON	11	hardware power-on of the transmit parts
RXON	12	hardware power-on of the receive parts
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
TXOIFA	19	transmit mixer IF output A (balanced)
TXOIFB	20	transmit mixer IF output B (balanced)

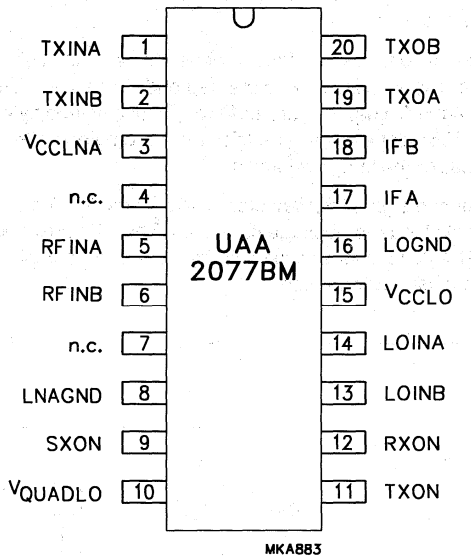


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 30 Ω, choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; i.e. a 1 kΩ resistor load at each IF output, plus a 2 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to V_{CC} + 3V_{be} or 3 diode forward voltage drops.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

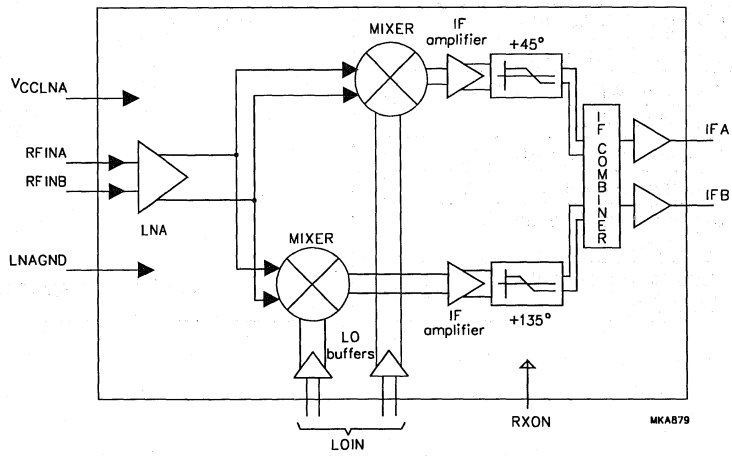


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by the voltage on pin V_{QUADLO}. This voltage trims the all-pass network to the selected LO frequency range. Over 30 dB of image rejection can be obtained by trimming at this point.

The LO input impedance is 35 Ω differential. A synthon mode is used to power-up all LO input buffers, thus minimizing the pulling effect on the external VCO when entering receive or transmit mode. This mode is active when SXON = 1.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF which is down-converted to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 30 Ω and a differential HIGH impedance output. The IF outputs are HIGH impedance (open-collector type); i.e. a 500 Ω resistor load at each IF output, plus a 1 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The mixer can also be used for frequency up-conversion.

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON.

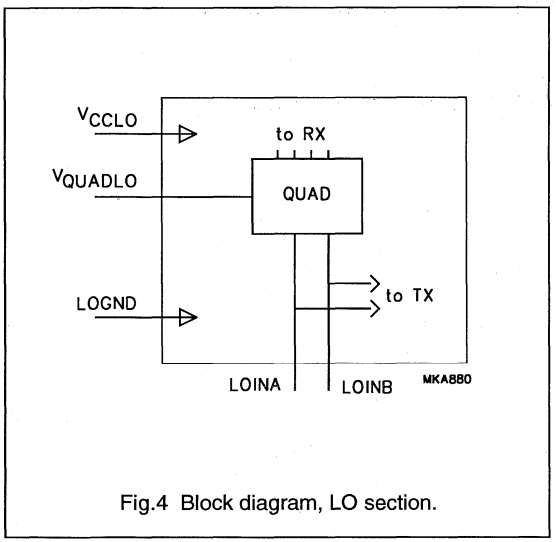


Fig.4 Block diagram, LO section.

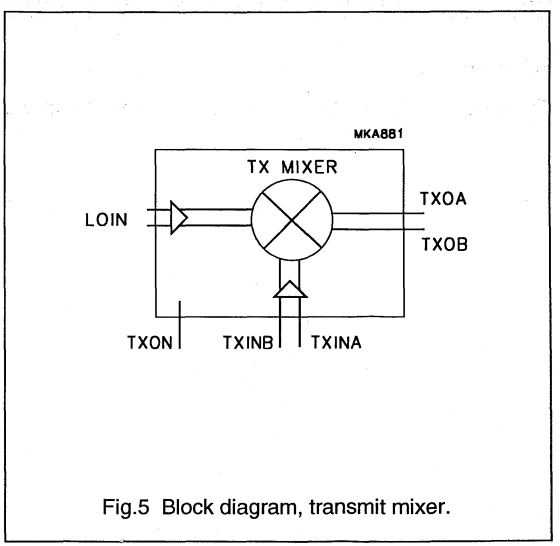


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SXON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	receive section on, infradyne reception
HIGH	LOW	LOW	transmit section on
LOW	LOW	HIGH	synthon mode
LOW	HIGH	HIGH	receive section on and synthon mode active, infradyne reception
HIGH	LOW	HIGH	transmit section on and synthon mode active
HIGH	HIGH	LOW	receive section on supradyne reception
HIGH	HIGH	HIGH	receive section on and synthon mode active, supradyne reception

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	v
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CCLNA}, V_{CCLO}						
V_{CC}	supply voltage	over full temperature range	3.6	4.0	5.3	V
I_{CCRX}	supply current	receive mode active; DC tested	22	27	33	mA
I_{CCTX}	supply current	transmit mode active; DC tested	10	14	18	mA
I_{CCPD}	supply current in power-down mode	DC tested	–	–	50	µA
I_{CCSX}	supply current	synthon mode only	4	7	10	mA
I_{CCSRX}	supply current	receive and synthon mode active	–	29	–	mA
I_{CCSTX}	supply current	transmit and synthon mode active	–	18	–	mA
Pins: RXON, TXON and SXON						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	µA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	1.8	2.0	2.2	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	2.0	2.5	3.5	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	1.8	2.0	2.2	V
Pins: TXOIFA and TXOIFB						
I_O	DC output current	transmit section enabled	–	0.9	–	mA
Pins: LOINA and LOINB						
V_{LOIN}	DC input voltage level	RX, TX or SXON HIGH	–	3.3	–	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RFI}	RF input impedance	balanced at 1850 MHz	–	35	–	Ω
f_{RFI}	RF input frequency		1800	–	2000	MHz
RL_{RF}	return loss on matched RF input	balanced; note 1	11	15	–	dB
G_{CP}	conversion power gain	differential RF input to differential IF outputs loaded to 1 kΩ differential	17	20	23	dB
G_{rip}	gain ripple as a function of RF frequency	between 1805 and 1880 MHz; note 2	–	0.1	–	dB
ΔG/T	gain variation with temperature	note 2	−20	−15	−10	mdB/K
$CP1_{RX}$	1 dB input compression point	note 1	−25	−22.5	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF input differential	differential output; note 2	–	tbf	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	−20	−17	–	dBm
F_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	4.3	5.0	dB
$Z_{L(IF)}$	typical application IF output load impedance	balanced	–	1	–	kΩ
RL_{IF}	return loss on matched IF input	balanced; note 1	11	15	–	dB
f_{IF}	IF frequency range	RF < LO	170	188	210	MHz
f_{IR}	image frequency rejection	V_{QUADLO} tuned	–	32	–	dB
IR	image rejection	infradyne; f_{IF} = 188 MHz; note 4	25	27	–	dB
Local oscillator section (receive section enabled)						
f_{LO}	LO input frequency		1600	–	2200	MHz
Z_{LO}	LO input impedance	balanced	–	35	–	Ω
RL_{LO}	return loss on matched input (including standby mode)	note 2	9	12	–	dB
$P_{i(LO)}$	LO input power level		−6	−3	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section enabled)						
Z_L	TX IF typical load impedance		–	500	–	Ω
RL_{TXIF}	return loss on matched transmitter IF input		11	15	–	dB
$Z_{i(RF)}$	TX RF input impedance	balanced at 1750 MHz	–	40	–	Ω
f_{TXmix}	TX mixer input frequency		1600	–	2000	MHz
RL_{TX}	return loss on matched TX input	note 2	10	15	–	dB
G_{CP}	conversion power gain	differential transmitter input to differential transmitter IF output loaded with 500 Ω differential	6	9	12	dB
$f_{o(TX)}$	TX mixer output frequency		50	–	400	MHz
$CP1_{TX}$	1 dB input compression point		–23	–20	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+22	–	dBm
$IP3_{TX}$	3rd order intercept point		–17	–14	–	dBm
F_{TX}	noise figure	double sideband; note 2	–	6	9	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2077BM demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2077BM demonstration board.
3. This value includes printed-circuit board and balun losses.
4. V_{QUADLO} open-circuit.

Zero IF front-end receiver for DECT applications

UAA2078M

FEATURES

- Balanced RF input
- Low noise amplifier
- Dual mixers
- 90 degree on-chip phase shifter; no adjustments
- AGC circuit
- RSSI function
- Power-down and standby modes
- Low power dissipation; 51 mW at V_{CC} = 3.0 V
- Low power supply voltage; >2.8 V.

APPLICATIONS

- Zero IF receiver for Digital European Cordless Telephone (DECT).

GENERAL DESCRIPTION

The UAA2078M is a low-power front-end for use with the UAA2079M baseband part in a zero IF DECT receiver. It converts a 1.9 GHz antenna input signal to two IF signals centred around a frequency of approximately zero. The phases of the two IF signals differ by 90 degrees.

The UAA2078M and 2079M chip-set is designed to meet the European Telecommunications Standards Institute (ETSI) ETS 300 175-2 specification.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	2.8	3.0	5.5	V
I_{CC}	supply current	–	17	19	mA
I_{CCSB}	supply current in standby mode	–	5.5	6.0	mA
I_{CCPD}	supply current in power-down mode	–	–	10	µA
T_{amb}	operating ambient temperature	–10	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2078M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

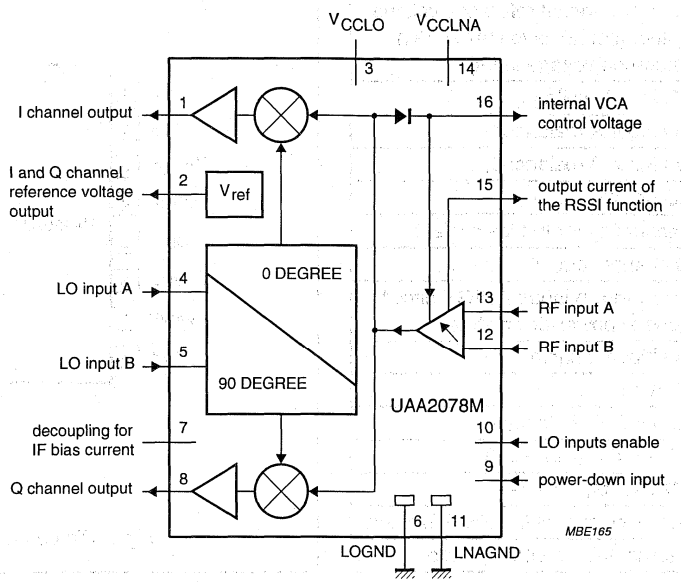


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
I_{out}	1	I channel output
V_{ref}	2	I and Q channel reference voltage output (connects to UAA2079M reference voltage input)
V_{CCLO}	3	LO supply voltage
LOINA	4	LO input A (balanced)
LOINB	5	LO input B (balanced)
LOGND	6	LO ground
BIASIF	7	decoupling for IF bias current
Q_{out}	8	Q channel output
PD	9	power-down input; if HIGH circuit goes to power-down state
LOEN	10	LO inputs enable
LNAGND	11	LNA ground
RFINB	12	RF input B (balanced)
RFINA	13	RF input A (balanced)
V_{CCLNA}	14	LNA supply voltage
I_{RSSI}	15	output current of the RSSI function
V_{AGC}	16	internal VCA control voltage

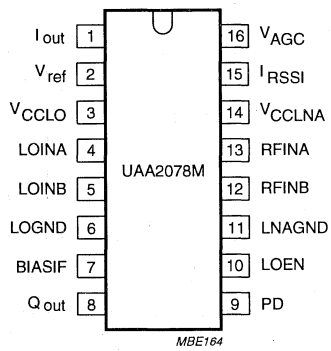


Fig.2 Pin configuration.

Zero IF baseband receiver for DECT applications

UAA2079M

FEATURES

- Single-chip IF
- No off-chip filters
- Low component count
- No adjustments
- High dynamic range
- Low power
- 3 V operation
- Built-in power-down mode.

GENERAL DESCRIPTION

The UAA2079M is a low-power, integrated IF strip, demodulator and data slicer, designed for Digital European Cordless Telephone (DECT) applications. It features fully integrated channel selectivity filters, requiring only one off-chip resistor to set the frequency. The IC provides analog Receiver Signal Strength Indicator (RSSI) and CMOS compatible data outputs, for interfacing to a burst mode controller. The circuit can be fully powered-down during the idle locked state, to save power. An additional feature includes a data filter between demodulator and slicer, to improve bit error rate (BER).

APPLICATIONS

- DECT zero IF baseband receiver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.8	–	5.5	V
I_{CC}	supply current	note 1	–	10	–	mA
I_{CCPD}	supply current in power-down mode	note 2	–	–	25	µA
IPR	input reference voltage		V_{CC} – 1.55	V_{CC} – 1.50	V_{CC} – 1.45	V
$I_{I(I)}$	I-channel input current		–40	–	+40	µA
$I_{I(Q)}$	Q-channel input current		–40	–	+40	µA
T_{amb}	operating ambient temperature		–10	–	+70	°C

Notes

1. Current consumption depends on the values of the external resistors R_t and R_d.
2. Power-down current depends on the time after power-down and should decrease to 0 µA. The maximum limit is mentioned for test purposes only.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2079M	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

Zero IF baseband receiver for DECT applications

UAA2079M

BLOCK DIAGRAM

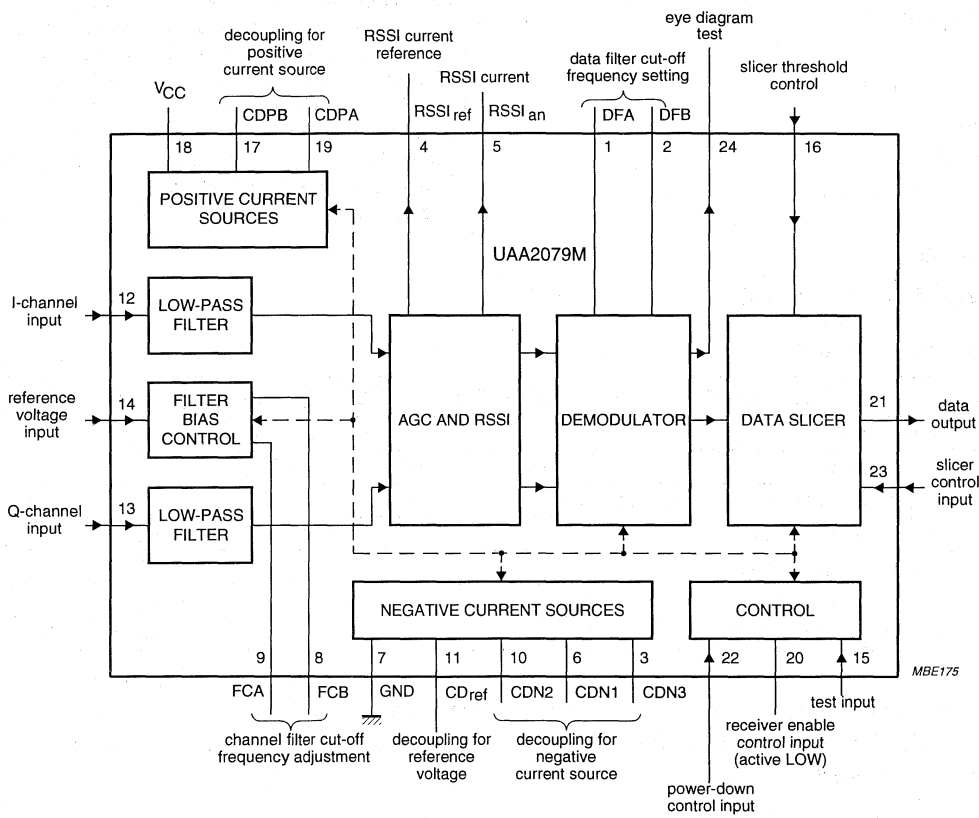


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DFA	1	data filter cut-off frequency setting A (one resistor)
DFB	2	data filter cut-off frequency setting B (one resistor)
CDN3	3	decoupling for negative current source 3
$RSSI_{ref}$	4	full range RSSI current reference output
$RSSI_{an}$	5	analog RSSI current output
CDN1	6	decoupling for negative current source 1
GND	7	negative supply
FCB	8	channel filter cut-off frequency adjustment B (one resistor)
FCA	9	channel filter cut-off frequency adjustment A (one resistor)
CDN2	10	decoupling for negative current source 2
CD_{ref}	11	decoupling for reference voltage
IPI	12	I-channel input
IPQ	13	Q-channel input
IPR	14	reference voltage input
TEST	15	test input
FP	16	slicer threshold control input (Fixed or Portable)
CDPB	17	decoupling for positive current source B
V_{CC}	18	supply voltage
CDPA	19	decoupling for positive current source A
$\overline{ENABLE}$	20	receiver enable control input (active LOW)
DATA	21	data output
PD	22	power-down control input
SLCCTRL	23	slicer control input
MONITOR	24	eye diagram test output

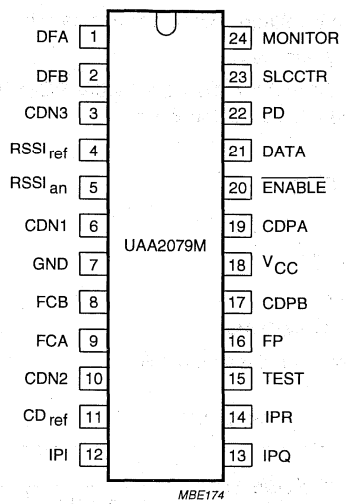


Fig.2 Pin configuration.

Advanced pager receiver UAA2080

FEATURES

- Wide frequency range: VHF, UHF and 900 MHz bands
- High sensitivity
- High dynamic range
- Electronically adjustable filters on chip
- Suitable for data rates up to 2400 bits/s
- Wide frequency offset and deviation range
- Fully POCSAG compatible FSK receiver
- Power on/off mode selectable by the chip enable input
- Low supply voltage; low power consumption
- High integration level
- Interfaces directly to the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.

APPLICATIONS

- Wide area paging
- On-site paging
- Telemetry
- RF security systems
- Low bit-rate wireless data links.

GENERAL DESCRIPTION

The UAA2080 is a high-performance low-power radio receiver circuit primarily intended for VHF, UHF and 900 MHz pager receivers for wide area digital paging systems, employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK).

The receiver design is based on the direct conversion principle where the input signal is mixed directly down to the baseband by a local oscillator on the signal frequency. Two complete signal paths with signals of 90° phase difference are required to demodulate the signal. All channel selectivity is provided by the built-in IF filters. The circuit makes extensive use of on-chip capacitors to minimize the number of external components.

The UAA2080 was designed to operate together with the PCA5000A, PCF5001 or PCD5003 POCSAG decoders, which contain a digital input filter for optimum call success rate.

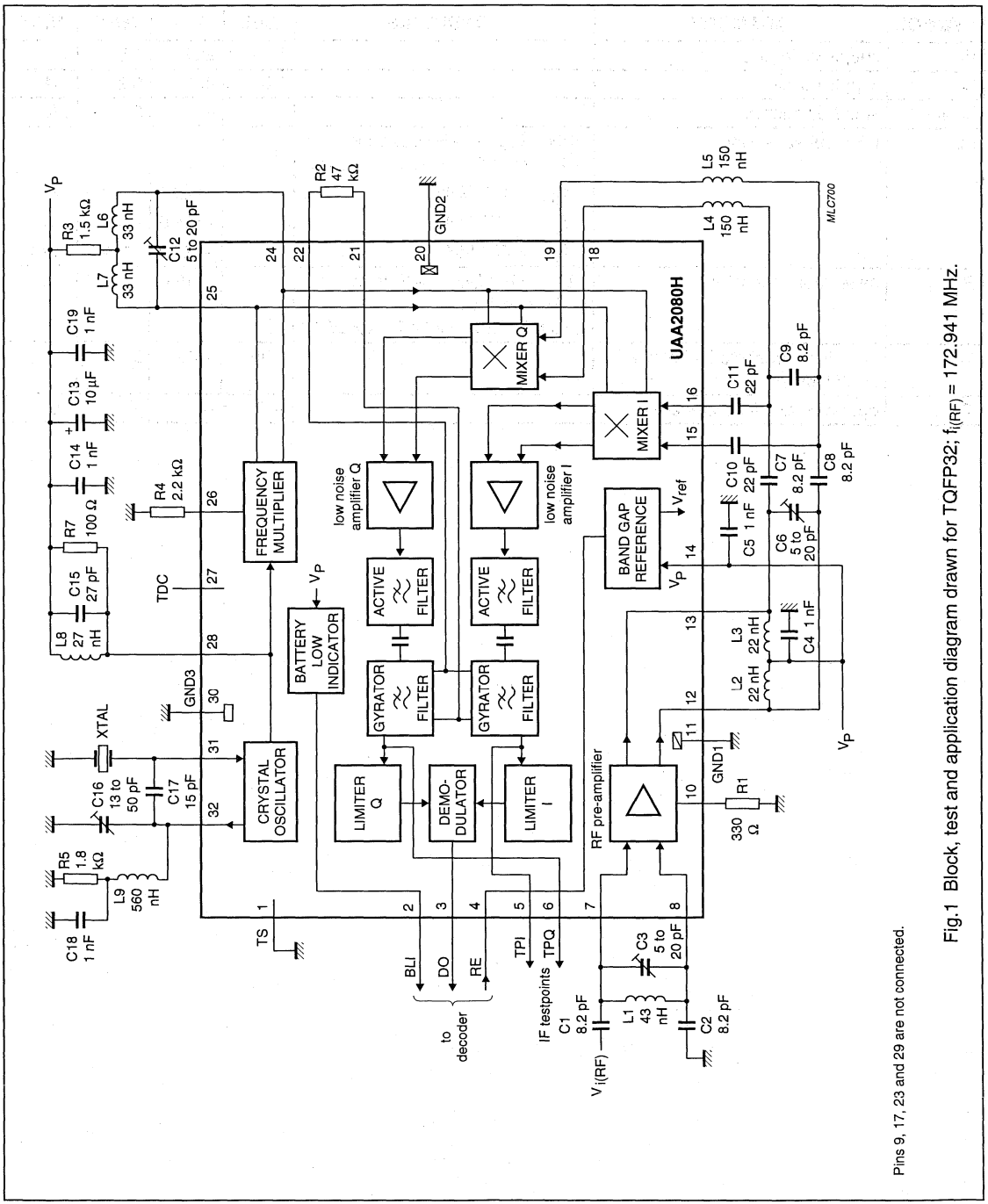
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2080H	TQFP32	plastic thin quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-2
UAA2080T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UAA2080U	28 pads	naked die; see Fig.9	

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current		2.3	2.7	3.2	mA
$I_{P(off)}$	stand-by current		–	–	3	µA
$P_{i(ref)}$	RF input sensitivity	BER ≤ $^3/_{100}$; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C				
		$f_{i(RF)}$ = 173 MHz	–	−126.5	−123.5	dBm
		$f_{i(RF)}$ = 470 MHz	–	−124.5	−121.5	dBm
		$f_{i(RF)}$ = 930 MHz	–	−120.0	−114.0	dBm
$P_{i(mix)}$	mixer input sensitivity	BER ≤ $^3/_{100}$; $f_{i(RF)}$ = 470 MHz; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C	–	−115.0	−110.0	dBm
V_{th}	detection threshold for battery LOW indicator		1.95	2.05	2.15	V
T_{amb}	operating ambient temperature		−10	–	+70	°C

BLOCK AND TEST DIAGRAMS (173 MHz)



Pins 9, 17, 23 and 29 are not connected.

Fig.1 Block, test and application diagram drawn for TQFP32; $f_{i(RF)}$ = 172.941 MHz.

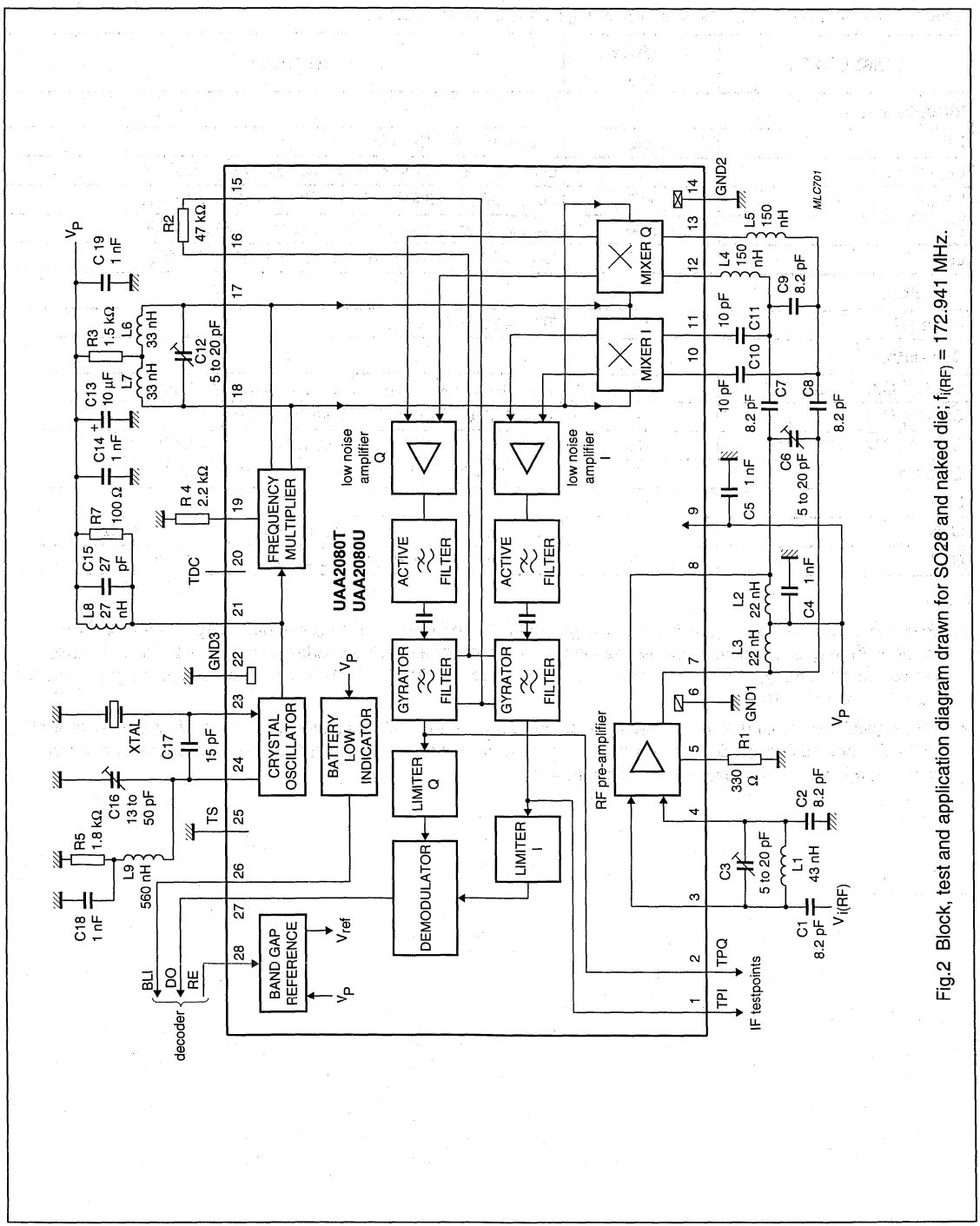


Fig.2 Block, test and application diagram drawn for SO28 and naked die; $f_{i(RF)}$ = 172.941 MHz.

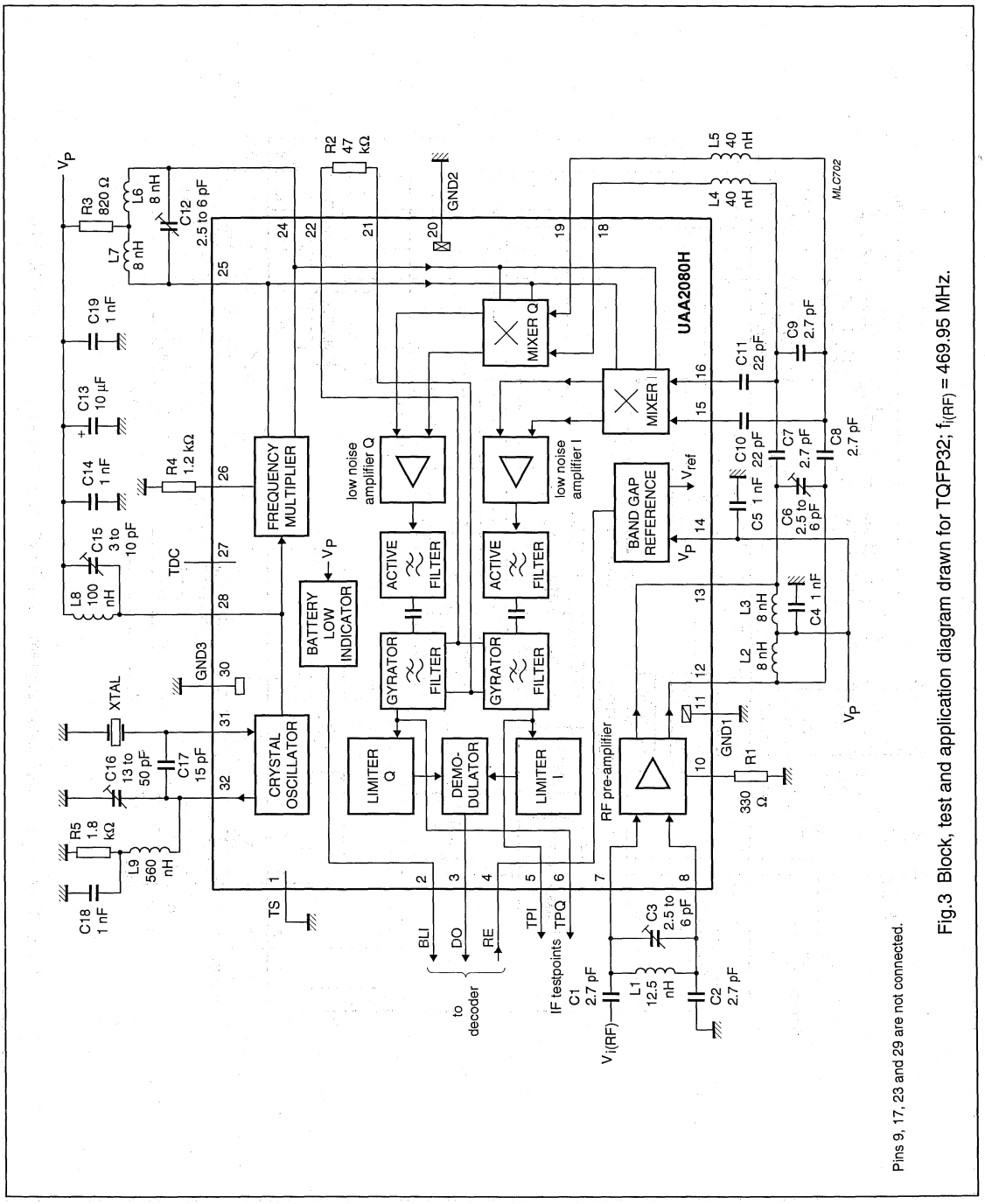
Table 1 Tolerances of components shown in Figs 1 and 2 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±5	Q_{min} = 100 at 173 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±20	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 30 at 57 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R7	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12	–	TC = (–750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18, C19	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (–1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 57.647 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF series capacitor at 25 °C), dynamic resistance R1 < 40 Ω, Δf = ±5 × 10^{-6} for T_{amb} = –10 to +55 °C with 25 °C reference, calibration plus aging tolerance: –5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAMS (470 MHz)



Pins 9, 17, 23 and 29 are not connected.

Fig.3 Block, test and application diagram drawn for TQFP32; $f_{i(RF)}$ = 469.95 MHz.

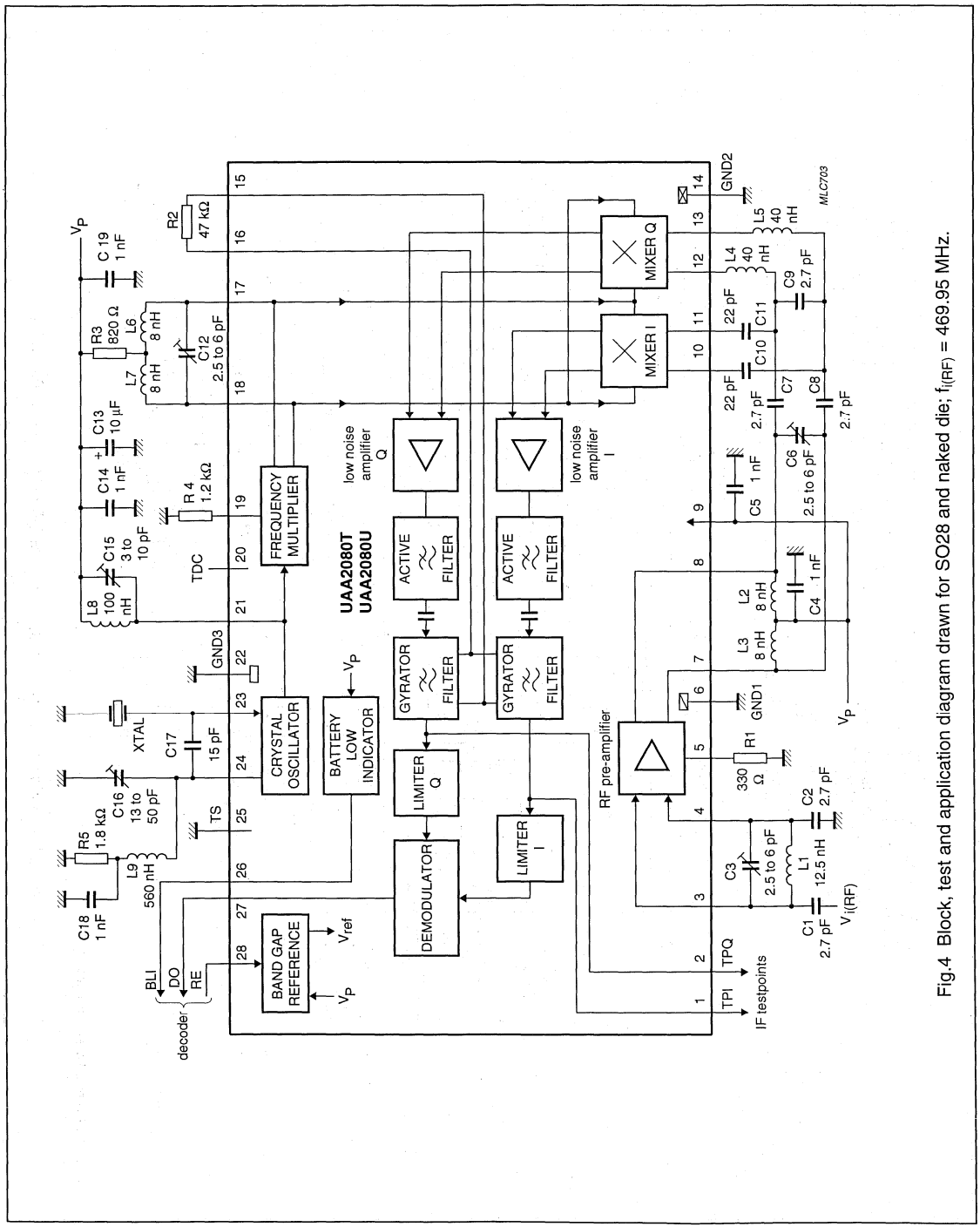


Fig.4 Block, test and application diagram drawn for SO28 and naked die; $f_{i(RF)}$ = 469.95 MHz.

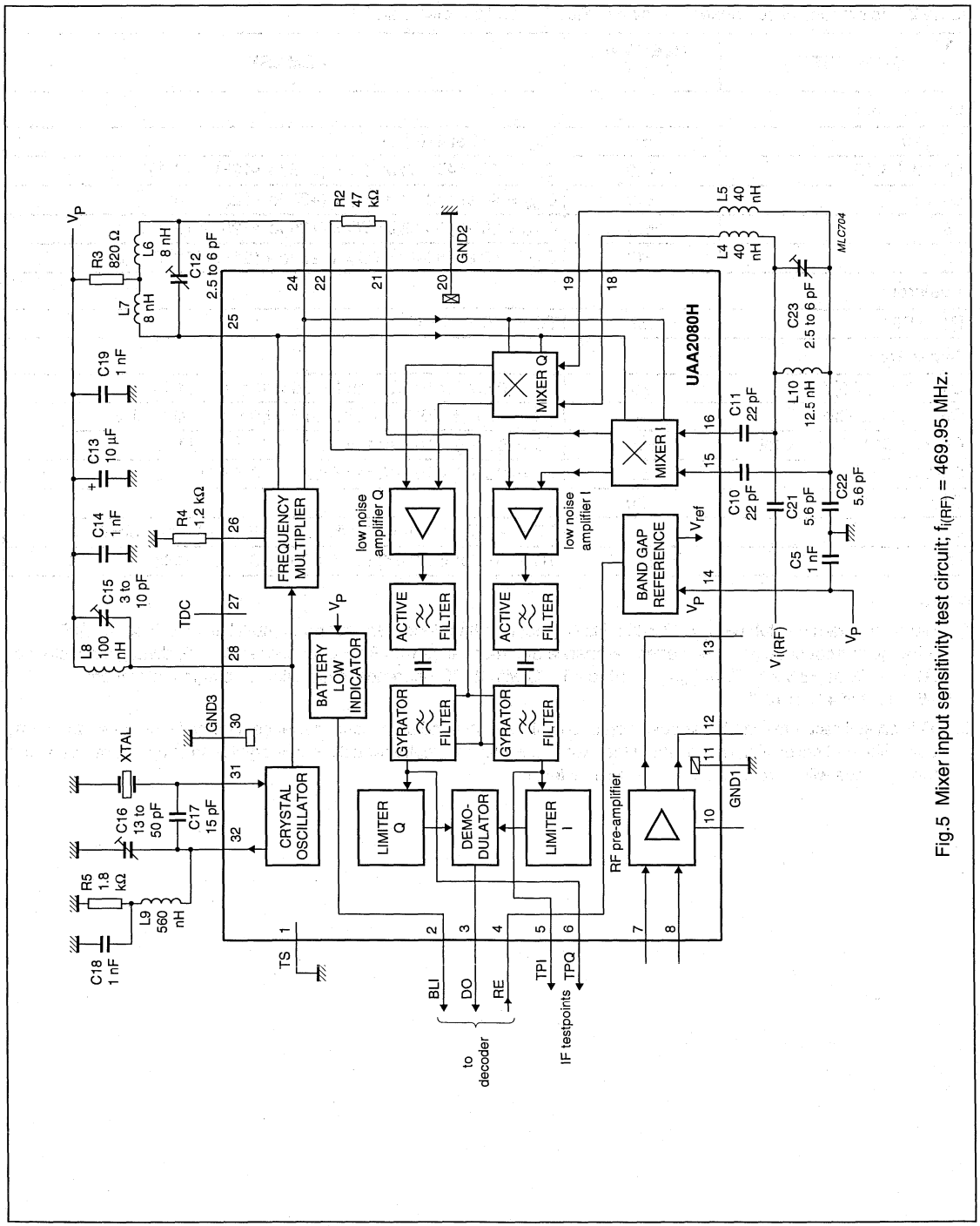


Fig.5 Mixer input sensitivity test circuit; $f_{i(RF)}$ = 469.95 MHz.

Table 2 Tolerances of components shown in Figs 3, 4 and 5 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1, L10	±5	Q_{min} = 145 at 470 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 40 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±10	Q_{min} = 30 at 156 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 40 at 78 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R5	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12, C23	–	TC = (–750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18 to C22	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (–1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 78.325 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF capacitor at 25 °C), dynamic resistance R1 < 30 Ω, Δf = ±5 × 10^{-6} for T_{amb} = –10 to +55 °C with 25 °C reference, calibration plus aging tolerance: –5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAM (930 MHz)

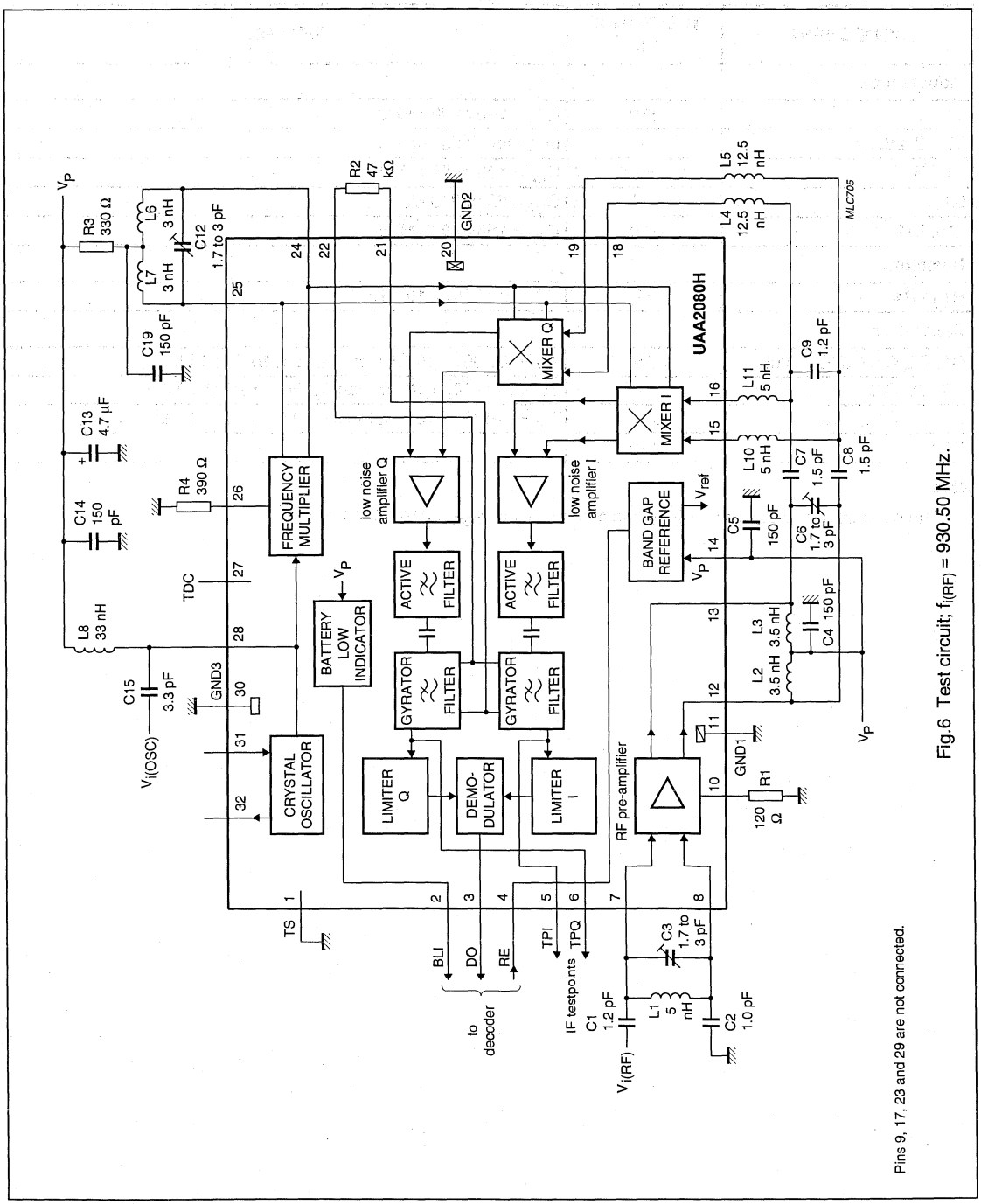


Fig.6 Test circuit; $f_{i(RF)}$ = 930.50 MHz.

Table 3 Tolerances of components shown in Fig.6 (note 1)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±10	Q_{typ} = 150 at 930 MHz
L2, L3, L6, L7	–	microstrip inductor
L4, L5	±5	Q_{typ} = 100 at 930 MHz
L8	±10	Q_{typ} = 65 at 310 MHz
L10, L11	±10	Q_{typ} = 150 at 930 MHz
Resistors		
R1 to R4	±2	TC = (0 ±200) × 10^{-6}/K;
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz
C3, C6, C12	–	TC = (0 ±200) × 10^{-6}/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz
C4, C5, C14, C19	±10	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 10 \times 10^{-4}$ at 1 MHz
C13	±20	

Note

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz.

PINNING (TQFP32)

SYMBOL	PIN	DESCRIPTION
TS	1	test switch; connection to ground for normal operation
BLI	2	battery LOW indicator output
DO	3	data output
RE	4	receiver enable input
TPI	5	IF test point; I channel
TPQ	6	IF test point; Q channel
VI1RF	7	pre-amplifier RF input 1
VI2RF	8	pre-amplifier RF input 2
n.c.	9	not connected
RRFA	10	external emitter resistor for pre-amplifier
GND1	11	ground 1 (0 V)
VO2RF	12	pre-amplifier RF output 2
VO1RF	13	pre-amplifier RF output 1
V_P	14	supply voltage
VI2MI	15	I channel mixer input 2
VI1MI	16	I channel mixer input 1
n.c.	17	not connected
VI1MQ	18	Q channel mixer input 1
VI2MQ	19	Q channel mixer input 2
GND2	20	ground 2 (0 V)
COM	21	gyrator filter resistor; common line
RGYR	22	gyrator filter resistor
n.c.	23	not connected
VO1MUL	24	frequency multiplier output 1
VO2MUL	25	frequency multiplier output 2
RMUL	26	external emitter resistor for frequency multiplier
TDC	27	DC test point; no external connection for normal operation
OSC	28	oscillator collector
n.c.	29	not connected
GND3	30	ground 3 (0 V)
OSB	31	oscillator base; crystal input
OSE	32	oscillator emitter

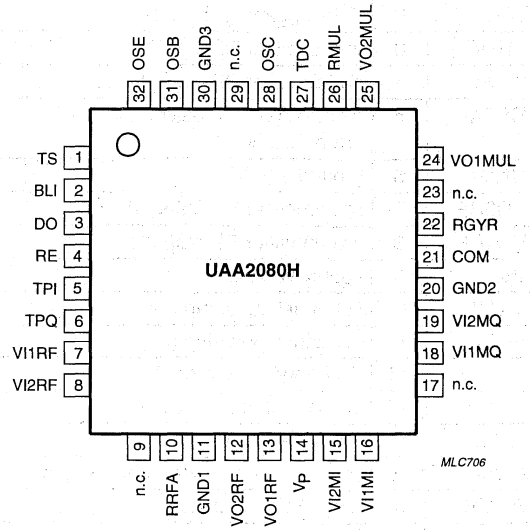


Fig.7 Pin configuration; TQFP32.

PINNING (SO28)

SYMBOL	PIN	DESCRIPTION
TPI	1	IF test point; I channel
TPQ	2	IF test point; Q channel
VI1RF	3	pre-amplifier RF input 1
VI2RF	4	pre-amplifier RF input 2
RRFA	5	external emitter resistor for pre-amplifier
GND1	6	ground 1 (0 V)
VO2RF	7	pre-amplifier RF output 2
VO1RF	8	pre-amplifier RF output 1
V_P	9	supply voltage
VI2MI	10	I channel mixer input 2
VI1MI	11	I channel mixer input 1
VI1MQ	12	Q channel mixer input 1
VI2MQ	13	Q channel mixer input 2
GND2	14	ground 2 (0 V)
COM	15	gyrator filter resistor; common line
RGYR	16	gyrator filter resistor
VO1MUL	17	frequency multiplier output 1
VO2MUL	18	frequency multiplier output 2
RMUL	19	external emitter resistor for frequency multiplier
TDC	20	DC test point; no external connection for normal operation
OSC	21	oscillator collector
GND3	22	ground 3 (0 V)
OSB	23	oscillator base; crystal input
OSE	24	oscillator emitter
TS	25	test switch; connection to ground for normal operation
BLI	26	battery LOW indicator output
DO	27	data output
RE	28	receiver enable input

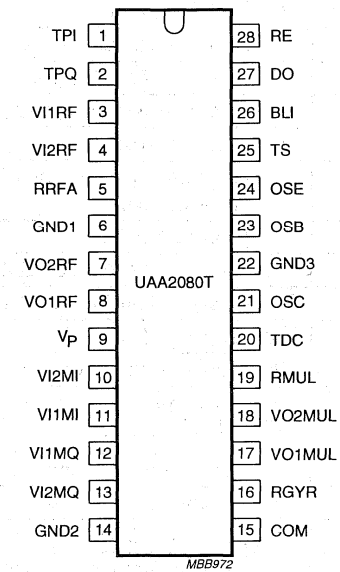
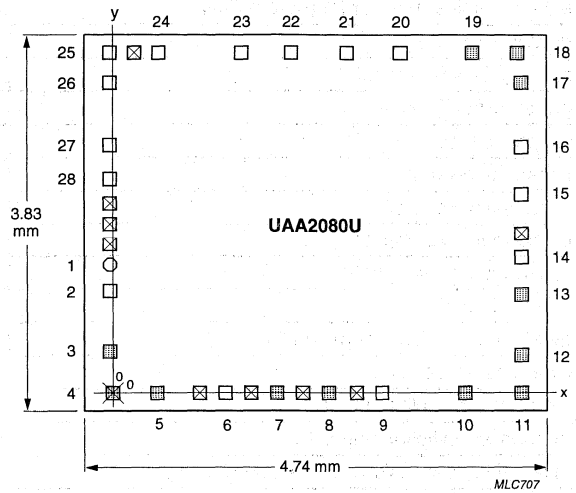


Fig.8 Pin configuration; SO28.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

See Table 4 for bonding pad description and locations for x/y co-ordinates.



Where:

- ○ Pad number 1 (diameter 124 µm)
- □ Pad 124 µm x 124 µm
- ⊠ Pad not used
- ▨ Pad 100 µm x 100 µm
- ⊠ Pad 100 µm x 100 µm with reference point

Chip area: 18.15 mm^2.
Chip thickness: 380 ±20 µm.
Drawing not to scale.

Fig.9 Bonding pad locations.

Table 4 Bonding pad centre locations (dimensions in μm)

SYMBOL	PAD	DESCRIPTION	x	y
TPI	1	IF test point; I channel	−32	1296
TPQ	2	IF test point; Q channel	−32	1000
VI1RF	3	pre-amplifier RF input 1	−32	360
VI2RF	4	pre-amplifier RF input 2; note 1	0	0
RRFA	5	external emitter resistor for pre-amplifier	472	0
GND1	6	ground 1 (0 V)	1160	0
VO2RF	7	pre-amplifier RF output 2	1688	0
VO1RF	8	pre-amplifier RF output 1	2232	0
V_P	9	supply voltage	2760	0
VI2MI	10	I channel mixer input 2	3608	0
VI1MI	11	I channel mixer input 1	4216	0
VI1MQ	12	Q channel mixer input 1	4216	360
VI2MQ	13	Q channel mixer input 2	4216	960
GND2	14	ground 2 (0 V)	4216	1360
COM	15	gyrator filter resistor; common line	4216	2024
RGYR	16	gyrator filter resistor	4216	2496
VO1MUL	17	frequency multiplier output 1	4216	3136
VO2MUL	18	frequency multiplier output 2	4176	3456
RMUL	19	external emitter resistor for frequency multiplier	3668	3458
SENSE	20	battery LOW detector sense input	2952	3456
OSC	21	oscillator collector	2312	3456
GND3	22	ground 3 (0 V)	1832	3456
OSB	23	oscillator base; crystal input	1328	3456
OSE	24	oscillator emitter	432	3456
TS	25	test switch; connection to ground for normal operation	−32	3456
BLI	26	battery LOW indicator output	−32	3136
DO	27	data output	−32	2512
RE	28	receiver enable input	−32	2152
		lower left corner of chip (typical values)	−278	−186

Note

1. All x/y co-ordinates are referenced to the centre of pad 4 (VI2RF); see Fig.9.

INTERNAL CIRCUITS

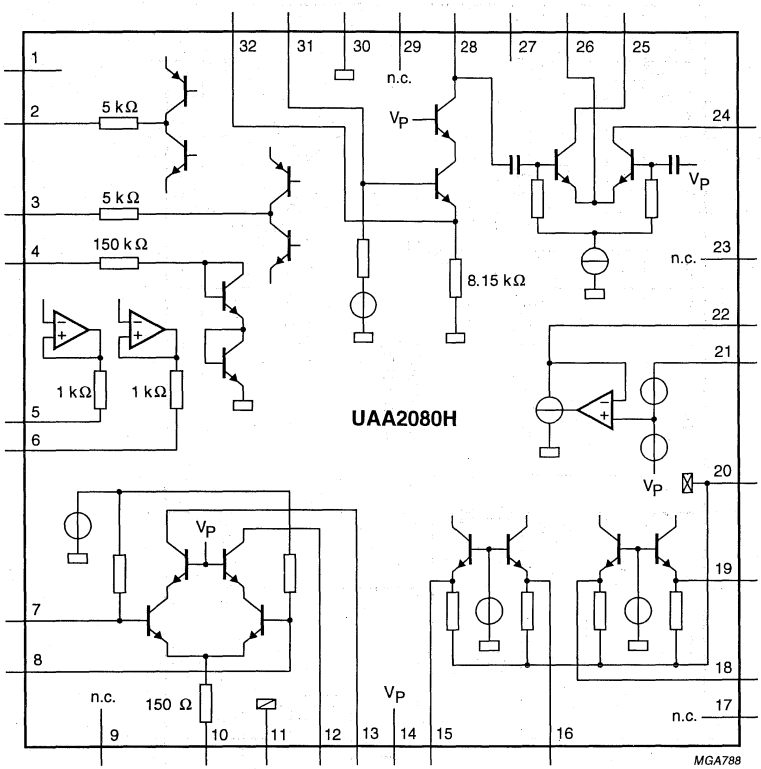


Fig.10 Internal circuits drawn for TQFP32.

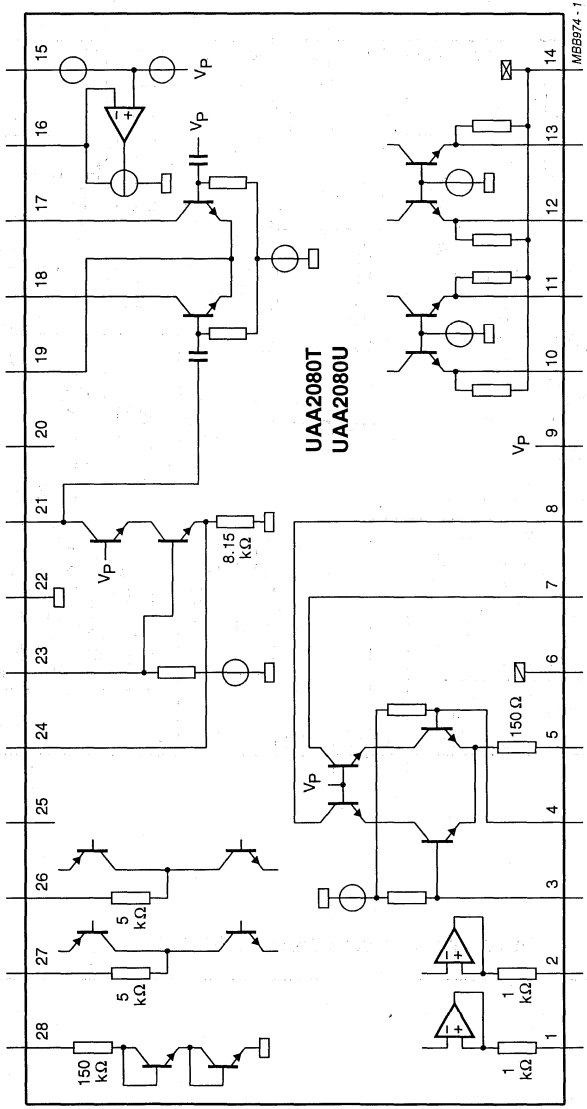


Fig.11 Internal circuits drawn for SO28 and naked die.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Figs 1 to 6.

Radio frequency amplifier

The RF amplifier is an emitter-coupled pair driving a balanced cascode stage, which drives an external balanced tuned circuit. Its bias current is set by an external 300 Ω resistor R1 to typically 770 μA. With this bias current the optimum source resistance is 1.3 kΩ at VHF and 1.0 kΩ at UHF. At 930 MHz a higher bias current is required to achieve optimum gain. A value of 120 Ω is used for R1, which corresponds with a bias current of approximately 1.3 mA and an optimum source resistance of approximately 600 Ω.The capacitors C1 and C2 transform a 50 Ω source resistance to this optimum value. The output drives a tuned circuit with capacitive divider (C7, C8 and C9) to provide maximum power transfer to the phase-splitting network and the mixers.

Mixers

The double balanced mixers consist of common base input stages and upper switching stages driven from the frequency multiplier. The 300 Ω input impedance of each mixer acts together with external components (C10, C11; L4, L5 respectively) as phase shifter/power splitter to provide a differential phase shift of 90 degrees between the I channel and the Q channel. At 930 MHz all external phase shifter components are inductive (L10, L11; L4, L5).

Oscillator

The oscillator is based on a transistor in common collector configuration. It is followed by a cascode stage driving a tuned circuit which provides the signal for the frequency multiplier. The oscillator bias current (typically 250 μA) is determined by the 1.8 kΩ external resistor R5. The oscillator frequency is controlled by an external 3rd overtone crystal in parallel resonance mode. External capacitors between base and emitter (C17) and from emitter to ground (C16) make the oscillator transistor appear as having a negative resistance for small signals; this causes the oscillator to start. Inductance L9 connected in parallel with capacitor C16 to the emitter of the oscillator transistor prevents oscillation at the fundamental frequency of the crystal.

The resonant circuit at output pin OSC selects the second harmonic of the oscillator frequency. In other applications a different multiplication factor may be chosen.

At 930 MHz an external oscillator circuit is required to provide sufficient local oscillator signal for the frequency multiplier.

Frequency multiplier

The frequency multiplier is an emitter-coupled pair driving an external balanced tuned circuit. Its bias current is set by external resistor R4 to typically 190 μA (173 MHz), 350 μA (470 MHz) and 1 mA (930 MHz). The oscillator signal is internally AC coupled to one input of the emitter-coupled pair while the other input is internally grounded via a capacitor. The frequency multiplier output signal between pins VO1MUL and VO2MUL drives the upper switching stages of the mixers. The bias voltage on pins VO1MUL and VO2MUL is set by external resistor R3 to allow sufficient voltage swing at the mixer outputs. The value of R3 depends on the operating frequency: 1.5 kΩ (173 MHz), 820 Ω (470 MHz) and 330 Ω (930 MHz).

Low noise amplifiers, active filters and gyrator filters

The low noise amplifiers ensure that the noise of the following stages does not affect the overall noise figure. The following active filters before the gyrator filters reduce the levels of large signals from adjacent channels. Internal AC couplings block DC offsets from the gyrator filter inputs.

The gyrator filters implement the transfer function of a 7th order elliptic filter. Their cut-off frequencies are determined by the 47 kΩ external resistor R2 between pins RGYR and COM. The gyrator filter output signals are available on IF test pins TPI and TPQ.

Limiters

The gyrator filter output signals are amplified in the limiter amplifiers to obtain IF signals with removed amplitude information.

Demodulator

The limiter amplifier output signals are fed to the demodulator. The demodulator output DO is going LOW or HIGH depending upon which of the input signals has a phase lead.

Battery LOW indicator

The battery LOW indicator senses the supply voltage and sets its output HIGH when the supply voltage is less than V_{th} (typically 2.05 V). Low battery warning is available at BLI.

Band gap reference

The whole chip can be powered-up and powered-down by enabling and disabling the band gap reference via the receiver enable pin RE.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
Ground pins GND1, GND2 and GND3 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	−0.3	+8.0	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−10	+70	°C
V_{es}	electrostatic handling (note 1)			
	pins VI1RF and VI2RF	−1500	+2000	V
	pin RRFA	−500	+2000	V
	pins VO1RF and VO2RF	−2000	+250	V
	pins V_P and OSB	−500	+500	V
	pins OSC and OSE	−2000	+500	V
	other pins	−2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor.

DC CHARACTERISTICS

V_P = 2.05 V; T_{amb} = −10 to +70 °C (typical values at T_{amb} = 25 °C); measurements taken in test circuit Fig.1, 2, 3 or 4 with crystal at pin OSB disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current	V_{RE} = HIGH; $f_{i(RF)}$ = 173 and 470 MHz	2.3	2.7	3.2	mA
		V_{RE} = HIGH; $f_{i(RF)}$ = 930 MHz	2.9	3.4	3.9	mA
$I_{P(off)}$	stand-by current	V_{RE} = LOW	–	–	3	µA
Receiver enable input (pin RE)						
V_{IH}	HIGH level input voltage		1.4	–	V_P	V
V_{IL}	LOW level input voltage		0	–	0.3	V
I_{IH}	HIGH level input current	$V_{IH} = V_P$ = 3.5 V	–	–	20	µA
V_{IL}	LOW level input current	V_{IL} = 0 V	0	–	−1.0	µA
Battery LOW indicator output (pin BLI)						
V_{OH}	HIGH level output voltage	$V_P < V_{th}$; I_{BLI} = −10 µA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	$V_P > V_{th}$; I_{BLI} = +10 µA	–	–	0.5	V
V_{th}	voltage threshold for battery LOW indicator		1.95	2.05	2.15	V
Demodulator output (pin DO)						
V_{OH}	HIGH level output voltage	I_{DO} = −10 µA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	I_{DO} = +10 µA	–	–	0.5	V

AC CHARACTERISTICS (173 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.1 or 2; $f_{i(RF)}$ = 172.941 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ±25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–126.5	–123.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–120.5	dBm
		V_P = 1.9 V	–	–	–117.5	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	69	72	–	dB
		T_{amb} = –10 to +70 °C	67	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	78	85	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (470 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.3 or 4; $f_{i(RF)}$ = 469.950 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–124.5	–121.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–118.5	dBm
		V_P = 1.9 V	–	–	–115.5	dBm
Mixer input						
$P_{i(mix)}$	input sensitivity	BER ≤ $^3/_{100}$; note 3	–	–115.0	–110.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	67	70	–	dB
		T_{amb} = –10 to +70 °C	65	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	$\Delta f > \pm 1$ MHz; note 4	75	82	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 5	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Test circuit Fig.5. $P_{i(mix)}$ is the maximum available power at the input of the test board. The bit error rate BER is measured using the test facility shown in Fig.13.
4. Δf is the frequency offset between the required signal and the interfering signal.
5. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (930 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.6 (note 1); $f_{i(RF)}$ = 930.500 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 2	–	–120.0	–114.0	dBm
		V_P = 1.9 V	–	–	–108.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	60	69	–	dB
α_c	co-channel rejection		–	5	10	dB
α_{sp}	spurious immunity		40	60	–	dB
α_{im}	intermodulation immunity		53	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	65	74	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz and a level of –15 dBm.
2. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

TEST INFORMATION

Tuning procedure for AC tests

1. Turn on the signal generator: $f_{gen} = f_{i(RF)} + 4$ kHz, no modulation, $V_{i(RF)} = 1$ mV (RMS).
2. Measure the IF with a counter connected to test pin TPI. Tune C16 to set the crystal oscillator to achieve $f_{IF} = 4$ kHz Change the generator frequency to $f_{gen} = f_{i(RF)} - 4$ kHz and check that f_{IF} is also 4 kHz. For a received input frequency $f_{i(RF)} = 172.941$ MHz the crystal frequency is $f_{XTAL} = 57.647$ MHz, while for $f_{i(RF)} = 469.950$ MHz the crystal frequency is $f_{XTAL} = 78.325$ MHz. For a received input frequency $f_{i(RF)} = 930.500$ MHz an external oscillator signal must be used with $f_{i(OSC)} = 310.1667$ MHz and a level of –15 dBm (for definition of crystal frequency, see Table 1).
3. Set the signal generator to nominal frequency ($f_{i(RF)}$) and turn on the modulation deviation ±4.0 kHz, 600 Hz square wave modulation, $V_{i(RF)} = 1$ mV (RMS). Note that the RF signal should be reduced in the following tests, as the receiver is tuned, to ensure $V_{o(IF)} = 10$ to 50 mV (p-p) on test pins TPI or TPQ.
4. Tune C15 (oscillator output circuit) and C12 (frequency multiplier output) to obtain a peak audio voltage on pin TPI.
5. Tune C3 and C6 (RF input and mixer input) to obtain a peak audio voltage on pin TPI. When testing the mixer input sensitivity tune C23 instead of C3 and C6 (test circuit Fig.5).
6. Check that the output signal on pin TPQ is within 3 dB in amplitude and at 90° (±20°) relative phase of the signal on pin TPI.
7. Check that data signal appears on output pin DO and proceed with the AC test.

AC test conditions

Table 5 Definitions for AC test conditions (see Table 6)

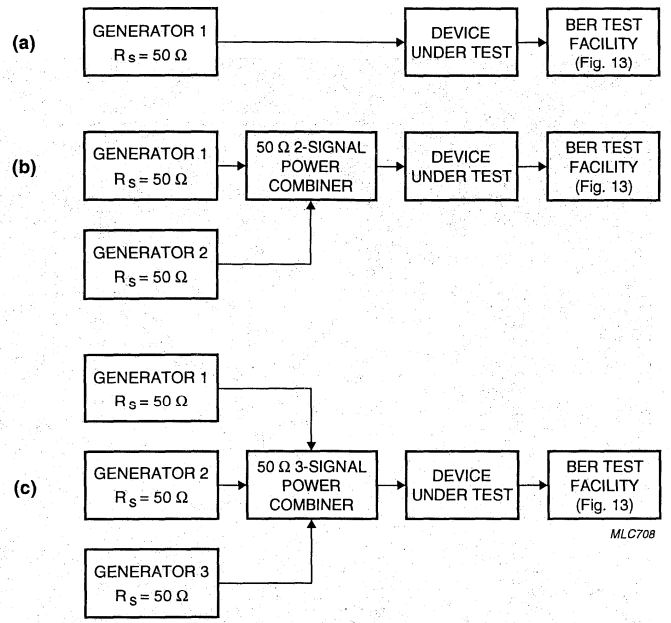
SIGNAL	DESCRIPTION
Modulated test signal 1	
Frequency	172.941, 469.950 or 930.500 MHz
Deviation	±4.0 kHz
Modulation	1200 baud pseudo random bit sequence
Rise time	250 ±25 µs (between 10% and 90% of final value)
Modulated test signal 2	
Deviation	±2.4 kHz
Modulation	400 Hz sine wave
Other definitions	
f_1	frequency of signal generator 1
f_2	frequency of signal generator 2
f_3	frequency of signal generator 3
Δf_{cs}	channel spacing (20 kHz)
P_1	maximum available power from signal generator 1 at the test board input
P_2	maximum available power from signal generator 2 at the test board input
P_3	maximum available power from signal generator 3 at the test board input
$P_{i(ref)}$	maximum available power at the test board input to give a Bit Error Rate (BER) $\leq 3/100$ for the modulated test signal 1, in the absence of interfering signals and under the conditions as specified in Chapters "AC characteristics (173 MHz)", "AC characteristics (470 MHz)" and "AC characteristics (930 MHz)"

Table 6 AC test conditions (notes 1 and 2)

SYMBOL	PARAMETER	CONDITIONS	TEST SIGNALS
α_a	adjacent channel selectivity; Fig.12(b)	$f_2 = f_1 \pm \Delta f_{CS}$	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{a(min)}$
α_c	co-channel rejection; Fig.12(b)	$f_2 = f_1 \pm$ up to 3 kHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 - \alpha_{c(max)}$
α_{sp}	spurious immunity; Fig.12(b)	f_2 = 100 kHz to 2 GHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{sp(min)}$
α_{im}	intermodulation immunity; Fig.12(c)	$f_2 = f_1 \pm \Delta f_{cs}$; $f_3 = f_1 \pm 2\Delta f_{cs}$	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: unmodulated	$P_2 = P_1 + \alpha_{im(min)}$
		generator 3: modulated test signal 2	$P_3 = P_2$
α_{bl}	blocking immunity; Fig.12(b)	$f_2 = f_1 \pm 1$ MHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{bl(min)}$
f_{offset}	frequency offset range; Fig.12(a)	deviation = ±4.0 kHz, $f_1 = f_{i(RF)} \pm 2$ kHz ($f_{offset(min)}$)	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
Δf_{dev}	deviation range; Fig.12(a)	deviation = ±2.5 to ±7 kHz; ($\Delta f_{dev(min)}$ to $\Delta f_{dev(max)}$)	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
t_{on}	receiver turn-on time; Fig.12(a)	note 3	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 10$ dB

Notes

1. The tests are executed without load on pins TPI and TPQ.
2. All minimum and maximum values correspond to a bit error rate (BER) $\leq 3/100$ in the wanted signal (P_1).
3. The BER measurement is started 5 ms ($t_{on(max)}$) after V_{RE} goes HIGH; BER is then measured for 100 bits (BER $\leq 3/100$).



(a) One generator.
(b) Two generators.
(c) Three generators.

Fig.12 Test configurations.

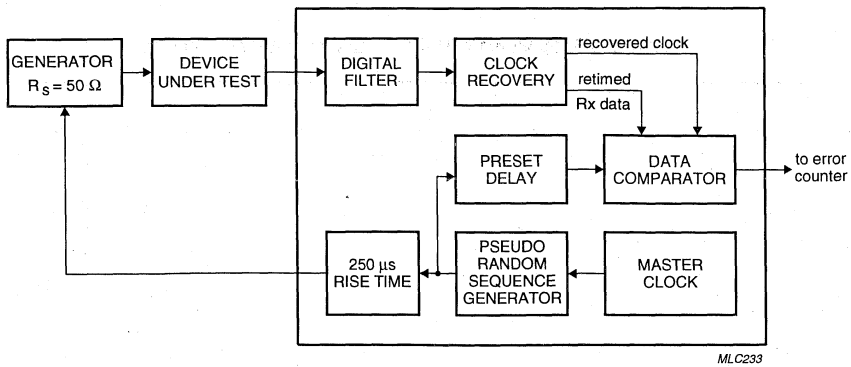


Fig.13 BER test facility.

PRINTED-CIRCUIT BOARDS

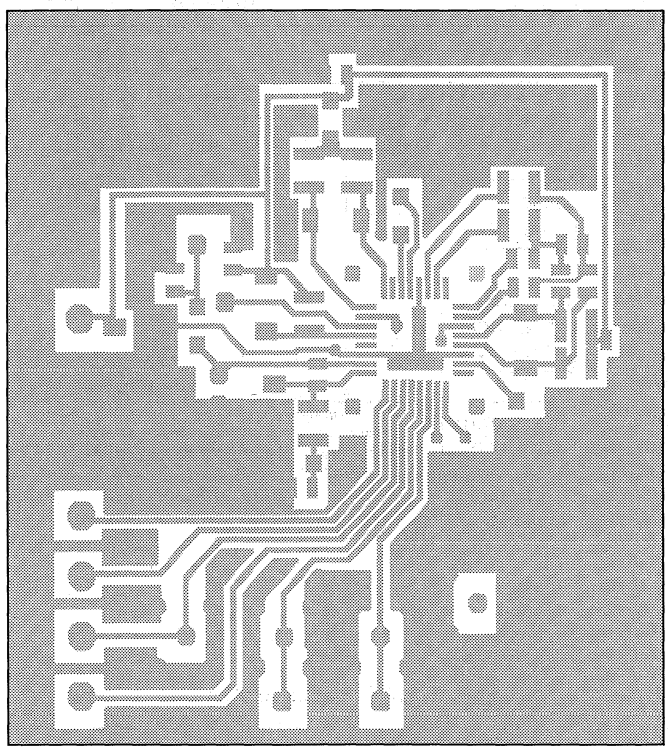


Fig.14 PCB top view for TQFP32; test circuit Figs 1 and 3.

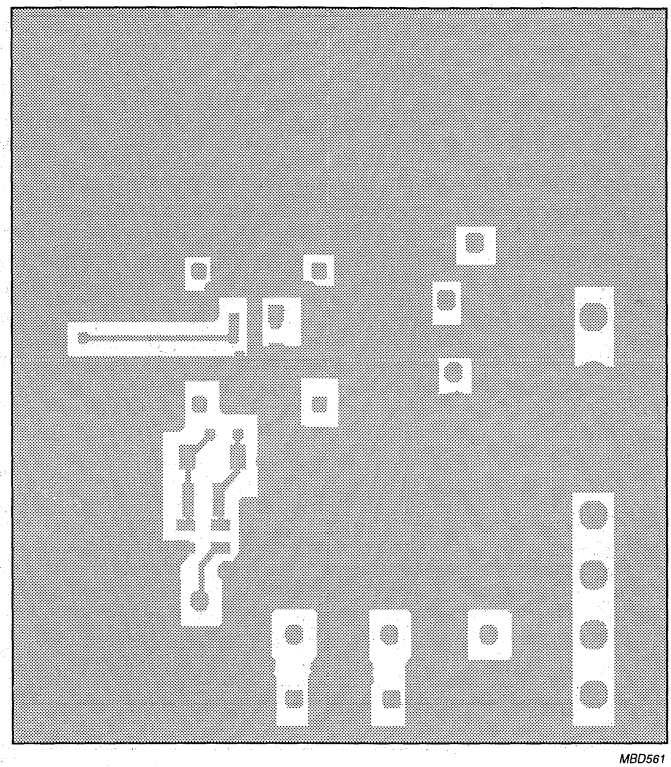
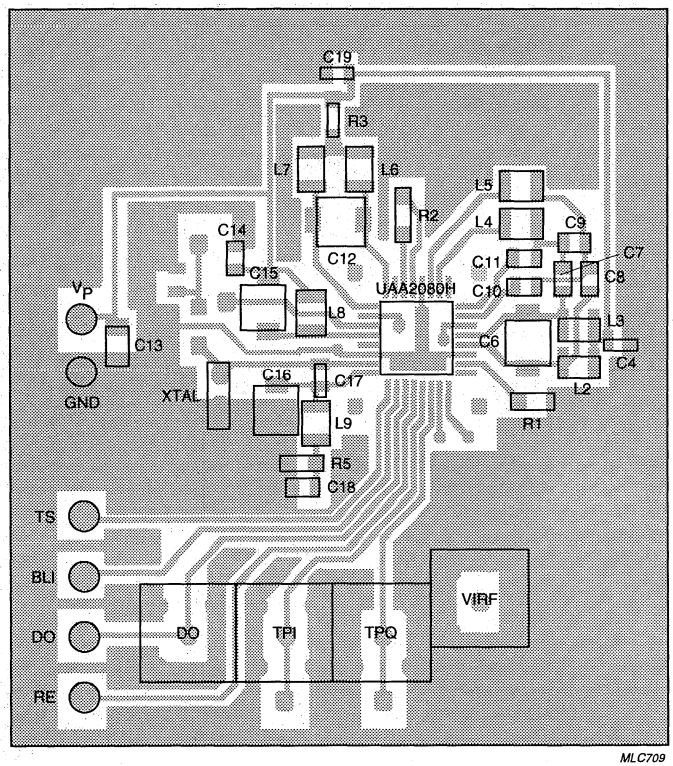


Fig.15 PCB bottom view for TQFP32; test circuit Figs 1 and 3.



V_{EE} = GND; V_C = V_P.

Fig.16 PCB top view with components for TQFP32; test circuit Fig.3.

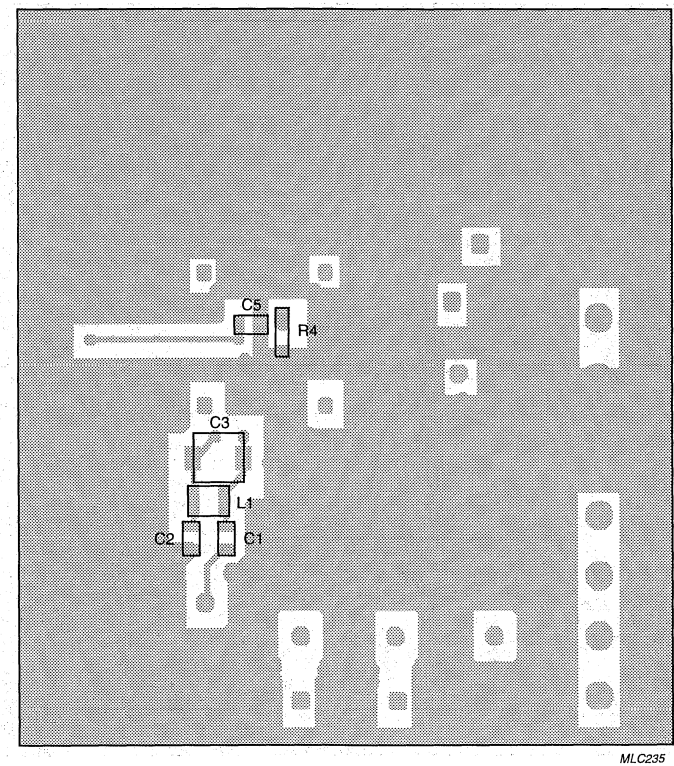


Fig.17 PCB bottom view with components for TQFP32; test circuit Fig.3.

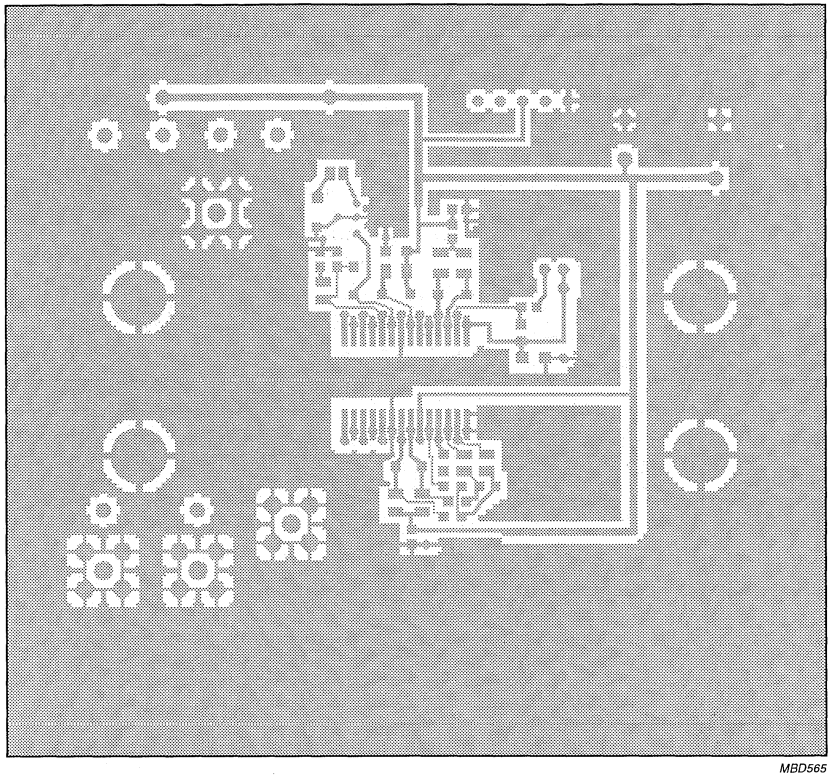


Fig.18 PCB top view for SO28; test circuit Figs 2 and 4.

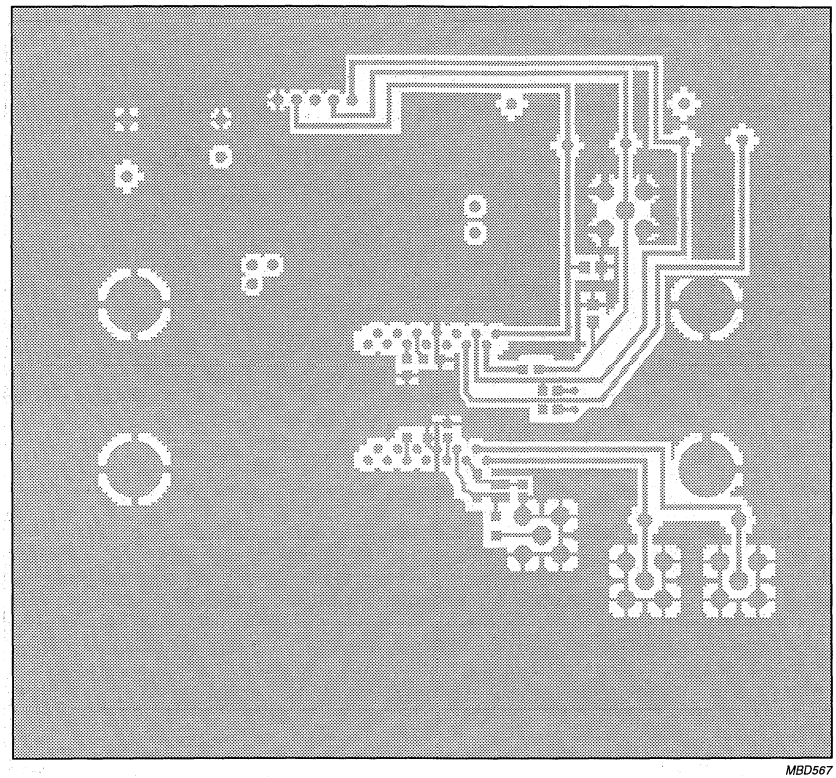
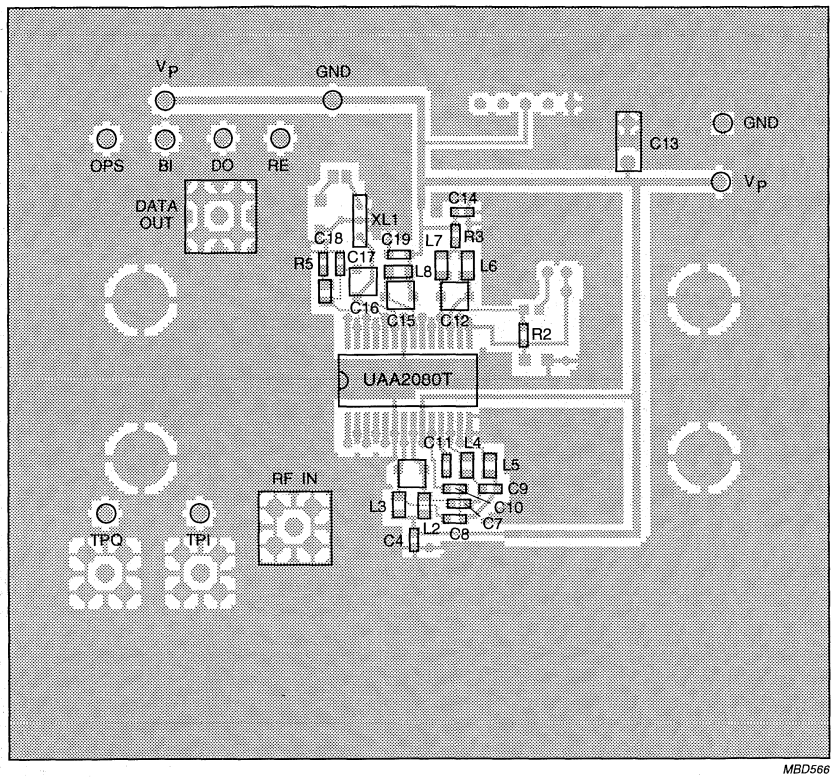


Fig.19 PCB bottom view for SO28; test circuit Figs 2 and 4.



V_{EE} = GND; V_{CC} = V_P; BI = BLI; OPS = TS.

Fig.20 PCB top view with components for SO28; test circuit Fig.4.

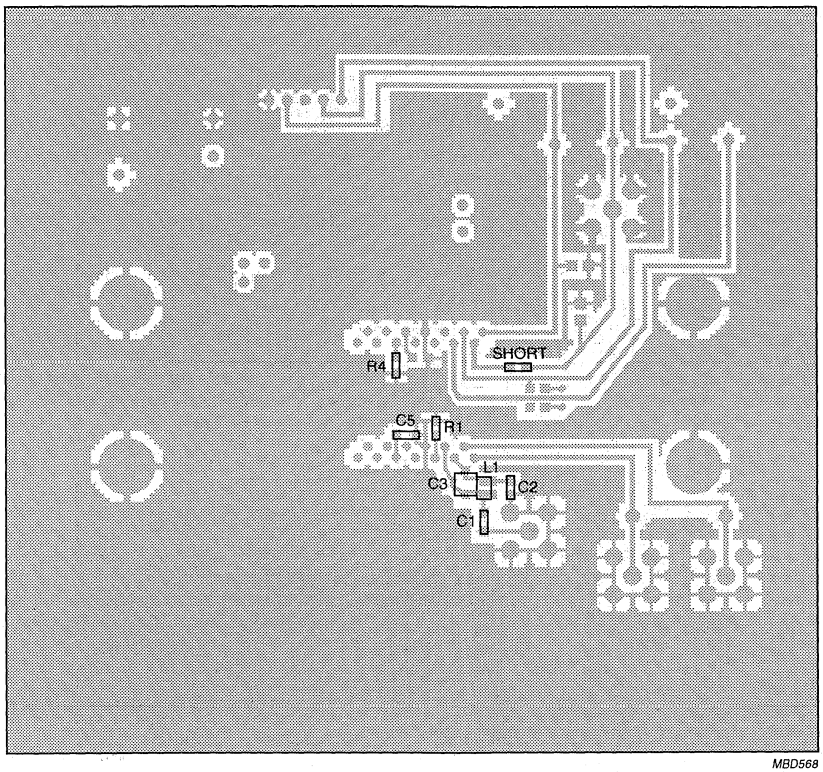


Fig.21 PCB bottom view with components for SO28; test circuit Fig.4.

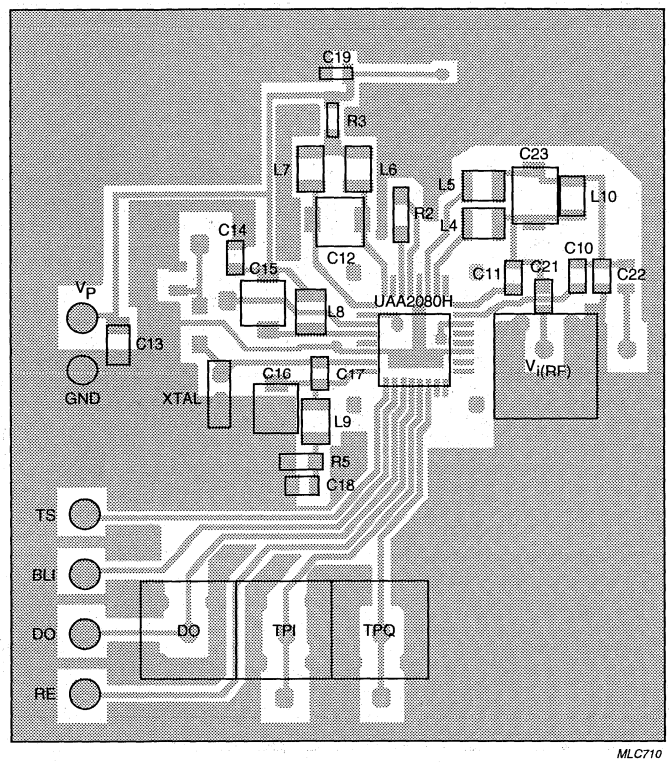


Fig.22 PCB top view with components for TQFP32; test circuit Fig.5.

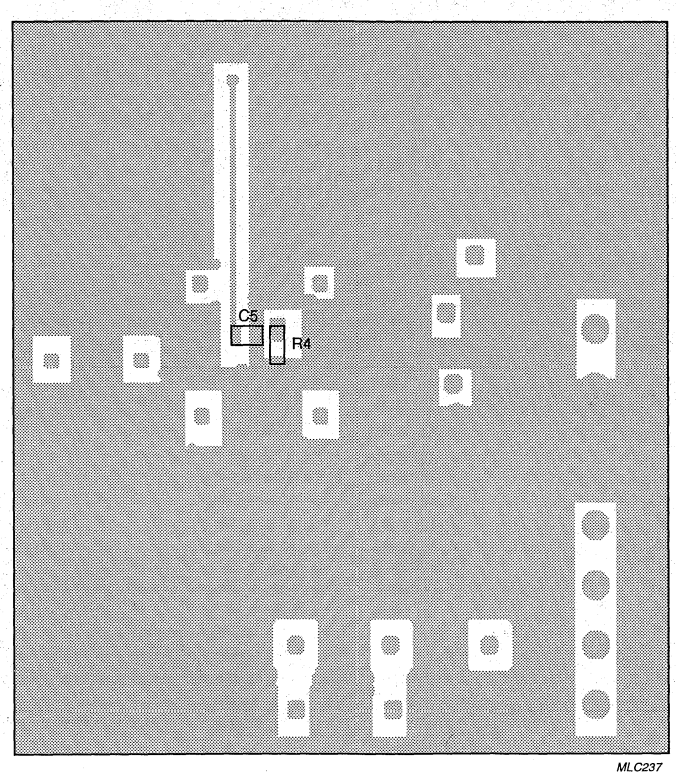


Fig.23 PCB bottom view with components for TQFP32; test circuit Fig.5.

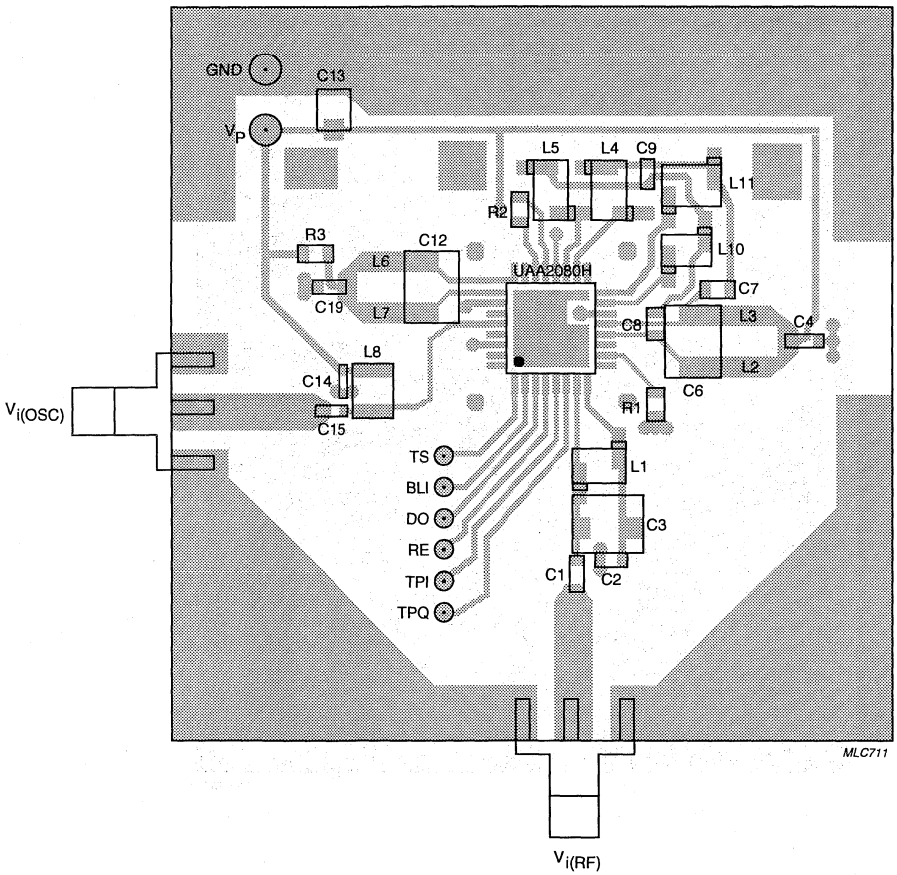


Fig.24 PCB top view with components for TQFP32; test circuit Fig.6.

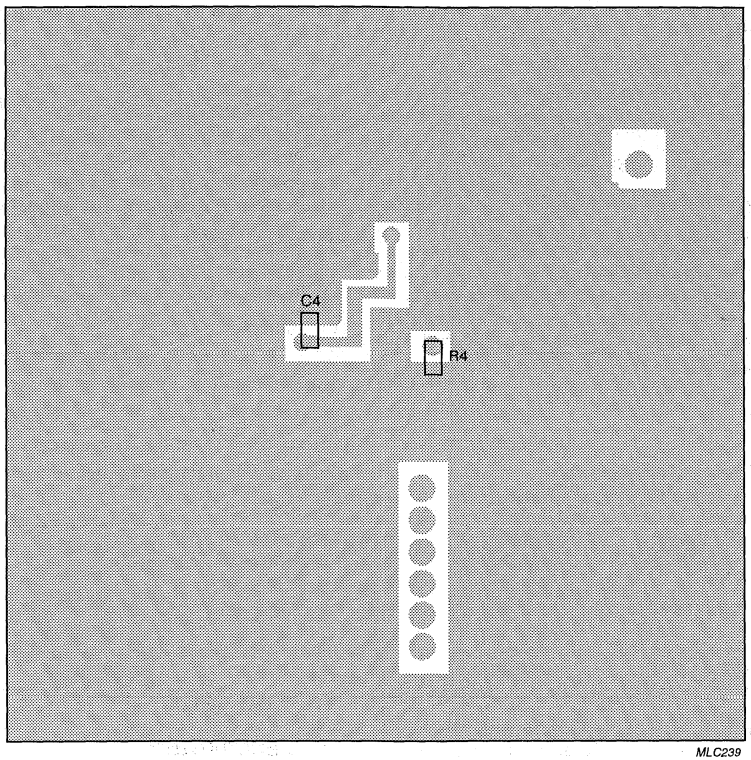


Fig.25 PCB bottom view with components for TQFP32; test circuit Fig.6.

Advanced pager receiver UAA2082

FEATURES

- Wide frequency range: VHF, UHF and 900 MHz bands
- High sensitivity
- High dynamic range
- Electronically adjustable filters on chip
- Suitable for data rates up to 2400 bits/s
- Wide frequency offset and deviation range
- Fully POCSAG compatible FSK receiver
- Power on/off mode selectable by the chip enable input
- Low supply voltage; low power consumption
- 1-cell battery-low detection circuit
- High integration level
- Interfaces directly to the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.

APPLICATIONS

- Wide area paging
- On-site paging
- Telemetry
- RF security systems
- Low bit-rate wireless data links.

GENERAL DESCRIPTION

The UAA2082 is a high-performance low-power radio receiver circuit primarily intended for VHF, UHF and 900 MHz pager receivers for wide area digital paging systems, employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK).

The receiver design is based on the direct conversion principle where the input signal is mixed directly down to the baseband by a local oscillator on the signal frequency. Two complete signal paths with signals of 90° phase difference are required to demodulate the signal. All channel selectivity is provided by the built-in IF filters. The circuit makes extensive use of on-chip capacitors to minimize the number of external components.

The battery monitoring circuit has an external sense input and a 1.1 V detection threshold for easy operation in a single-cell supply concept.

The UAA2082 was designed to operate together with the PCA5000A, PCF5001 or PCD5003 POCSAG decoders, which contain a digital input filter for optimum call success rate.

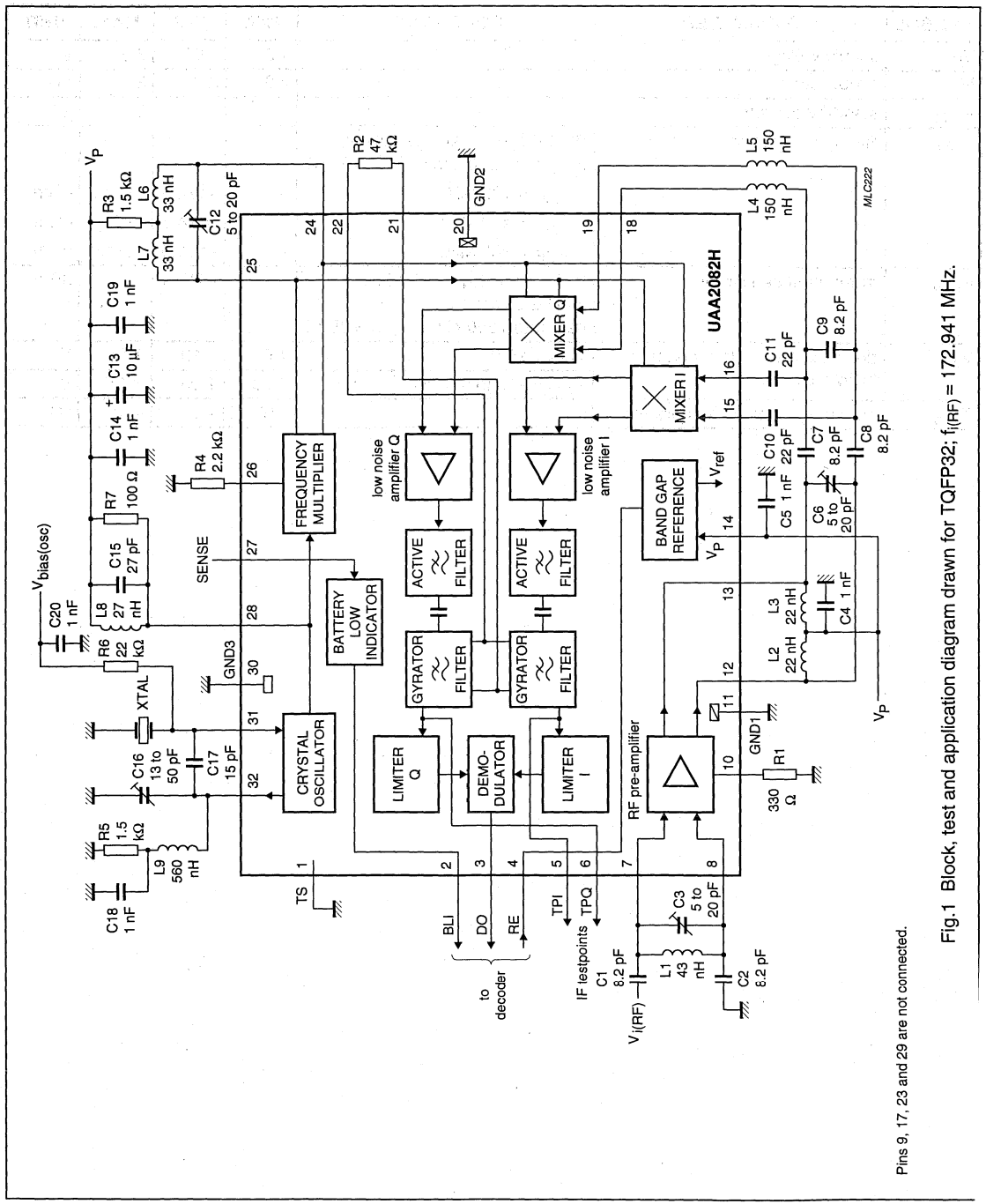
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2082H	TQFP32	plastic thin quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-2
UAA2082U	28 pads	naked die; see Fig.8	

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current		2.3	2.7	3.2	mA
$I_{P(off)}$	stand-by current		–	–	3	µA
$P_{i(ref)}$	RF input sensitivity	BER ≤ $^3/_{100}$; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C				
		$f_{i(RF)}$ = 173 MHz	–	−126.5	−123.5	dBm
		$f_{i(RF)}$ = 470 MHz	–	−124.5	−121.5	dBm
		$f_{i(RF)}$ = 930 MHz	–	−120.0	−114.0	dBm
$P_{i(mix)}$	mixer input sensitivity	BER ≤ $^3/_{100}$; $f_{i(RF)}$ = 470 MHz; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C	–	−115.0	−110.0	dBm
V_{th}	detection threshold for battery LOW indicator	T_{amb} = 25 °C	1.05	1.10	1.15	V
		T_{amb} = −10 to +70 °C	1.03	1.10	1.17	V
T_{amb}	operating ambient temperature		−10	–	+70	°C

BLOCK DIAGRAMS (173 MHz)



Pins 9, 17, 23 and 29 are not connected.

Fig.1 Block, test and application diagram drawn for TQFP32; $f_{i(RF)}$ = 172.941 MHz.

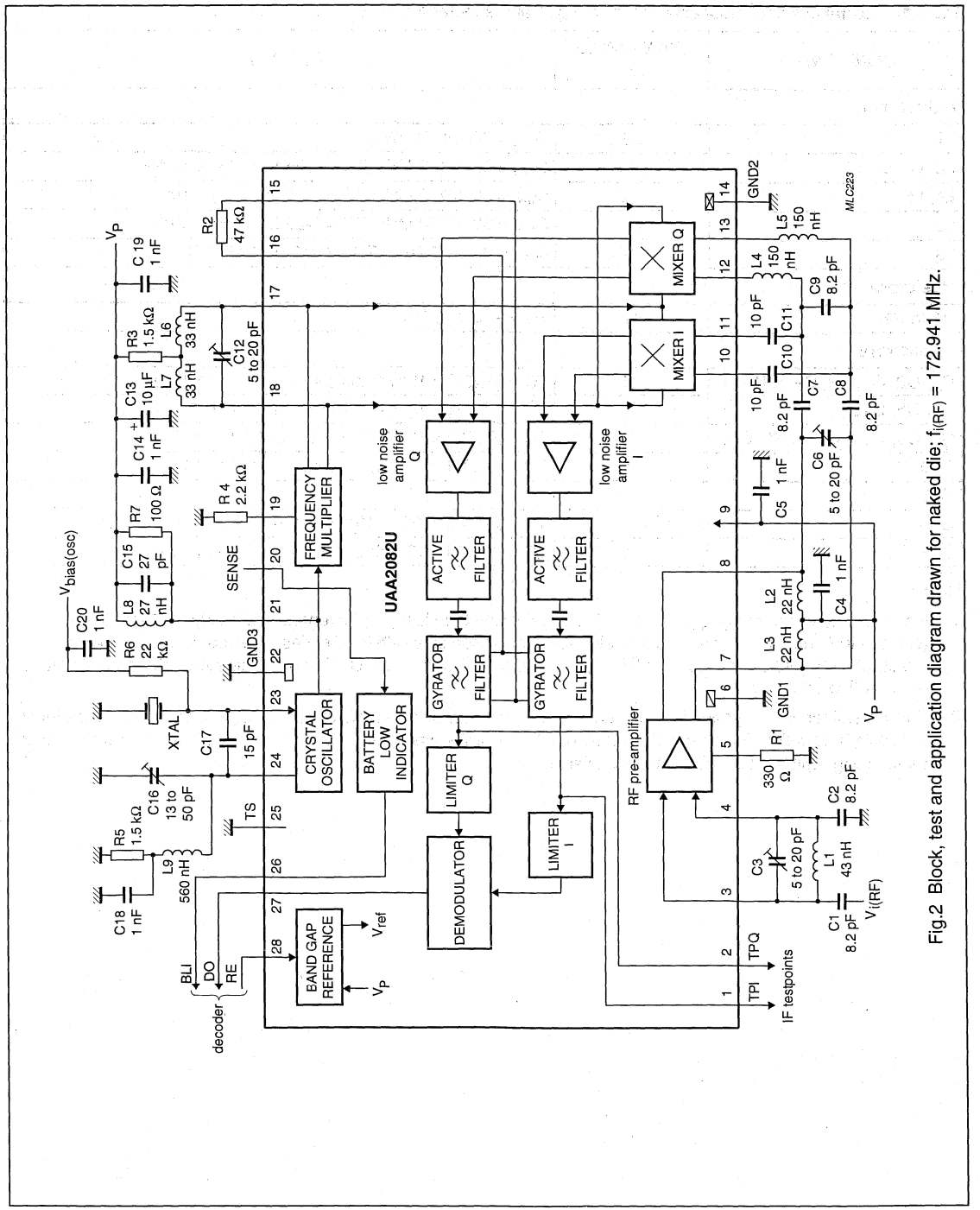


Fig.2 Block, test and application diagram drawn for naked die; $f_{i(RF)}$ = 172.941 MHz.

Table 1 Tolerances of components shown in Figs 1 and 2 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±5	Q_{min} = 100 at 173 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±20	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 30 at 57 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R7	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12	–	TC = (–750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18, C19, C20	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (–1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 57.647 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF series capacitor at 25 °C), dynamic resistance R1 < 40 Ω, Δf = ±5 × 10^{-6} for T_{amb} = –10 to +55 °C with 25 °C reference, calibration plus aging tolerance: –5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAMS (470 MHz)

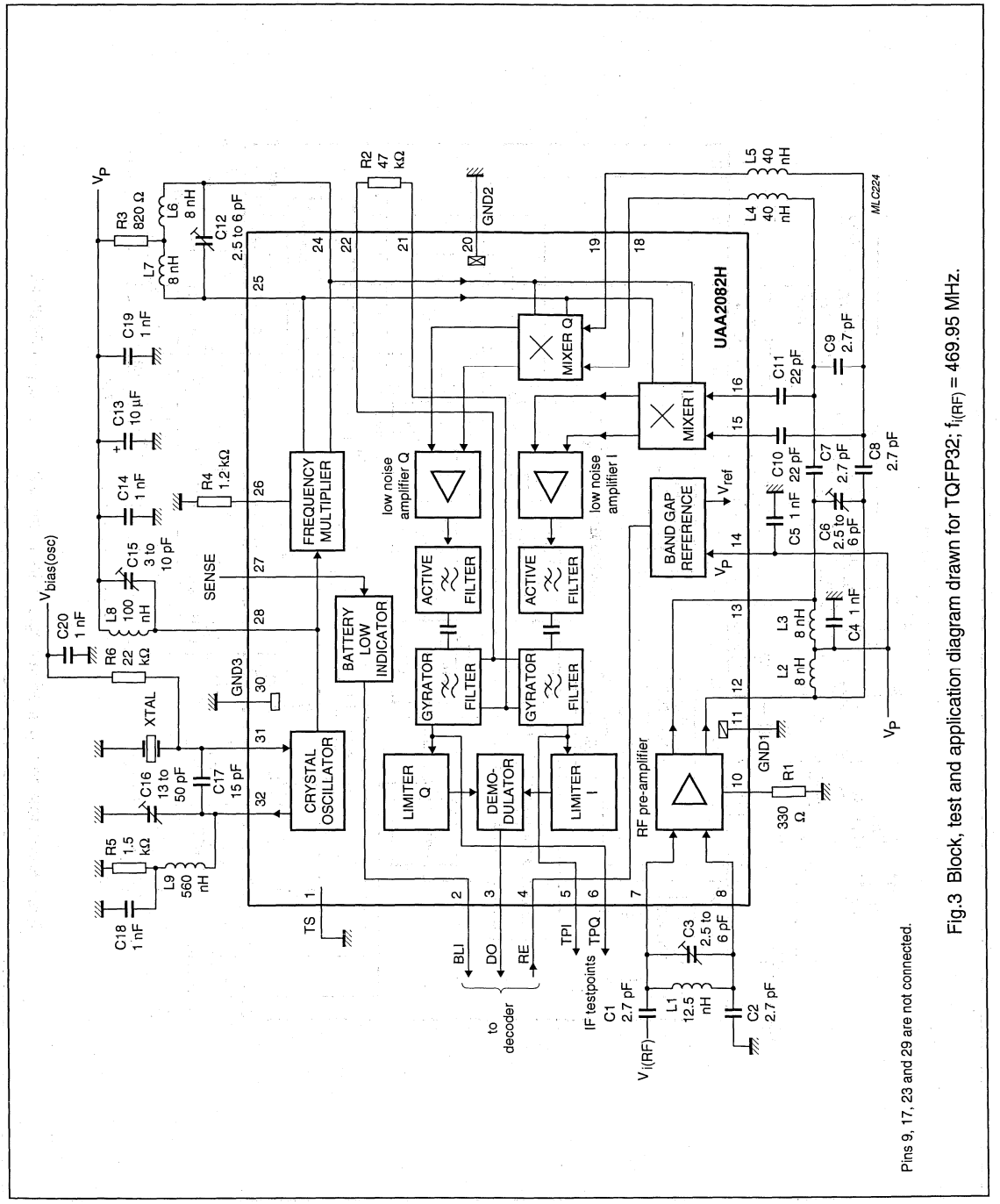


Fig.3 Block, test and application diagram drawn for TQFP32; $f_{i(RF)}$ = 469.95 MHz.

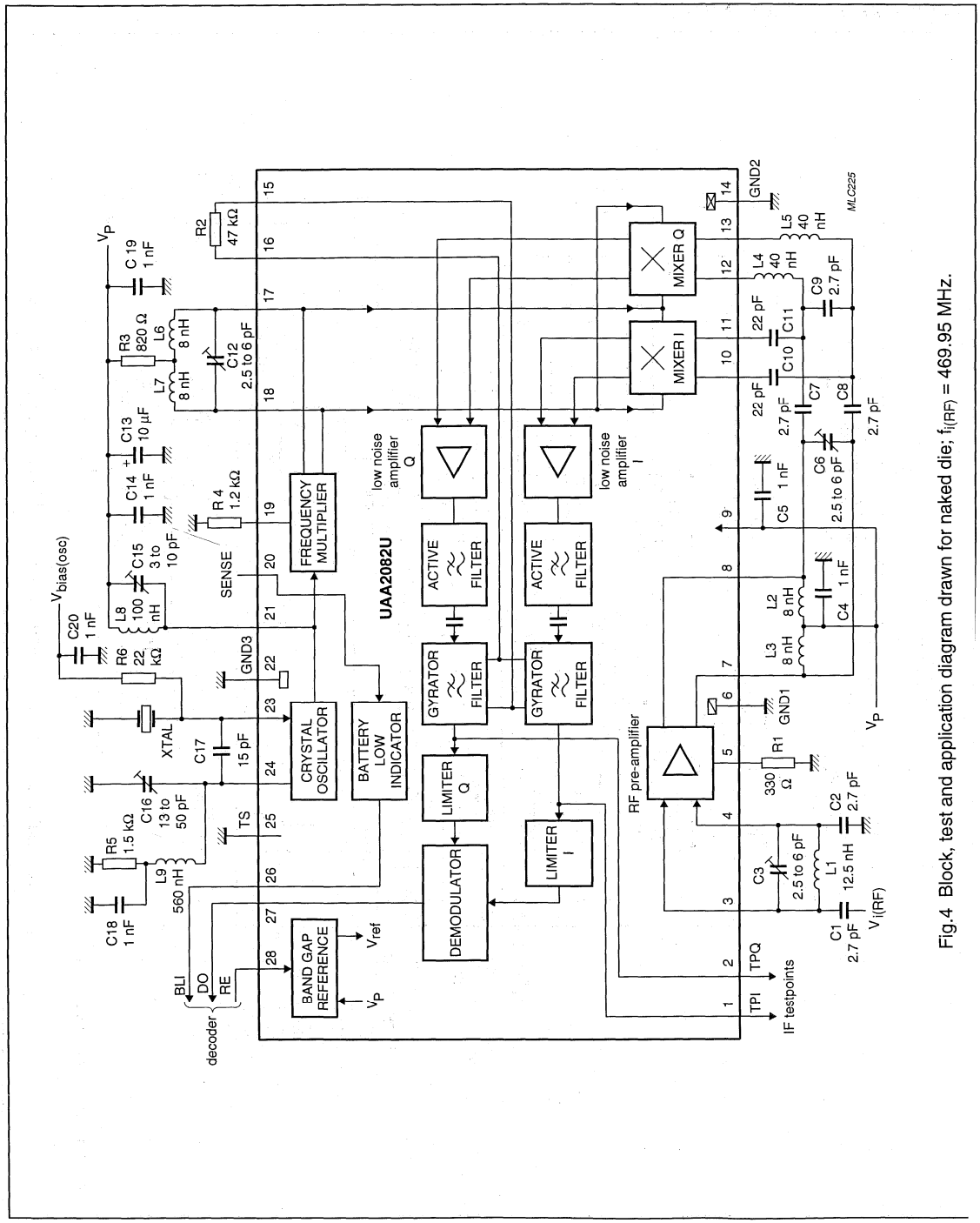


Fig.4 Block, test and application diagram drawn for naked die; $f_{i(RF)}$ = 469.95 MHz.

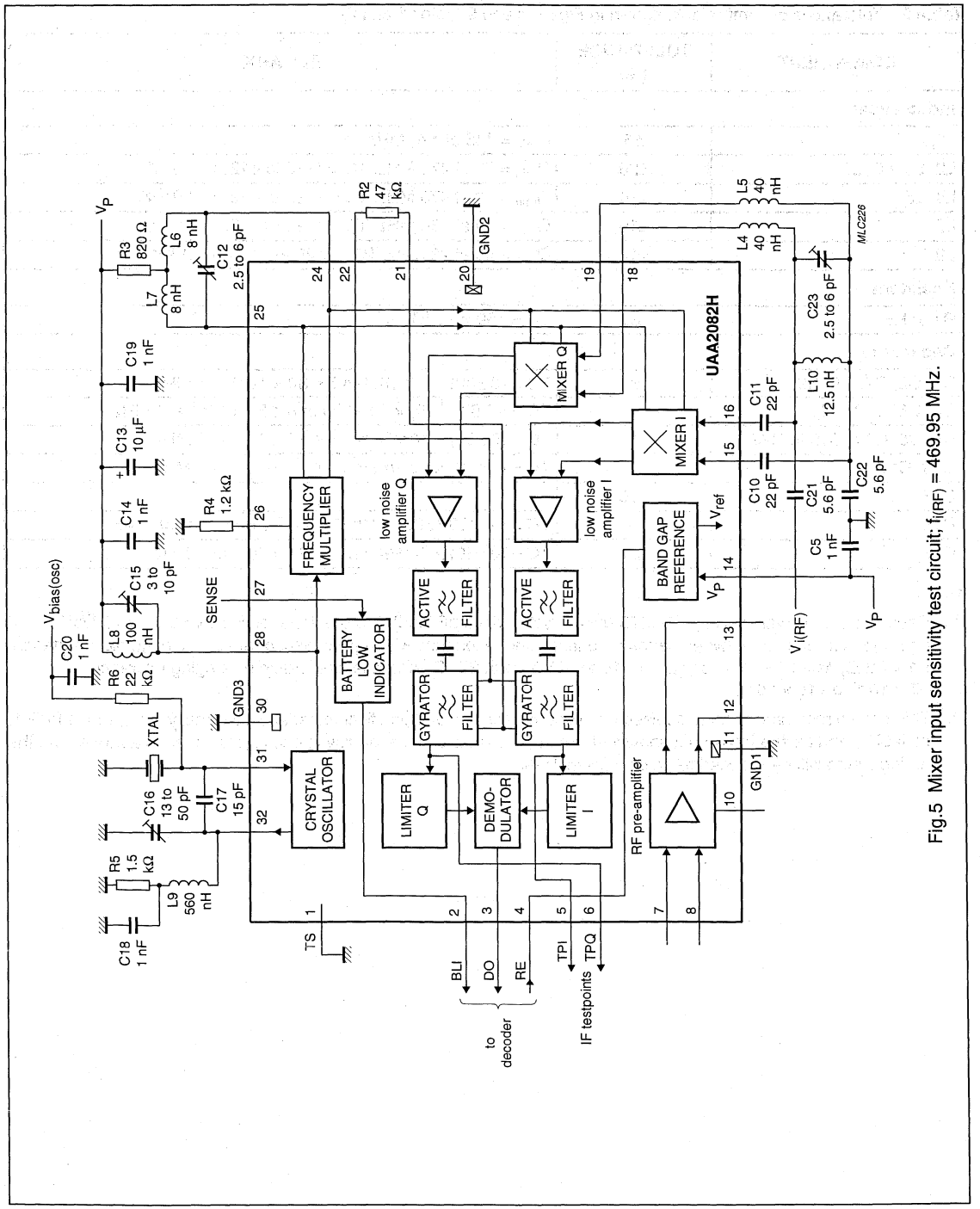


Fig.5 Mixer input sensitivity test circuit; $f_{i(RF)}$ = 469.95 MHz.

Table 2 Tolerances of components shown in Figs 3, 4 and 5 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1, L10	±5	Q_{min} = 145 at 470 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 40 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±10	Q_{min} = 30 at 156 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 40 at 78 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R6	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12, C23	–	TC = (–750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18 to C22	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (–1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 78.325 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF capacitor at 25 °C), dynamic resistance R1 < 30 Ω, Δf = ±5 × 10^{-6} for T_{amb} = –10 to +55 °C with 25 °C reference, calibration plus aging tolerance: –5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAM (930 MHz)

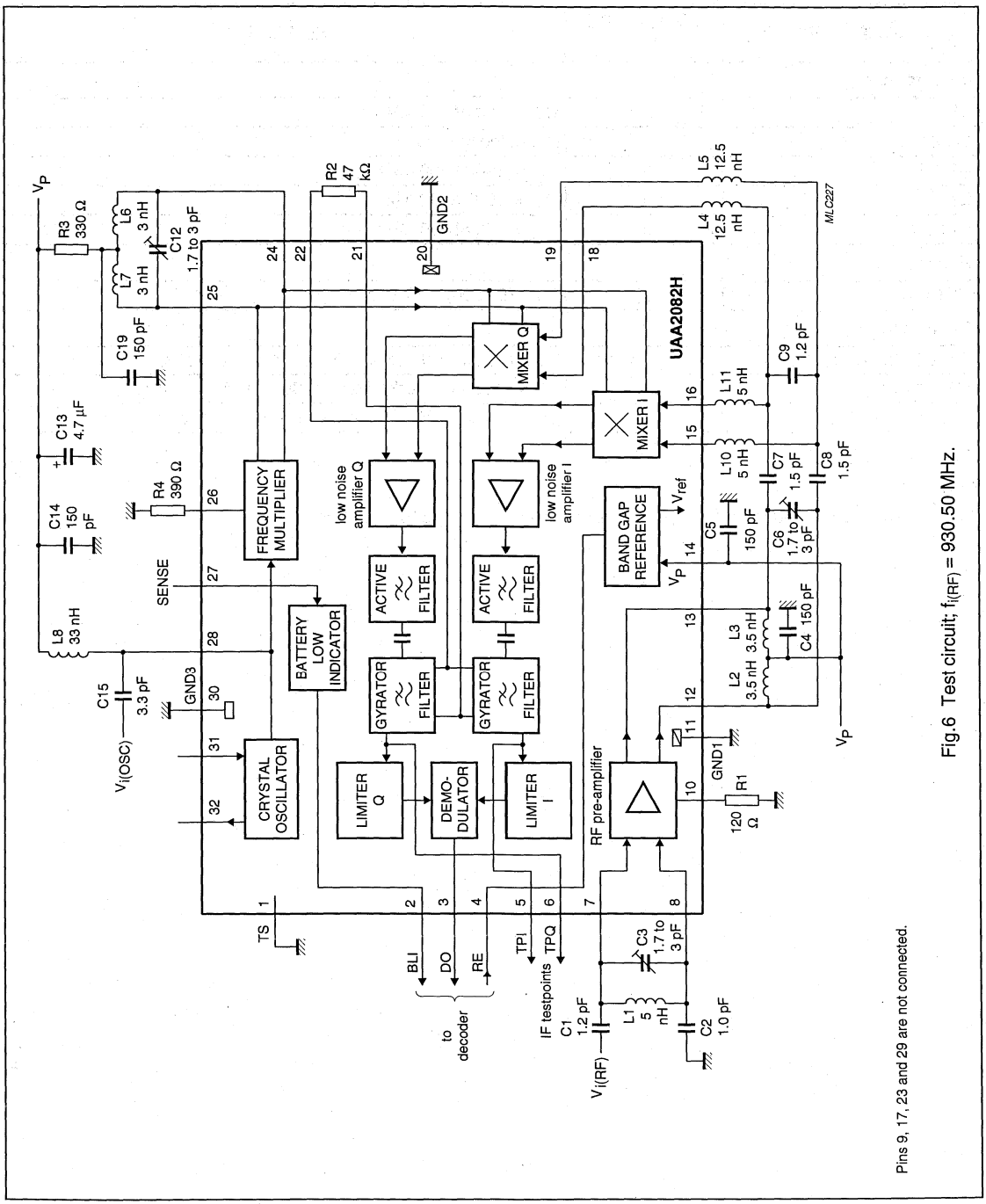


Fig.6 Test circuit; $f_{i(RF)}$ = 930.50 MHz.

Pins 9, 17, 23 and 29 are not connected.

Table 3 Tolerances of components shown in Fig.6 (note 1)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±10	Q_{typ} = 150 at 930 MHz
L2, L3, L6, L7	–	microstrip inductor
L4, L5	±5	Q_{typ} = 100 at 930 MHz
L8	±10	Q_{typ} = 65 at 310 MHz
L10, L11	±10	Q_{typ} = 150 at 930 MHz
Resistors		
R1 to R4	±2	TC = (0 ±200) × 10^{-6}/K;
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12	–	TC = (0 ±200) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C4, C5, C14, C19	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C13	±20	

Note

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz.

PINNING (TQFP32)

SYMBOL	PIN	DESCRIPTION
TS	1	test switch; connection to ground for normal operation
BLI	2	battery LOW indicator output
DO	3	data output
RE	4	receiver enable input
TPI	5	IF test point; I channel
TPQ	6	IF test point; Q channel
VI1RF	7	pre-amplifier RF input 1
VI2RF	8	pre-amplifier RF input 2
n.c.	9	not connected
RRFA	10	external emitter resistor for pre-amplifier
GND1	11	ground 1 (0 V)
VO2RF	12	pre-amplifier RF output 2
VO1RF	13	pre-amplifier RF output 1
V_P	14	supply voltage
VI2MI	15	I channel mixer input 2
VI1MI	16	I channel mixer input 1
n.c.	17	not connected
VI1MQ	18	Q channel mixer input 1
VI2MQ	19	Q channel mixer input 2
GND2	20	ground 2 (0 V)
COM	21	gyrator filter resistor; common line
RGYR	22	gyrator filter resistor
n.c.	23	not connected
VO1MUL	24	frequency multiplier output 1
VO2MUL	25	frequency multiplier output 2
RMUL	26	external emitter resistor for frequency multiplier
SENSE	27	battery LOW detector sense input
OSC	28	oscillator collector
n.c.	29	not connected
GND3	30	ground 3 (0 V)
OSB	31	oscillator base; crystal input
OSE	32	oscillator emitter

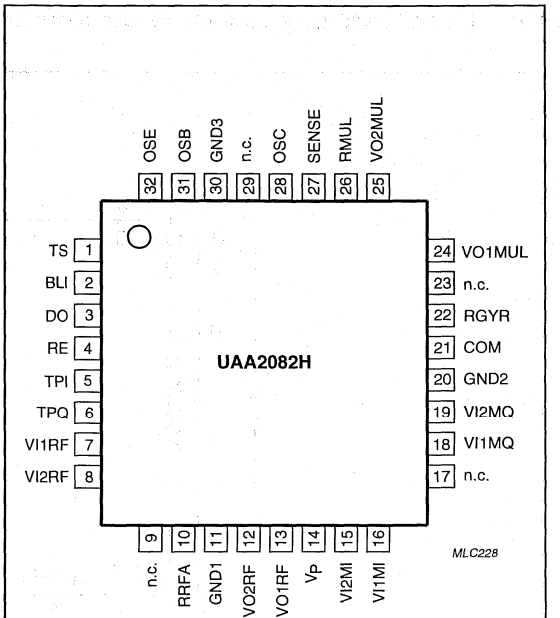
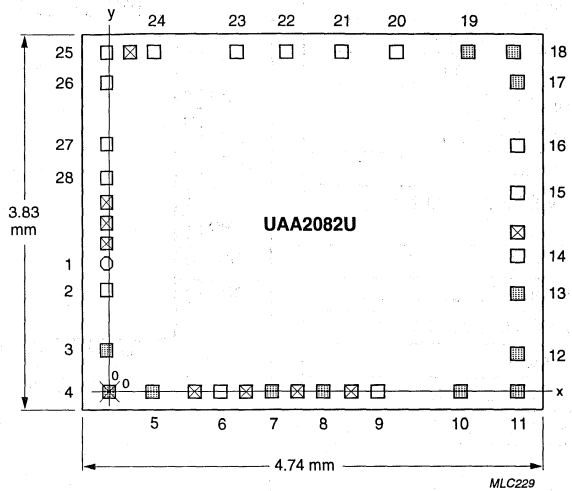


Fig.7 Pin configuration; TQFP32.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

See Table 4 for bonding pad description and locations for x/y co-ordinates.



Where:

- ○ Pad number 1 (diameter 124 µm)
- □ Pad 124 µm x 124 µm
- ⊠ Pad not used
- ▥ Pad 100 µm x 100 µm
- ⊠ Pad 100 µm x 100 µm with reference point

Chip area: 18.15 mm^2.
Chip thickness: 380 ±20 µm.
Drawing not to scale.

Fig.8 Bonding pad locations.

Table 4 Bonding pad centre locations (dimensions in μm)

SYMBOL	PAD	DESCRIPTION	x	y
TPI	1	IF test point; I channel	−32	1296
TPQ	2	IF test point; Q channel	−32	1000
VI1RF	3	pre-amplifier RF input 1	−32	360
VI2RF	4	pre-amplifier RF input 2; note 1	0	0
RRFA	5	external emitter resistor for pre-amplifier	472	0
GND1	6	ground 1 (0 V)	1160	0
VO2RF	7	pre-amplifier RF output 2	1688	0
VO1RF	8	pre-amplifier RF output 1	2232	0
V_P	9	supply voltage	2760	0
VI2MI	10	I channel mixer input 2	3608	0
VI1MI	11	I channel mixer input 1	4216	0
VI1MQ	12	Q channel mixer input 1	4216	360
VI2MQ	13	Q channel mixer input 2	4216	960
GND2	14	ground 2 (0 V)	4216	1360
COM	15	gyrator filter resistor; common line	4216	2024
RGYR	16	gyrator filter resistor	4216	2496
VO1MUL	17	frequency multiplier output 1	4216	3136
VO2MUL	18	frequency multiplier output 2	4176	3456
RMUL	19	external emitter resistor for frequency multiplier	3668	3458
SENSE	20	battery LOW detector sense input	2952	3456
OSC	21	oscillator collector	2312	3456
GND3	22	ground 3 (0 V)	1832	3456
OSB	23	oscillator base; crystal input	1328	3456
OSE	24	oscillator emitter	432	3456
TS	25	test switch; connection to ground for normal operation	−32	3456
BLI	26	battery LOW indicator output	−32	3136
DO	27	data output	−32	2512
RE	28	receiver enable input	−32	2152
		lower left corner of chip (typical values)	−278	−186

Note

1. All x/y co-ordinates are referenced to the centre of pad 4 (VI2RF); see Fig.8.

INTERNAL CIRCUITS

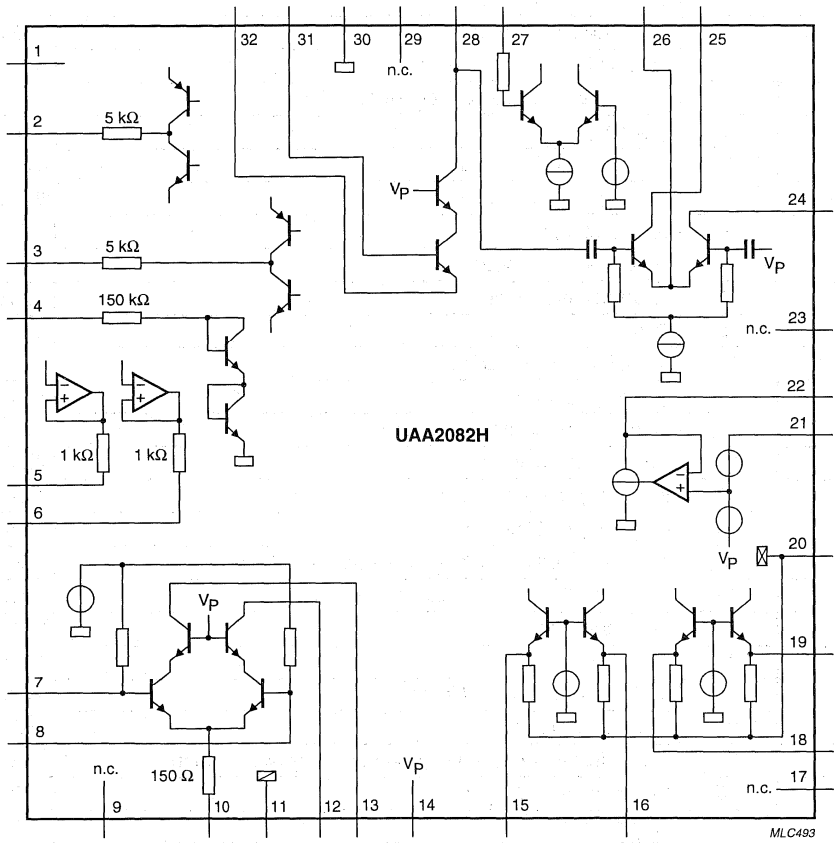


Fig.9 Internal circuits drawn for TQFP32.

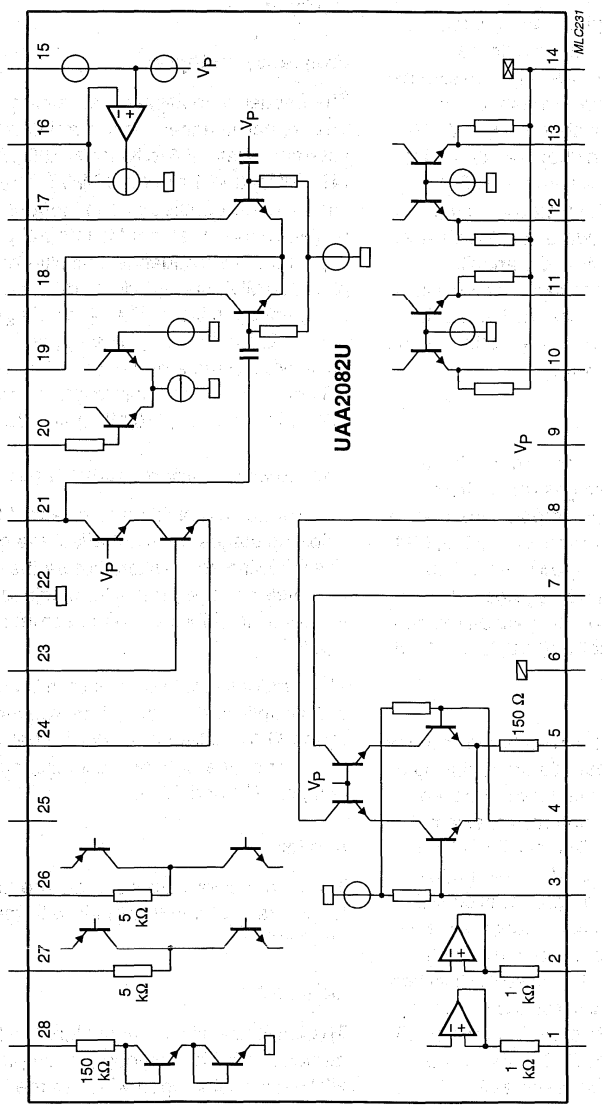


Fig.10 Internal circuits drawn for naked die.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Figs 1 to 6.

Radio frequency amplifier

The RF amplifier is an emitter-coupled pair driving a balanced cascode stage, which drives an external balanced tuned circuit. Its bias current is set by an external 300 Ω resistor R1 to typically 770 μA. With this bias current the optimum source resistance is 1.3 kΩ at VHF and 1.0 kΩ at UHF. At 930 MHz a higher bias current is required to achieve optimum gain. A value of 120 Ω is used for R1, which corresponds with a bias current of approximately 1.3 mA and an optimum source resistance of approximately 600 Ω.The capacitors C1 and C2 transform a 50 Ω source resistance to this optimum value. The output drives a tuned circuit with capacitive divider (C7, C8 and C9) to provide maximum power transfer to the phase-splitting network and the mixers.

Mixers

The double balanced mixers consist of common base input stages and upper switching stages driven from the frequency multiplier. The 300 Ω input impedance of each mixer acts together with external components (C10, C11; L4, L5 respectively) as phase shifter/power splitter to provide a differential phase shift of 90 degrees between the I channel and the Q channel. At 930 MHz all external phase shifter components are inductive (L10, L11; L4, L5).

Oscillator

The oscillator is based on a transistor in common collector configuration. It is followed by a cascode stage driving a tuned circuit which provides the signal for the frequency multiplier. The oscillator transistor requires an external bias voltage $V_{bias(osc)}$ (1.22 V typ.). The oscillator bias current (typically 250 μA) is determined by the 1.5 kΩ external resistor R5. The oscillator frequency is controlled by an external 3rd overtone crystal in parallel resonance mode. External capacitors between base and emitter (C17) and from emitter to ground (C16) make the oscillator transistor appear as having a negative resistance for small signals; this causes the oscillator to start. Inductance L9 connected in parallel with capacitor C16 to the emitter of the oscillator transistor prevents oscillation at the fundamental frequency of the crystal.

The resonant circuit at output pin OSC selects the second harmonic of the oscillator frequency. In other applications a different multiplication factor may be chosen.

At 930 MHz an external oscillator circuit is required to provide sufficient local oscillator signal for the frequency multiplier.

Frequency multiplier

The frequency multiplier is an emitter-coupled pair driving an external balanced tuned circuit. Its bias current is set by external resistor R4 to typically 190 μA (173 MHz), 350 μA (470 MHz) and 1 mA (930 MHz). The oscillator signal is internally AC coupled to one input of the emitter-coupled pair while the other input is internally grounded via a capacitor. The frequency multiplier output signal between pins VO1MUL and VO2MUL drives the upper switching stages of the mixers. The bias voltage on pins VO1MUL and VO2MUL is set by external resistor R3 to allow sufficient voltage swing at the mixer outputs. The value of R3 depends on the operating frequency: 1.5 kΩ (173 MHz), 820 Ω (470 MHz) and 330 Ω (930 MHz).

Low noise amplifiers, active filters and gyrator filters

The low noise amplifiers ensure that the noise of the following stages does not affect the overall noise figure. The following active filters before the gyrator filters reduce the levels of large signals from adjacent channels. Internal AC couplings block DC offsets from the gyrator filter inputs.

The gyrator filters implement the transfer function of a 7th order elliptic filter. Their cut-off frequencies are determined by the 47 kΩ external resistor R2 between pins RGYR and COM. The gyrator filter output signals are available on IF test pins TPI and TPQ.

Limiters

The gyrator filter output signals are amplified in the limiter amplifiers to obtain IF signals with removed amplitude information.

Demodulator

The limiter amplifier output signals are fed to the demodulator. The demodulator output DO is going LOW or HIGH depending upon which of the input signals has a phase lead.

Battery LOW indicator

The battery LOW indicator senses the supply voltage and sets its output HIGH when the voltage at input SENSE is less than V_{th} (typically 1.10 V). Low battery warning is available at BLI.

Band gap reference

The whole chip except the oscillator section can be powered-up and powered-down by enabling and disabling the band gap reference via the receiver enable pin RE.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
Ground pins GND1, GND2 and GND3 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	−0.3	+8.0	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−10	+70	°C
V_{es}	electrostatic handling (note 1)			
	pins VI1RF and VI2RF	−1500	+2000	V
	pin RRFA	−500	+2000	V
	pins VO1RF and VO2RF	−2000	+250	V
	pins V_P and OSB	−500	+500	V
	pins OSC and OSE	−2000	+500	V
	other pins	−2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor.

DC CHARACTERISTICS

V_P = 2.05 V; T_{amb} = −10 to +70 °C (typical values at T_{amb} = 25 °C); measurements taken in test circuit Fig.1, 2, 3 or 4 with crystal at pin OSB disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current	V_{RE} = HIGH; $f_{i(RF)}$ = 173 and 470 MHz	2.3	2.7	3.2	mA
		V_{RE} = HIGH; $f_{i(RF)}$ = 930 MHz	2.9	3.4	3.9	mA
$I_{P(off)}$	stand-by current	V_{RE} = LOW	–	–	3	µA
$V_{bias(osc)}$	oscillator bias voltage		1.20	1.22	1.24	V
Receiver enable input (pin RE)						
V_{IH}	HIGH level input voltage		1.4	–	V_P	V
V_{IL}	LOW level input voltage		0	–	0.3	V
I_{IH}	HIGH level input current	$V_{IH} = V_P$ = 3.5 V	–	–	20	µA
V_{IL}	LOW level input current	V_{IL} = 0 V	0	–	−1.0	µA
Battery LOW indicator output (pin BLI)						
V_{OH}	HIGH level output voltage	$V_{SENSE} < V_{th}$; I_{BLI} = −10 µA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	$V_{SENSE} > V_{th}$; I_{BLI} = +10 µA	–	–	0.5	V
V_{th}	voltage threshold for battery LOW indicator	V_P = 2.05 V; T_{amb} = 25 °C	1.05	1.10	1.15	V
		V_P = 2.05 to 3.5 V; T_{amb} = −10 to +70 °C	1.03	1.10	1.17	V
Demodulator output (pin DO)						
V_{OH}	HIGH level output voltage	I_{DO} = −10 µA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	I_{DO} = +10 µA	–	–	0.5	V

AC CHARACTERISTICS (173 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.1 or 2; $f_{i(RF)}$ = 172.941 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ±25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–126.5	–123.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–120.5	dBm
		V_P = 1.9 V	–	–	–117.5	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	69	72	–	dB
		T_{amb} = –10 to +70 °C	67	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	78	85	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (470 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.3 or 4; $f_{i(RF)}$ = 469.950 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–124.5	–121.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–118.5	dBm
		V_P = 1.9 V	–	–	–115.5	dBm
Mixer input						
$P_{i(mix)}$	input sensitivity	BER ≤ $^3/_{100}$; note 3	–	–115.0	–110.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	67	70	–	dB
		T_{amb} = –10 to +70 °C	65	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 4	75	82	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 5	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Test circuit Fig.5. $P_{i(mix)}$ is the maximum available power at the input of the test board. The bit error rate BER is measured using the test facility shown in Fig.12.
4. Δf is the frequency offset between the required signal and the interfering signal.
5. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (930 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.6 (note 1); $f_{i(RF)}$ = 930.500 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 2	–	–120.0	–114.0	dBm
		V_P = 1.9 V	–	–	–108.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	60	69	–	dB
α_c	co-channel rejection		–	5	10	dB
α_{sp}	spurious immunity		40	60	–	dB
α_{im}	intermodulation immunity		53	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	65	74	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz and a level of –15 dBm.
2. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

TEST INFORMATION

Tuning procedure for AC tests

1. Turn on the signal generator: $f_{gen} = f_{i(RF)} + 4$ kHz, no modulation, $V_{i(RF)} = 1$ mV (RMS).
2. Measure the IF with a counter connected to test pin TPI. Tune C16 to set the crystal oscillator to achieve $f_{IF} = 4$ kHz Change the generator frequency to $f_{gen} = f_{i(RF)} - 4$ kHz and check that f_{IF} is also 4 kHz. For a received input frequency $f_{i(RF)} = 172.941$ MHz the crystal frequency is $f_{XTAL} = 57.647$ MHz, while for $f_{i(RF)} = 469.950$ MHz the crystal frequency is $f_{XTAL} = 78.325$ MHz. For a received input frequency $f_{i(RF)} = 930.500$ MHz an external oscillator signal must be used with $f_{i(OSC)} = 310.1667$ MHz and a level of −15 dBm (for definition of crystal frequency, see Table 1).
3. Set the signal generator to nominal frequency ($f_{i(RF)}$) and turn on the modulation deviation ±4.0 kHz, 600 Hz square wave modulation, $V_{i(RF)} = 1$ mV (RMS). Note that the RF signal should be reduced in the following tests, as the receiver is tuned, to ensure $V_{o(IF)} = 10$ to 50 mV (p-p) on test pins TPI or TPQ.
4. Tune C15 (oscillator output circuit) and C12 (frequency multiplier output) to obtain a peak audio voltage on pin TPI.
5. Tune C3 and C6 (RF input and mixer input) to obtain a peak audio voltage on pin TPI. When testing the mixer input sensitivity tune C23 instead of C3 and C6 (test circuit Fig.5).
6. Check that the output signal on pin TPQ is within 3 dB in amplitude and at 90° (±20°) relative phase of the signal on pin TPI.
7. Check that data signal appears on output pin DO and proceed with the AC test.

AC test conditions

Table 5 Definitions for AC test conditions (see Table 6)

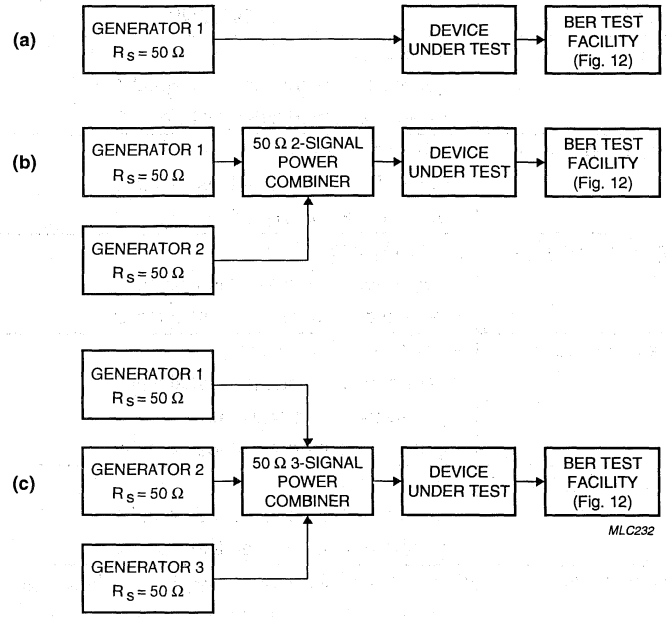
SIGNAL	DESCRIPTION
Modulated test signal 1	
Frequency	172.941, 469.950 or 930.500 MHz
Deviation	±4.0 kHz
Modulation	1200 baud pseudo random bit sequence
Rise time	250 ±25 µs (between 10% and 90% of final value)
Modulated test signal 2	
Deviation	±2.4 kHz
Modulation	400 Hz sine wave
Other definitions	
f_1	frequency of signal generator 1
f_2	frequency of signal generator 2
f_3	frequency of signal generator 3
Δf_{cs}	channel spacing (20 kHz)
P_1	maximum available power from signal generator 1 at the test board input
P_2	maximum available power from signal generator 2 at the test board input
P_3	maximum available power from signal generator 3 at the test board input
$P_{i(ref)}$	maximum available power at the test board input to give a Bit Error Rate (BER) $\leq 3/100$ for the modulated test signal 1, in the absence of interfering signals and under the conditions as specified in Chapters "AC characteristics (173 MHz)", "AC characteristics (470 MHz)" and "AC characteristics (930 MHz)"

Table 6 AC test conditions (notes 1 and 2)

SYMBOL	PARAMETER	CONDITIONS	TEST SIGNALS
α_a	adjacent channel selectivity; Fig.11(b)	$f_2 = f_1 \pm \Delta f_{CS}$	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{a(min)}$
α_c	co-channel rejection; Fig.11(b)	$f_2 = f_1 \pm$ up to 3 kHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 - \alpha_{c(max)}$
α_{sp}	spurious immunity; Fig.11(b)	f_2 = 100 kHz to 2 GHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{sp(min)}$
α_{im}	intermodulation immunity; Fig.11(c)	$f_2 = f_1 \pm \Delta f_{cs}$; $f_3 = f_1 \pm 2\Delta f_{cs}$	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: unmodulated	$P_2 = P_1 + \alpha_{im(min)}$
		generator 3: modulated test signal 2	$P_3 = P_2$
α_{bl}	blocking immunity; Fig.11(b)	$f_2 = f_1 \pm 1$ MHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{bl(min)}$
f_{offset}	frequency offset range; Fig.11(a)	deviation = ±4.0 kHz, $f_1 = f_{i(RF)} \pm 2$ kHz ($f_{offset(min)}$)	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
Δf_{dev}	deviation range; Fig.11(a)	deviation = ±2.5 to ±7 kHz; ($\Delta f_{dev(min)}$ to $\Delta f_{dev(max)}$)	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
t_{on}	receiver turn-on time; Fig.11(a)	note 3	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 10$ dB

Notes

1. The tests are executed without load on pins TPI and TPQ.
2. All minimum and maximum values correspond to a bit error rate (BER) $\leq 3/100$ in the wanted signal (P_1).
3. The BER measurement is started 5 ms ($t_{on(max)}$) after V_{RE} goes HIGH; BER is then measured for 100 bits (BER $\leq 3/100$).



(a) One generator.
(b) Two generators.
(c) Three generators.

Fig.11 Test configurations.

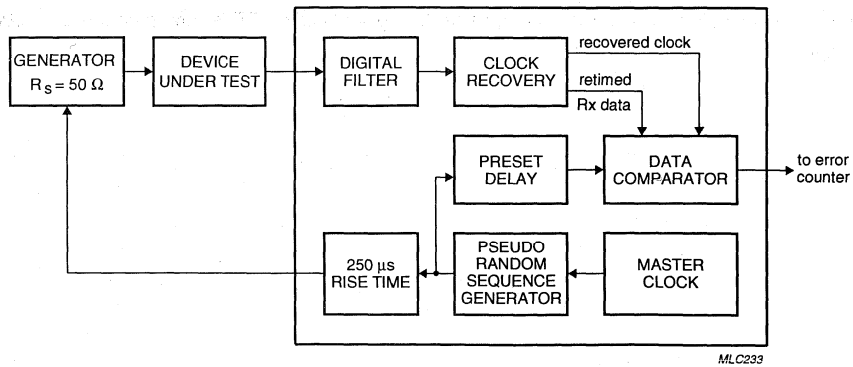


Fig.12 BER test facility.

PRINTED-CIRCUIT BOARDS

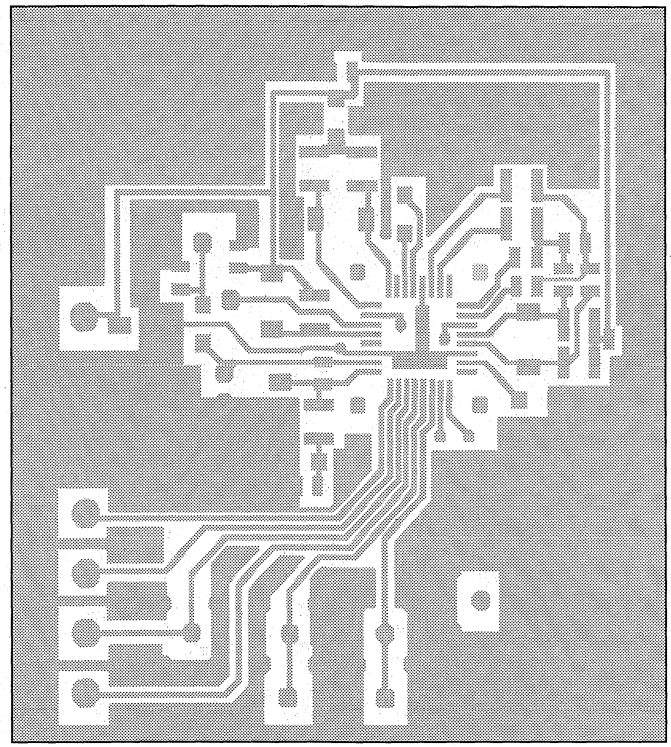


Fig.13 PCB top view for TQFP32; test circuit Figs 1 and 3.

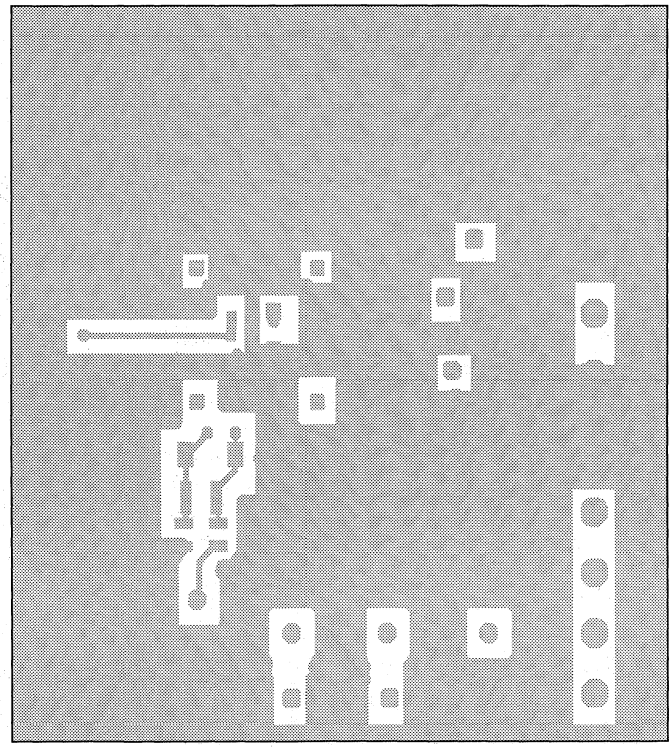
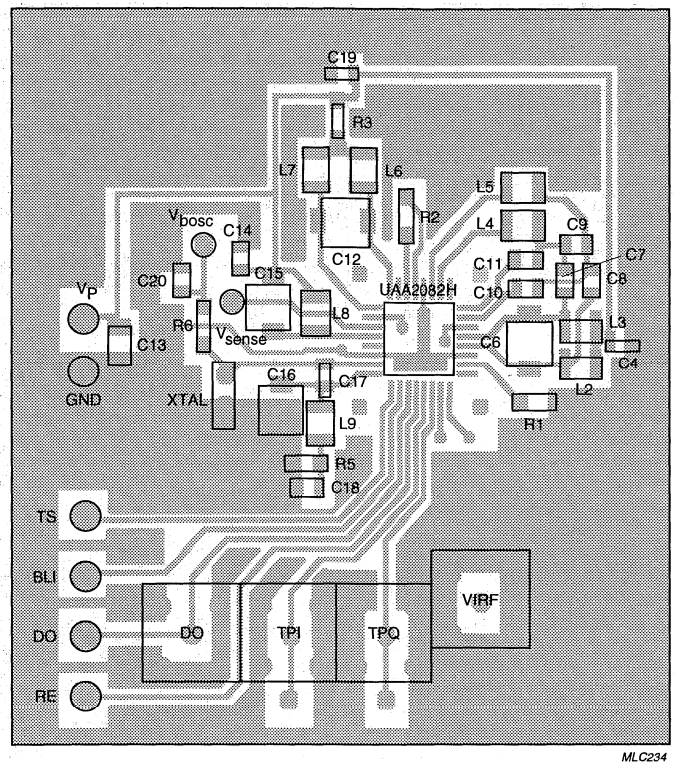


Fig.14 PCB bottom view for TQFP32; test circuit Figs 1 and 3.



V_{EE} = GND; V_C = V_P.

Fig.15 PCB top view with components for TQFP32; test circuit Fig.3.

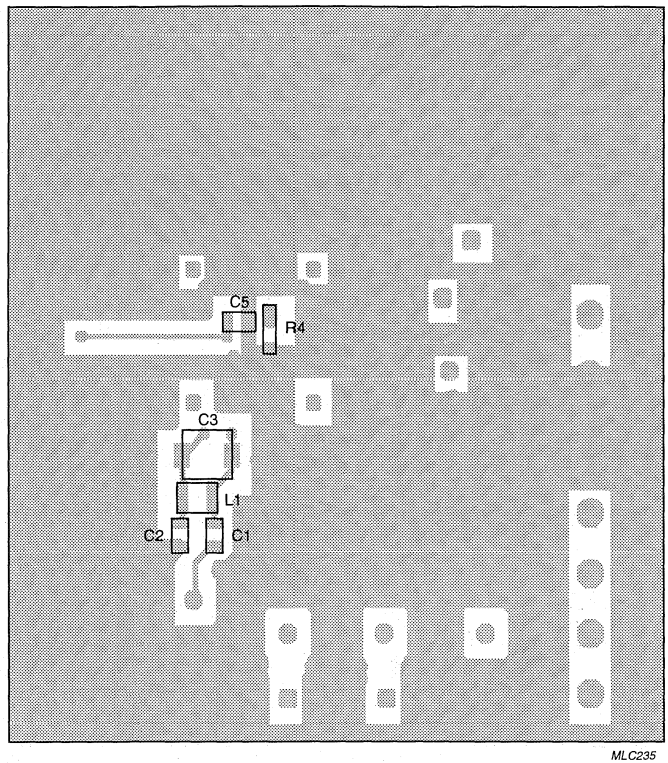


Fig.16 PCB bottom view with components for TQFP32; test circuit Fig.3.

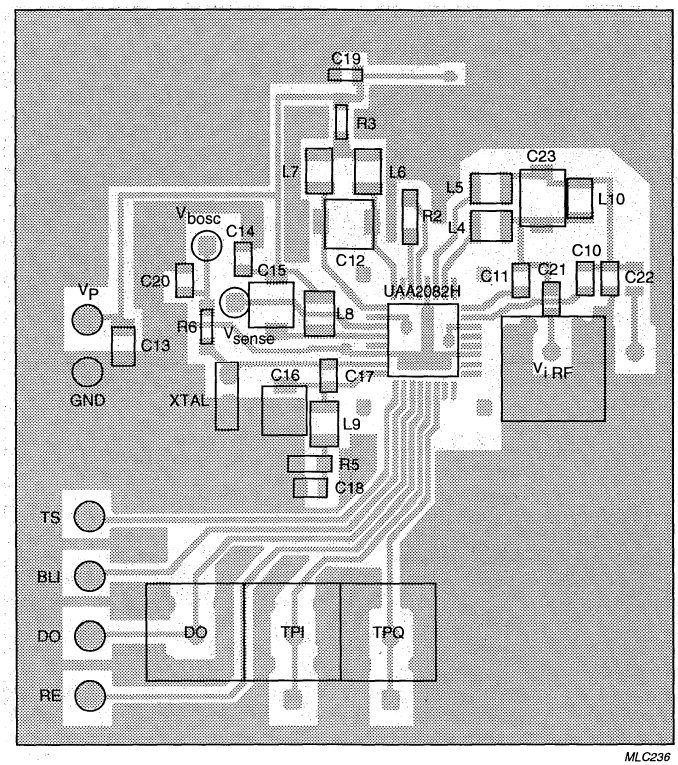


Fig.17 PCB top view with components for TQFP32; test circuit Fig.5.

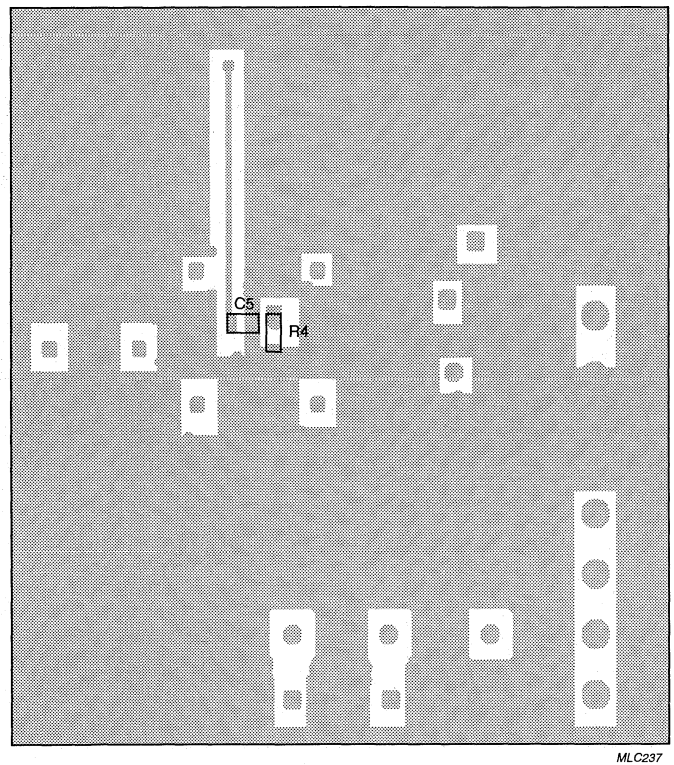


Fig.18 PCB bottom view with components for TQFP32; test circuit Fig.5.

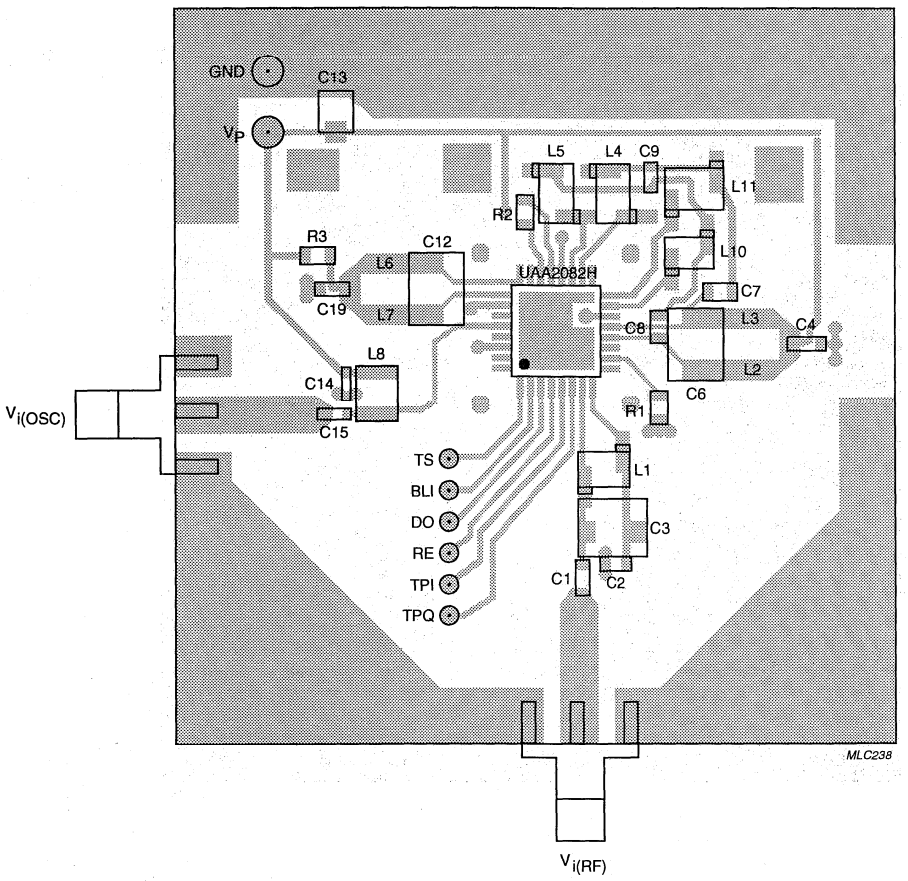


Fig.19 PCB top view with components for TQFP32; test circuit Fig.6.

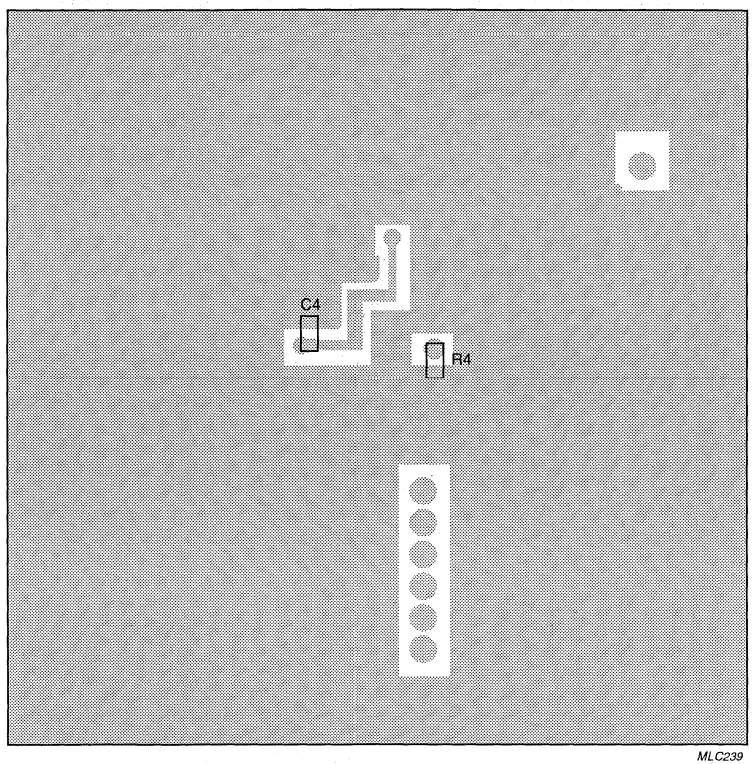


Fig.20 PCB bottom view with components for TQFP32; test circuit Fig.6.

Line interrupter driver and ringer UBA1702; UBA1702A

FEATURES

Speech part

- Driver for the line interrupter that can be either a PMOST when UBA1702 is used or a PNP when UBA1702A is used
- Adjustable over-current protection
- Adjustable over-voltage protection for transmission circuit
- Adjustable mute (dialling mode voltage; DMO or NSA)
- Adjustable current loop detection (hook-switch status)
- Microcontroller supply
- Provision for electronic hook-switch.

Ringer part

- Over-voltage protection
- Ringer frequency output for frequency discrimination
- Adjustable ringer threshold for piezo-driver enable
- Three bits ringer volume control
- Bridge-tied-load output stage for piezo transducer
- Fast start-up microcontroller supply.

Miscellaneous

- Separated ground pins for transmission circuit interface and control signals (e.g. for TEA1064A)
- Possibility to supply the microcontroller with an external voltage source.

APPLICATIONS

- Telephone sets with software controlled ringer function
- Telephone sets with electronic hook-switch.

DESCRIPTION

The UBA1702; UBA1702A performs the high voltage interface and ringer functions of the corded analog telephone set in close co-operation with a microcontroller and transmission circuit.

The UBA1702; UBA1702A incorporates several protections, a driver for the line interrupter and a ringer. Because of the practical division of functions between the microcontroller, the transmission circuit and the UBA1702; UBA1702A, it is possible to have a higher integration level reducing significantly the number of discrete components in a telephone set.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA1702	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
UBA1702A	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
UBA1702T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UBA1702AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

Speech part: I_{line} = 20 mA; DPI = LOW; T_{amb} = 25 °C; V_{EE} = 0 V; unless otherwise specified.
Ringer part: $V_{line(rms)}$ = 45 V; f = 25 Hz; using an R-C combination of 2.2 kΩ and 820 nF and a diode bridge between the line and the RPI input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Speech part						
SWITCH DRIVER AND REFERENCES (SDI, SDO, EHI AND DPI); UBA1702A ONLY						
R_{SDO}	resistance between SDO and V_{EE}	V_{SDO} < 15 V	–	2	–	kΩ
SWITCH DRIVER AND REFERENCES (SDI, SDO, EHI AND DPI); UBA1702 AND UBA1702A						
$R_{SDI/O}$	resistance between SDI and SDO	$V_{SDI/O}$ < 10 V	–	1	–	MΩ
R_{SDI}	resistance between SDI and V_{EE}	V_{SDI} = 240 V; DPI = HIGH	5	–	–	MΩ
MUTE SWITCH AND ADJUSTABLE PROTECTION ZENER VOLTAGE (MSI, MSA AND ZPA)						
$V_{SPO(M)}$	adjustable mute voltage referenced to V_{EE}	MSI = HIGH; MSA open-circuit	–	tbf	3	V
$V_{SPO(Z)}$	adjustable Zener voltage referenced to V_{EE}	MSI = LOW; ZPA open-circuit	tbf	12	tbf	V
CURRENT LIMITING AND DETECTION (SPI, SPO, CDA, CLA AND CDO)						
$I_{SPI(lim)}$	SPI current limitation	CLA short-circuited to V_{EE}	–	140	–	mA
$I_{SPI(det)}$	SPI current detection	CDA open-circuit	2	3	5	mA
MICROCONTROLLER SUPPLY (V_{DD}, V_{BB})						
V_{DD}	output supply voltage referenced to V_{SS}	V_{BB} > 3.7 V; I_{DD} = –1 mA	–3.0	–3.3	–3.6	V
Ringer part						
PROTECTION (RPI)						
I_{RPI}	maximum input current		70	–	–	mA
RINGER THRESHOLD AND FREQUENCY DETECTION (V_{RR}, RTA, RFO)						
$V_{RR(th)}$	ringer threshold voltage referenced to V_{EE}	RTA open-circuit	–	10.5	–	V
VOLUME CONTROL (RV0, RV1 AND RV2)						
ΔG_s	step resolution	RV2, RV1 and RV0: from 0 0 0 to 1 1 0; note 1	–	6	–	dB
ΔG_s	last step resolution	RV2, RV1, RV0: from 1 1 0 to 1 1 1; note 2	–	–	10	dB
RINGER MELODY INPUT AND PIEZO DRIVER (RMI, ROA AND ROB)						
$V_{ROA(p-p)}$ $V_{ROB(p-p)}$	maximum output voltage (peak-to-peak value)	RV2, RV1 and RV0 = 1 1 1	–	–	32	V

Notes

1. Independent of V_{RR} if >10 V.
2. Without piezo transducer, dependent on V_{RR}.

BLOCK DIAGRAM

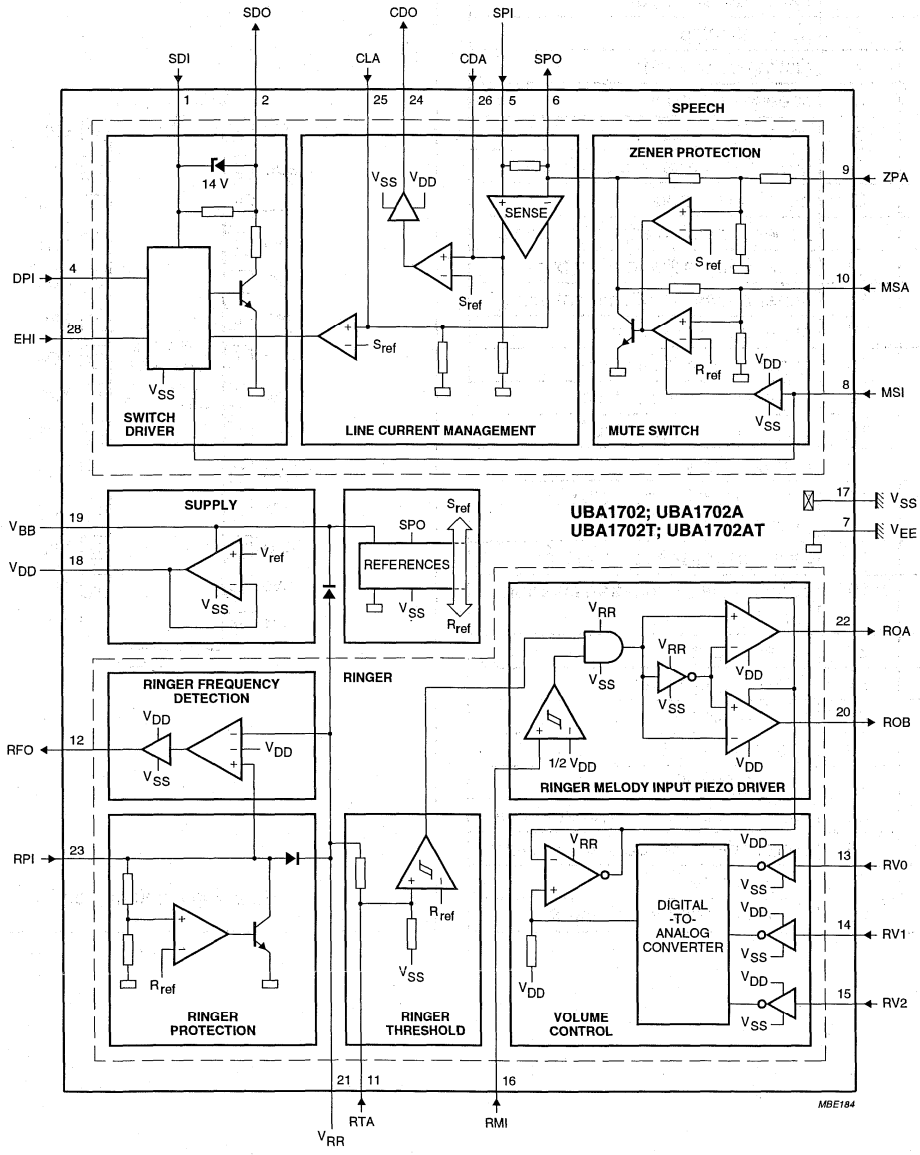


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDI	1	switch driver input
SDO	2	switch driver output
n.c.	3	not connected
DPI	4	dialling pulse input
SPI	5	speech part input
SPO	6	speech part output
V_{EE}	7	ground for transmission circuit
MSI	8	mute switch input
ZPA	9	Zener protection adjustment input
MSA	10	mute switch adjustment input
RTA	11	ringer threshold adjustment input
RFO	12	ringer frequency output
RV0	13	ringer volume input; bit 0
RV1	14	ringer volume input; bit 1
RV2	15	ringer volume input; bit 2
RMI	16	ringer melody input
V_{SS}	17	ground for microcontroller and ringer
V_{DD}	18	microcontroller supply voltage
V_{BB}	19	supply voltage from transmission circuit
ROB	20	ringer output B
V_{RR}	21	ringer supply voltage
ROA	22	ringer output A
RPI	23	ringer part input
CDO	24	current detection output
CLA	25	current limitation adjustment input
CDA	26	current detection adjustment input
n.c.	27	not connected
EHI	28	electronic hook-switch input

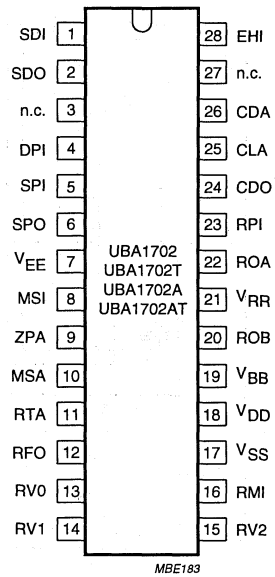


Fig.2 Pin configuration.

Data processor for cellular radio (DPROC)

UMA1000LT

FEATURES

- Single chip solution to all the data handling and supervisory functions
- Configuration to both AMPS and TACS
- I²C serial bus control
- All analog interface and filtering functions fully implemented on chip
- Error handling in hardware reduces software requirements
- Robust SAT decoding and transponding circuitry
- Low current consumption
- Small physical size
- Minimum external peripheral components required.

GENERAL DESCRIPTION

The UMA1000LT is a low power CMOS LSI device incorporating the data tranceiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pin 28)	3.0	5.0	5.5	V
I_{DD}	supply current (pin 28) normal operation with external clock	–	2.5	–	mA
T_{amb}	operating ambient temperature	–30	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1000LT	28	SO28	plastic	SOT136A

Data processor for cellular radio (DPROC)

UMA1000LT

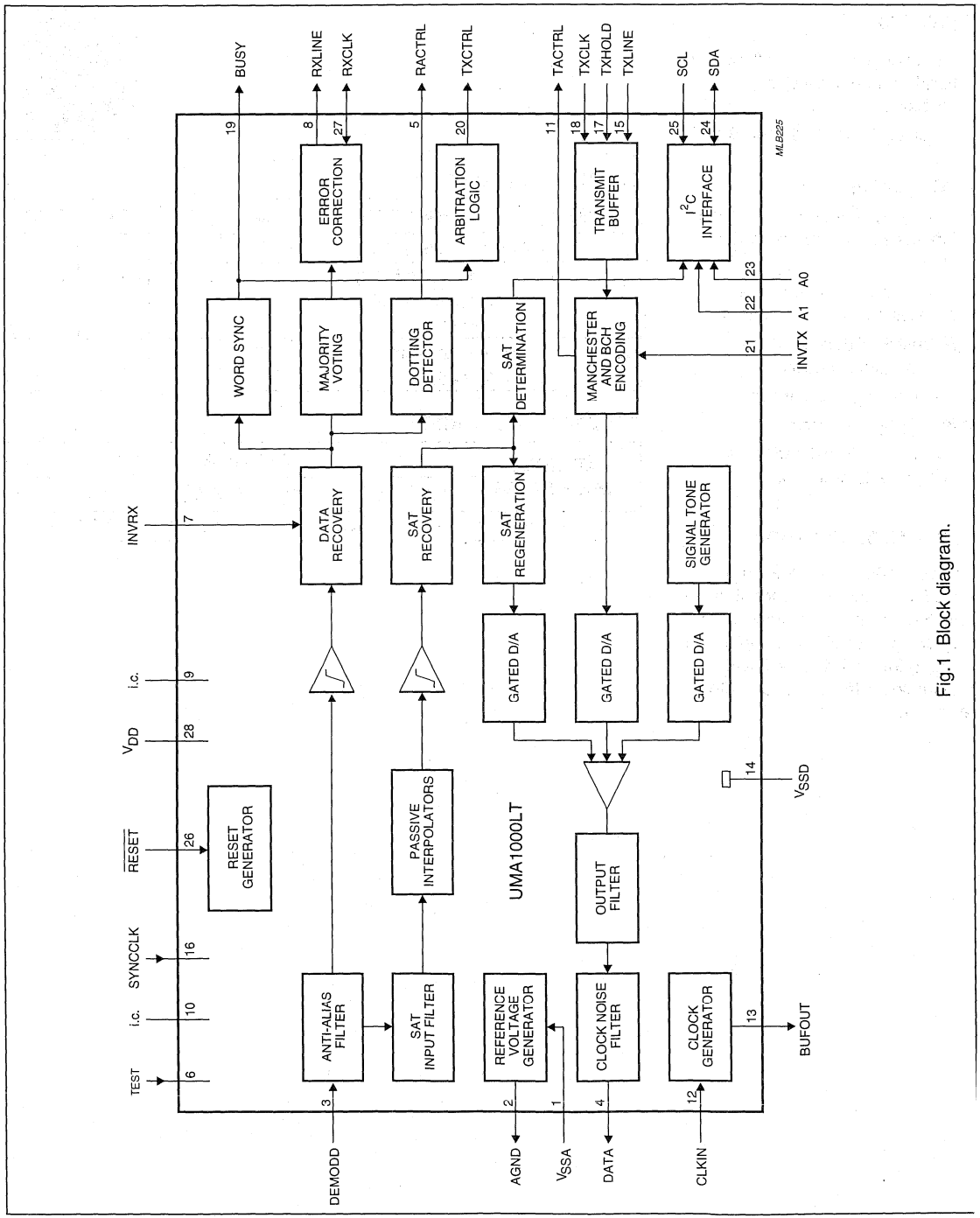


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA}	1	analog negative supply (0 V)
AGND	2	$(V_{DD} - V_{SSA})/2$ analog reference ground
DEMODD	3	received data signal input
DATA	4	transmitted data signal output
RACTRL	5	received audio control output
TEST	6	SCAN control input; used for power-on reset
INVRX	7	inverts sense of received data stream
RXLINE	8	received data signal output
i.c	9	internally connected; must be left open-circuit
i.c	10	internally connected; must be left open-circuit
TACTRL	11	transmitter audio control output
CLKIN	12	1.2 MHz external master clock input
BUFOUT	13	buffered output of internal clock oscillator
V_{SSD}	14	digital ground
TXLINE	15	transmitted data signal
SYNCCLK	16	SCAN CLOCK control input; used for power-on reset
TXHOLD	17	holds off transmission of data
TXCLK	18	transmitted data clock input
BUSY	19	reverse control channel status output
TXCTRL	20	transmitter control output
INVTX	21	inverts sense of transmitted data stream
A1	22	address input 1; used for power-on reset (I^2C-bus)
A0	23	address input 0 (I^2C-bus)
SDA	24	serial data input/output (I^2C-bus)
SCL	25	serial clock input (I^2C-bus)
$\overline{RESET}$	26	master reset input
RXCLK	27	received data clock input
V_{DD}	28	supply voltage (+5 V)

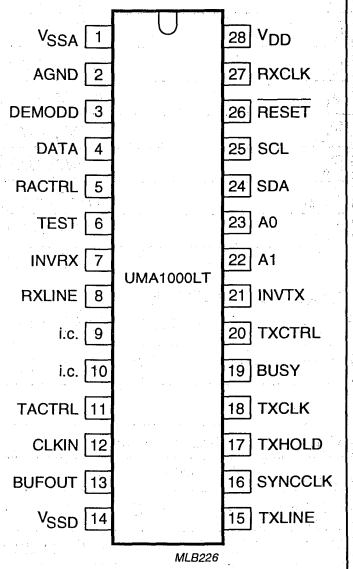


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+8.0	V
I_{DD}	supply current	–	50	mA
I_I	DC current (any input)	–	±10	mA
I_O	DC current (any output)	–	±10	mA
V_I	all input voltages	−0.8	V_{DD}+0.8	V
P_{tot}	total power dissipation	–	300	mW
P_o	power dissipation per output	–	50	mW
T_{amb}	operating ambient temperature	−30	+70	°C
T_{stg}	storage temperature	−65	+150	°C

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = −30 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	normal operation; note 1	–	2.5	–	mA
Digital inputs (note 2)						
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}+0.3	V
C_I	input capacitance		–	–	6	pF
Digital outputs (note 2)						
V_{OL}	LOW level output voltage	I_{sink} = 1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = 1 mA	V_{DD}−0.4	–	–	V
Open-drain outputs (note 3)						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	–	0.4	V
Open-drain SDA						
V_{OL}	LOW level output voltage	I_{sink} = 3 mA	–	–	0.4	V

Notes

1. 1.2 MHz clock on CLKIN, SYNCCLK HIGH, outputs unloaded analog part operating.
2. All digital inputs and outputs of DPROC are compatible with standard CMOS devices and the following general characteristics apply.
3. Open-drain outputs have no internal pull-up resistors.

FUNCTIONAL DESCRIPTION

General

The UMA1000LT (DPROC) is a single-chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.

These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction, decoding and encoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation.

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels. Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticeable by the user. A data rate of 10 kbits/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig.3.

A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz), is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analogous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the 'loop'. At the base station this signal is used to ascertain the overall quality of the communication link.

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

The key requirements of a hand-held portable cellular set are:

- Small physical size
- Minimum number of interconnections (serial bus)
- Low power consumption
- Low cost.

The DPROC is a member of our Cellular Radio chip set, based on the I²C-bus, which meets these requirements. A cellular radio system schematic using the chip set is shown in Fig.4.

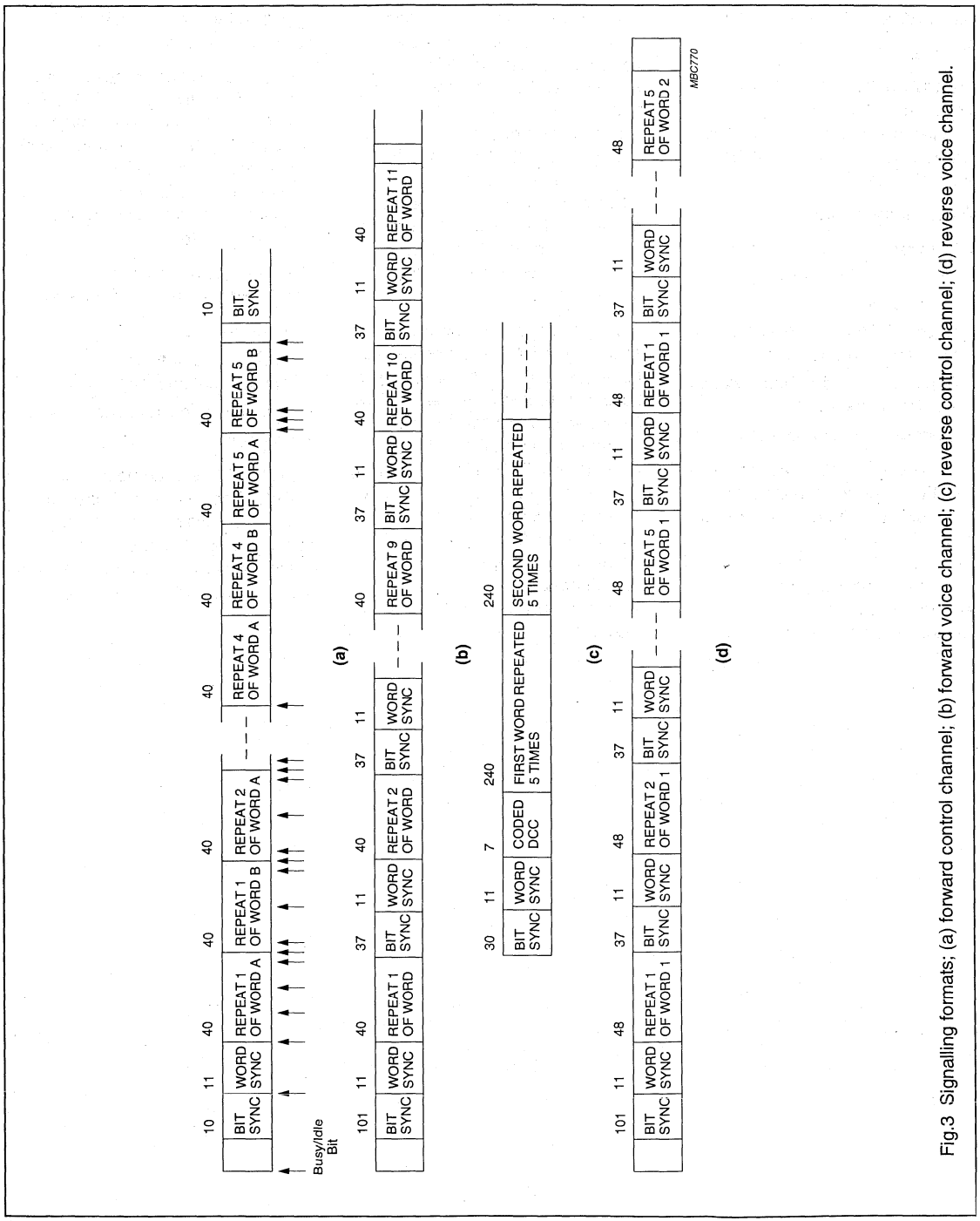


Fig.3 Signalling formats; (a) forward control channel; (b) forward voice channel; (c) reverse control channel; (d) reverse voice channel.

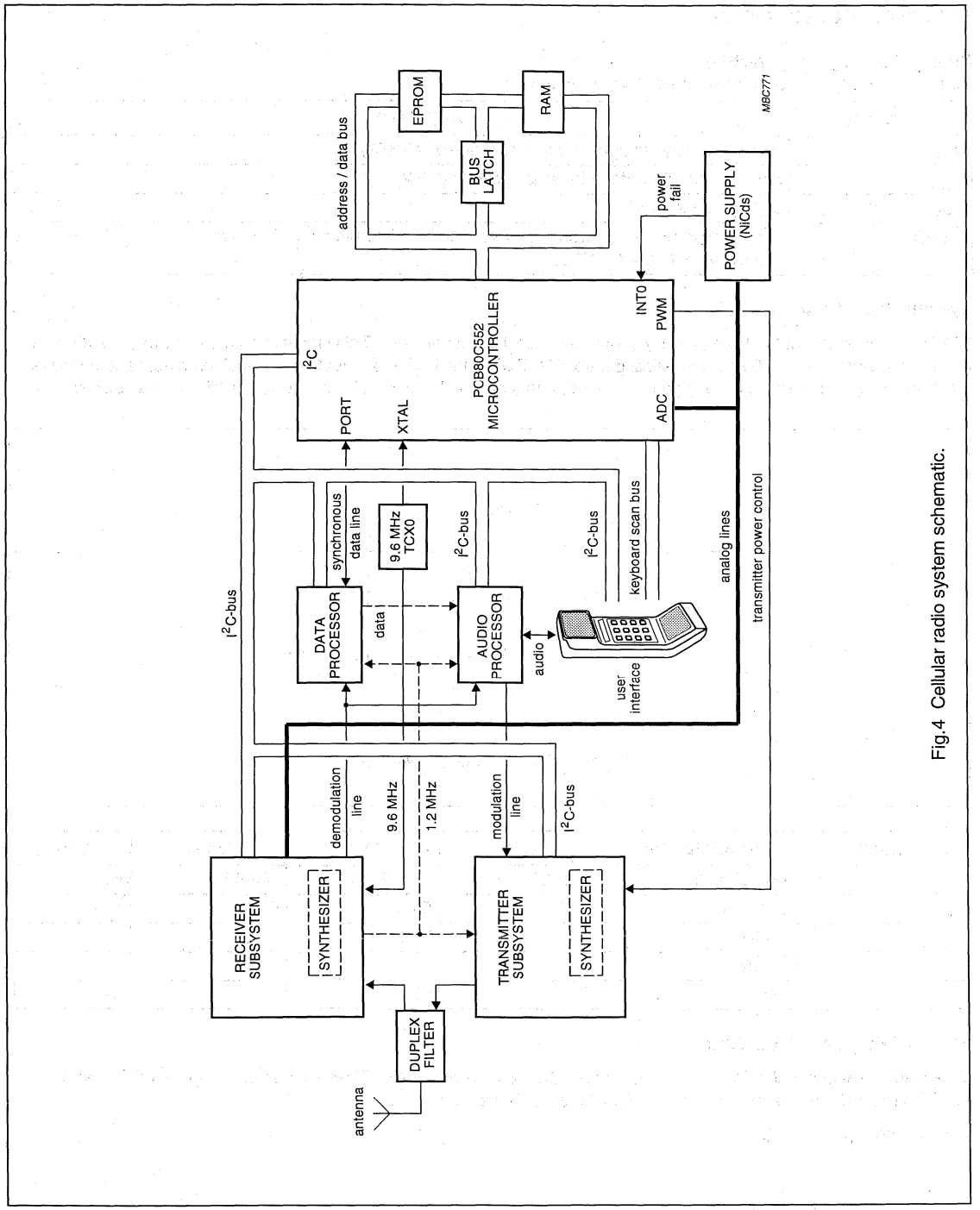


Fig.4 Cellular radio system schematic.

EXTERNAL PIN DESCRIPTION

Supply (V_{DD}; V_{SSA}; V_{SSD}; AGND)

Both V_{SSA} and V_{SSD} must be connected to common ground.

SYMBOL	DESCRIPTION
V_{DD}	positive supply voltage for digital and analog circuitry
V_{SSA}	negative supply voltage for analog circuitry (0 V)
V_{SSD}	digital ground (0 V)
AGND	internally generated reference ground based by internal analog circuitry; voltage level $(V_{DD}-V_{SSA})/2$ ±2%

System clock (CLKIN; BUFOUT)

CLKIN is a digital input for the externally generated 1.2 MHz master clock. This signal should be accurate to 100 x 10^{-6} and have a worst case of 60:40 mark-space ratio. BUFOUT is the buffered output of the clock oscillator and provides the option of generating the clock signal on chip by connecting a 1.2 MHz crystal between BUFOUT and CLKIN.

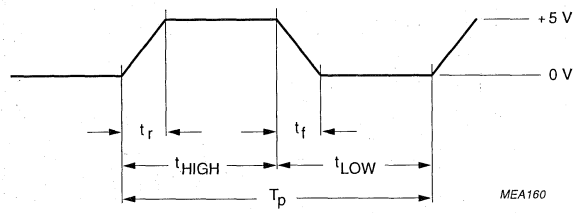


Fig.5 System clock timing diagram.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
T_p	clock period time	833.25	833.33	833.42	ns
t_{HIGH}	HIGH time	40%	50%	60%	T_p
t_{LOW}	LOW time	–	T_p-t_{HIGH}	–	
t_r	rise time	–	50	–	ns
t_f	fall time	–	50	–	ns

I²C serial data link (SDA; SCL)

SDA is the bi-directional data line; SCL the clock input from an I²C master. These constitute a typical I²C link and conform to standard characteristics as defined in the I²C-bus specification.

- Data rate: up to 100 kbits/s

Slave Address Select (A0; A1)

Selection of the device slave address is achieved by connecting A0 to either V_{SSD} or V_{DD} and connecting A1 to either pin 16 and pin 6 or to V_{DD}. The slave address is defined in accordance with the I²C specifications as shown in Fig.6.

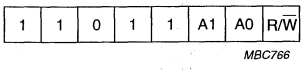


Fig.6 Device slave address.

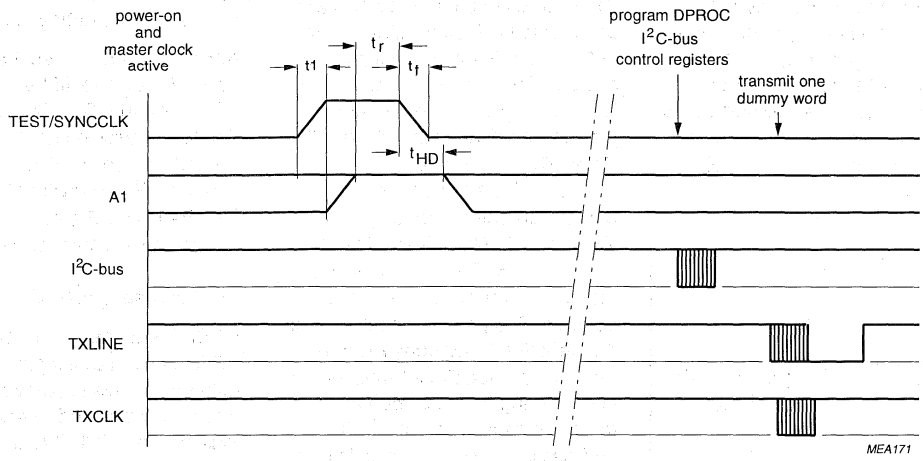
Power-up state

DPROC will not respond reliably to any inputs (including $\overline{\text{RESET}}$) until 100 µs after the power supply has settled within the specified tolerance. The analog sections of the device will have stabilized within 5 ms. No power-on reset is provided, therefore before the device can enter normal operation TEST and SYNCCLK must be pulsed HIGH. The reset pulse on these pins must have a minimum period of 250 µs and the fall time of the negative going edge must be faster than 1 µs. Pin A1 must remain HIGH during this reset period therefore if the A1 bit of the I²C address is required to be logic 0. A1 may be connected to TEST and SYNCCLK. If it is required to be at logic 1 then A1 may be permanently connected to V_{DD}. If it is required that A0 = logic 1, then a normal master reset (pin 26) sequence must follow the power-on reset sequence to get the internal registers in the defined state.

After the power-on reset a dummy transmission should be made to initiate internal DPROC counters. This transmission should be made with arbitration (ABREN) disabled and the RF transmitter stage switched OFF. Figure 7 shows the power-on reset sequence.

Master reset ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ is an asynchronous active LOW master reset input, with a minimum active pulse width of 2 µs which may be used to reset certain logic within DPROC to a predefined state as illustrated in Tables 1 and 2. Alternatively, DPROC may be set into a known initial state be setting the I²C control register as required. The internal reset sequence after a negative pulse on $\overline{\text{RESET}}$ takes 250 µs.



Where:

t1 = time not critical

t_r = reset time = 250 µs maximum

t_f = pulse fall time = 1 µs maximum

t_{HD} = A1 hold time = 0 µs minimum

Note

The RF transmitter is OFF during reset sequence.

Fig.7 Power-on reset programming sequence.

Table 1 Predefined state of the digital output pins.

OUTPUT	STATE
RXLINE	HIGH
TXCTRL	HIGH
TACTRL	HIGH
RACTRL	HIGH
BUSY	HIGH

Table 2 Predefined state of I²C registers.

REGISTER	BIT							
	7	6	5	4	3	2	1	0
Control	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
SATD	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
TST	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

Data Transfer Link (RXLINE; TXLINE; TXHOLD; TXCLK and RXCLK)

RXLINE, TXLINE, TXCLK and RXCLK provide a dedicated serial data link for the transfer of system data messages between DPROC and the system controller at variable rates of up to 200 kbits/s.
TXHOLD allows the system controller to preload the DPROC transmit register with one word without the data being transmitted. DPROC then starts transmitting the instant TXHOLD is driven LOW.

- RXCLK: clock input from system controller
- RXLINE: data output from DPROC to system controller
- TXCLK: clock input from system controller
- TXLINE: open drain data bi-directional line to the system controller
- TXHOLD: (HIGH) holds off transmission of data
- Data rate: up to 200 kbits/s

Note

A minimum mean data transfer rate for the received data of 2.1 kbits/s (AMPS) and 1.7 kbits/s (TACS) is required to ensure contiguity of message words.

The format for received and transmitted data words is shown in Fig.15(a) and Fig.15(b) respectively. The receive and transmit data timing is illustrated in Fig.16(a) and Fig.16(b) respectively.

Transmitter Control (TXCTRL)

TXCTRL is an open-drain output used to disable the transmitter during a Reverse Control Channel access failure.

- output level HIGH: RF enable
- output level LOW: RF disable

Transmitter Audio Enable (TACTRL)

TACTRL is an open-drain digital output signal used to blank the audio path and enable the data path to the modulator during data bursts on the Reverse Voice Channel.

- output level HIGH: audio enabled
- output level LOW: audio muted

Receiver Audio Enable (RACTRL)

RACTRL is an open-drain digital output used to blank the audio path to the earpiece when a sequence of dotting and word sync is detected.

RACTRL and TACTRL functions can be combined using one line.

- output level HIGH: audio enabled
- output level LOW: audio muted

Reverse Control Channel Status (BUSY)

BUSY is a digital output giving the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits and has the following logic levels:

- output level HIGH: channel busy
- output level LOW: channel idle

On a voice channel BUSY indicates channel idle.

Invert Receive Data (INVRX)

Enables an additional inverter in the receive data path. This allows RF demodulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC depends on the receiver local oscillator.

- input HIGH: data inverted
- input LOW: data normal

Invert Transmit Data (INVTX)

Enables an additional inverter in the transmit data path. This allows RF modulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator.

- input HIGH: data inverted
- input LOW: data normal

Transmitted Data Output (DATA)

Data is an analog output which provides Manchester encoded and filtered data signal SAT and signalling tone. This signal should normally be AC coupled into the Audio/Data summer.

- DC level: analog ground (AGND)
- signal level: $\frac{2}{5}V_{DD}$ V (p-p) for signalling tone; signal level with filtered data signal
- signal tolerance: 2% + supply voltage variation (ΔV_{DD})
- minimum load capacitance: 10 kΩ
- maximum load capacitance: 2 nF
- maximum output impedance: 50 Ω

Received Data Input (DEMODD)

Demodd inputs analog data and SAT signals from the RF demodulator. This pin should normally be AC coupled.

- DC level: analog ground (AGND)
- maximum data level: $\frac{V_{DD}}{5}$ x 1 V (p-p)
- nominal data level: $\frac{V_{DD}}{5}$ x 250 mV (p-p)
- minimum data level: $\frac{V_{DD}}{5}$ x 200 mV (p-p)
- minimum SAT level: 50 mV (p-p)
- input impedance: min. 1 MΩ

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig.12.

Where:

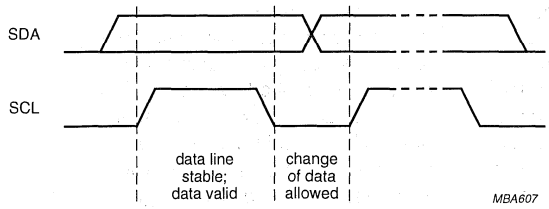


Fig.8 Bit transfer.

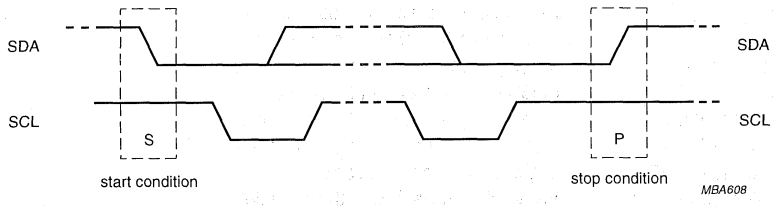


Fig.9 Definition of start and stop conditions.

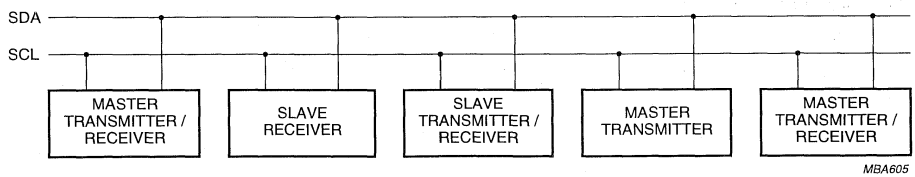


Fig.10 System configuration.

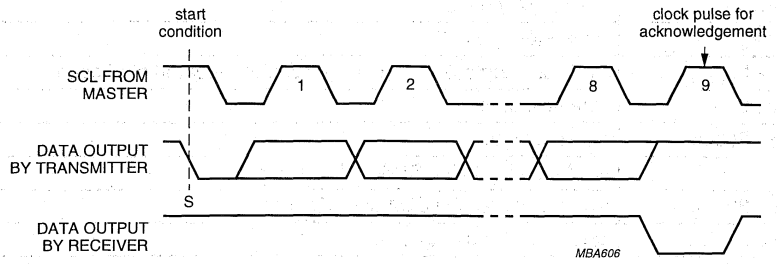


Fig.11 Acknowledgement on the I²C-bus.

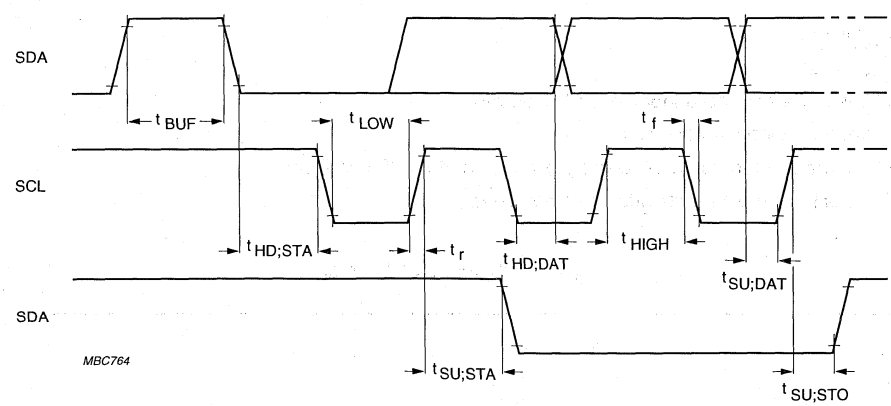
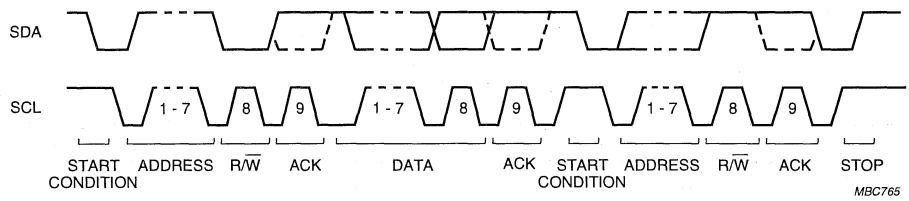


Fig.12 Timing.

All the values refer to 10% and 90% levels with a voltage swing of V_{DD} to V_{SS}.

SYMBOL	TIMING	DESCRIPTION
t_{BUF}	$t \geq t_{LOW(min)}$	the minimum time the bus must be free before a new transmission can start
$t_{HD;\ STA}$	$t \geq t_{HIGH(min)}$	start condition hold time
$t_{LOW(min)}$	4.7 µs	clock LOW period
$t_{HIGH(min)}$	4 µs	clock HIGH period
$t_{SU;\ STA}$	$t \geq t_{LOW(min)}$	start condition set-up time, only valid for repeated start code
$t_{HD;\ DAT}$	$t \geq 0$ µs	data hold time
$t_{SU;\ DAT}$	$t \geq 250$ ns	data set-up time
t_r	$t \leq 1$ µs	rise time of both the SDA and SCL line
t_f	$t \leq 300$ ns	fall time of both the SDA and SCL line
$t_{SU;\ STO}$	$t \geq t_{LOW(min)}$	stop condition set-up time



Where:

Clock $t_{LOW(min)}$: 4.7 µs

Clock $t_{HIGH(min)}$: 4 µs

The dashed line is the acknowledgement of the receiver

Maximum number of bytes: unrestricted

Premature termination of transfer: allowed by generation of STOP condition

Acknowledge clock bit: must be provided by the master.

Fig.13 Complete data transfer.

I²C REGISTERS

General

The I²C register block resides internally within the I²C interface block and contains various items of status and control information which are transferred to and from DPROC via the I²C-bus. The block is organized into four 8-bit registers:

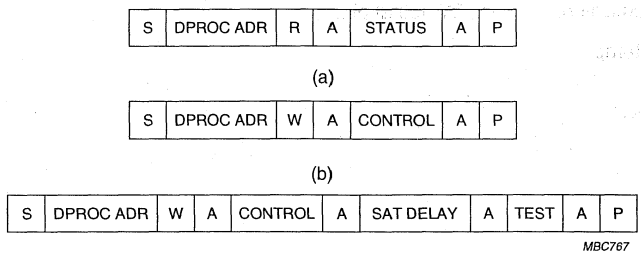
- Status Register: contain read only items
- Control Register: contain write only items
- SAT Programmable Phase Shift Register: contain write only items
- TEST Register

Note

In normal operation the SAT delay register and the TEST register require programming only after a device reset.

Table 3 Register map.

REGISTER	BIT							
	7	6	5	4	3	2	1	0
Status	–	–	WYNSC	BUSY	TXABRT	TXIP	MSCC1	MSCC0
Control	–	SERV	STS	TXRST	ABREN	FVC	STEN	SATEN
SATD	<----------SAT delay data---------->							



Where:

S: START condition

W: read/write bit (logic 0 = write)

R: read/write bit (logic 1 = read)

A: acknowledge bit

P: STOP condition

DPROC ADR: slave address of DPROC

TEST: must be programmed to logic 0 for normal operation.

Fig.14 I²C data format; (a) read from DPROC status register; (b) write to DPROC control register; (c) write to all DPROC registers.

Status Register

This is read only register containing DPROC status information.

MEASURED SAT COLOUR CODE (MSCC1; MSCC0)

MSCC1 and MSCC0 provide information about the current measured SAT colour code in accordance with Table 4.

Table 4 Measured SAT colour code.

MSCC1	MSCC0	SAT frequency (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

TRANSMISSION IN PROGRESS (TXIP)

TXIP indicates whether DPROC is currently accessing the Reverse Control or Voice Channels.

- logic 1: data transmission in progress
- logic 0: transmission not in progress

TRANSMISSION ABORT STATUS (TXABRT)

TXABRT indicates that a Reverse Control Channel Access Attempt has been aborted by DPROC without successful message transmission.

- logic 1: transmission attempt aborted
- logic 0: no access collision detected

REVERSE CONTROL CHANNEL STATUS (BUSY)

BUSY gives the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits on the Forward Control Channel.

- logic 1: channel busy
- logic 0: channel idle

On a voice channel the BUSY bit defaults to the set state.

Note

This signal is also routed to the BUSY output pin.

WORD SYNCHRONIZATION INDICATOR (WSYNC)

WSYNC indicates whether DPROC has acquired frame synchronization according to the Forward Control Channel format.

- logic 1: frame synchronization acquired
- logic 0: no frame synchronization

Control Register

This is a write only register containing DPROC control information.

SAT PATH ENABLE (SATEN)

SATEN enables the SAT transponded signal to be output on external pin DATA.

- logic 1: SAT tone enabled
- logic 0: SAT tone inhibited

SIGNALLING TONE (ST) PATH ENABLE (STEN)

STEN enables the Signalling Tone to be output on external pin DATA.

- logic 1: ST enabled
- logic 0: ST inhibited

CHANNEL FORMAT SELECT (FVC)

FVC selects the required channel format.

- logic 1: voice channel format
- logic 0: control channel format

TRANSMISSION ABORT PERMISSION (ABREN)

ABREN indicates whether DPROC has permission to abort data transmission and disable RF on the Reverse Control Channel following the detection of a channel access attempt collision.

- logic 1: RF disable allowed
- logic 0: RF disable inhibited

MESSAGE TRANSMISSION ABORT (TXRST)

TXRST terminates a message being transmitted on the reverse channel. It is a monostable signal which when activated causes a reset of the message transmission circuitry and causes TXABRT and TXIP I²C signals to be reset.

This signal does not clear the DPROC transmit register; therefore if a word has been loaded into DPROC after a TXABRT has occured the control line TXHOLD should be held LOW to allow the word to be cleared from the DPROC input register.

- logic 1: reset active
- logic 0: reset inactive

SYSTEM TYPE SELECT (STS)

STS selects required system format.

- logic 1: AMPS
- logic 0: TACS

Note

Toggling this signal also resets the receive logic in DPROC.

SERVING SYSTEM SELECT (SERV)

SERV selects which of the serving system data streams (A or B) is accepted.

- logic 1: system A selected
- logic 0: system B selected

SAT PROGRAMMABLE DELAY REGISTER (SATD)

SATD programs the value of phase shift which is applied to the SAT tones in the SAT Regeneration Block. This value will be determined and programmed into the System Controller during manufacture. The recovered SAT is delayed in time by approximately 0.8 µs x value in the register which corresponds to approximately 1.8 degrees x value in the register. The total phase shift is limited to 360 degrees.

The ability to adjust SAT phase angle is not necessary in current AMPS and TACS systems. Therefore this register should normally be in AMPS and TACS, this function is not necessary and should programmed to zero.

DIGITAL CIRCUIT BLOCKS

General

The majority of the digital circuitry within the DPROC device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig.1.

Data Recovery

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Strobed Comparator Block, on which it performs the following functions:

- clock recovery
- Manchester decoding
- data regeneration

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase-locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable 'bandwidth' to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1.2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output. The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a 1 otherwise it is latched as a 0.

SAT Processing

The Supervisory Audio Tone processing consists of the following functions:

- SAT recovery
- SAT determination
- SAT regeneration

SAT RECOVERY

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.
The recovery is performed using a digital phase-locked-loop.

SAT DETERMINATION

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the I²C status registers MSCC0 and MSCC1 as shown in Table 5.

SAT REGENERATION

The SAT Regeneration Block generates a digital SAT stream from the recovered SAT stream for transponding back to the base station. The AMPS and TACS specifications require the SAT to be transponded with a maximum phase shift of 20 degrees between the point the modulated RF signal enters the mobile from the base station, and the point the modulated RF leaves the mobile. A variable phase compensation circuit is provided in DPROC to shift the recovered SAT through 0 to 360 degrees before being passed to the output summing network. The degree of phase shift is determined during manufacture of the set and the required additional phase shift is stored in non-volatile RAM and programmed via I²C at each power-on cycle. The phase correction is performed by a counter delay method using signals which are phase locked to the recovered SAT.

Dotting Detector

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of 32 bits of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL, after a Word Synchronization Block has been received, for the duration of the burst.

Table 5 Status registers MSCC0, MSCC1; decoded SAT frequencies.

REGISTER		SAT frequency band (Hz ±2 Hz)	decoded SAT (Hz)
MSCC0	MSCC1		
1	1	max. 5956	not valid
0	0	5956 to 5986	5970
0	1	5986 to 6014	6000
1	0	6014 to 6046	6030
1	1	min. 6046	not valid

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

- Frame Synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11-bit Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC has achieved frame synchronization. In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode. On the Forward Voice Channel detection of the synchronization word indicates that the following 40 bits are valid data. Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

Majority Voting Block

The Majority Voting Block performs the following functions:

- identifying position and validity of frames in the received data stream
- extracting five repeats of each word from a valid frame
- performing a bit-wise majority decision on the five repeats of the data word.

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searched for and extracted by DPROC. On the forward Voice Channel DPROC will extract the first five words that occur for which a correct synchronization word is found. These words can occur in any position in the frame. A serial majority vote is performed as the fifth word is being extracted.

Error Correction Block

The Error Correction Block performs the following functions:

- extraction of a valid message from the Majority-Voted Word
- computation of the S1 and S3 syndromes
- correction of up to one error in the word
- communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$1 + X + X^6$ and $1 + X + X^2 + X^4 + X^6$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC only corrects up to one error although the code used has a Hamming distance of five. The occurence of two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

Received Data Serial Link

The Received Data Serial Link transfers data and control information from DPROC to the System Controller. The data is transferred on RXLINE under control of a clock signal RXCLK, generated by the System Controller. The system controller is informed of the arrival of a decoded data word in the DPROC output register by RXLINE being driven LOW. If the system controller chooses to ignore the received data or only partially clock the data out, the DPROC will reset the receive buffer for the next word after the period RWIN (see Fig.16).

DATA FORMAT

Each Received Data word consists of 4 bytes. The word format is shown in Fig.15(a). The sense and function of the fields is shown in Table 6.

LINK PROTOCOL

The Received Data protocol is described by the timing diagram Fig.16(a) and has the following parameters:

- maximum receive window (RWIN)
  Control Channel (TACS) = 47 ms
  Control Channel (AMPS) = 37 ms
- minimum clock period ($t_{CLK(min)}$) = 2 µs
- minimum clock hold-off (t_{WAIT}) = 100 µs

Transmit Data Serial Interface

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

DATA FORMAT

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig.15(b). The sense and function of the fields is shown in Table 7.

LINK PROTOCOL

Messages are normally up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. However, DPROC will transmit messages of any word length. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC to control the transfer of data words. DPROC has an on-chip buffer which can hold one complete word of a message. While new words are being loaded into DPROC, within the time period Buffer clear to end of TWIN, DPROC will maintain uninterrupted data transmission. The System Controller can abort the transmission of a message at any point activating the I²C signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 3). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig.16(b) and has the following parameters:

- maximum transmit window (TWIN)
  voice channel (TACS) = 60 ms
  voice channel (AMPS) = 48 ms
  control channel (TACS) = 29 ms
  control channel (AMPS) = 23 ms
- minimum clock period ($t_{CLK(min)}$) = 2 µs

Table 6 Received Data word.

BIT	TITLE	SENSE	FUNCTION
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	LOW	if detected as HIGH indicates that a transmission error has occured on the microprocessor to DPROC serial link
0	stop	HIGH	identifies end of the word

Table 7 Transmit data word.

BIT	TITLE	SENSE	FUNCTION
39	start	LOW	identifies start of word
38, 37	DCC	binary data	digital colour code
36 to 1	transmit data	binary data	transmit data word
0	stop	HIGH	identifies end of the word

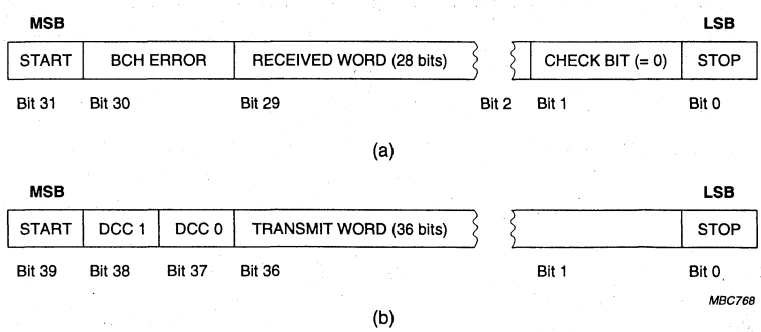
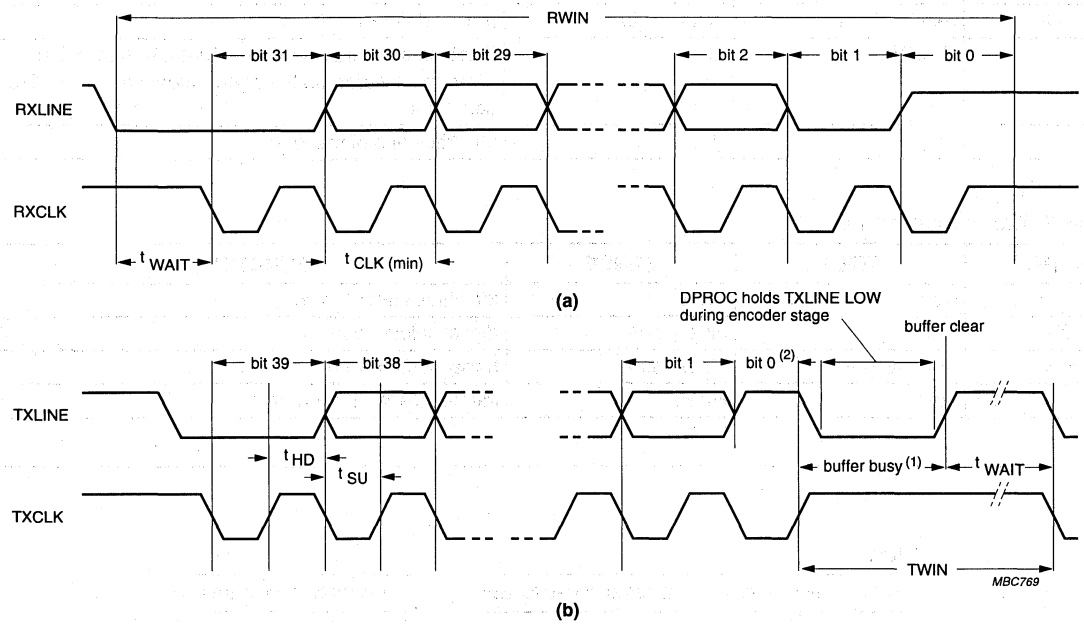


Fig.15 Data word formats; (a) received data word; (b) transmit data word.



Where:

t_{HD} = 100 ns minimum

t_{SU} = 0 ns minimum

t_{WAIT} = 0 ns minimum

(1) The buffer busy time depends on whether the first or subsequent words are being loaded.

(2) The system controller should monitor the TXLINE during bit 0, if the status of TXLINE does not change from a HIGH to a LOW on the rising edge of TXCLK, then a framing error has occured. This can be caused by glitches on the clock line or if an arbitration error occured while the DPROC transmit register was being loaded. The system controller should recover the situation by holding TXLINE HIGH and supplying clocks on TXCLK until TXLINE goes LOW. Then the situation should be treated as a normal channel arbitration failure as described in **Reverse Control Channel Access Arbitration** - Abort Procedure.

Fig.16 Data timing diagrams; (a) DPROC to microcontroller link; receive data timing; (b) microcontroller to DPROC link; transmit data timing.

BCH and Manchester Encoding Block

The functions performed by this circuit block include:

- reception of data from the System Controller
- parity generation
- message construction
- Manchester encoding

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48-bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic equation:

$1 + X^3 + X^4 + X^5 + X^8 + X^{10} + X^{12}$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.
The streams are formed out of the four possible field types:

- Dotting (data inversions)
- 11-bit Synchronization Word
- Digital Colour Code
- 48-bit code word

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 8.

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

Reverse Control Channel Access Arbitration

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time. This function is performed by DPROC monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ANDed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing I^2C register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

INITIAL STATE

- transmitter power off via I^2C
- DPROC transmit circuitry in power-up state
- TXCTRL line HIGH

ACCESS ATTEMPT PROCEDURE

1. System Controller decides to send message (see **Note to the Access Attempt Procedure**).
2. System Controller drives TXCTRL LOW directly.
3. System Controller switches transmitter power-on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).
4. System Controller sets TXRST via I^2C to DPROC.
5. System Controller sets ABREN via I^2C (if required) allowing DPROC to control the transmitter.
6. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.
7. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.
8. System Controller transfers the first word of the message to DPROC via serial link (see **Note to the Access Attempt Procedure**).
9. DPROC sets I^2C signal TXIP and starts sending message while monitoring Busy/Idle status.
10. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.
11. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.
12. System controller loads the subsequent words of the message into DPROC when the buffer becomes clear (Fig.16b).

13. On completion of entire message DRPCO clears TXIP and 25 ms later the System Controller disables transmitter via I²C.
14. System Controller finally sends TXRST to prepare DPROC for next transmission.

Note to the Access Attempt Procedure

At stage 1 the system controller may choose to preload DPROC with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC. Figure 17 illustrates the DPROC data transmission timing.

ABORT PROCEDURE (SEE FIG.18)

1. DPROC immediately disables transmitter output by driving TXCTRL LOW.
2. DPROC sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC for next transmission.

Note to the Abort Procedure

If a message is loaded into DPROC after a TXABRT has occured this word will remain in the DPROC transmit register and will not be cleared to TXRST.
If this situation arises the method of clearing the buffer ready for a second access attempt is to leave TXHOLD LOW and then send a TXRST prior to setting up a new transmission after TXLINE goes HIGH; this will clear any residual data in the buffer.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

ANALOG CIRCUIT BLOCKS

General

The analog signal processing functions on DPROC are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by distributed RC active filters, passive interpolators and comparators.

The distributed RC sections, the Anti-Alias Filter and the Clock Noise Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolators increase the sampling rate from 300 kHz to 1.2 MHz. The sampled analog signals from the Passive Interpolators are converted to sampled 2-state digital signals by the Strobed Comparators. The Gated Digital-to-Analog converters and Analog Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROC output signals, and conversion to the sampled analog domain.

These analog section of the device are shown in Fig.1.

Reference Voltage Generator

The Reference Voltage Generator generates the analog ground reference voltage (AGND) used internally within the DPROC device. To minimize noise AGND must be externally decoupled to VSSA as shown in Fig.19.

Anti-Alias Filter

The Anti-Alias Filter is placed before the SAT sampling block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Alias Filter is a continuous time-distributed RC-active low-pass filter.

Table 8 Digital Colour Code; 7-bit word.

DCC1	DCC0	Coded DCC						
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1
1	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	0	0
		DCC1			DCC0		DCC1.EXOR.DCC0	

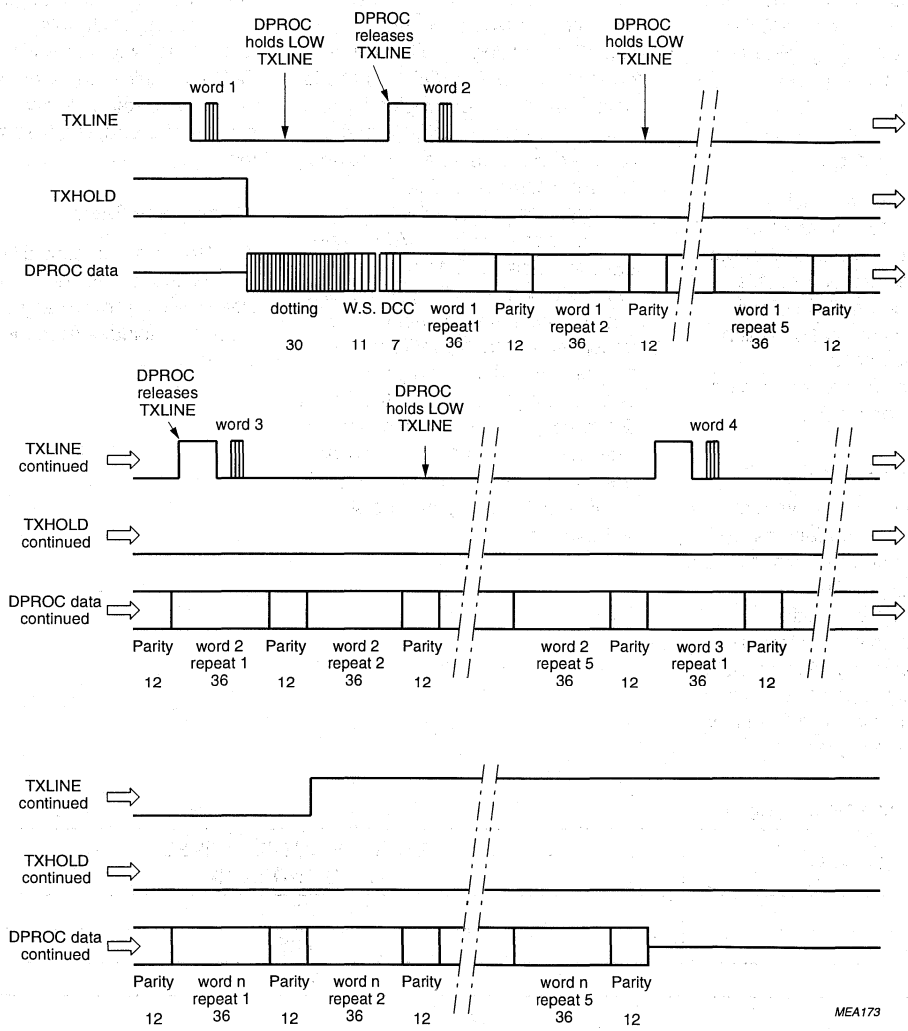


Fig.17 DPROC data transmission timing/microcontroller interface.

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the switched-capacitor filters. This reduces the coarseness of the zero-crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Strobed Comparators

The Strobed Comparators form the analog-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers which convert the filtered sampled analog signals into 2-state sampled digital signals containing only the zero-crossing information from the analog signal.

Gated Digital-to-Analog and Analog Summer

The Gated Digital-to-Analog converters and Analog Summer form the interface between the digital and analog circuitry on the transmit path of DPROC. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal.
The data streams are enabled by the I^2C signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analog conversion and sub-sampling operation is performed by the Gated Digital-to-Analog converters and Analog Summer. The relative signal weights applied in the summer (with respect to the data path) are shown in Table 9.

Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC coupling from the DATA pin.

Clock Noise Filter

The filter is a non-critical continuous time-distributed RC-active low-pass filter used to remove any switching transient residues from the output signal.

Table 9 Relative signal weights.

SIGNAL	RELATIVE OUTPUT LEVEL AMPS AND TACS
ST	1.0
SAT	0.25
DATA	1.0

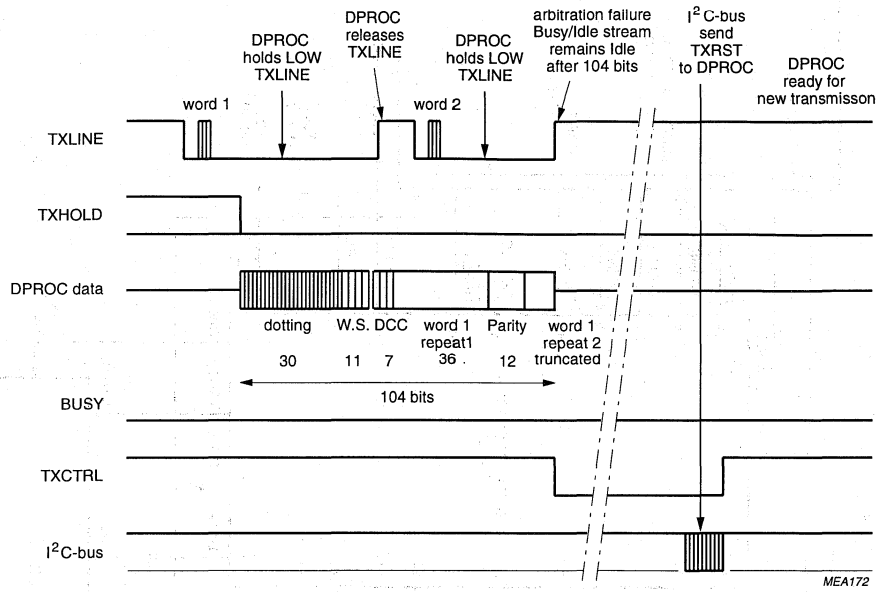


Fig.18 DPROC data transmission timing/microcontroller interface during arbitration failure.

APPLICATION INFORMATION

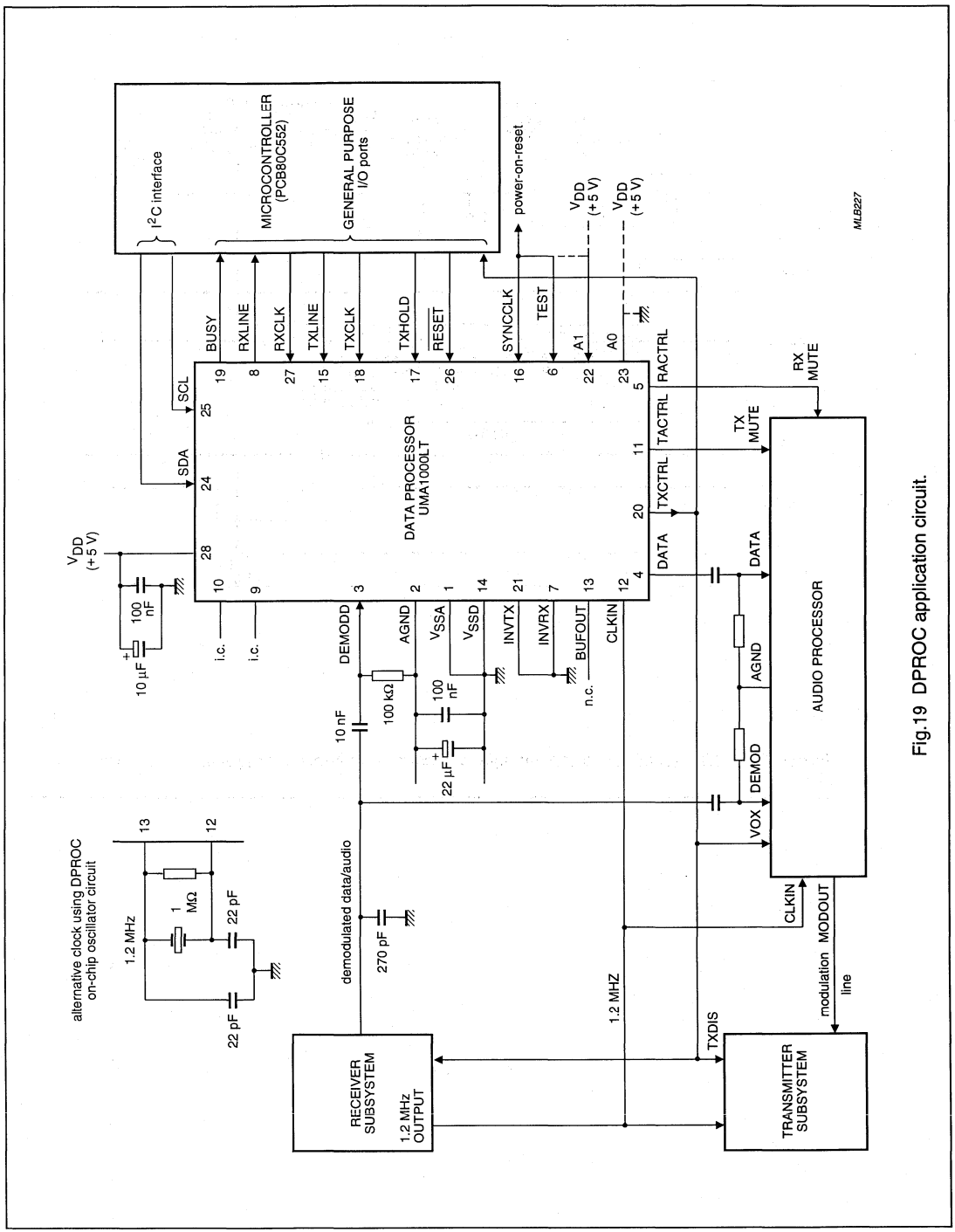


Fig.19 DPROC application circuit.

Dual low-power frequency synthesizer UMA1005T

FEATURES

- Fast locking by 'Fractional-N' divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High-speed serial input
- Low-power consumption
- Programmable charge pump currents
- Supply voltage range 2.9 to 5.5 V.

APPLICATIONS

- Mobile telephony
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1005T is a low-power, high-performance dual frequency synthesizer fabricated in CMOS technology. Fractional-N division with selectable modulo 5 or 8 is implemented in the main synthesizer.

The detectors and charge pumps are designated to achieve 10 to 5000 kHz channel spacing using fractional-N decreases the channel spacing by a factor 5 or 8. Together with an external standard 2, 3 or 4 ratio prescaler the main synthesizer can operate in the GHz frequency range.

Channel selection and programming is realized by a high-speed 3-wire serial interface.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1005T	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

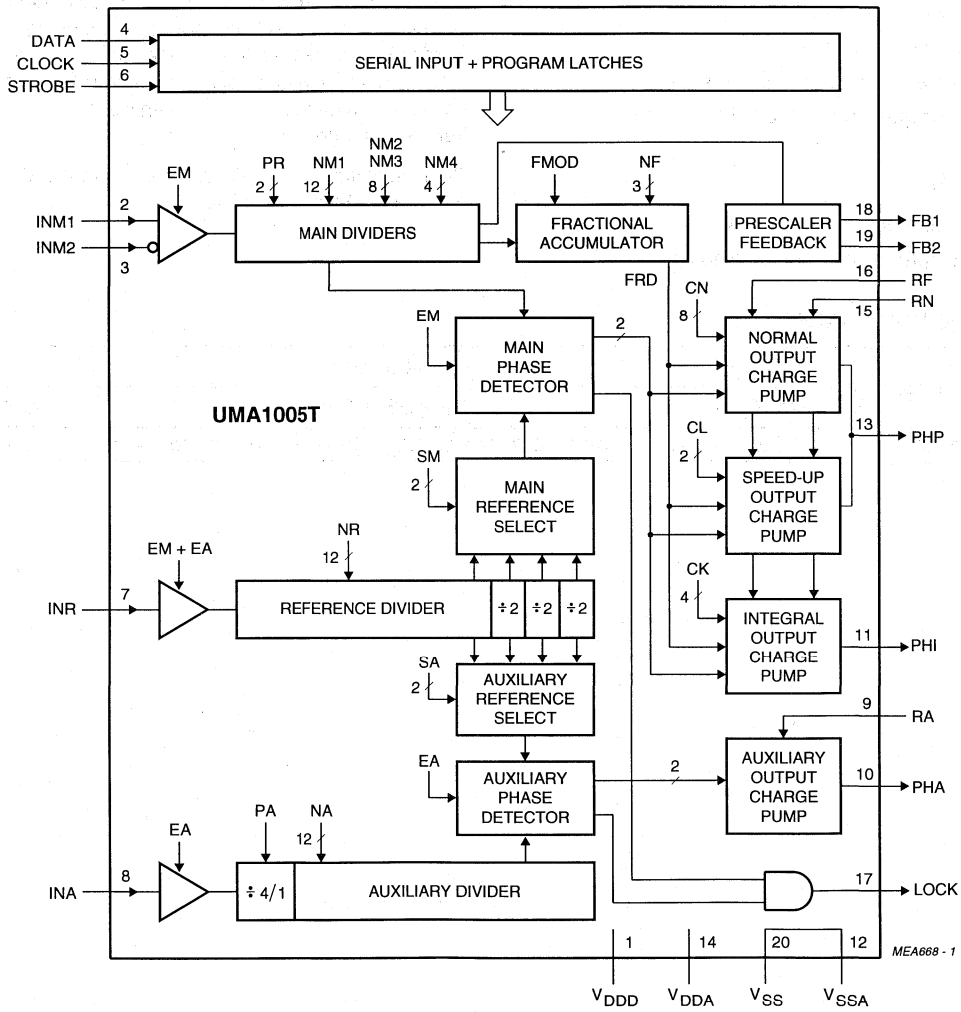


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDD}	1	digital supply voltage
INM1	2	main divider positive input; rising edge active
INM2	3	main divider negative input; falling edge active
DATA	4	serial data input line
CLOCK	5	serial clock input line
STROBE	6	serial strobe input line
INR	7	reference divider input line; rising edge active
INA	8	auxiliary divider input line; rising edge active
RA	9	auxiliary current setting; resistor to V_{SS}
PHA	10	auxiliary phase detector output
PHI	11	integral phase detector output
V_{SSA}	12	analog ground; internally connected to V_{SS}
PHP	13	proportional phase detector output
V_{DDA}	14	analog supply voltage
RN	15	main current setting input; resistor to V_{SS}
RF	16	fractional compensation current setting input; resistor to V_{SS}
LOCK	17	lock detector output
FB1	18	feedback output 1 for prescaler modulus control
FB2	19	feedback output 2 for prescaler modulus control
V_{SS}	20	common ground connection

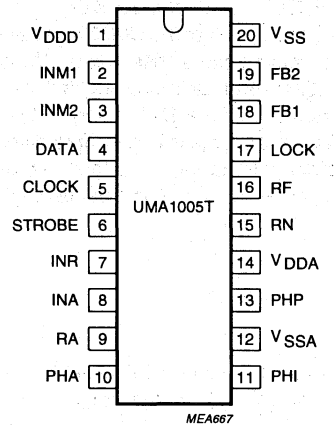


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Serial programming input

The serial input is a 3-wire input (CLOCK, STROBE and DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32-bit words. Each word includes 1 or 4 address bits. Figure 3 shows the timing diagram of the serial input. When the STROBE = LOW, the clock driver is enabled and on the positive edges of the CLOCK the signal on the DATA input is clocked into a shift register. When the STROBE = HIGH, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent:

1. D word.
2. C word.
3. B word.
4. A word.

Figure 4 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for NM4, CN and PR is stored by the B word temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24-bit A0 word is used. CN will be directly loaded by programming a long 32-bit A1 word. The flag LONG in the D word determines whether A0 (LONG = 0) or A1 (LONG = 1) format is applicable.

The A word contains new data for the main divider. The A word is loaded only when a main divider synchronization signal is also active, to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. It disables the loading of the A word each main divider cycle during maximum 300 main divider input cycles. To make sure that the A word will be correctly loaded the STROBE signal must be HIGH for at least 300 main divider input cycles. Programming the A word also means that the main charge pumps on outputs PHP and PHI are set into the speed-up mode as long as the STROBE remains HIGH.

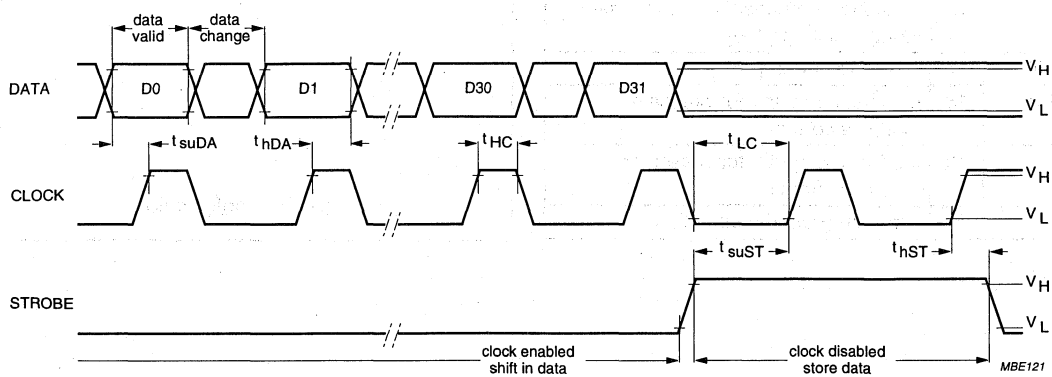


Fig.3 Serial input timing sequence.

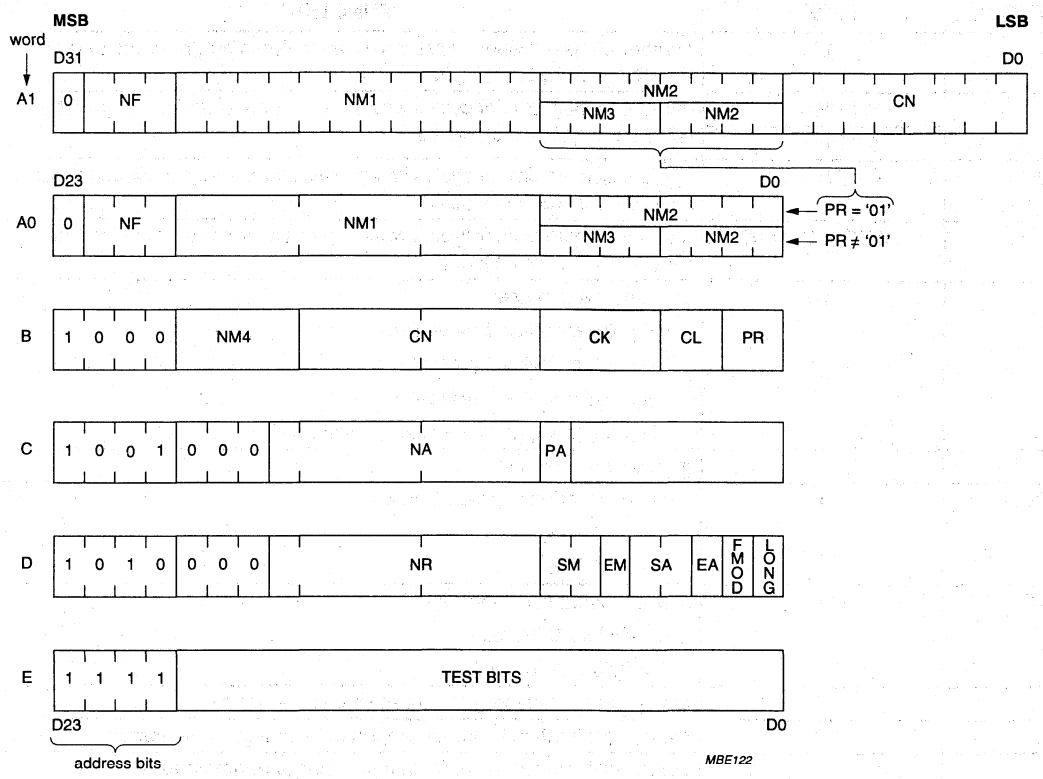


Fig.4 Serial input word format.

Table 1 Description of symbols used in Fig.4

SYMBOL	BITS[1]	FUNCTION
NM1	12	number of main divider cycles when prescaler is programmed in ratio R1 (FB1 = 1; FB2 = 0); note 2
NM2	8 if PR = 01	number of main divider cycles when prescaler is programmed in ratio R2 (FB1 = 0; FB2 = 0); note 2
	4 if PR ≠ 01	
NM3	4 if PR = 1X	number of main divider cycles when prescaler is programmed in ratio R3 (FB1 = 0; FB2 = 1); note 2
NM4	4 if PR = 11 or 00	number of main divider cycles when prescaler is programmed in ratio R4 (FB1 = 1; FB2 = 1); note 2
PR	2	prescaler type in use: PR = 01; modulus 2 prescaler PR = 10; modulus 3 prescaler PR = 11; modulus 4 prescaler PR = 00; modulus 4 prescaler (inhibit ratio 3)
NF	3	fractional-N increment
FMOD	1	fraction-N modulus selection flag: 1 = modulo 8 0 = modulo 5
LONG	1	A word format selection flag: 0 = 24-bit A0 format 1 = 32-bit A1 format
CN	8	binary current setting factor for main charge pumps
CL	2	binary acceleration factor for proportional charge pump current
CK	4	binary acceleration factor for integral charge pump current
EM	1	main divider enable flag
EA	1	auxiliary divider enable flag
SM	2	reference select for main phase detector
SA	2	reference select for auxiliary phase detector
NR	9	reference divider ratio
NA	9	auxiliary divider ratio
PA	1	auxiliary prescaler mode: PA = 0; divide-by-4 PA = 1; divide-by-1

Notes

1. X = don't care.
2. Not including reset cycles and fractional-N effects.

Auxiliary variable divider

The input signal on INA is amplified to a logic level by a single ended input buffer, which accepts LOW level AC coupled input signals. This input stage is enabled if the serial control bit EA = 1. Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = 0. This divider has been optimized to accept a high-frequency (90 MHz at a supply voltage range of 4.75 to 5.5 V) input signal. If PA = 1 this divider is disabled and the input signal is fed directly to the second

stage, which is a 9-bit programmable divider with standard input frequency (30 MHz). The division ratio can be expressed as:

If PA = 0; N = 4 × NA.

If PA = 1; N = NA; with NA = 4 to 511.

Reference variable divider (Fig.5)

The input signal on INR is amplified to a logic level by a single ended input buffer, which accepts LOW level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 511) followed by a 3-bit binary counter. The 2-bit SM determines which of the 4 output pulses is selected as main phase detector input. The 2-bit SA determines the selection of the auxiliary phase detector signal. To obtain the best time spacing for the main and auxiliary reference signals, the opposite output will be used for the auxiliary phase detector, reducing the possibility of unwanted interactions. For this reason the programmable divider produces a symmetric output pulse for even ratios and a 1 input cycle asymmetric pulse for odd ratios.

Main variable divider

The input signals on INM1 and INM2 are amplified to a logic level by a balanced input comparator giving a common mode rejection. This input stage is enabled when serial control bit EM = 1. Disabling means that all currents in the comparator are switched off. The main divider is built-up by a 12-bit counter plus a sign bit. Depending on the serial input values of NM1, NM2, NM3, NM4 and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles in accordance with the information in Table 2.

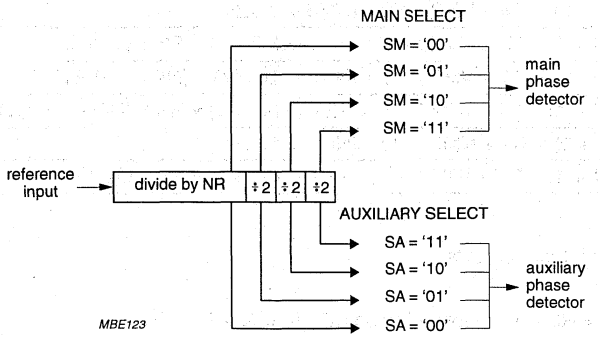


Fig.5 Reference variable divider.

Table 2 Selection of prescaler ratio

COUNTER STATUS	FB1	FB2	PRESCALER RATIO[1]
(–NM1 – 1) to 0	1	0	R1
(–NM1 – 1) to –1	1	0	R1[2]
1 to NM2	0	0	R2
0 to NM2	0	0	R2[2]
0 to NM3	0	1	R3; if PR = 1X
0 to NM4	1	1	R4; if PR = 11 or 00

Notes

1. X = don't care.
2. When the fractional accumulator overflows.

The total division ratio from prescaler to the phase detector expressions are given in Table 3.

Table 3 Total division from prescaler to phase detector expressions

CONDITION	EXPRESSION
PR = 01	$N = (NM1 + 2) \times R1 + NM2 \times R2$
	$N' = (NM1 + 1) \times R1 + (NM2 + 1) \times R2$; note 1
PR = 10	$N = (NM1 + 2) \times R1 + NM2 \times R2 + (NM3 + 1) \times R3$
	$N' = (NM1 + 1) \times R1 + (NM2 + 1) \times R2 + (NM3 + 1) \times R3$; note 1
PR = 11	$N = (NM1 + 2) \times R1 + NM2 \times R2 + (NM3 + 1) \times R3 + (NM4 + 1) \times R4$
	$N' = (NM1 + 1) \times R1 + (NM2 + 1) \times R2 + (NM3 + 1) \times R3 + (NM4 + 1) \times R4$; note 1
PR = 00	$N = (NM1 + 2) \times R1 + NM2 \times R2 + (NM4 + 1) \times R4$
	$N' = (NM1 + 1) \times R1 + (NM2 + 1) \times R2 + (NM4 + 1) \times R4$; note 1

Note

1. When the fractional accumulator overflows.

When the prescaler ratio is R2 = R1 + 1 the total division ratio N′ = N + 1.

Table 4 Modulus prescaler

PR	MODULUS PRESCALER	BIT CAPACITY			
		NM1	NM2	NM3	NM4
00	4	12	4	–	4
01	2	12	8	–	–
10	3	12	4	4	–
11	4	12	4	4	4

The loading of the work registers NM1, NM2, NM3, NM4 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as is explained in Section "Serial programming input".

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = 1. Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider cycles will then be: $NQ = N + \frac{NF}{Q}$

Programming a fraction means the prescaler with main divider will divide by N or N + 1.

The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

Phase detectors (Fig.6)

The auxiliary and main phase detectors are a 2 D-type flip-flop phase and frequency detector. The flip-flops are set by the negative edges of output signals of the dividers. The reset inputs are activated when both flip-flops have been set and when the reset enable signal is active (LOW). Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or dead band around zero phase error. The flip-flops drive on-chip charge pumps. A pull-up current from the charge pump indicates that the VCO frequency shall be increased while a pull-down pulse indicates that the VCO frequency shall be decreased.

Current settings

The UMA1005T has 3 current setting pins RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current in the current setting pins. This current I_R can be set by an external resistor to be connected between the current setting pin (pin 9) and V_{SS}. The typical value for R (current setting resistor) can be calculated with the equation:

$$R = \frac{(V_{DDA} - 0.5) - 237\sqrt{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary output charge pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor (R_{ext}) at pin RA. The active charge pump current is typically: $|I_{PHA}| = 8 \times I_{RA}$.

Main output charge pumps and fractional compensation currents

The main charge pumps on pins PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 7 shows the waveforms for a typical case.

When the serial input A word is loaded, the output circuits are in the 'speed-up mode' as long as the STROBE is HIGH, else the 'normal mode' is active.

NORMAL MODE

In the 'normal mode' the current output at PHP is: $I_{PHP(N)} = I_{pump10} + I_{comp10}$.

Where:

$|I_{pump10}| = \frac{CN \times I_{RN}}{29}$; charge pump current.

$I_{comp10} = \frac{FRD \times I_{RF}}{128}$; fractional compensation current.

In 'normal mode' the current at output PHI is zero.

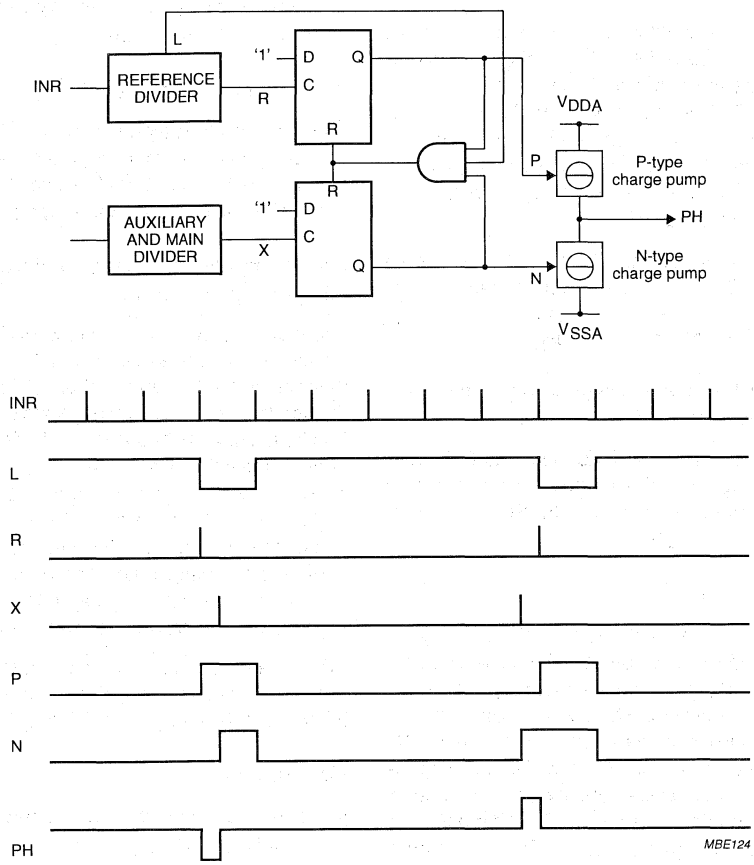


Fig.6 Phase detector structure with timing.

SPEED-UP MODE

In 'speed-up mode' the current in output PHP is:
$I_{PHP(S)} = I_{PHP(N)} + I_{pump11} + I_{comp11}$.

Where:

$I_{pump11} = I_{pump10} \times 2^{(CL+1)}$; charge pump current.

$I_{comp11} = I_{comp10} \times 2^{(CL+1)}$; fractional compensation current.

In 'speed-up mode' the current in output PHI is:
$I_{PHI(S)} = I_{pump21} + I_{comp21}$.

Where:

$I_{pump21} = I_{pump11} \times CK$; charge pump current.

$I_{comp21} = I_{comp11} \times CK$; fractional compensation current.

Figure 7 shows that for a proper fractional compensation the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output. This means that the current setting on the inputs RN and RF must have following ratio: $\frac{I_{RN}}{I_{RF}} = \frac{29 \times Q \times f_{VCO}}{64 \times CN \times f_{i(max)2}}$.

Where:

Q = fractional-N modulus.

$f_{VCO} = f_{i(max)1} \times N$; input frequency of the prescaler.

$f_{i(max)1}$ = maximum input frequency of the main divider (pins INM1 and INM2).

$f_{i(max)2}$ = maximum input frequency of the reference divider (pin INR).

Lock detect

The output LOCK is HIGH when the auxiliary phase detector and the main phase detector indicate a lock condition. The lock condition is defined as a phase difference of less than ±1 cycle on the reference input INR. The lock condition is also fulfilled when the relative counter is disabled (EM = 0 or EA = 0 respectively) for the main or auxiliary counter respectively.

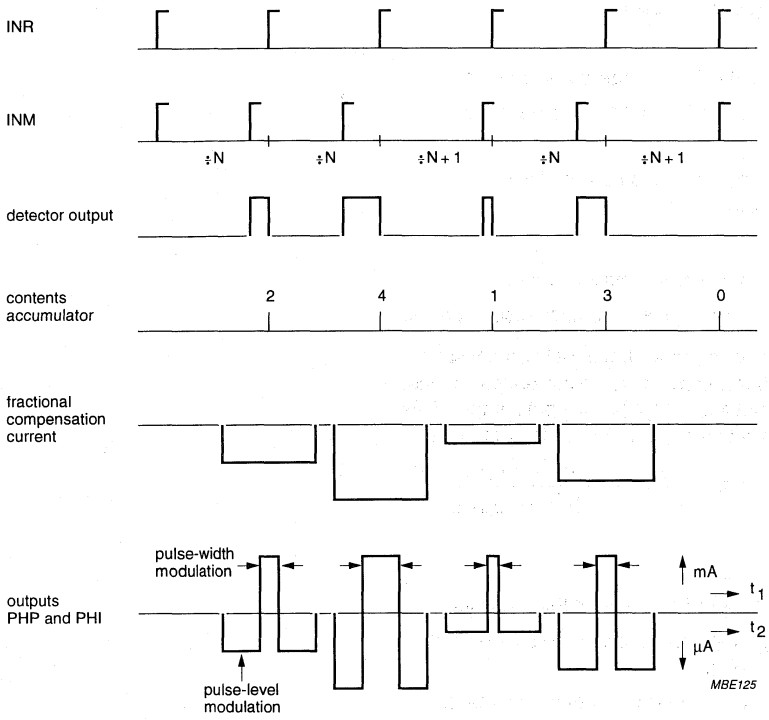


Fig.7 Waveforms for NF = 2 and fraction = 0.4.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	−0.5	6.5	V
V_{DDA}	analog supply voltage	−0.5	6.5	V
V_I	voltage on any input	−0.5	V_{DD} + 0.5	V
I_n	DC current into any input or output	−10	+10	mA
P_{tot}	total power dissipation	−	25	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+70	°C

DC CHARACTERISTICS

$V_{DDD} = V_{DDA}$ = 2.9 to 5.5 V; T_{amb} = −40 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$I_{DDD(stb)}$	digital standby supply current	EM = EA = 0; inputs on V_{DD} or 0	−	−	5	µA
I_{DDD}	operating digital supply current	note 1	−	−	5	mA
$I_{DDA(stb)}$	analog standby supply current	$V_{RA} = V_{DDA}$; $V_{RF} = V_{DDA}$; $V_{RN} = V_{DDA}$	−	−	10	µA
I_{DDA}	operating analog supply current	note 1	−	−	0.6	mA
Digital inputs CLK, DATA and STROBE						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
Digital outputs FB1, FB2 and LOCK						
V_{OL}	LOW level output voltage	I_O = 2 mA; note 2	−	−	0.4	V
V_{OH}	HIGH level output voltage	I_O = −2 mA; note 2	V_{DD} − 0.4	−	−	V
Charge pump PHA						
$\|I_{PHA}\|$	output current	I_{RA} = −62.5 µA; $V_{PHA} = \frac{1}{2}V_{DD}$; note 2	400	500	600	µA
		I_{RA} = −25 µA; $V_{PHA} = \frac{1}{2}V_{DD}$	160	200	240	µA
$\frac{\Delta\|I_{PHA}\|}{\|I_{PHA}\|}$	relative output current variation	I_{RA} = −62.5 µA; notes 2 and 3	−	2	6	%
$\Delta I_{PHA\,M}$	output current matching	I_{RA} = −62.5 µA; $V_{PHA} = \frac{1}{2}V_{DD}$; notes 2 and 4	−	−	±50	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump PHP; normal mode (notes 5, 6 and 7); $V_{RF} = V_{DD}$						
$\lvert I_{PHP(N)} \rvert$	output current	I_{RN} = –62.5 µA; $V_{PHP} = \frac{1}{2}V_{DD}$; note 2	440	550	660	µA
		I_{RN} = –25 µA; $V_{PHP} = \frac{1}{2}V_{DD}$	175	220	265	µA
$\Delta I_{PHP(N)}$	relative output current variation	I_{RN} = –62.5 µA; note 3	–	2	6	%
$\Delta I_{PHP(N\,M)}$	output current matching	I_{RN} = –62.5 µA; $V_{PHP} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±50	µA
Charge pump PHP; speed-up mode (notes 5, 6 and 8); $V_{RF} = V_{DD}$						
$\lvert I_{PHP(S)} \rvert$	output current	I_{RN} = –62.5 µA; $V_{PHP} = \frac{1}{2}V_{DD}$; note 2	2.20	2.75	3.30	mA
		I_{RN} = –25 µA; $V_{PHP} = \frac{1}{2}V_{DD}$	0.85	1.1	1.35	mA
$\Delta I_{PHP(S)}$	relative output current variation	I_{RN} = –62.5 µA; notes 2 and 3	–	2	6	%
$\Delta I_{PHP(S\,M)}$	output current matching	I_{RN} = –62.5 µA; $V_{PHP} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±250	µA
Charge pump PHI; speed-up mode (notes 5, 6 and 9); $V_{RF} = V_{DD}$						
$\lvert I_{PHI(S)} \rvert$	output current	I_{RN} = –62.5 µA; $V_{PHI} = \frac{1}{2}V_{DD}$; note 2	4.4	5.5	6.6	mA
		I_{RN} = –25 µA; $V_{PHI} = \frac{1}{2}V_{DD}$	1.75	2.2	2.65	mA
$\Delta I_{PHI(S)}$	relative output current variation	I_{RN} = –62.5 µA; notes 2 and 3	–	2	8	%
$\Delta I_{PHI(S\,M)}$	output current matching	I_{RN} = –62.5 µA; $V_{PHI} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±500	µA
Fractional compensation PHP; normal mode (notes 5, 10 and 11); $V_{RN} = V_{DD}$; $V_{PHP} = \frac{1}{2}V_{DD}$						
$I_{PHP(F\,N)}$	fractional compensation output current PHP as a function of FRD	I_{RF} = –62.5 µA; FRD = 1 to 7; notes 2 and 12	–675	–500	–325	nA
		I_{RF} = –25 µA; FRD = 1 to 7; note 12	–270	–200	–130	nA
Fractional compensation PHP; speed-up mode (notes 5, 11 and 13); $V_{RN} = V_{DD}$; $V_{PHP} = \frac{1}{2}V_{DD}$						
$I_{PHP(F\,S)}$	fractional compensation output current PHP as a function of FRD	I_{RN} = –62.5 µA; FRD = 1 to 7; notes 2 and 12	–3.35	–2.50	–1.65	µA
		I_{RN} = –25 µA; FRD = 1 to 7; note 12	–1.35	–1.00	–0.65	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fractional compensation PHI; speed-up mode (notes 5, 11 and 14); $V_{RN} = V_{DD}$; $V_{PHP} = \frac{1}{2}V_{DD}$						
$I_{PHI(F)}$	fractional compensation output current PHI as a function of FRD	I_{RN} = −62.5 µA; FRD = 1 to 7; notes 2 and 12	−5.4	−4.0	−2.6	µA
		I_{RN} = −25 µA; FRD = 1 to 7; note 12	−2.15	−1.60	−1.05	µA
Charge pump leakage currents; charge pump not active						
$I_{PHP(LO)}$	output leakage current PHP	normal mode; V_{PHP} = 0.7 to V_{DDA} − 0.8 V note 5	–	10	750	nA
$I_{PHI(LO)}$	output leakage current PHI	normal mode; V_{PHI} = 0.7 to V_{DDA} − 0.8 V note 5	–	10	100	nA
$I_{PHA(LO)}$	output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} − 0.8 V	–	10	750	nA

Notes

1. Operational conditions:
   a) Main and auxiliary divider enabled (EM = EA = 1).
   b) NA = 125.
   c) NR = 125.
   d) NM1 = 60.
   e) NM2 = 63.
   f) $f_{i(max)1} = f_{i(max)2}$ = 15 MHz.
   g) $f_{i(max)3}$ = 60 MHz.
   h) Lock condition.
   i) Normal mode; note 5
   j) $I_{RN} = I_{RF} = I_{RA}$ = 25 µA.
   k) CN = 255.
   l) PA = 0.
2. Limited supply voltage range 4.5 to 5.5 V.
3. The relative output current variation is defined as:
   $\frac{\Delta I_O}{I_O} = 2 \times \frac{I_2 - I_1}{|I_2 + I_1|}$; with V_1 = 0.7 V; $V_2 = V_{DD}$ − 0.8 V (see Fig.8).
4. The output current matching is measured when both (positive and negative current) sections of the output charge pumps are on.
5. When a serial 'A' word is programmed, the main charge pumps on PHP and PHI are in the 'speed-up mode' as long as STROBE = HIGH, otherwise the main charge pumps are in the 'normal mode'.
6. Monotonicity is guaranteed with CN = 0 to 255.
7. Typical output current: $|I_{PHP(N)}| = -I_{RN} \times \frac{CN}{29}$; specification condition: CN = 255.

8. Typical output current: $|I_{PHP(S)}| = -I_{RN} \times CN \times \frac{2^{(CL+1)}+1}{29}$; specification conditions:
   a) CN = 255; CL = 1 or,
   b) CN = 75; CL = 3.
9. Typical output current: $|I_{PHI}| = -I_{RN} \times CN \times 2^{(CL+1)} \times \frac{CK}{29}$; specification conditions:
   a) CN = 160; CL = 3; CK = 1 or,
   b) CN = 160; CL = 2; CK = 2 or,
   c) CN = 160; CL = 1; CK = 4 or,
   d) CN = 160; CL = 0; CK = 8.
10. Typical fractional compensation output current: $I_{PHP(FN)} = I_{RF} \times \frac{FRD}{128}$; specification condition: FRD = 1 to 7.
11. The compensation current specified does not include the leakage current of this output.
12. FRD is the value of the 3-bit fractional accumulator.
13. Typical fractional compensation output current: $I_{PHP(FS)} = I_{RF} \times FRD \times \frac{2^{(CL+1)}+1}{128}$; specification conditions: FRD = 1 to 7; CL = 1.
14. Typical fractional compensation output current: $I_{PHI(F)} = I_{RF} \times FRD \times 2^{(CL+1)} \times \frac{CK}{128}$; specification conditions:
   a) FRD = 1 to 7; CL = 1; CK = 2 or,
   b) FRD = 1 to 7; CL = 2; CK = 1.

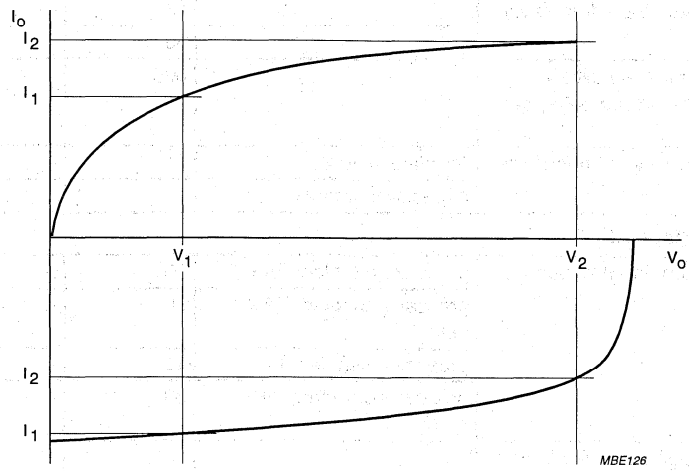


Fig.8 Relative output current variation.

AC CHARACTERISTICS

$V_{DDD} = V_{DDA} = 2.9$ to 5.5 V; $T_{amb} = -40$ to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main divider (inputs INM1 and INM2)						
$f_{i(max)1}$	maximum input frequency		10	–	–	MHz
		note 1	30	–	–	MHz
$\Delta V_{INM(p-p)}$	differential input signal amplitude $V_{INM1} - V_{INM2}$ (peak-to-peak value)		600	–	–	mV
V_{CM}	common mode range for V_{INM1} and V_{INM2}		1	–	$V_{DD} - 1$	V
t_{pd}	propagation delay time from I_{NM1} and I_{NM2} to FB1 and FB2		–	–	60	ns
		note 1	–	18	30	ns
msr	mark-to-space ratio for differential input signals		35 : 65	–	65 : 35	
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference divider (input INR)						
$f_{i(max)2}$	maximum input frequency		15	–	–	MHz
		note 1	30	–	–	MHz
$V_{i(p-p)}$	input signal amplitude AC coupled (peak-to-peak value)		300	–	–	mV
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF
Auxiliary divider (input INA)						
$f_{i(max)3}$	maximum input frequency	prescaler enabled; PA = 0	35	–	–	MHz
		prescaler enabled; PA = 0; note 1	90	–	–	MHz
		prescaler disabled; PA = 1	15	–	–	MHz
		prescaler disabled; PA = 1; note 1	30	–	–	MHz
$V_{i(p-p)}$	input signal amplitude AC coupled (peak-to-peak value)		300	–	–	mV
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF
Serial interface (inputs DATA, CLOCK and STROBE); see Fig.3						
f_{clk}	clock frequency		–	–	10	MHz
t_{HC}	clock HIGH time		30	–	–	ns
t_{LC}	clock LOW time		30	–	–	ns
t_{suDA}	DATA set-up time		30	–	–	ns
t_{hDA}	DATA hold time		30	–	–	ns
t_{suST}	STROBE set-up time		30	–	–	ns
t_{hST}	STROBE hold time		30	–	–	ns

Notes

1. Limited supply voltage range 4.5 to 5.5 V.
2. Periodically sampled; not 100% tested.

Low-power frequency synthesizer for mobile radio communications

UMA1014

FEATURES

- Single chip synthesizer; compatible with Philips cellular radio chipset
- Fully programmable RF divider
- I²C interface for two-line serial bus
- On-chip crystal oscillator/TCXO buffer from 3 to 16 MHz
- 16 reference division ratios allowing 5 to 100 kHz channel spacing
- 1/8 crystal frequency output
- On-chip out-of-lock indication
- Two extra VCO control outputs
- Latched synthesizer alarm output
- Status register including out-of-lock indication and power failure
- Power-down mode.

GENERAL DESCRIPTION

The UMA1014 is a low-power universal synthesizer which has been designed for use in channelized radio communication. The IC is manufactured in bipolar technology and is designed to operate at 5 to 100 kHz channel spacing with an RF input from 50 to 1100 MHz. The channel is programmed via a standard I²C-bus. A low-power sensitive RF divider is incorporated together with a dead-zone eliminated, 3-state phase comparator. The low-noise charge pump delivers 1 mA or 1/2 mA output current to enable a better compromise between fast switching and loop bandwidth. A power-down circuit enables the synthesizer to be set to idle mode.

APPLICATIONS

- Cellular mobile radio (NMT, AMPS, TACS)
- Private mobile radio (PMR)
- Cordless telephones

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{CP}	supply voltage range	4.5	5.0	5.5	V
$I_{CC} + I_{CP}$	supply current	–	13	–	mA
I_{CCpd}	I_{CC} in power-down	–	2.5	–	mA
f_{ref}	phase comparator reference frequency	5	–	100	kHz
f_{RF}	RF input frequency	50	–	1100	MHz
T_{amb}	operating ambient temperature range	–40	–	85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1014T	16	SO16	plastic	SOT109A

Low-power frequency synthesizer for mobile radio communications

UMA1014

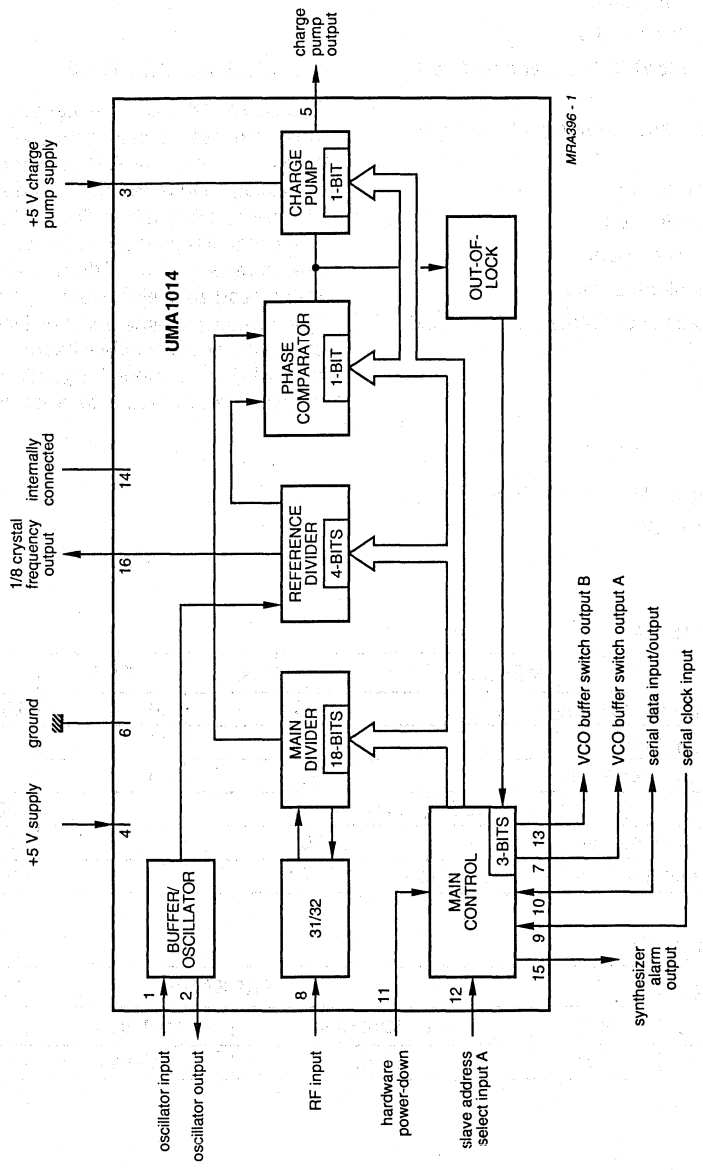


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCIN	1	oscillator or TCXO input
OSCOUT	2	oscillator output
V_{CP}	3	5 V charge pump supply
V_{CC}	4	5 V supply
PCD	5	charge pump output
GND	6	ground
VCOA	7	VCO buffer switch output A (including out-of-lock)
RF	8	RF input
SCL	9	serial clock input
SDA	10	serial data input/output
$\overline{HPD}$	11	hardware power-down (active LOW)
SAA	12	slave address select input A
VCOB	13	VCO buffer switch output B
i.c.	14	internally connected
SYA	15	synthesizer alarm output
FX8	16	1/8 crystal frequency output

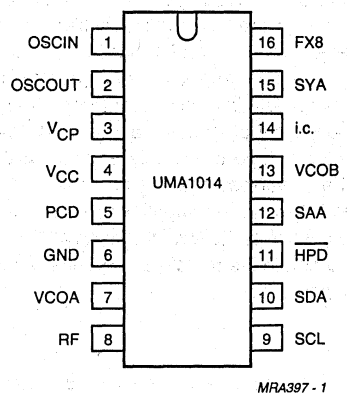


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The UMA1014 is a low-power frequency synthesizer for radio communication which operates in the 50 to 1100 MHz range. The device includes an oscillator/buffer circuit, a reference divider, an RF divider, a 3-state phase comparator, a charge pump and a main control circuit to transfer the serial data into the four internal 8-bit registers. The V_{CC} supply feeds the logic part, the V_{CP} supply feeds the charge-pump only. Both supplies are +5 V (±10%). The power-down facility puts the synthesizer in the idle mode (all current supplies are switched off except in the control part). This allows any I²C transfer and all information in the registers is retained thus enabling fast power-up.

Main divider

The main divider is a pulse swallow type counter which is fully programmable. After a sensitive input amplifier (50 mV, −13 dBm), the RF signal is applied to a 31/32 duo-modulus counter. The output is then used as the clock for the 5-bit swallow counter R = (MD4 to MD0) and the 13-bit main counter N = (MD17 to MD5). The ratio is transferred via the I²C-bus to the registers B, C and D, and then buffered in an 18-bit latch. The ratio in the divider chain is updated with the new information when the least significant bit is received (i.e. D0). This update is synchronized to the output of the divider in order to limit the phase error during small jumps of the synthesized frequency.

The main divider can be programmed to any value between 2048 and 262143 (i.e. $2^{18}-1$). If ratio X, below 2048, is sent to the divider, the ratio (X + 2048) will be programmed. When it is required to switch between adjacent channels it is possible to program register D only, thus allowing shorter I²C programming time.

Oscillator

The oscillator is a common collector Colpitts type with external capacitive feedback. The oscillator has very small temperature drift and high voltage supply rejection. A TCXO or other type of clock can be used to drive the oscillator by connecting the source (preferably AC-coupled) to pin 1 and leaving pin 2 open-circuit. The oscillator acts as a buffer in this mode and requires no additional external components. The signal from the clock source should have a minimum space width of 31 ns.

Reference divider

The reference divider is semi-programmable with 16 division ratios which can be selected via the I²C-bus. The programming uses four bits of the register A (A3 to A0) as listed in Table 2. These ratios allow the use of a large number of crystal frequencies from 3 MHz up to 16 MHz. All main channel spacings can be obtained with a single crystal/TXCO frequency of 9.6 MHz.

Phase comparator

A diagram of the phase comparator and charge pump is illustrated in Fig.3.

The phase comparator is both a phase and frequency detector. The detector comprises dual flip-flops together with logic circuitry to eliminate the dead-zone. When a phase error is detected the UP or DOWN signal goes HIGH. This switches on the corresponding current generator which produces a source or sink current for the loop filter. When no phase error is detected PCD goes high impedance. The final tuning voltage for the VCO is provided by the loop filter. The charge pump current is programmable via the I²C-bus. When IPCD (bit 5) is set to logic 1 the charge pump delivers 1 mA; when IPCD is set to logic 0 the charge pump delivers 0.5 mA.

The phase comparator has a phase inverter logic input (PHI). This allows the use of inverted or non-inverted loop filter configurations. It is thus possible to use a passive loop filter which offers higher performances without an operational amplifier. The function of the phase comparator is given in Table 3 and a typical transfer curve is illustrated in Fig.4.

Out-of-lock detector

An out-of-lock detector using the UP and DOWN signals from the phase comparator is included on-chip. The pin VCOA is an open collector output which is forced LOW during an out-of-lock condition. The same information is also available via the I²C-bus in the status register (bit OOL). When the phase error (measured at the phase comparator) is greater than approximately 200 ns, an out-of-lock condition is immediately flagged. The flag is only released after 6 reference cycles when the phase error is less than 200 ns.

Table 1 Division ratio in the main divider

MAIN COUNTER: N								SWALLOW COUNTER: R		
MD17	MD16	MD15	...	MD8	MD7	...	MD5	MD4	...	MD0
B1	B0	C7	...	C0	D7	...	D5	D4	...	D0
MSB										LSB

Table 2 Reference divider programming

A3(RD3)	A2(RD2)	A1(RD1)	A0(RD0)	REFERENCE DIVISION RATIO	CHANNEL SPACING FOR 9.6 MHz AT OSCIN
0	0	0	0	128	75 kHz
0	0	0	1	160	60 kHz
0	0	1	0	192	50 kHz
0	0	1	1	240	40 kHz
0	1	0	0	256	37.5 kHz
0	1	0	1	320	30 kHz
0	1	1	0	384	25 kHz
0	1	1	1	480	20 kHz
1	0	0	0	512	18.75 kHz
1	0	0	1	640	15 kHz
1	0	1	0	768	12.5 kHz
1	0	1	1	960	10 kHz
1	1	0	0	1024	9.375 kHz
1	1	0	1	1280	7.5 kHz
1	1	1	0	1536	6.25 kHz
1	1	1	1	1920	5 kHz

Table 3 Operation of the phase comparator

	PHI = 0 (PASSIVE LOOP FILTER)			PHI = 1 (ACTIVE LOOP FILTER)		
	$f_{ref} < f_{var}$	$f_{ref} > f_{var}$	$f_{ref} = f_{var}$	$f_{ref} < f_{var}$	$f_{ref} > f_{var}$	$f_{ref} = f_{var}$
UP	0	1	0	1	0	0
DOWN	1	0	0	0	1	0
I_{pcd}	−1 mA	1 mA	< ±5 nA	1 mA	−1 mA	< ±5 nA

MAIN CONTROL

The control part consists mainly of the I²C-bus control interface and a set of four registers A, B, C and D. The serial input data (SDA) is converted into 8-bit parallel words and stored in the appropriate registers. The data transmission to the synthesizer is executed in the burst mode with the following format:

//slave addr./subaddr./data1/data2/.../datan// ; n up to 4

Data byte 1 is written in the register indicated by the subaddress. An auto-increment circuit, if enabled (AVI = 1), then provides the correct addressing for the ensuing data bytes. Since the length of the data burst is not fixed, it is possible to program only one register or the whole set. The registers are structured in such a way so that the burst, for normal operation, is kept as short as possible. The bits that are only programmed during the set-up (reference division ratio, power-down, phase inversion and current on PCD) are stored in registers A and B.

In the slave address six bits are fixed, the remaining two bits depend on the application.

Table 4 Slave address

1	1	0	0	0	1	$\overline{SAA}$	R/$\overline{W}$

SAA is the slave address. When SAA goes HIGH then $\overline{SAA}$ = 0, when SAA goes LOW then $\overline{SAA}$ = 1. This allows the use of two UMA1014s on the same bus but using a different address. R/$\overline{W}$ should be set to logic 0 when writing to the synthesizer or set to logic 1 when reading the status register.

The subaddress includes the register pointer, and sets the two flags related to the auto-increment (AVI) and the alarm disable (DI)

Table 5 Subaddress

X	X	X	DI	AVI	X	SB1	SB0

Where:

X = not used

DI (Disable Interrupt):
DI = 1 disables the alarm on SYA
DI = 0 enables the alarm.

AVI (Auto Value Increment):
AVI = 1 enables the automatic increment
AVI = 0 disables the auto-increment.

SB1/SB0 are the pointers of the register where DATA1 will be written (see Table 6).

When the auto-increment is disabled (AVI = 0), the subaddress pointer will maintain the same value during the I²C-bus transfer. All the data bytes will then be written consecutively in the register pointed by the subaddress.

Table 6 Pointer of the registers

SB1	SB0	REGISTER POINTED
0	0	A
0	1	B
1	0	C
1	1	D

Status register and synthesizer alarm

When an out-of-lock condition or a power dip occurs, SYA, which is an open collector output, is forced LOW and latched. The pin SYA will be released after the status register is read via the I²C-bus.

The status register contains the following information:

Table 7 Status register

0	0	0	OOL	0	LOOL	LPD	DI

Where:

OOL = momentary out-of-lock
LOOL = latched out-of-lock
LPD = latched power dip
DI = disable interrupt (of the last write cycle)

The I²C-bus protocol to read this internal register is a single byte without subaddressing:

//slave address (R/$\overline{W}$ = 1)/status register (read)//

Table 8 Bit allocation

REGISTER	POINTER	BIT ALLOCATION								PRESET
		7	6	5	4	3	2	1	0	
A	00	PD	X	IPCD	X	RD3	RD2	RD1	RD0	00001110
B	01	1	0	1	PHI	VCOB	VCOA	MD17	MD16	10100101
C	10	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	00111000
D	11	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	10000000

Where X = not used

Table 9 Register allocation

REGISTER NAME	BIT NAME	FUNCTION		PRESET VALUE
A	PD	power down	PD = 0 normal operation	0
	IPCD	programmable charge pump current	IPCD = 1 = 1 mA; IPCD = 0 = 0.5 mA	0
	RD3...RD0	reference ratio	see Table 2	1110; r = 1536
B	PHI	phase inverter	PHI = 0 passive loop filter	0
	VCOA	VCO switch A	set pin 7	1
	VCOB	VCO switch B	set pin 13	0
	MD17, MD16	bits 17 and 16	MSB of main divider ratio	01
C	MD15 to MD8	bits 15 to 8	main divider ratio	00111000
D	MD7 to MD0	bits 7 to 0	main divider ratio	10000000; r = 80000

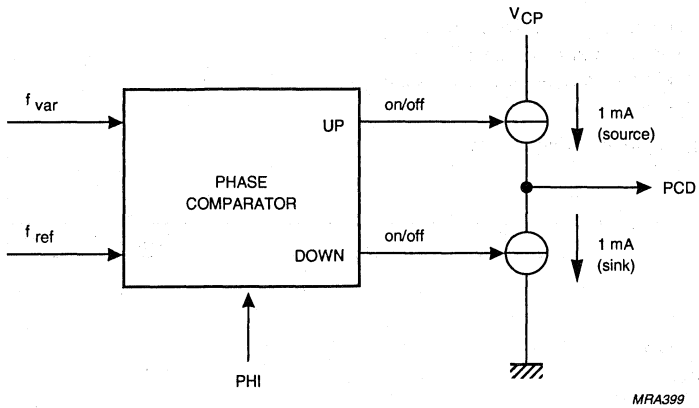


Fig.3 Phase comparator block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage range	−0.3	7.0	V
V_i	voltage range to ground (all pins)	0	V_{CC}	V
T_{stg}	IC storage temperature range	−55	+125	°C
T_{amb}	operating ambient temperature range	−40	+85	°C

HANDLING

Every pin referenced to ground withstands ESD (HMB) tests in accordance with MIL-STD-883C method 3015 class 2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling Integrated Circuits.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

CHARACTERISTICS

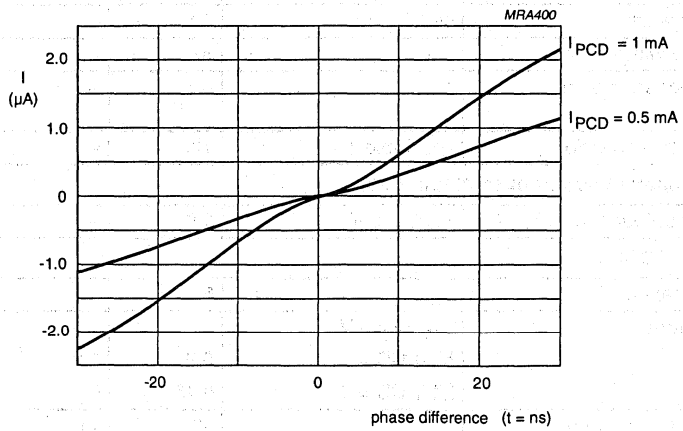
T_{amb} = 25 °C; V_{CC} = 4.5 to 5.5 V; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{CC} and V_{CP})						
V_{CC}	supply voltage range		4.5	–	5.5	V
I_{CC}	supply current		–	11.5	13.5	mA
I_{CCpd}	supply current	power-down	–	2.5	3.3	mA
V_{CP}	charge pump supply voltage		4.5	–	5.5	V
I_{CP}	charge pump supply current	IPCD = 0.5 mA	–	1.4	1.8	mA
I_{CPpd}	charge pump supply current	power-down	–	0.01	–	mA
RF dividers (pin RF)						
f_{RF}	frequency range		50	–	1100	MHz
$V_{RF(rms)}$	input voltage level (RMS value)	50 to 100 MHz	150	–	200	mV
		100 to 1100 MHz	50	–	150	mV
R_I	input resistance	at 1 GHz	–	200	–	Ω
		at 100 MHz	–	600	–	Ω
C_I	input capacitance	note 1	–	2.0	–	pF
R_{RF}	division ratios		2048	–	262143	–
Oscillator and reference divider (pins OSCIN and OSCOUT)						
f_{OSC}	oscillator frequency range		3	–	16	MHz
$V_{OSC(RMS)}$	input level sine wave (RMS value)		0.15	–	$V_{CC}/2.8$	V
$V_{OSC(p-p)}$	input level square wave (peak-to-peak value)		0.45	–	V_{CC}	V
t_{OSC_mk}	input mark width	see Fig.8	10	–	–	ns
t_{OSC_sp}	input space width		31	–	–	ns
Z_{OSC}	output impedance at pin OSCOUT		–	–	2	kΩ
R_{ref}	reference division ratio	see Table 1	128	–	1920	
1/8 crystal frequency (open collector output) (pin FX8)						
I_{OL}	LOW level output current	$V_{OL} \geq 0.6$ V	1.0	–	–	mA
Phase comparator (pin PCD)						
f_{PCD}	frequency range		5	–	100	kHz
I_{PCD}	output current	V_{PCD} = 2.5 V				
		bit IPCD = 1	0.9	1.2	1.4	mA
		bit IPCD = 0	0.45	0.6	0.75	mA
I_{PCDL}	output leakage current		–5	±1	+5	nA
V_{PCD}	output voltage		0.4	–	V_{CP}–0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock and serial data input (pins SCL and SDA)						
f_{CLK}	clock frequency		0	–	100	kHz
V_{IH}	HIGH level input voltage		3	–	–	V
V_{IL}	LOW level input voltage		–	–	1.5	V
I_{IH}	HIGH level input current		–	3	10	µA
I_{IL}	LOW level input current		–10	–5	–	µA
C_I	input capacitance		–	–	10	pF
I_{sink}	SDA sink current	V_{OL} = 0.4 V	3	–	–	mA
Slave address select input (pin SAA) and Hardware power-down input (pin HPDN)						
V_{IH}	HIGH level input voltage		3	–	–	V
V_{IL}	LOW level input voltage		–	–	0.4	V
I_{IH}	HIGH level input current		–	–	0.1	µA
I_{IL}	LOW level input current		–10	–	–	µA
VCO output switches (pins VCOA and VCOB) and synthesizer alarm (pin SYA); note 2						
I_{OL}	LOW level sink current	$V_{OL} \geq 0.4$ V	400	–	–	µA

Notes to the characteristics

1. C_I is in parallel with R_I
2. Pin VCOA is forced to logic 0 during out-of-lock condition



The current I_{PCD} is averaged over a reference period of 24 µs.

Fig.4 Gain of phase detector and charge pump.

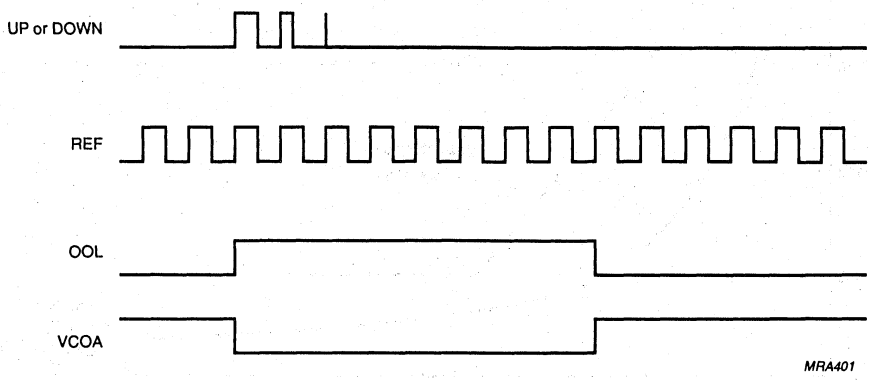


Fig.5 Out-of-lock function.

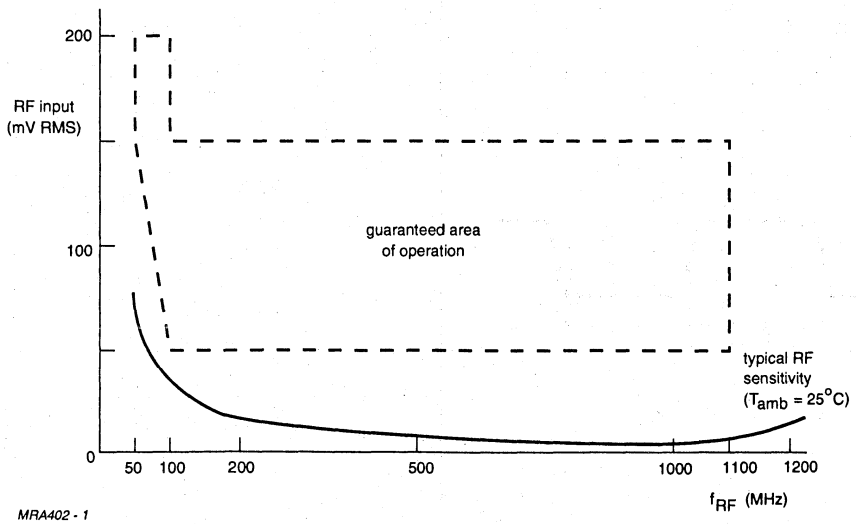


Fig.6 RF input high frequency sensitivity.

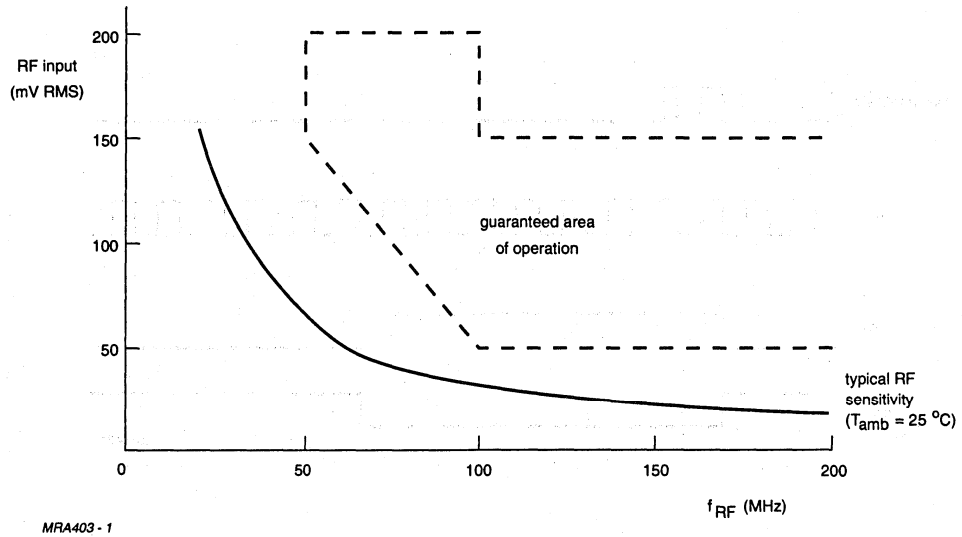


Fig.7 RF input low frequency sensitivity.

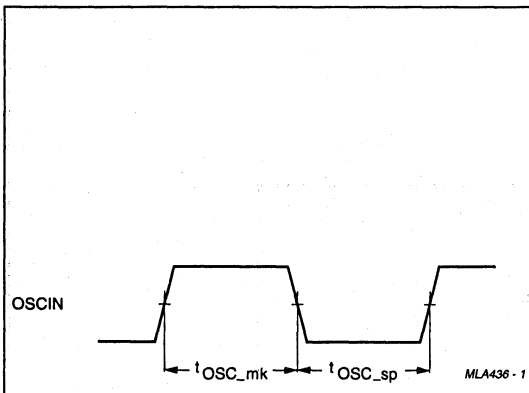
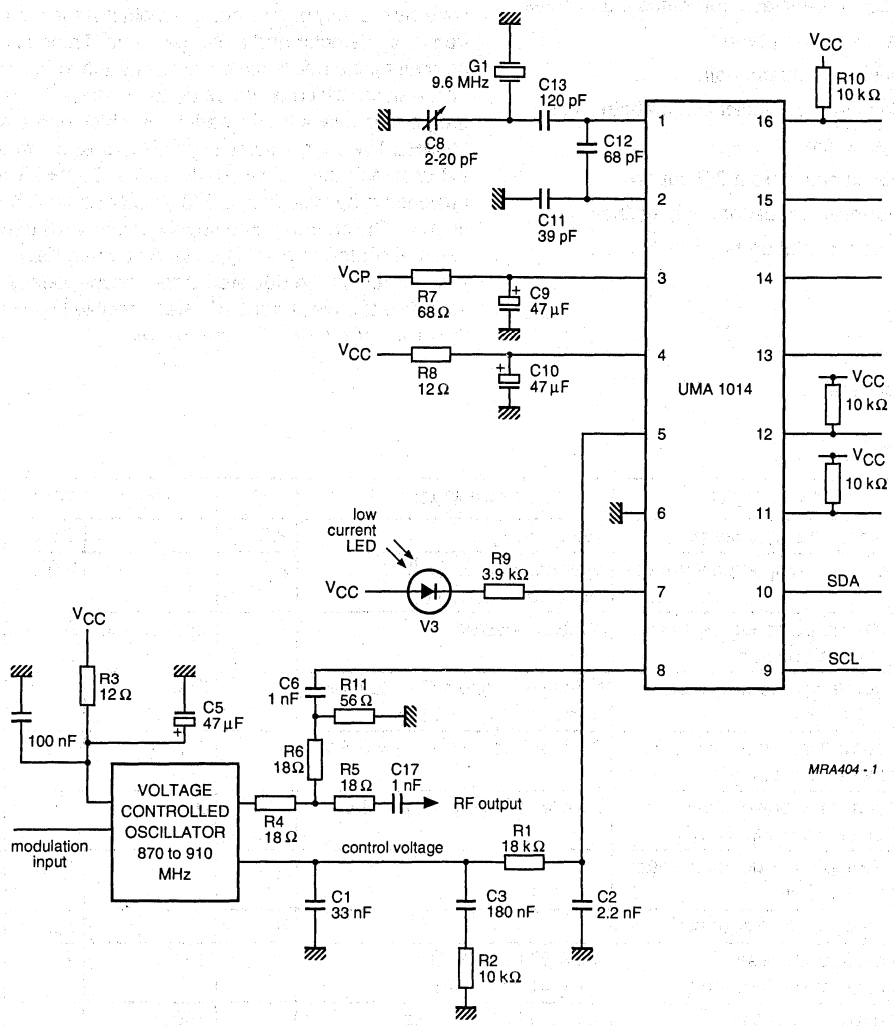


Fig.8 Oscillator input timing.



ETACS application for:

V_{CO} sensitivity = 11 MHz/V.

Channel spacing = 12.5 kHz.

Fig.9 Typical cellular mobile radio application.

Low-power dual frequency synthesizer for radio communications

UMA1015M

FEATURES

- Two fully programmable RF dividers up to 1.1 GHz
- Fully programmable reference divider up to 35 MHz
- 2 : 1 or 1 : 1 ratio of selectable reference frequencies
- Fast three-line serial bus interface
- Adjustable phase comparator gain
- Programmable out-of-lock indication for both loops
- On-chip voltage doubler
- Low current consumption from 3 V supply
- Separate power-down mode for each synthesizer
- Up to 4 open-drain output ports.

APPLICATIONS

- Cordless telephone
- Hand-held mobile radio.

GENERAL DESCRIPTION

The UMA1015M is a low-power dual frequency synthesizer for radio communications which operates in the 50 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz. The device is programmed via a 3-wire serial bus which operates up to 10 MHz. The charge pump currents (gains) are fixed by an external resistance at pin 20 (I_{SET}). The BiCMOS device is designed to operate from 2.6 (3 Ni-Cd cells) to 5.5 V at low current. The charge pump supply can be provided by external source or on-chip voltage doubler. Each synthesizer can be powered-down independently via the serial bus to save current. It is also possible to power-down the device via the HPD input (pin 5).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.6	–	5.5	V
V_{CC}	charge pump supply voltage	external supply; doubler disabled; $V_{CC} \geq V_{DD}$	2.6	–	6.0	V
V_{CCvd}	charge pump supply from voltage doubler	doubler enabled	–	$2V_{DD1} - 0.6$	6.0	V
$I_{DDO1} + I_{DDO2} + I_{CCO}$	operating supply current	both synthesizers ON; doubler disabled; $V_{DD1} = 5.5$ V	–	9.6	–	mA
$I_{DD1pd} + I_{DD2pd} + I_{CCpd}$	current in power-down mode per supply	doubler disabled; $V_{DD1} = 5.5$ V	–	0.01	–	mA
I_{DD1pd}	current in power-down mode from supply V_{DD}	doubler enabled; $V_{DD1} = 3$ V	–	0.15	–	mA
f_{RFA}, f_{RFB}	RF input frequency for each synthesizer		50	–	1100	MHz
f_{XTALIN}	crystal input frequency		3	–	35	MHz
$f_{ref(min)}$	minimum phase comparator frequency	$f_{RF} = 50$ to 1100 MHz; $f_{XTAL} = 3$ to 35 MHz	–	10	–	kHz
$f_{ref(max)}$	maximum phase comparator frequency	$f_{RF} = 50$ to 1100 MHz; $f_{XTAL} = 3$ to 35 MHz	–	750	–	kHz
T_{amb}	operating ambient temperature	synthesizer A $2.6 \text{ V} \leq V_{DD} \leq 5.5$ V	–30	–	+85	°C
		synthesizer B $2.6 \text{ V} \leq V_{DD} \leq 4.5$ V	–30	–	+85	°C
		synthesizer B $2.6 \text{ V} \leq V_{DD} \leq 5.0$ V	0	–	+85	°C

Low-power dual frequency synthesizer for radio communications

UMA1015M

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1015M/C2	20	SSOP20	plastic	SOT266-1

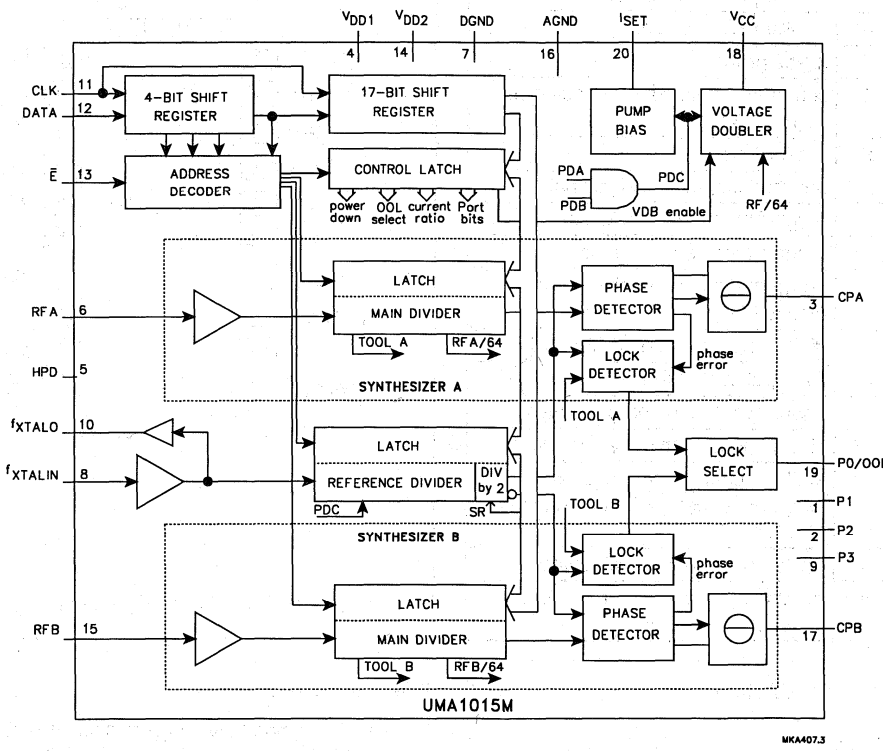


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
P1	1	output Port 1
P2	2	output Port 2
CPA	3	charge-pump output synthesizer A
V_{DD1}	4	digital supply voltage 1 (2.6 to 5.5 V)
HPD	5	hardware power-down (input LOW = power-down)
RFA	6	RF input synthesizer A
DGND	7	digital ground
f_{XTALIN}	8	common reference frequency input from TCXO
P3	9	output Port 3
f_{XTALO}	10	buffered output of f_{XTAL} signal
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
V_{DD2}	14	digital supply voltage 2 (2.6 to 5.5 V)
RFB	15	RF input synthesizer B
AGND	16	analog ground to charge pumps
CPB	17	charge pump output synthesizer B
V_{CC}	18	analog supply to charge pump; external or voltage doubler output (2.6 to 6.0 V)
P0/OOL	19	Port output 0/out-of-lock output
I_{SET}	20	regulator pin to set charge-pump currents

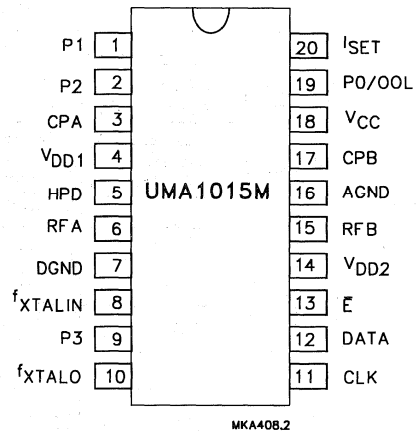


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main dividers

Each synthesizer has a fully programmable 17-bit main divider. The RF input drives a pre-amplifier to provide the clock to the first divider bit. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from below 50 mV (RMS) up to 250 mV (RMS), and at frequencies up to 1.1 GHz. The high frequency sections of the divider are implemented using bipolar transistors, while the slower section uses CMOS technology. The range of division ratios is 512 to 131071.

Reference divider

There is a common fully programmable 12-bit reference divider for the two synthesizers. The input f_{XTALIN} drives a pre-amplifier to provide the clock input for the reference divider. This clock signal is also buffered and output on pin f_{XTALO} (open drain). An extra divide-by-2 block allows a reference comparison frequency for synthesizer B to be half that of synthesizer A. This feature is selectable using the program bit SR. If the programmed reference divider ratio is R then the ratio for each synthesizer is as given in Table 1.

The range for the division ratio R is 8 to 4095. Opposite edges of the divider output are used to drive the phase detectors to ensure that active edges arrive at the phase detectors of each synthesizer at different times. This minimizes the potential for interference between the charge pumps of each loop. The reference divider consists of CMOS devices operating beyond 35 MHz.

Table 1 Synthesizer ratio of reference divider

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Phase comparators

For each synthesizer, the outputs of the main and reference dividers drive a phase comparator where a charge pump produces phase error current pulses for integration in an external loop filter. The charge pump current is set by an external resistance R_{SET} at pin I_{SET}, where a temperature-independent voltage of 1.2 V is generated. R_{SET} should be between 12 kΩ and 60 kΩ (to give an I_{SET} of 100 μA and 20 μA respectively).
The charge-pump current, I_{CP}, can be programmed to be either ($12 \times I_{SET}$) or ($24 \times I_{SET}$) with the maximum being 2.4 mA. The dead zone, caused by finite switching of current pulses, is cancelled by an internal delay in the phase detector thus giving improved linearity. The charge pump has a separate supply, V_{CC}, which helps to reduce the interference on the charge pump output from other parts of the circuit. Also, V_{CC} can be higher than V_{DD1} if a wider range on the VCO input is required.

Voltage doubler

If required, there is a voltage doubler on-chip to supply the charge pumps at a higher level than the nominal available supply. The doubler operates from the digital supply V_{DD1}, and has a maximum output of 6 V. An external capacitor is required on pin V_{CC} for smoothing, the capacitor required to develop the extra voltage is integrated on-chip. To minimize the noise being introduced to the charge pump output from the voltage doubler, the doubler clock is suppressed (provided both loops are in-lock) for the short time that the charge pumps are active. The doubler clock (RF/64) is derived from whichever main divider is operating (synthesizer A has priority). While both synthesizers are powered down (and the doubler is enabled), the doubler clock is supplied by a low-current internal oscillator. The doubler can be disabled by programming the bit VDON to logic 0, in order to allow an external charge pump supply to be used.

Out-of-lock indication/output ports

There is a lock detector on-chip for each synthesizer. The lock condition of each, or both loops, is output via an open-drain transistor which drives the pin P0/OOL (when out-of-lock, the transistor is turned on and therefore the output is forced LOW). The lock condition output is software selectable (see Table 4). An out-of-lock condition is flagged when the phase error is greater than T_{00L}, the value of which is approximately equal to 80 cycles of the relevant RF input. The out-of-lock flag is only released after 8 consecutive reference cycles where the phase error is less than T_{00L}. The out-of-lock function can be disabled, via the serial bus, and the pin P0/OOL can be used as an output port. Three other port outputs P1, P2 and P3 (open-drain transistors) are also available.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. This is allowed when CLK is in either state without causing any consequences to the register data. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down of both synthesizers.

However when either synthesizer A or synthesizer B or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTALIN}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The data format and register bit allocations are shown in Table 2.

Table 2 Bit allocation

FIRST	REGISTER BIT ALLOCATION																			LAST
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
X	X	VDON	PO	OLA	OLB	CRA	CRB	X	X	sPDA	sPDB	P3	P2	P1	X	X	0	0	0	1
MA16	SYNTHESIZER A MAIN DIVIDER COEFFICIENT															MA0	0	1	0	0
0	0	0	0	SR	R11	REFERENCE DIVIDER COEFFICIENT										R0	0	1	0	1
MB16	SYNTHESIZER B MAIN DIVIDER COEFFICIENT															MB0	0	1	1	0
RESERVED FOR TEST[1]																	0	0	0	0

Note

1. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Bit allocation description

SYMBOL	DESCRIPTION
sPDA, sPDB	software power-down for synthesizers A and B (0 = power-down)
P3, P2, P1 and P0	bits output to pins 1, 2, 9 and 19 (1 = high impedance)
VDON	voltage doubler enable (1 = doubler enabled)
OLA, OLB	out-of-lock select; selects signal output to pin 19 (see Table 4)
CRA, CRB	charge pump A/B current to I_{SET} ratio select (see Table 5)
SR	reference frequency ratio select (see Table 6)

Table 4 Out-of-lock select

OLA	OLB	OUTPUT AT PIN 19
0	0	P0
0	1	lock status of loop B; OOLB
1	0	lock status of loop A; OOLA
1	1	logic OR function of loops A and B

Table 5 Charge pump current ratio

CRA/CRB	CURRENT AT PUMP
0	$I_{CP} = 12 \times I_{SET}$
1	$I_{CP} = 24 \times I_{SET}$

Table 6 Reference division ratio

SR	RATIO A	RATIO B
0	R	R
1	R	2R

Power-down modes

The device can be powered down via pin HPD (active LOW = power-down) or via the serial bus (bits SPDA and SPDB, logic 0 = power-down). When only one synthesizer is powered down, the functions common to both will be maintained. When both synthesizers are switched off, only the voltage doubler (if enabled) will remain active drawing a reduced current. An internal oscillator will drive the doubler in this situation. If both synthesizers have been in a power-down condition, then when one or both synthesizers are reactivated, the reference and main dividers restart in such a way as to avoid large random phase errors at the phase comparator.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}, V_{DD2}	DC range of digital power supply voltage with respect to DGND	−0.3	+6.0	V
V_{CC}	DC charge pump supply voltage with respect to AGND	−0.3	+6.0	V
$\Delta V_{CC\text{-}DD}$	difference in voltage between V_{CC} and V_{DD1}, V_{DD2}	−0.3	+6.0	V
V_n	DC voltage at pins 1, 2, 5, 6, 8 to 15, 19 and 20 with respect to DGND	−0.3	V_{DD1} + 0.3	V
$V_{3, 17}$	DC voltage at pins 3 and 17 with respect to AGND	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.6$ to 5.5 V; $V_{CC} = 2.6$ to 6.0 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; (V_{DD1}, V_{DD2} and V_{CC}) voltage doubler disabled, external supply on V_{CC}						
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.6	–	5.5	V
$I_{DD1} + I_{DD2}$	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2} = 3$ V	–	8.5	–	mA
		f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2} = 5.5$ V	–	–	12.5	mA
I_{DDpda}, I_{DDpdb}	total digital supply current from V_{DD1} and V_{DD2} with one synthesizer in power-down mode	f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2} = 3$ V	–	5.5	–	mA
		f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2} = 5.5$ V	–	–	7.5	mA
I_{DDpd}	digital supply current in power-down mode	both synthesizers powered down; $V_{HPD} = 0$ V	–	–	60	µA
V_{CC}	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.6	–	6.0	V
I_{CC}	charge pump supply current	both synthesizers on and in lock; f_{ref} = 12.5 kHz	–	–	25	µA
I_{CCpd}	charge pump supply current in power-down mode	both synthesizers powered down	–	–	25	µA
Voltage doubler enabled						
I_{DD}	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on and in lock; $V_{DD1} = 3$ V; $f_{doubler}$ = 16 MHz	–	8.5	12	mA
I_{DDpd}	total digital supply current in power-down mode from V_{DD1} and V_{DD2}	both synthesizers powered down; $V_{DD1} = 3$ V; $V_{HPD} = 0$ V	–	0.15	0.3	mA
V_{CCvd}	charge pump supply voltage	DC current drawn from V_{CC} = 50 µA	$2V_{DD1} - 1.2$	$2V_{DD1} - 0.6$	6.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF main divider input; RFA and RFB						
f_{RF}	RF input frequency		50	–	1100	MHz
$V_{RF(rms)}$	RF input signal voltage (RMS value; AC coupled)	R_s = 50 Ω; $V_{DD1} = V_{DD2}$ = 2.6 to 3.5 V; f_{RF} = 400 to 1100 MHz	50	–	250	mV
		R_s = 50 Ω; $V_{DD1} = V_{DD2}$ = 3.5 to 5.5 V; f_{RF} = 400 to 1100 MHz	100	–	250	mV
		R_s = 50 Ω; $V_{DD1} = V_{DD2}$ = 2.6 to 5.5 V; f_{RF} = 50 to 400 MHz	150	–	400	mV
Z_I	input impedance (real part)	f_{RF} = 1 GHz; indicative, not tested	–	300	–	Ω
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{pm}	principle main divider ratio		512	–	131071	
Reference divider input; f_{XTALIN}						
f_{ref}	reference input frequency from crystal		3	–	35	MHz
$V_{XTALIN(rms)}$	sinusoidal input voltage (RMS value)		100	–	500	mV
Z_I	input impedance (real part)	f_{XTALIN} = 12.8 MHz; indicative, not tested	–	10	–	kΩ
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{rd}	reference divider ratio		8	–	4095	
Charge pump current setting resistor input; I_{SET}						
V_{SET}	voltage output on I_{SET}	R_{SET} = 12 kΩ to 60 kΩ	–	1.2	–	V
Charge pump outputs; CPA and CPB						
I_{CP}	charge pump sink or source current	R_{SET} = 15 kΩ; CRA/CRB = logic 1; $I_{cp} = I_{SET} \times 24$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	1.4	1.9	2.4	mA
		R_{SET} = 15 kΩ; CRA/CRB = logic 0; $I_{cp} = I_{SET} \times 12$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	0.7	0.96	1.2	mA
I_{LI}	charge pump off leakage current	$V_{cp} = 0.5V_{CC}$	–5	–	+5	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic input signal levels; DATA, CLK, $\overline{E}$ and HPD						
V_{IH}	HIGH level input voltage	at logic 1	$0.7V_{DD1}$	–	$V_{DD1} + 0.3$	V
V_{IL}	LOW level input voltage	at logic 0	–0.3	–	$0.3V_{DD1}$	V
I_{bias}	input bias currents	at logic 1 or logic 0	–5	–	+5	µA
C_I	input capacitance	indicative, not tested	–	1	–	pF
Port outputs/Out-of-lock; P0/OOL, P1, P2, P3 and f_{XTALO} - open drain outputs						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

SERIAL TIMING CHARACTERISTICS

V_{DD1} = 3 V; T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r, t_f	input rise and fall times	–	10	40	ns
t_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	2000	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

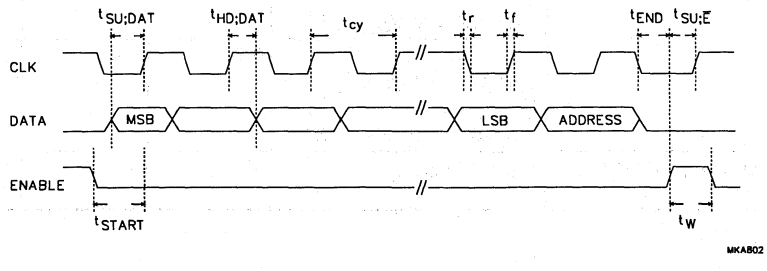
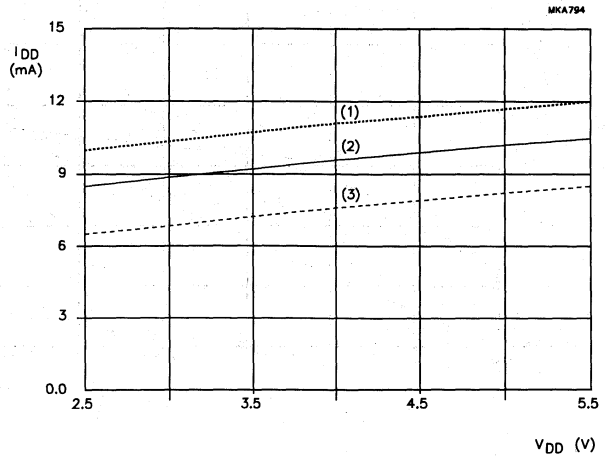


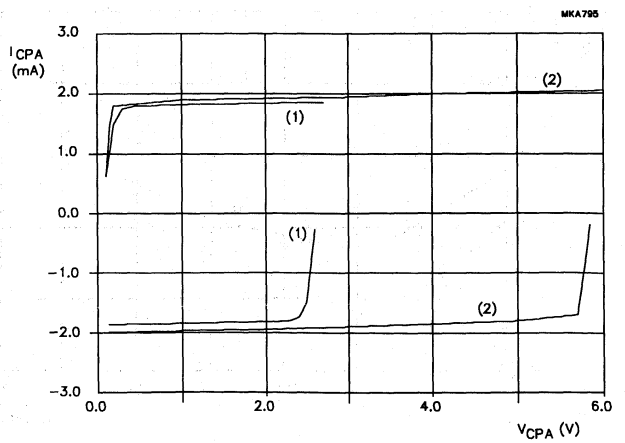
Fig.3 Serial bus timing diagram.

TYPICAL PERFORMANCE CHARACTERISTICS



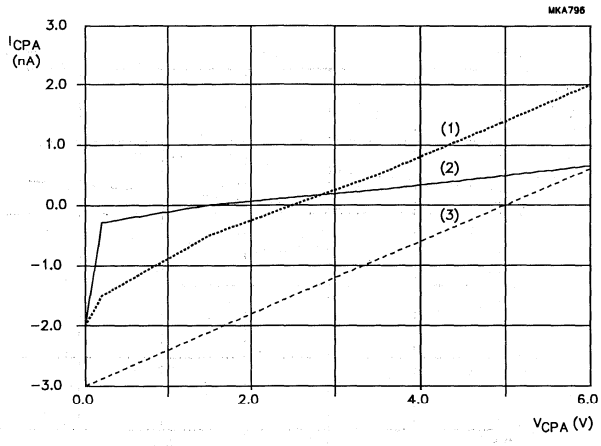
(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −30 °C.

Fig.4 I_{DD} as a function of V_{DD} with both synthesizers on and voltage doubler disabled.



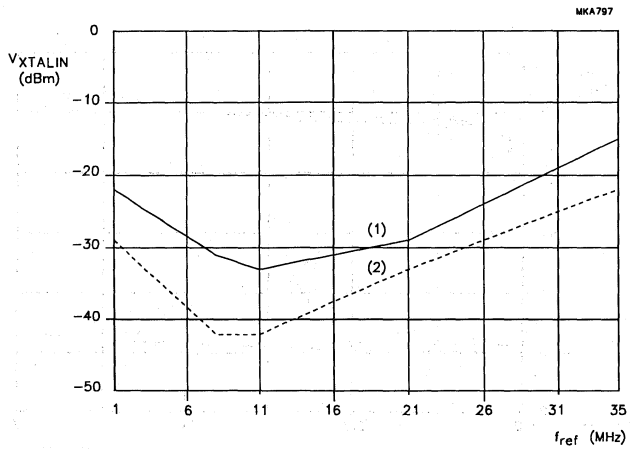
R_{SET} = 15 kΩ; CRA = 1.
(1) V_{CC} = 2.7 V.
(2) V_{CC} = 6.0 V.

Fig.5 Charge pump current as a function of CPA voltage.



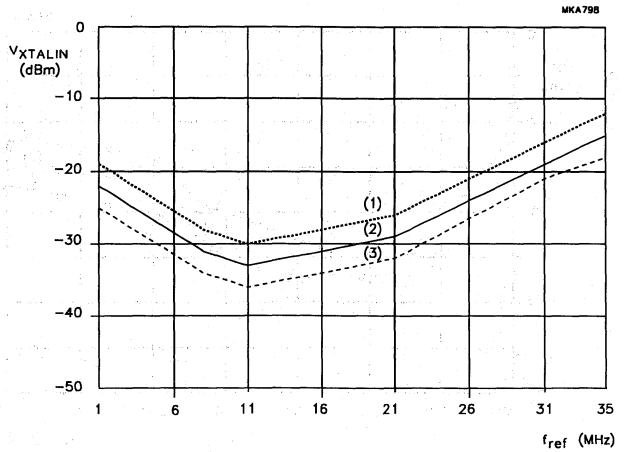
R_{SET} = 15 kΩ; CRA = 1.
(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −30 °C.

Fig.6 Charge pump 3-state current as a function of CPA voltage.



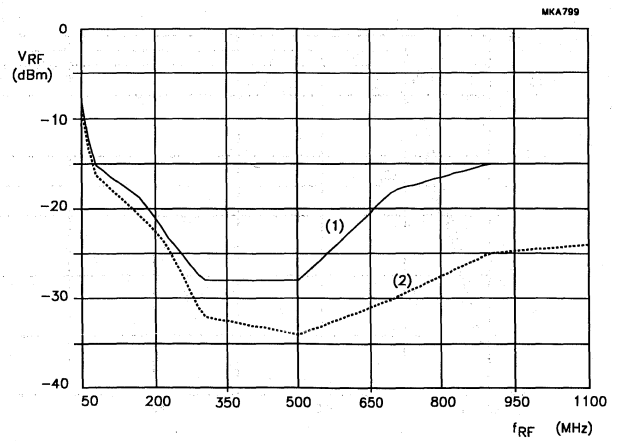
f_{XTALIN} externally terminated by 50 Ω load; AC-coupled.
(1) V_{DD} = 5.5 V.
(2) V_{DD} = 2.7 V.

Fig.7 Reference input sensitivity as a function of input frequency.



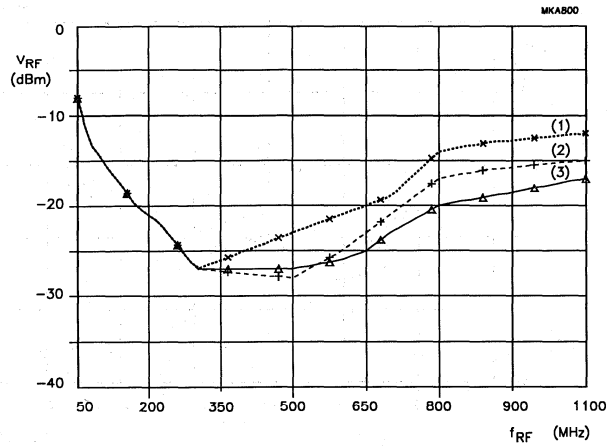
f_{XTALIN} externally terminated by 50 Ω load; AC-coupled.
(1) T_{amb} = −30 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.8 Reference input sensitivity as a function of input frequency with V_{DD} = 5.5 V.



RF input externally terminated by 50 Ω load; AC-coupled.
(1) V_{DD} = 5.5 V.
(2) V_{DD} = 2.7 V.

Fig.9 RF input sensitivity as a function of input frequency.



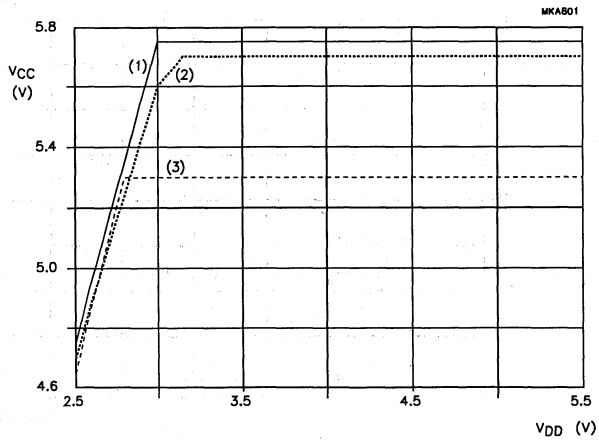
RF input externally terminated by 50 Ω load; AC-coupled.

(1) T_{amb} = −30 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = +85 °C.

Fig.10 RF input sensitivity as a function of input frequency with V_{DD} = 5.5 V.

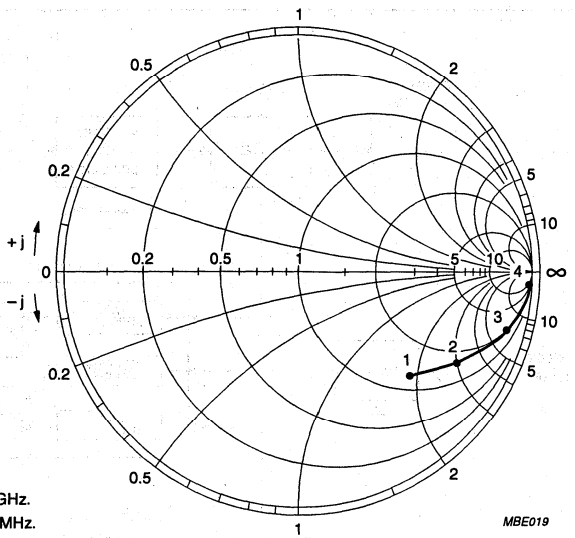


(1) T_{amb} = −30 °C.

(2) T_{amb} = +25 °C.

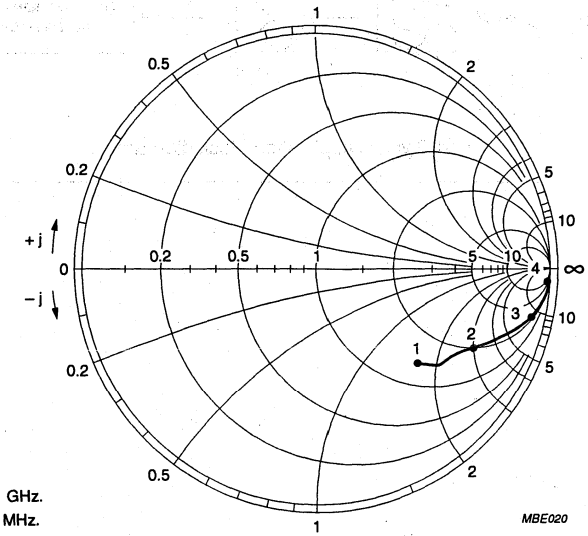
(3) T_{amb} = +85 °C.

Fig.11 Typical charge pump supply voltage as a function of V_{DD} voltage with voltage doubler enabled.



(1) 68.316 Ω, −92.457 Ω at 1.1 GHz.
(2) 85.914 Ω, −152.08 Ω at 800 MHz.
(3) 102.83 Ω, −354.66 Ω at 400 MHz.
(4) 853.75 Ω, −2.7735 kΩ at 50 MHz.

Fig.12 Input impedance as a function of input frequency; synthesizer A.



(1) 69.293 Ω, −78.027 Ω at 1.1 GHz.
(2) 100.2 Ω, −148.37 Ω at 800 MHz.
(3) 128.22 Ω, −378.81 Ω at 400 MHz.
(4) 674.25 Ω, −3.06 kΩ at 50 MHz.

Fig.13 Input impedance as a function of input frequency; synthesizer B.

APPLICATION INFORMATION

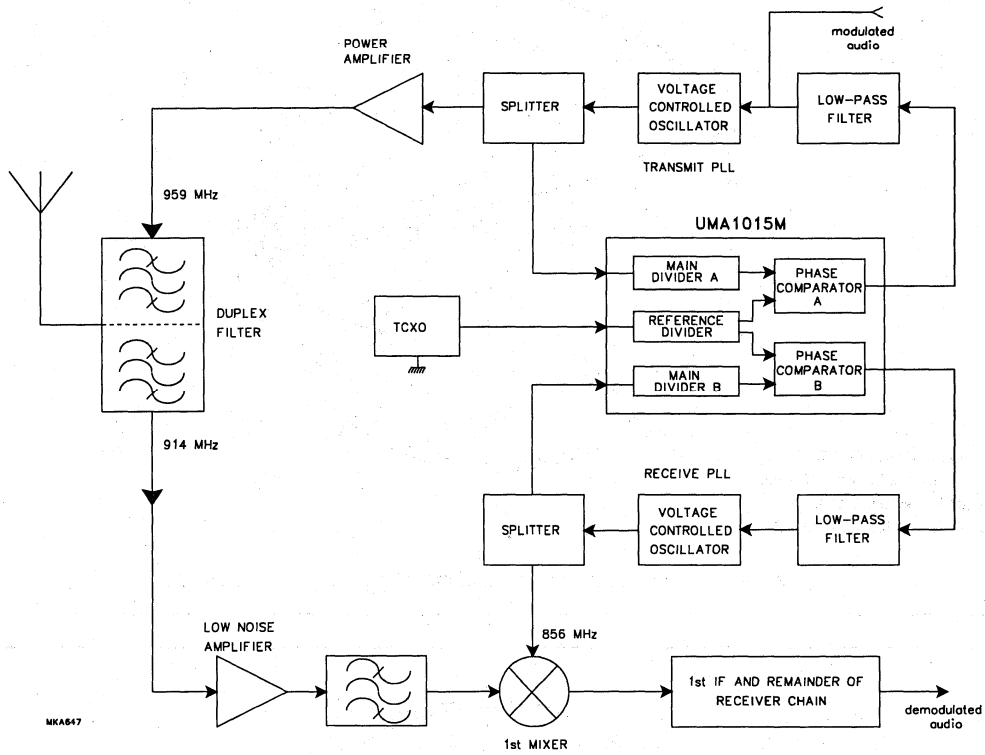


Fig.14 Typical application block diagram.

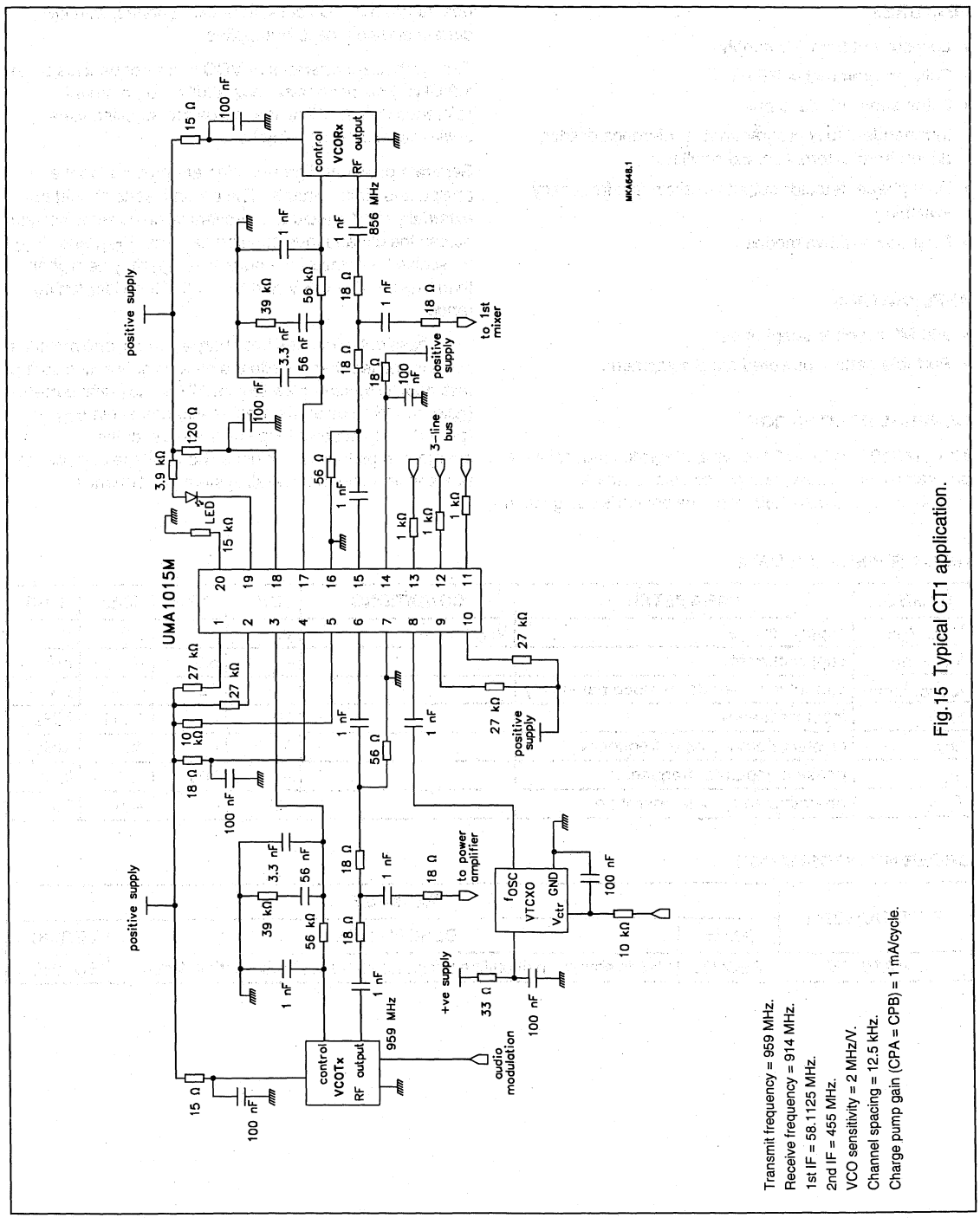


Fig.15 Typical CT1 application.

Low-voltage frequency synthesizer for radio telephones

UMA1017M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 900 MHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1017M BICMOS device integrates prescalers, a programmable divider, and phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The synthesizer operates at VCO input frequencies up to 1.2 GHz. The synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	supply current		–	6.9	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	µA
f_{VCO}	input frequency		50	–	1200	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1017M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

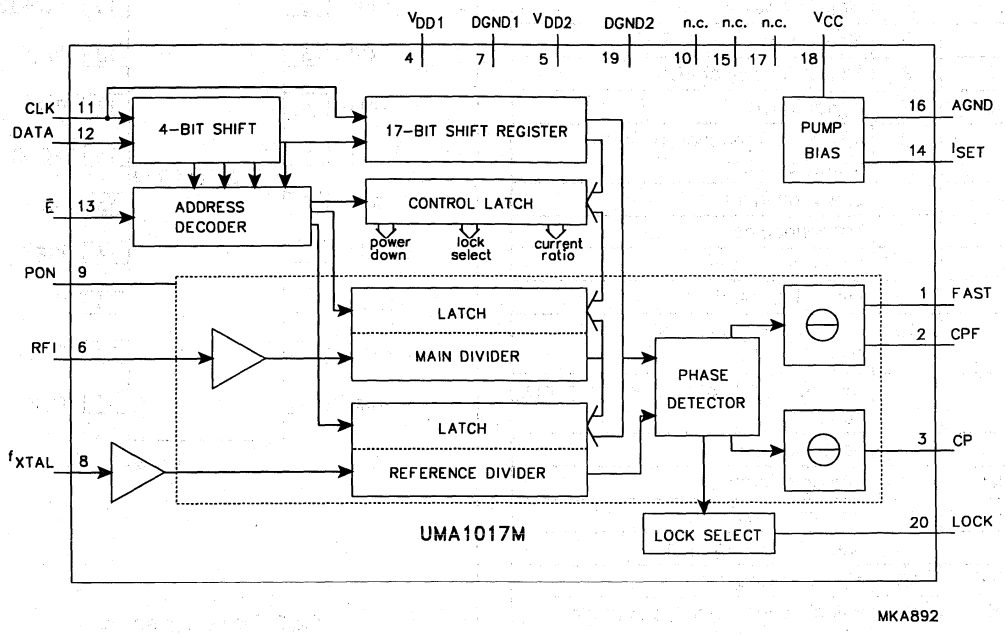


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPF	2	speed-up charge-pump output
CP	3	normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
RFI	6	1 GHz RF divider input
DGND1	7	digital ground 1
f_{XTAL}	8	reference frequency input from crystal oscillator
PON	9	power-on input
n.c.	10	not connected
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
n.c.	15	not connected
AGND	16	analog ground
n.c.	17	not connected
V_{CC}	18	supply for charge-pump
DGND2	19	digital ground 2
LOCK	20	in-lock detect output; test mode output

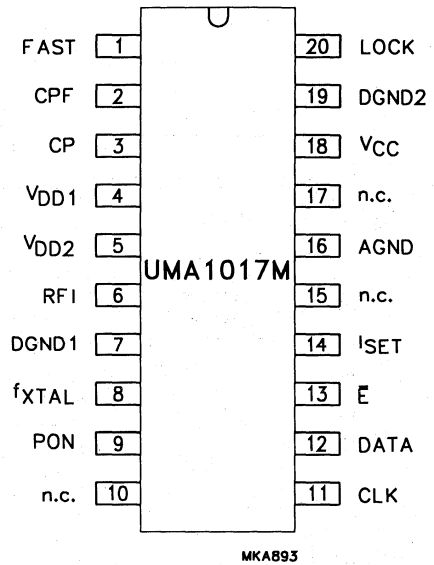


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

Programmable reference and main dividers drive the phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input PON (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The RFI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 50 mV up to 300 mV (RMS), and at frequencies as high as 1.2 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 1 MHz phase comparison with the 500 MHz inputs, and a 10 kHz phase comparison at 1.2 GHz RF.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The synthesizer speed-up charge pump (CPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μA. The output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

However when the synthesizer is powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1017M uses 4 of the 16 available addresses. These are chosen to allow direct compatibility with the UAA2072M integrated front-end. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Power-down mode

The power-down signal can be either hardware (PON) or software (sPON). The dividers are on when both PON and sPON are at logic 1.

When the synthesizer is reactivated after power-down the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

Table 1 Format of programmed data

LAST IN	PROGRAMMING REGISTER BIT USAGE							FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	REGISTER BIT ALLOCATION																				LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS(2)																	0	0	0	0
X	X	X	X	OOL	X	CR1	CR0	X	X	sPON	X	X	X	X	X	X	0	0	0	1
PM16	MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1

Notes

1. FT = first, LT = last; sPON = software power-up for synthesizer (1 = ON); OOL = out-of-lock (1 = enabled).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; bias current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
$\Delta V_{CC}-V_{DD}$	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8, 9, 11 to 14 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3}$	voltage at pins 2 and 3	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	V_{DD} = 5.5 V	–	6.5	8.5	mA
I_{CC}	charge pumps analog supply current	V_{CC} = 5.5 V; R_{ext} =12 kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	µA
RF main divider input; pin 6						
f_{VCO}	VCO input frequency	2.7 V < V_{DD} < 4.5 V	50	–	1200	MHz
		2.7 V < V_{DD} < 5.5 V	50	–	1100	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 2.7 V < V_{DD} < 3.5 V; 0.5 < f_{VCO} < 1.2 GHz	50	–	300	mV
		R_s = 50 Ω; 2.7 V < V_{DD} < 5.5 V; 0.5 < f_{VCO} < 1.1 GHz	100	–	300	mV
		R_s = 50 Ω; 2.7 V < V_{DD} < 5.5 V; 50 < f_{VCO} < 500 MHz	150	–	300	mV
Z_I	input impedance (real part)	f_{VCO} = 1 GHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_m	main divider ratio		512	–	131071	
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
f_{PCmin}	minimum loop comparison frequency		–	10	–	kHz
Synthesizer reference divider input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_r	reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump outputs; pins 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		−25	−	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	−	±5	−	%
I_{Lcp}	charge pump off leakage current	$V_{cp} = ½V_{CC}$	−5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	−	$V_{CC} - 0.4$	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		−0.3	−	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	−5	−	+5	µA
C_I	input capacitance	indicative, not tested	−	2	−	pF
Lock detect output signal; pin 20 (open-drain output)						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	−	−	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	2000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 µs provided all the following conditions are satisfied:

   a) Main divider input frequency $f_{VCO} > \frac{256}{t_W}$

   b) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$.

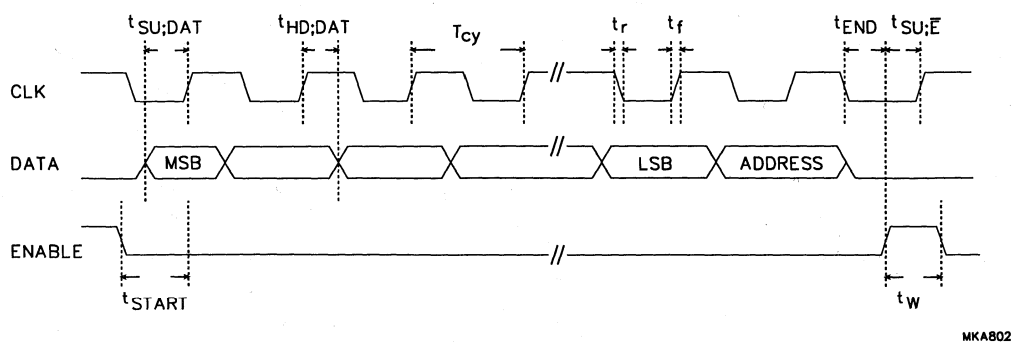


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

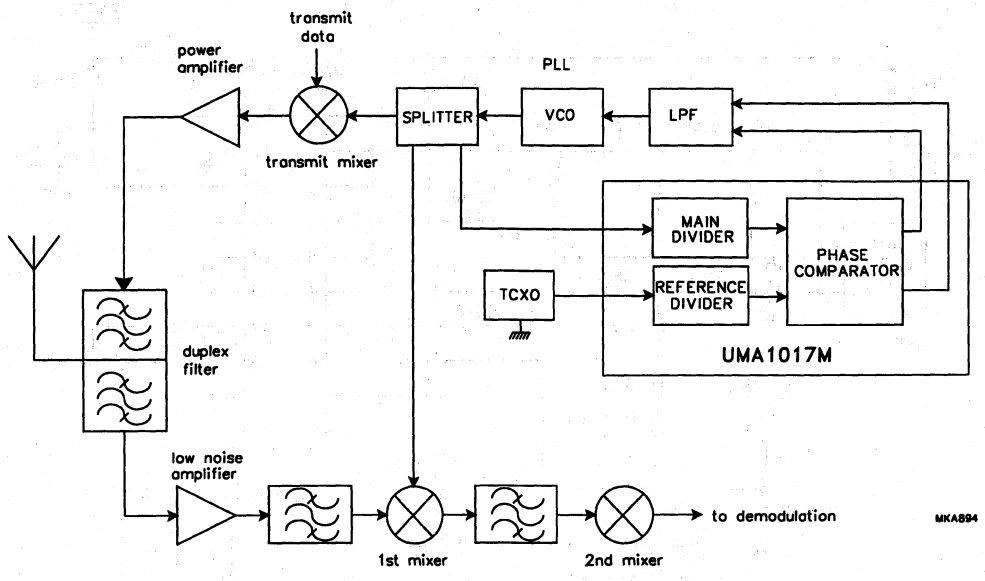


Fig.4 Typical application block diagram.

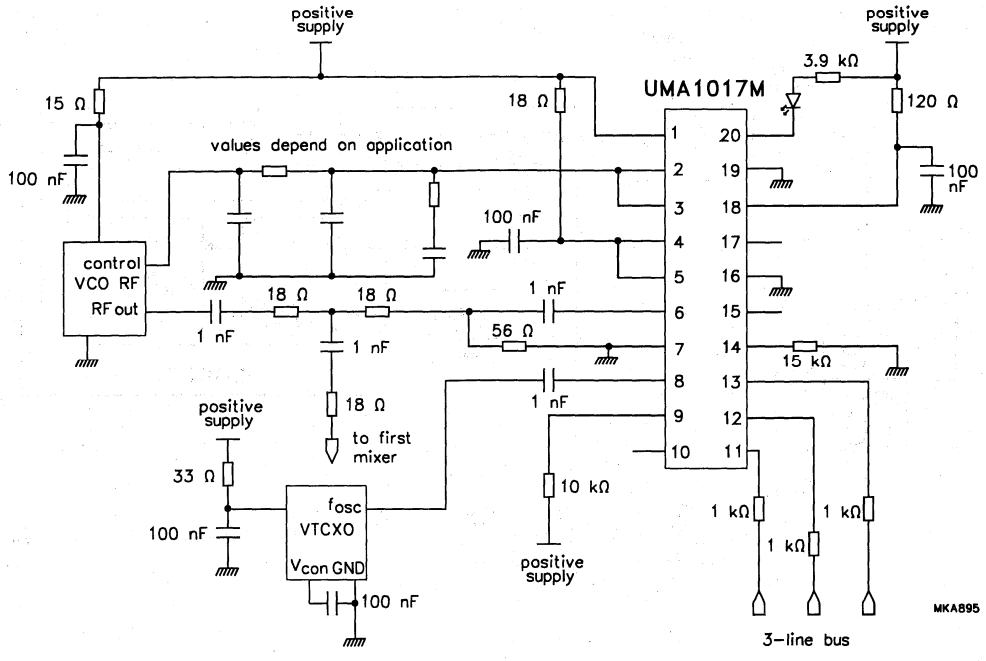


Fig.5 Typical test and application diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1018M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Integrated digital-to-analog converter
- Dual power-down modes.

APPLICATIONS

- 900 MHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1018M BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at VCO input frequencies up to1.2 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance. An on-chip 8-bit DAC enables adjustment of an external function, such as the temperature compensation of a crystal oscillator in Global System for Mobile communications (GSM).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	principal synthesizer supply current	auxiliary synthesizer in power-down mode	–	6.9	–	mA
	principal and auxiliary synthesizer supply current	principal and auxiliary synthesizer ON	–	9.6	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	µA
f_{PI}	principal input frequency		50	–	1200	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principal phase comparator frequency		–	200	–	kHz
f_{APC}	auxiliary phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

Low-voltage dual frequency synthesizer for radio telephones

UMA1018M

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1018M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

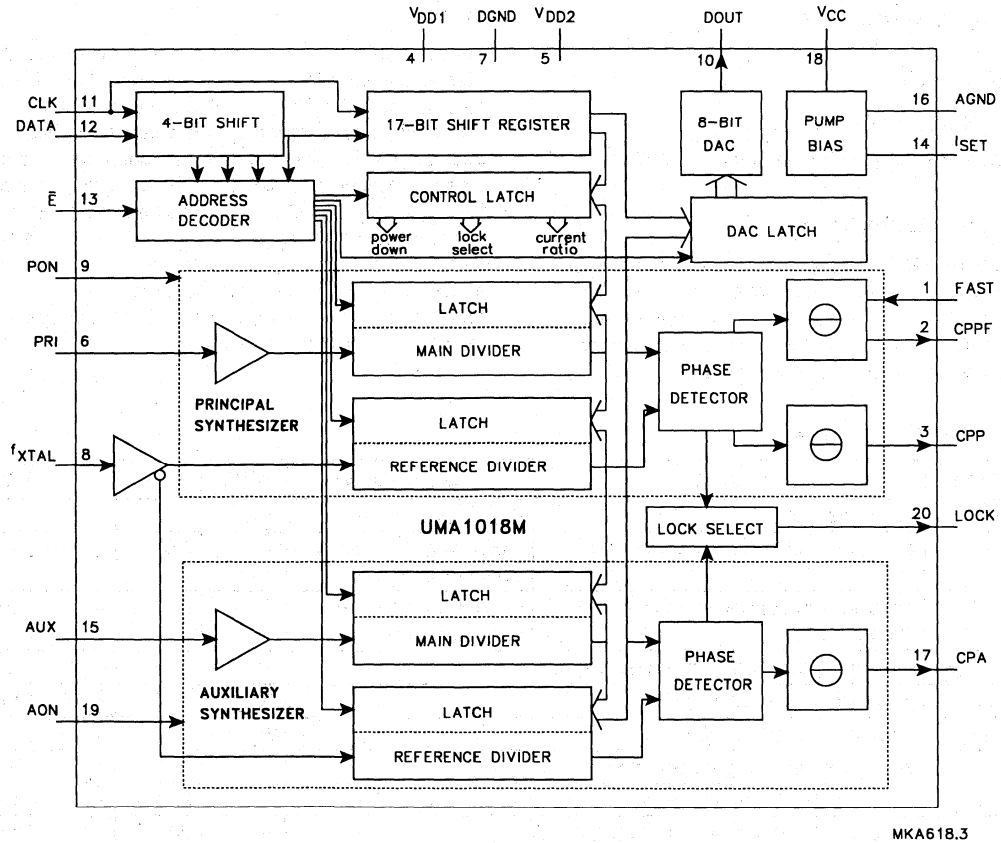


Fig.1 Block diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1018M

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principal synthesizer speed-up charge-pump output
CPP	3	principal synthesizer normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
PRI	6	1 GHz principal synthesizer RF divider input
DGND	7	digital ground
f_{XTAL}	8	common reference frequency input from crystal oscillator
PON	9	principal synthesizer power-on input
DOUT	10	8-bit digital-to-analog output
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump and DAC circuits
AON	19	auxiliary synthesizer power-on input
LOCK	20	in-lock detect output (main PLL); test mode output

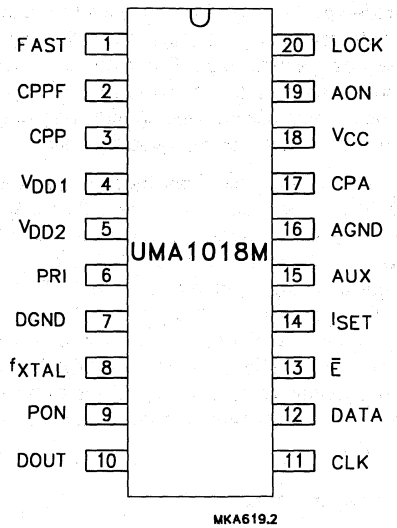


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input PON (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 50 mV up to 300 mV (RMS), and at frequencies as high as 1.2 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 1 MHz phase comparison with the 500 MHz inputs, and a 10 kHz phase comparison at 1.2 GHz RF.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus.

The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 µA. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AON (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the main reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1018M uses 6 of the 16 available addresses. These are chosen to allow direct compatibility with the UAA2072M integrated front-end. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data

LAST IN	PROGRAMMING REGISTER BIT USAGE							FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	REGISTER BIT ALLOCATION																				LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS[2]																	0	0	0	0
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPON	sAON	X	X	X	X	X	0	0	0	1
PM16	PRINCIPAL MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	PRINCIPAL REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR0	0	1	1	1
X	X	X	X	X	X	X	X	X	DA7	8-BIT DAC FOR EXTERNAL TRIM						DA0	1	0	0	0

Notes

1. FT = first, LT = last; sPON = software power-up for principal synthesizer (1 = ON); sAON = software power-up for auxiliary synthesizer (1 = ON).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Out-of-lock select

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principal phase error
1	1	both auxiliary and principal

Table 4 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	$I_{CPPF} : I_{CPP}$
0	0	$4 \times I_{SET}$	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$4 \times I_{SET}$	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$4 \times I_{SET}$	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps and DAC.

Table 5 Power-down modes

AON	PON	FAST	PRINCIPAL DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF	DAC AND BIAS
0	0	X	OFF	OFF	OFF	OFF	OFF	OFF
0	1	0	ON	OFF	OFF	ON	OFF	ON
0	1	1	ON	OFF	OFF	ON	ON	ON
1	0	X	OFF	ON	ON	OFF	OFF	ON
1	1	0	ON	ON	ON	ON	OFF	ON
1	1	1	ON	ON	ON	ON	ON	ON

Digital-to-analog converter

The byte loaded via the bus into the appropriate latch drives a digital-to-analog converter. The internal current is scaled by the external resistance (R_{ext}) at pin I_{SET}, similar to the charge pumps. The nominal full-scale current is $4 \times I_{SET}$. The output current is mirrored to produce a full-scale voltage into a user-defined ground referenced resistance, thereby allowing optimum swing from power supply rails within the 2.7 to 5.5 V limits. The band gap reference voltage at pin I_{SET} is temperature and supply independent. The DAC signal is monotonic across the full range of digital input codes to enable fine adjustment of other system blocks. The typical settling time for full-scale switching is 400 ns into a 12 kΩ // 20 pF load. DAC functionality is neither tested nor guaranteed on the UMA1018M/C1/S1 version.

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

Note that in Table 5 PON and AON can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 1.

When either synthesizer is reactivated after power-down the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	V_{DD} = 5.5 V	–	6.5	8.5	mA
	auxiliary synthesizer digital supply current	V_{DD} = 5.5 V	–	2.7	4.0	mA
I_{CC}	charge pumps and DAC analog supply current (DAC setting FFH)	V_{CC} = 5.5 V; R_{ext} = 12 kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF principal main divider input; pin 6						
f_{VCO}	VCO input frequency	2.7 V < V_{DD} < 4.5 V	50	–	1200	MHz
		2.7 V < V_{DD} < 5.5 V	50	–	1100	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 2.7 V < V_{DD} < 3.5 V; 0.5 < f_{VCO} < 1.2 GHz	50	–	300	mV
		R_s = 50 Ω; 2.7 V < V_{DD} < 5.5 V; 0.5 < f_{VCO} < 1.1 GHz	100	–	300	mV
		R_s = 50 Ω; 2.7 V < V_{DD} < 5.5 V; 50 < f_{VCO} < 500 MHz	150	–	300	mV
Z_I	input impedance (real part)	f_{VCO} = 1 GHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131071	
f_{PPCmax}	maximum principal loop comparison frequency		–	2000	–	kHz
f_{PPCmin}	minimum principal loop comparison frequency		–	10	–	kHz
Auxiliary loop main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 2.7 V < V_{DD} < 3.5 V	50	–	500	mV
		R_s = 50 Ω; 3.5 V < V_{DD} < 5.5 V	100	–	500	mV
Z_I	input impedance (real part)	f_{AI} = 100 MHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{APCmax}	maximum auxiliary loop comparison frequency		–	2000	–	kHz
f_{APCmin}	minimum auxiliary loop comparison frequency		–	10	–	kHz
Dual synthesizer reference divider input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference division ratio		8	–	2047	
R_{ar}	auxiliary reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 17, 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	V_{cp} = ½V_{CC}	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	V_{CC} – 0.4	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3V_{DD}	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	µA
C_I	input capacitance	indicative, not tested	–	2	–	pF
DAC output signal levels; pin 10, R_{ext} = 12 kΩ						
I_{DAC}	DAC full scale output current		3 × I_{SET}	4 × I_{SET}	5 × I_{SET}	mA
V_{10}	output voltage compliance	all codes	0	–	V_{DD} – 0.4	V
I_{10min}	minimum DAC current	00 code	–	2	5	µA
I_{monot}	worst case monotonicity test: $\Delta I \times 256/400$ µA	note 1	0.1	–	1.9	
Lock detect output signal; pin 20 open-drain output						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

Note

1. ΔI is the change in DAC output current when making the code transitions: 7FH/80H, 3FH/40H or 1FH/20H.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	2000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 µs provided all the following conditions are satisfied:

   a) Principal main divider input frequency $f_{VCO} > \frac{256}{t_W}$

   b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$

   c) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$

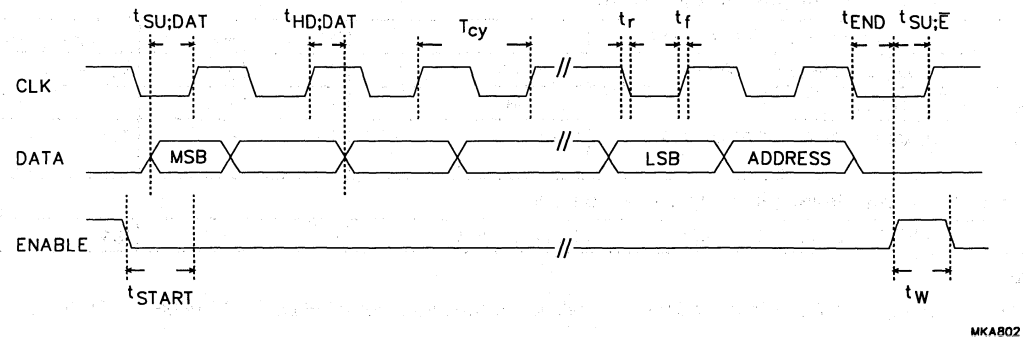


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

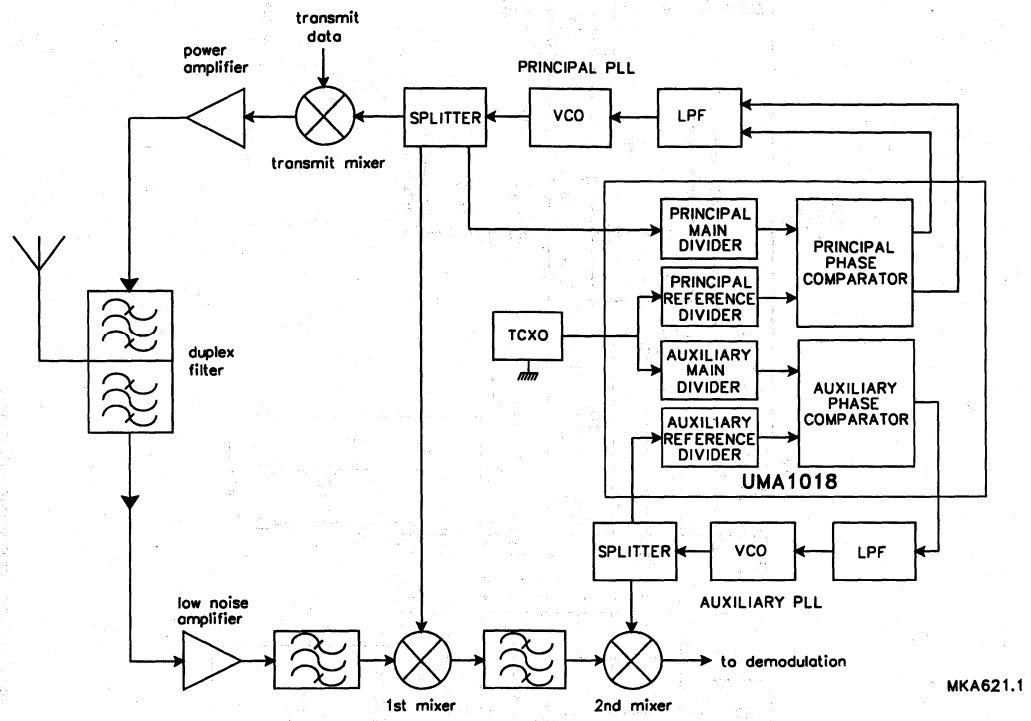


Fig.4 Typical application block diagram.

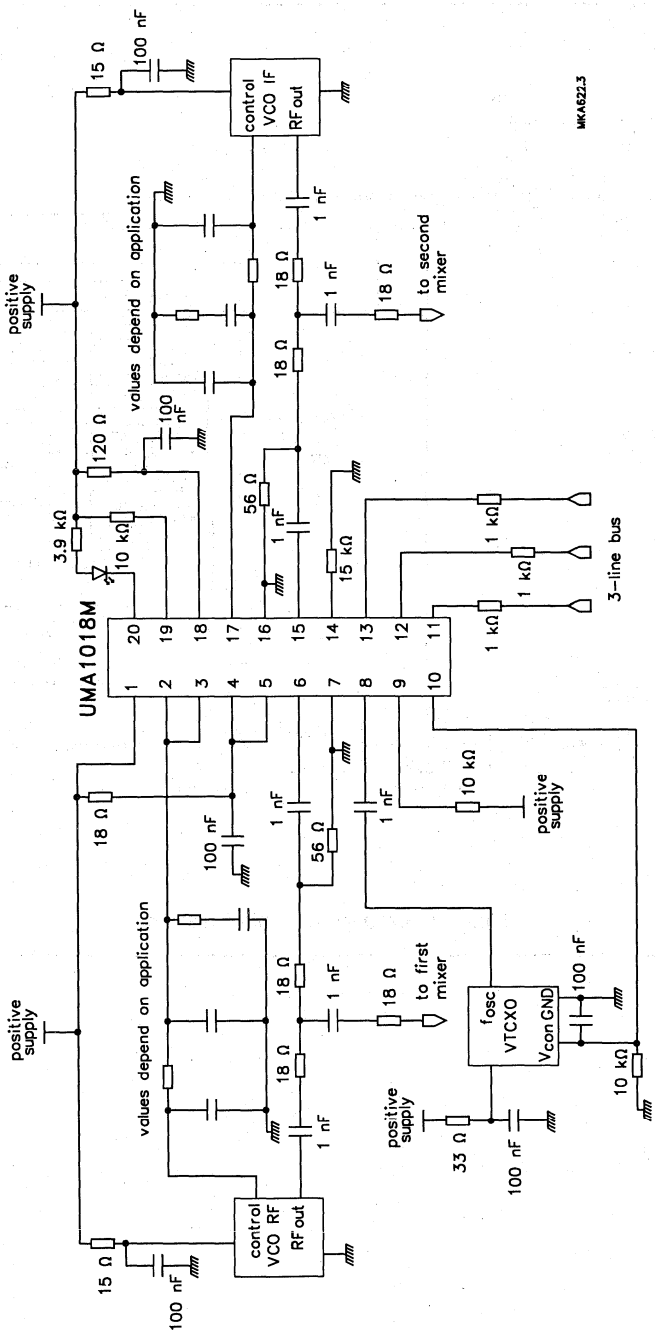


Fig.5 Typical test and application diagram.

Low-voltage frequency synthesizer for radio telephones

UMA1019AM

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 1 to 1.7 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1019AM BICMOS device integrates prescalers, a programmable divider, and phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The synthesizer operates at VCO input frequencies up to 1.7 GHz. The synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	supply current		–	9.4	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	µA
f_{VCO}	input frequency		1000	1500	1700	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1019AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

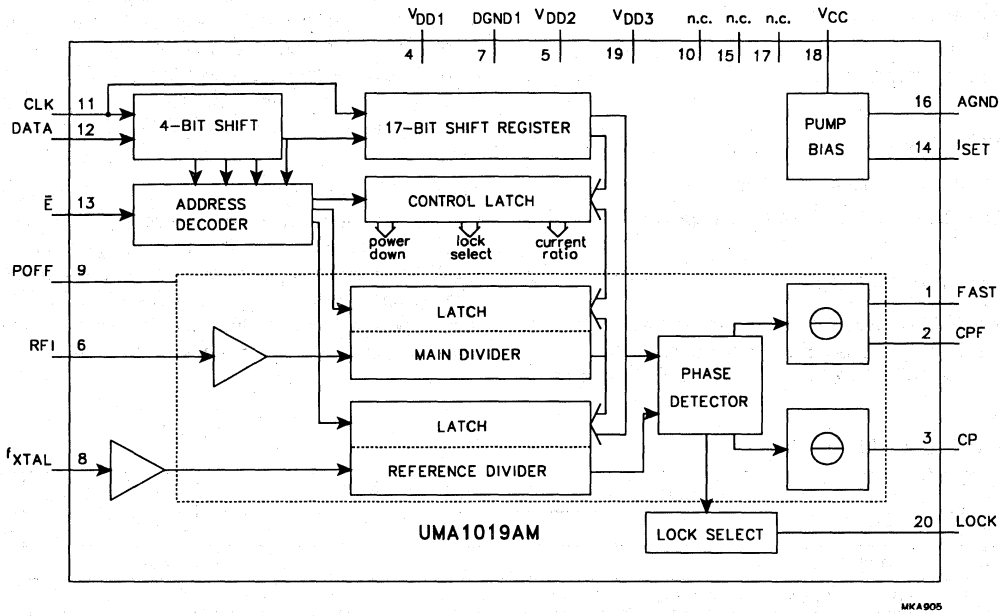


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPF	2	speed-up charge-pump output
CP	3	normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
RFI	6	1 GHz RF divider input
DGND1	7	digital ground 1
f_{XTAL}	8	reference frequency input from crystal oscillator
POFF	9	power-down input
n.c.	10	not connected
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
n.c.	15	not connected
AGND	16	analog ground
n.c.	17	not connected
V_{CC}	18	supply for charge-pump
V_{DD3}	19	digital power supply 3
LOCK	20	in-lock detect output; test mode output

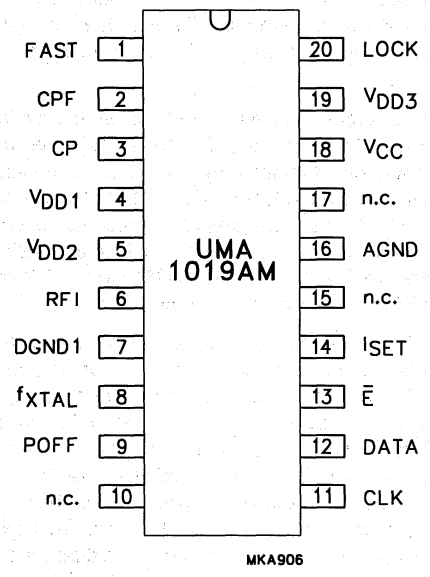


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

Programmable reference and main dividers drive the phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The RFI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 100 mV up to 500 mV (RMS), and at frequencies as high as 1.7 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow up to 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The synthesizer speed-up charge pump (CPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 µA. The output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

However when the synthesizer is powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1019AM uses 4 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Power-down mode

The power-down signal can be either hardware (POFF) or software (sPOFF). The dividers are on when both POFF and sPOFF are at logic 0.

When the synthesizer is reactivated after power-down the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

Table 1 Format of programmed data

LAST IN	PROGRAMMING REGISTER BIT USAGE							FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	REGISTER BIT ALLOCATION																			LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS[2]																	0	0	0	0
X	X	X	X	OOL	X	CR1	CR0	X	X	sPOFF	X	X	X	X	X	X	0	0	0	1
PM16	MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1

Notes

1. FT = first, LT = last; sPOFF = software power-down for synthesizer (1 = OFF); OOL = out-of-lock (1 = enabled).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; bias current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
$\Delta V_{CC}-V_{DD}$	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8, 9, 11 to 14 and 20	−0.3	V_{DD} + 0.3	V
$V_{2,3}$	voltage at pins 2 and 3	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2} = V_{DD3}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	V_{DD} = 5.5 V	–	9	11	mA
I_{CC}	charge pumps analog supply current	V_{CC} = 5.5 V; R_{ext} =12 kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF main divider input; pin 6						
f_{VCO}	VCO input frequency		1000	1500	1700	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω	100	–	500	mV
Z_I	input impedance (real part)	f_{VCO} = 2 GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_m	main divider ratio		512	–	131071	
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
f_{PCmin}	minimum loop comparison frequency		–	10	–	kHz
Synthesizer reference divider input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_r	reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	V_{cp} = ½V_{CC}	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	V_{CC} – 0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	µA
C_I	input capacitance	indicative, not tested	–	2	–	pF
Lock detect output signal; pin 20 (open-drain output)						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	−20	–	–	ns
t_W	minimum inactive pulse width	2000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 µs provided all the following conditions are satisfied:

   a) Main divider input frequency $f_{VCO} > \frac{512}{t_W}$

   b) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$.

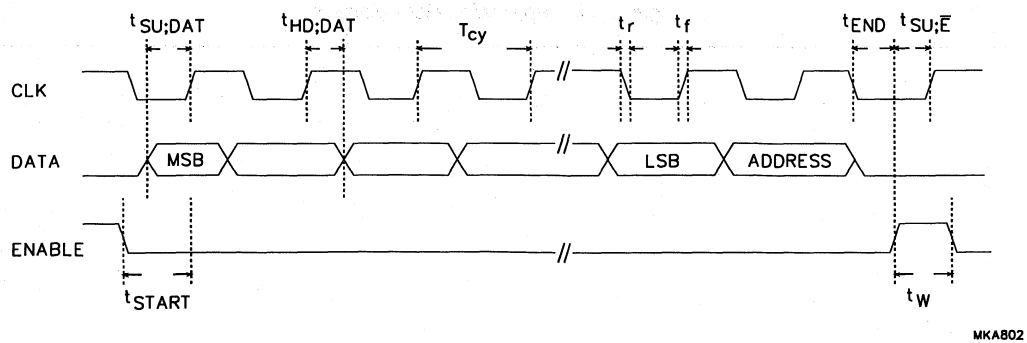


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

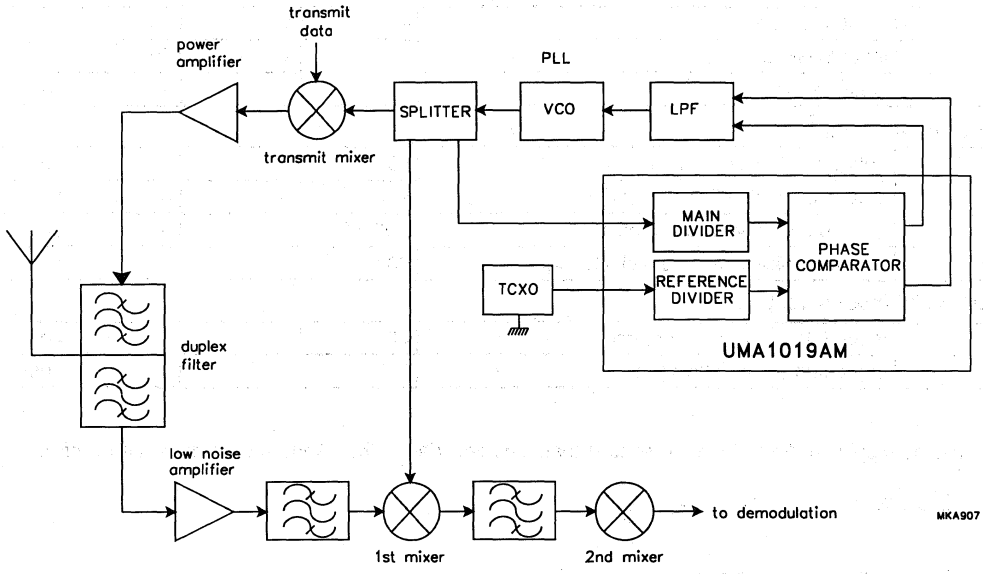


Fig.4 Typical application block diagram.

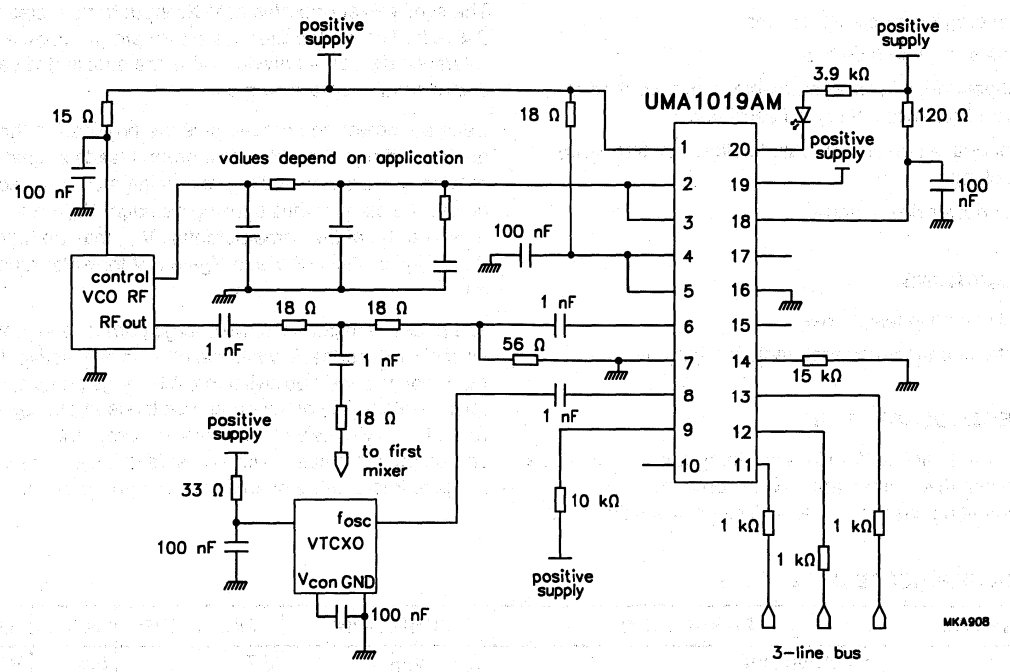


Fig.5 Typical test and application diagram.

Low-voltage frequency synthesizer for radio telephones

UMA1019M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1019M BICMOS device integrates prescalers, a programmable divider, and phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The synthesizer operates at VCO input frequencies up to 2.4 GHz. The synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	supply current		–	9.4	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	µA
f_{VCO}	input frequency		1650	1900	2400	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1019M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

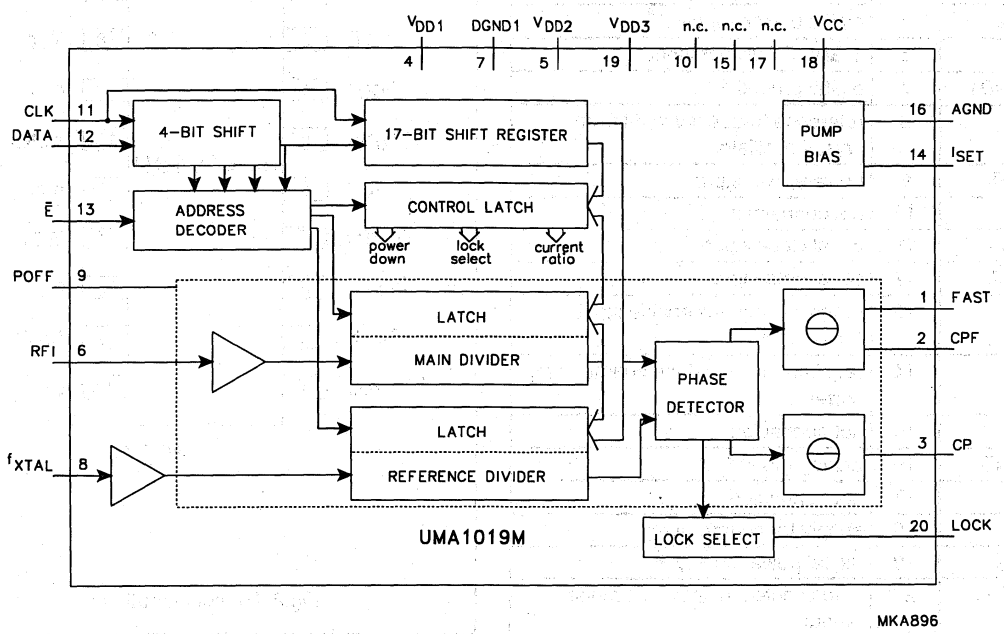


Fig.1 Block diagram.

Low-voltage frequency synthesizer for radio telephones

UMA1019M

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPF	2	speed-up charge-pump output
CP	3	normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
RFI	6	1 GHz RF divider input
DGND1	7	digital ground 1
f_{XTAL}	8	reference frequency input from crystal oscillator
POFF	9	power-down input
n.c.	10	not connected
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
n.c.	15	not connected
AGND	16	analog ground
n.c.	17	not connected
V_{CC}	18	supply for charge-pump
V_{DD3}	19	digital power supply 3
LOCK	20	in-lock detect output; test mode output

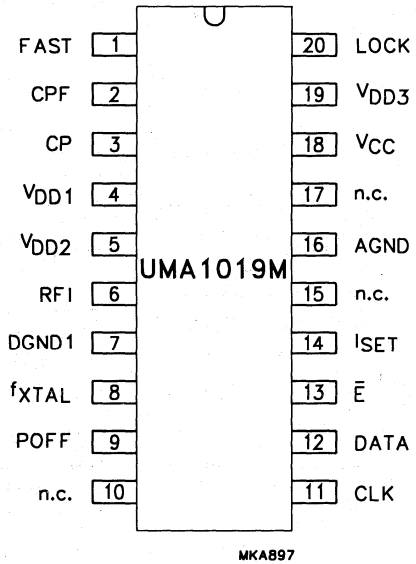


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

Programmable reference and main dividers drive the phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The RFI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 60 mV up to 180 mV (RMS), and at frequencies as high as 2.4 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The synthesizer speed-up charge pump (CPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μA. The output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

However when the synthesizer is powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1019M uses 4 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Power-down mode

The power-down signal can be either hardware (POFF) or software (sPOFF). The dividers are on when both POFF and sPOFF are at logic 0.

When the synthesizer is reactivated after power-down the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

Table 1 Format of programmed data

LAST IN			PROGRAMMING REGISTER BIT USAGE					FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT							REGISTER BIT ALLOCATION													LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS(2)																	0	0	0	0
X	X	X	X	OOL	X	CR1	CR0	X	X	sPOFF	X	X	X	X	X	X	0	0	0	1
PM16	MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1

Notes

1. FT = first, LT = last; sPOFF = software power-down for synthesizer (1 = OFF); OOL = out-of-lock (1 = enabled).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; bias current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
$\Delta V_{CC}-V_{DD}$	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8, 9, 11 to 14 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3}$	voltage at pins 2 and 3	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2} = V_{DD3}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	$V_{DD} = 5.5$ V	–	9	11	mA
I_{CC}	charge pumps analog supply current	$V_{CC} = 5.5$ V; $R_{ext} = 12$ kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF main divider input; pin 6						
f_{VCO}	VCO input frequency		1650	1900	2400	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω; $1.65 < f_{VCO} < 2$ GHz	60	–	400	mV
		$R_s = 50$ Ω; $1.65 < f_{VCO} < 2.4$ GHz	60	–	180	mV
Z_I	input impedance (real part)	$f_{VCO} = 2$ GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_m	main divider ratio		512	–	131071	
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
f_{PCmin}	minimum loop comparison frequency		–	10	–	kHz
Synthesizer reference divider input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz $< f_{XTAL} < 40$ MHz	50	–	500	mV
		3 MHz $< f_{XTAL} < 40$ MHz	100	–	500	mV
Z_I	input impedance (real part)	$f_{XTAL} = 30$ MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_r	reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	$R_{ext} = 12$ kΩ	–	1.15	–	V
Charge pump outputs; pins 3 and 2; $R_{ext} = 12$ kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	$V_{cp} = \frac{1}{2}V_{CC}$	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	$V_{CC} - 0.4$	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	µA
C_I	input capacitance	indicative, not tested	–	2	–	pF
Lock detect output signal; pin 20 (open-drain output)						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	2000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 µs provided all the following conditions are satisfied:
   a) Main divider input frequency $f_{VCO} > \frac{512}{t_W}$
   b) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$.

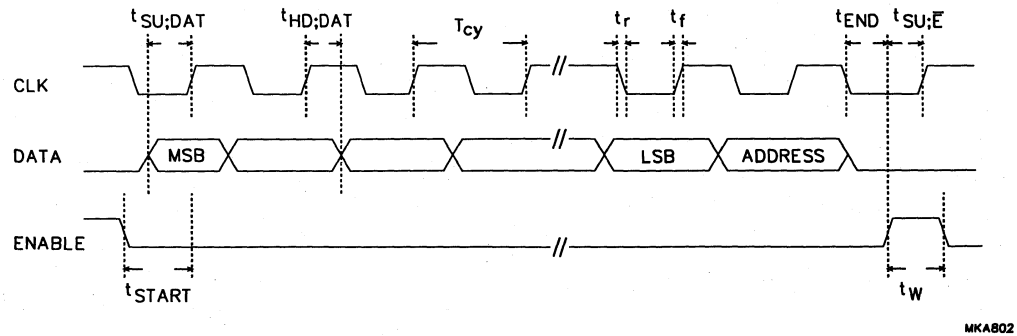


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

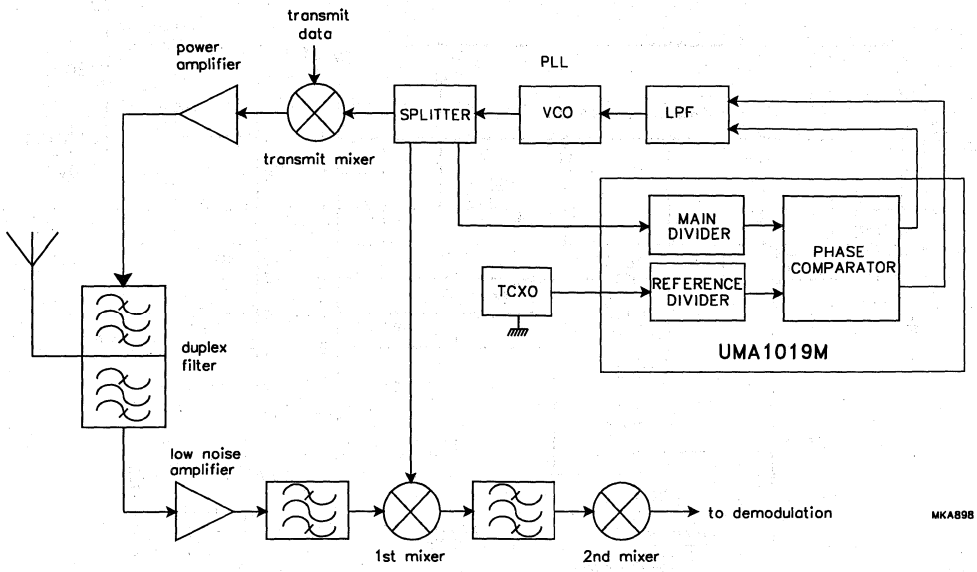


Fig.4 Typical application block diagram.

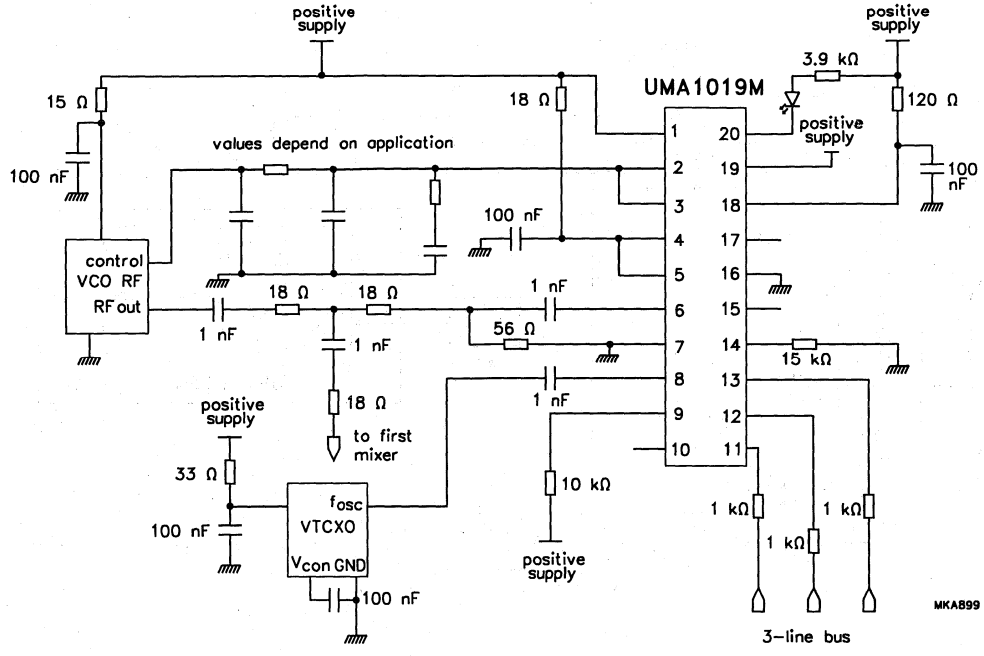


Fig.5 Typical test and application diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020AM

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 1 to 1.7 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1020AM BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at VCO input frequencies up to 1.7 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	principal synthesizer supply current	auxiliary synthesizer in power-down mode	–	9.4	–	mA
	principal and auxiliary synthesizer supply current	principal and auxiliary synthesizer ON	–	12.1	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	µA
f_{VCO}	principal input frequency		1000	1500	1700	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principal phase comparator frequency		–	200	–	kHz
f_{APC}	auxiliary phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1020AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

Low-voltage dual frequency synthesizer for radio telephones

UMA1020AM

BLOCK DIAGRAM

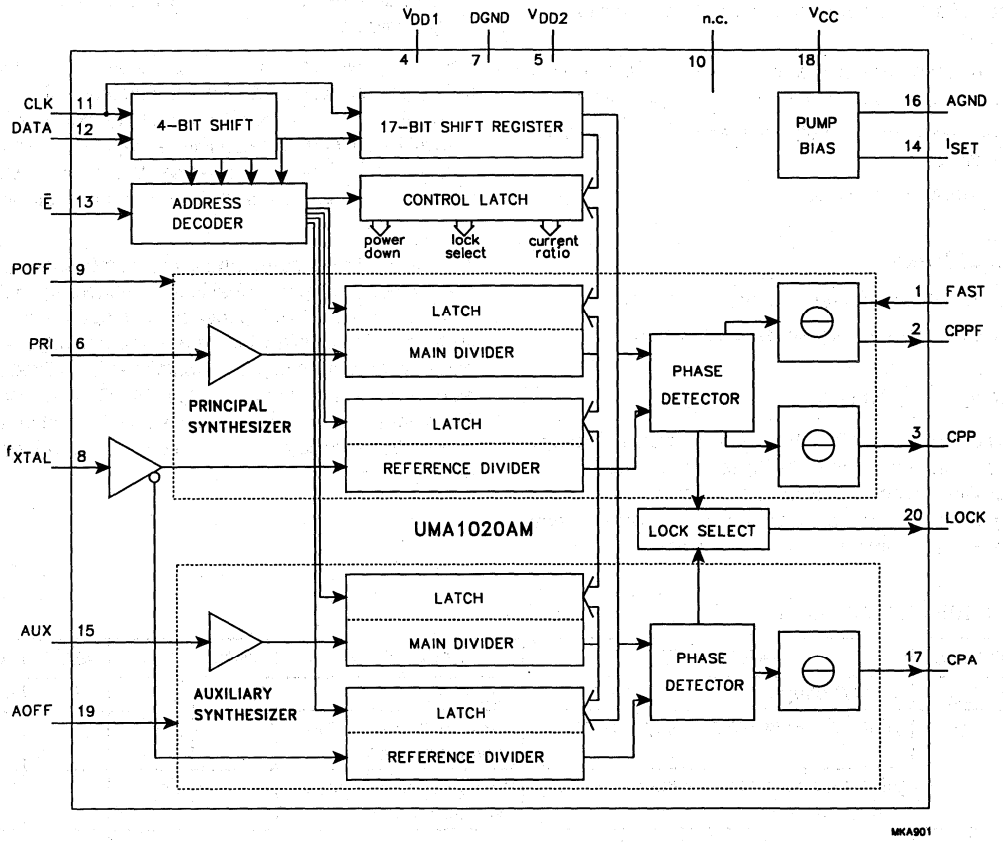


Fig.1 Block diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020AM

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principal synthesizer speed-up charge-pump output
CPP	3	principal synthesizer normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
PRI	6	1 GHz principal synthesizer RF divider input
DGND	7	digital ground
f_{XTAL}	8	common reference frequency input from crystal oscillator
POFF	9	principal synthesizer power-down input
n.c.	10	not connected
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump and DAC circuits
AOFF	19	auxiliary synthesizer power-down input
LOCK	20	in-lock detect output (main PLL); test mode output

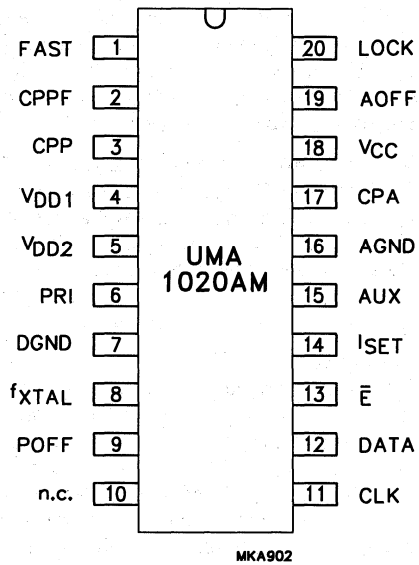


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 100 mV to 500 mV (RMS), and at frequencies up to 1.7 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow up to 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 μA. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AOFF (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the main reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1020AM uses 5 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers.

This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data

LAST IN			PROGRAMMING REGISTER BIT USAGE					FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT					REGISTER BIT ALLOCATION															LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS[2]																	0	0	0	0
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPOFF	sAOFF	X	X	X	X	X	0	0	0	1
PM16	PRINCIPAL MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	PRINCIPAL REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR0	0	1	1	1

Notes

1. FT = first, LT = last; sPOFF = software power-down for principal synthesizer (1 = OFF); sAOFF = software power-down for auxiliary synthesizer (1 = OFF).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Out-of-lock select

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principal phase error
1	1	both auxiliary and principal

Table 4 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	$I_{CPPF} : I_{CPP}$
0	0	$4 \times I_{SET}$	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$4 \times I_{SET}$	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$4 \times I_{SET}$	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps.

Table 5 Power-down modes

AOFF	POFF	FAST	PRINCIPAL DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF
1	1	X	OFF	OFF	OFF	OFF	OFF
1	0	0	ON	OFF	OFF	ON	OFF
1	0	1	ON	OFF	OFF	ON	ON
0	1	X	OFF	ON	ON	OFF	OFF
0	0	0	ON	ON	ON	ON	OFF
0	0	1	ON	ON	ON	ON	ON

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

Note that in Table 5 POFF and AOFF can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 0.

When either synthesizer is reactivated after power-down the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	V_{DD} = 5.5 V	–	9	11	mA
	auxiliary synthesizer digital supply current	V_{DD} = 5.5 V	–	2.7	4.0	mA
I_{CC}	charge pumps supply current	V_{CC} = 5.5 V; R_{ext} =12 kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	µA
RF principal main divider input; pin 6						
f_{VCO}	VCO input frequency		1000	1500	1700	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω	100	–	500	mV
Z_I	input impedance (real part)	f_{VCO} = 2 GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131071	
f_{PPCmax}	maximum principal loop comparison frequency		–	2000	–	kHz
f_{PPCmin}	minimum principal loop comparison frequency		–	10	–	kHz
Auxiliary loop main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 2.7 V < V_{DD} < 3.5 V	50	–	500	mV
		R_s = 50 Ω; 3.5 V < V_{DD} < 5.5 V	100	–	500	mV
Z_I	input impedance (real part)	f_{AI} = 100 MHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	
f_{APCmax}	maximum auxiliary loop comparison frequency		–	2000	–	kHz
f_{APCmin}	minimum auxiliary loop comparison frequency		–	10	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dual synthesizer reference dividers input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference division ratio		8	–	2047	
R_{ar}	auxiliary reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 17, 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	V_{cp} = ½V_{CC}	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	V_{CC} – 0.4	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3V_{DD}	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	µA
C_I	input capacitance	indicative, not tested	–	2	–	pF
Lock detect output signal; pin 20 open-drain output						
V_{OL}	LOW level output voltage	i_{sink} = 0.4 mA	–	–	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	2000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 µs provided all the following conditions are satisfied:

   a) Principal main divider input frequency $f_{VCO} > \frac{512}{t_W}$

   b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$

   c) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$.

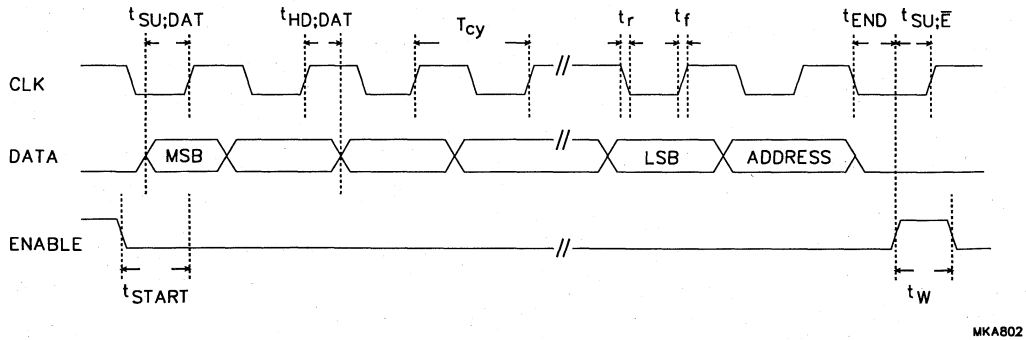


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

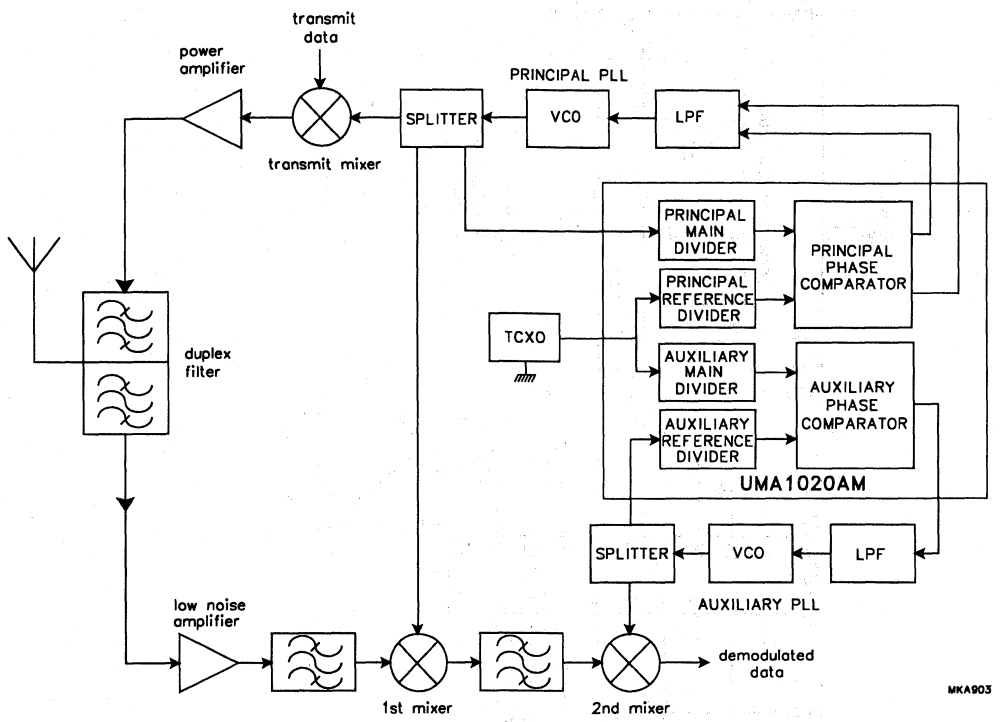


Fig.4 Typical application block diagram.

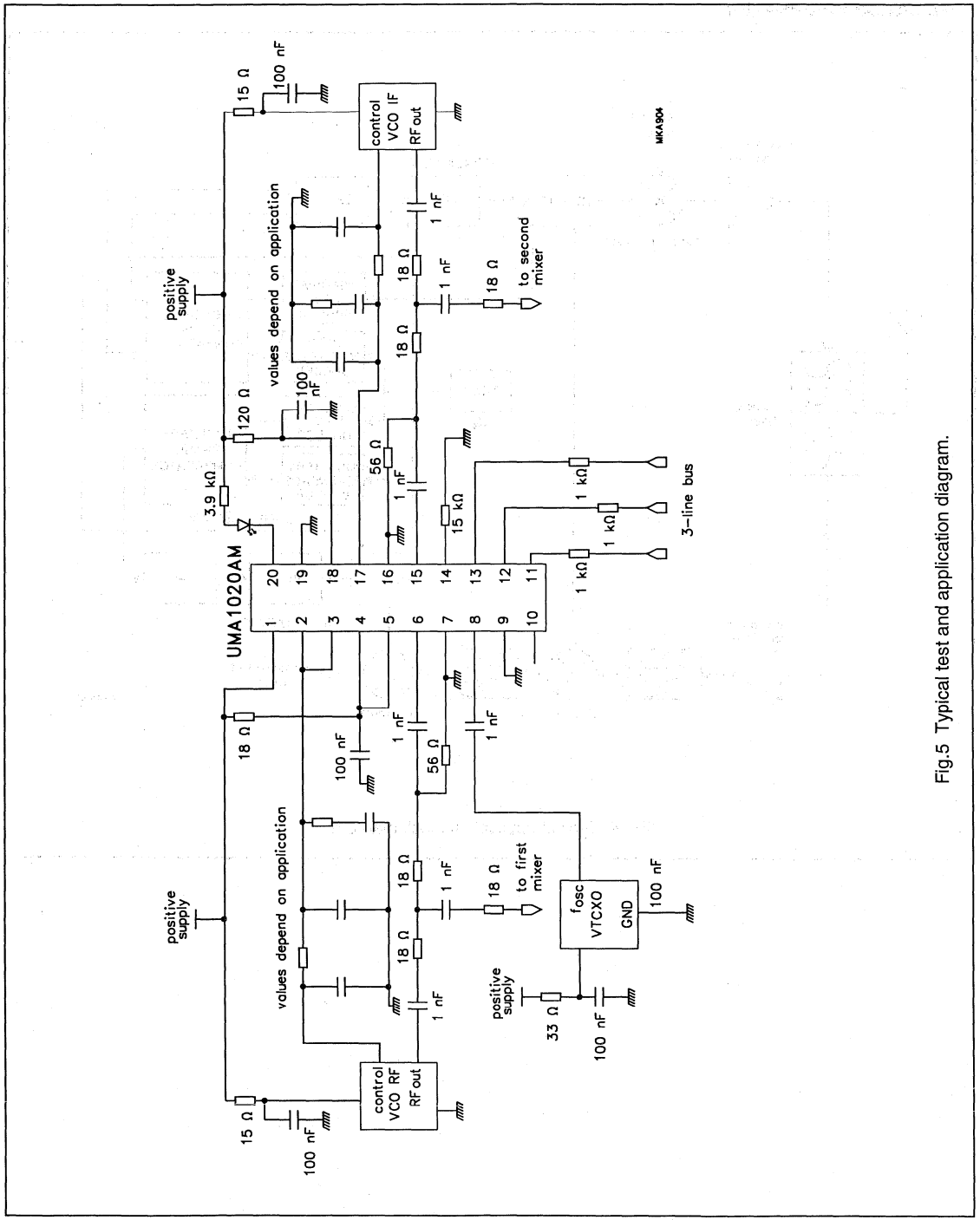


Fig.5 Typical test and application diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Integrated digital-to-analog converter
- Dual power-down modes.

APPLICATIONS

- 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1020M BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at VCO input frequencies up to 2.4 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance. An on-chip 8-bit DAC enables adjustment of an external function, such as the temperature compensation of a crystal oscillator.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	principal synthesizer supply current	auxiliary synthesizer in power-down mode	–	9.4	–	mA
	principal and auxiliary synthesizer supply current	principal and auxiliary synthesizer ON	–	12.1	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	µA
f_{VCO}	principal input frequency		1650	–	2400	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principal phase comparator frequency		–	200	–	kHz
f_{APC}	auxiliary phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

Low-voltage dual frequency synthesizer for radio telephones

UMA1020M

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1020M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

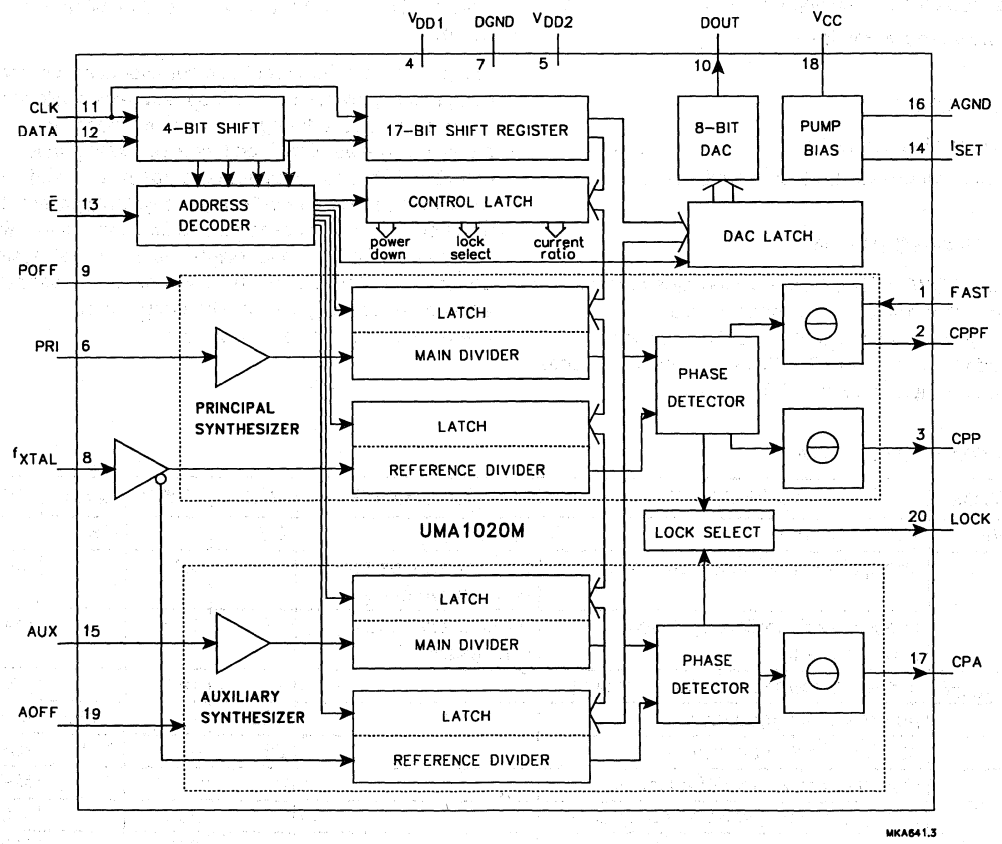


Fig.1 Block diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020M

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principal synthesizer speed-up charge-pump output
CPP	3	principal synthesizer normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
PRI	6	1 GHz principal synthesizer RF divider input
DGND	7	digital ground
f_{XTAL}	8	common reference frequency input from crystal oscillator
POFF	9	principal synthesizer power-down input
DOUT	10	8-bit digital-to-analog output
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump and DAC circuits
AOFF	19	auxiliary synthesizer power-down input
LOCK	20	in-lock detect output (main PLL); test mode output

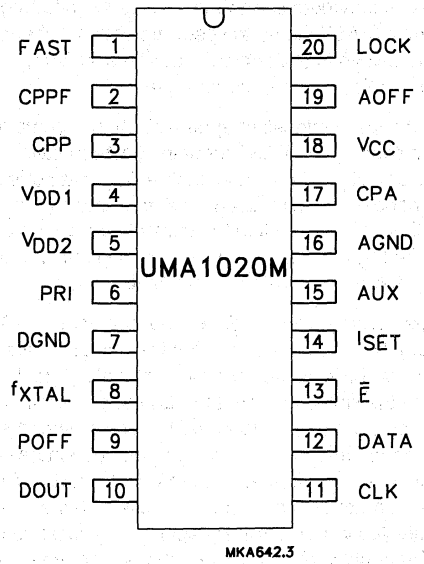


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 60 mV to 180 mV (RMS), and at frequencies up to 2.4 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 μA. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AOFF (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the main reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1020M uses 6 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers.
This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data

LAST IN			PROGRAMMING REGISTER BIT USAGE					FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT					REGISTER BIT ALLOCATION															LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS[2]																	0	0	0	0
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPOFF	sAOFF	X	X	X	X	X	0	0	0	1
PM16	PRINCIPAL MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	PRINCIPAL REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR0	0	1	1	1
X	X	X	X	X	X	X	X	X	DA7	8-BIT DAC FOR EXTERNAL TRIM						DA0	1	0	0	0

Notes

1. FT = first, LT = last; sPOFF = software power-down for principal synthesizer (1 = OFF); sAOFF = software power-down for auxiliary synthesizer (1 = OFF).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Out-of-lock select

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principal phase error
1	1	both auxiliary and principal

Table 4 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	$I_{CPPF} : I_{CPP}$
0	0	$4 \times I_{SET}$	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$4 \times I_{SET}$	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$4 \times I_{SET}$	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps and DAC.

Table 5 Power-down modes

AOFF	POFF	FAST	PRINCIPAL DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF	DAC AND BIAS
1	1	X	OFF	OFF	OFF	OFF	OFF	OFF
1	0	0	ON	OFF	OFF	ON	OFF	ON
1	0	1	ON	OFF	OFF	ON	ON	ON
0	1	X	OFF	ON	ON	OFF	OFF	ON
0	0	0	ON	ON	ON	ON	OFF	ON
0	0	1	ON	ON	ON	ON	ON	ON

Digital-to-analog converter

The byte loaded via the bus into the appropriate latch drives a digital-to-analog converter. The internal current is scaled by the external resistance (R_{ext}) at pin I_{SET}, similar to the charge pumps. The nominal full-scale current is $4 \times I_{SET}$. The output current is mirrored to produce a full-scale voltage into a user-defined ground referenced resistance, thereby allowing optimum swing from power supply rails within the 2.7 to 5.5 V limits. The bandgap reference voltage at pin I_{SET} is temperature and supply independent. The DAC signal is monotonic across the full range of digital input codes to enable fine adjustment of other system blocks. The typical settling time for full-scale switching is 400 ns into a 12 kΩ // 20 pF load.

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

Note that in Table 5 POFF and AOFF can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 0.

When either synthesizer is reactivated after power-down the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	V_{DD} = 5.5 V	–	9	11	mA
	auxiliary synthesizer digital supply current	V_{DD} = 5.5 V	–	2.7	4.0	mA
I_{CC}	charge pumps supply current	V_{CC} = 5.5 V; R_{ext} =12 kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	µA
RF principal main divider input; pin 6						
f_{VCO}	VCO input frequency		1650	–	2400	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 1.65 < f_{VCO} < 2.0 GHz	60	–	400	mV
		R_s = 50 Ω; 1.65 < f_{VCO} < 2.4 GHz	60	–	180	mV
Z_I	input impedance (real part)	f_{VCO} = 2 GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131071	
f_{PPCmax}	maximum principal loop comparison frequency		–	2000	–	kHz
f_{PPCmin}	minimum principal loop comparison frequency		–	10	–	kHz
Auxiliary loop main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 2.7 V < V_{DD} < 3.5 V	50	–	500	mV
		R_s = 50 Ω; 3.5 V < V_{DD} < 5.5 V	100	–	500	mV
Z_I	input impedance (real part)	f_{AI} = 100 MHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	
f_{APCmax}	maximum auxiliary loop comparison frequency		–	2000	–	kHz
f_{APCmin}	minimum auxiliary loop comparison frequency		–	10	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dual synthesizer reference dividers input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference division ratio		8	–	2047	
R_{ar}	auxiliary reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 17, 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	V_{cp} = ½V_{CC}	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	V_{CC} – 0.4	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3V_{DD}	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	µA
C_I	input capacitance	indicative, not tested	–	2	–	pF
DAC output signal levels; pin 10, R_{ext} = 12 kΩ						
I_{DAC}	DAC full scale output current		3 × I_{SET}	4 × I_{SET}	5 × I_{SET}	mA
V_{10}	output voltage compliance	all codes	0	–	V_{DD} – 0.4	V
I_{10min}	minimum DAC current	00 code	–	2	5	µA
I_{monot}	worst case monotonicity test: $\Delta I \times 256/400$ µA	note 1	0.1	–	1.9	
Lock detect output signal; pin 20 open-drain output						
V_{OL}	LOW level output voltage	i_{sink} = 0.4 mA	–	–	0.4	V

Note

1. ΔI is the change in DAC output current when making the code transitions: 7FH/80H, 3FH/40H or 1FH/20H.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	2000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 µs provided all the following conditions are satisfied:

   a) Principal main divider input frequency $f_{VCO} > \frac{512}{t_W}$

   b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$

   c) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$.

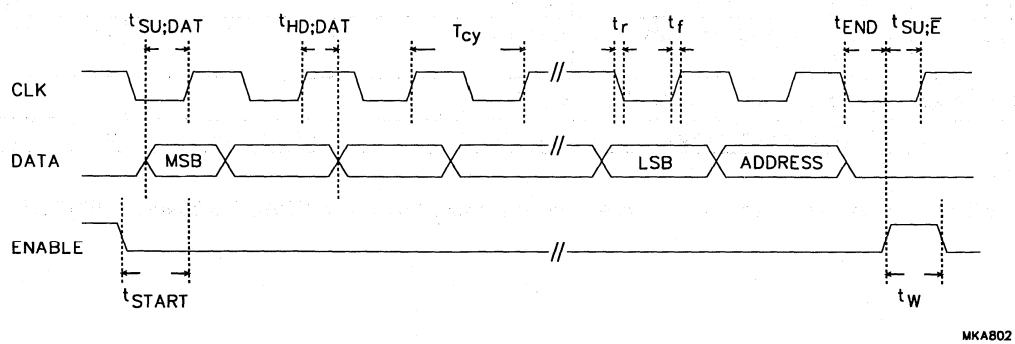


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

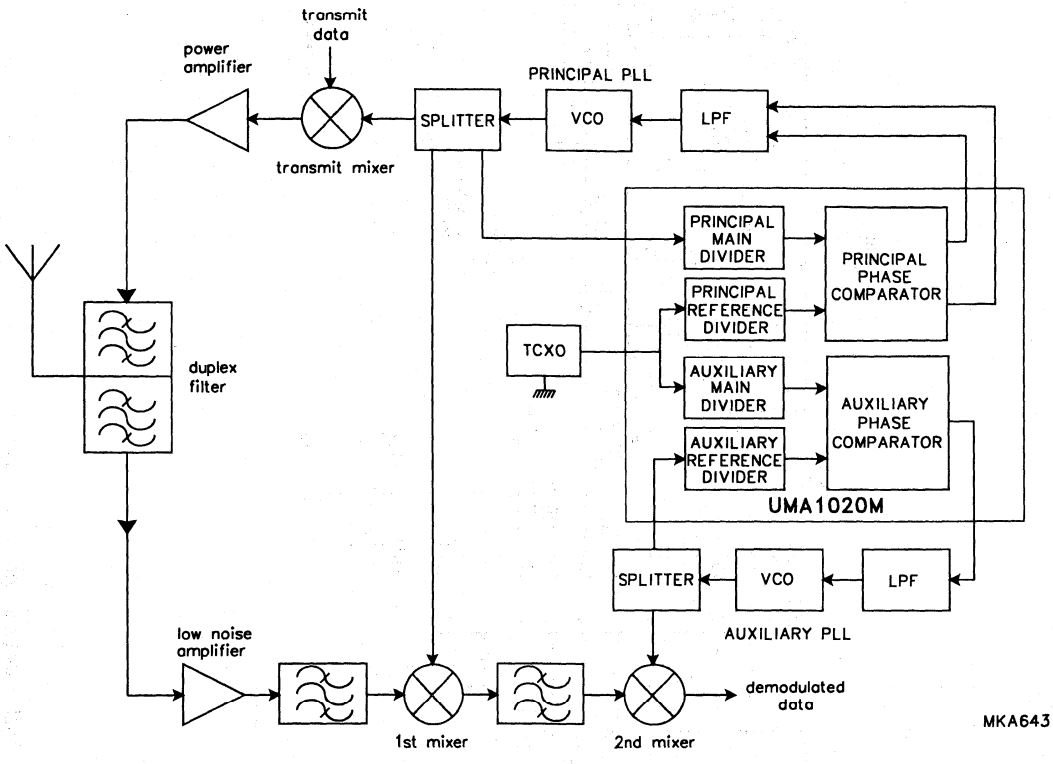


Fig.4 Typical application block diagram.

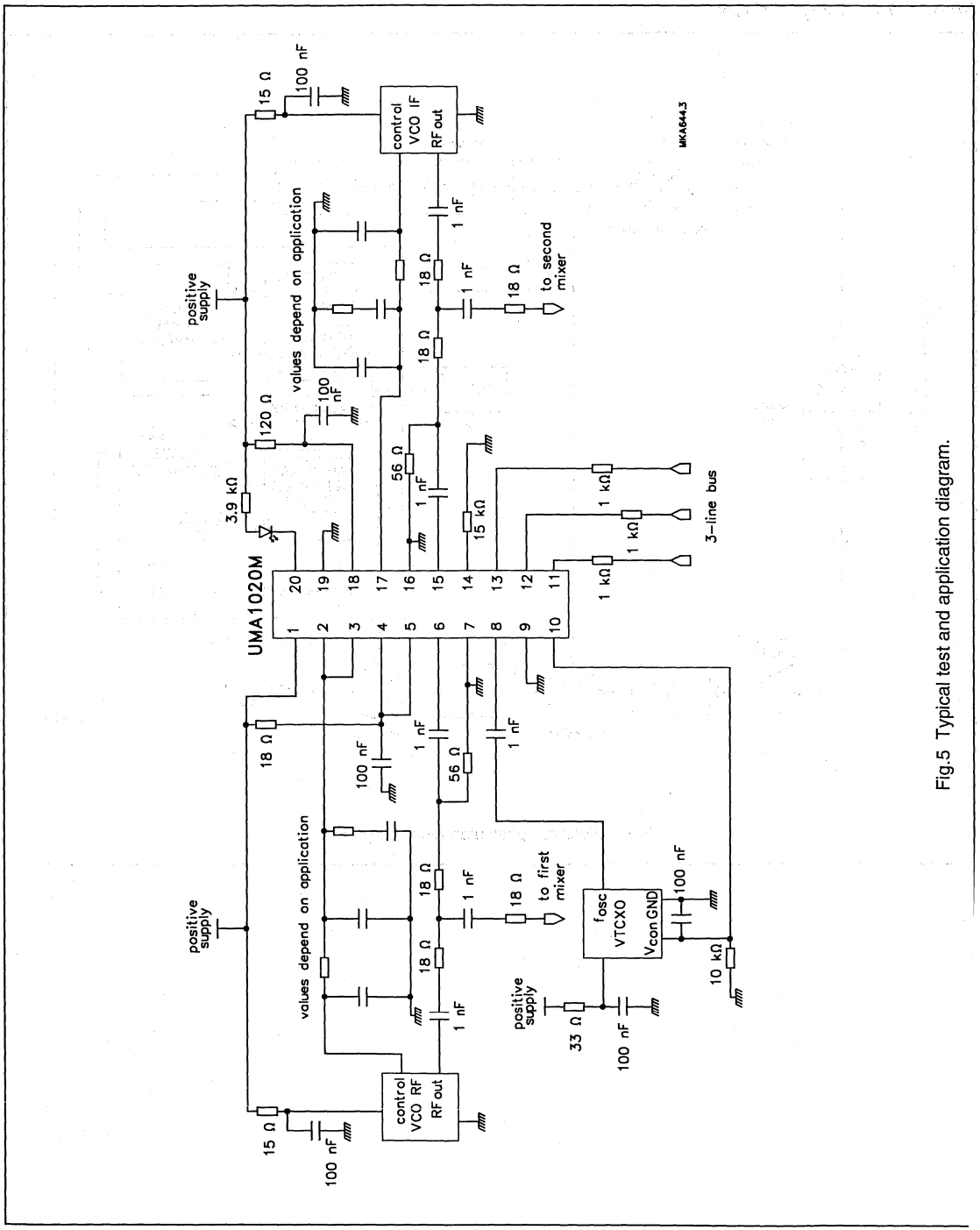


Fig.5 Typical test and application diagram.

Data processor for cellular radio (DPROC)

UMF1000T

FEATURES

- Single chip solution to all the data handling and supervisory functions
- Configuration to both AMPS and TACS
- I²C serial bus control
- All analog interface and filtering functions fully implemented on chip
- Error handling in hardware reduces software requirements
- Robust SAT decoding and transponding circuitry
- Low current consumption
- Small physical size
- Minimum external peripheral components required.

GENERAL DESCRIPTION

The UMF1000T is a low power CMOS LSI device incorporating the data tranceiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage (pin 28)	4.5	5.0	5.5	V
I_{DD}	supply current (pin 28) normal operation with external clock	–	2.5	–	mA
T_{amb}	operating ambient temperature range	–40	–	+85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMF1000T	28	SO28	plastic	SOT136A

Data processor for cellular radio (DPROC)

UMF1000T

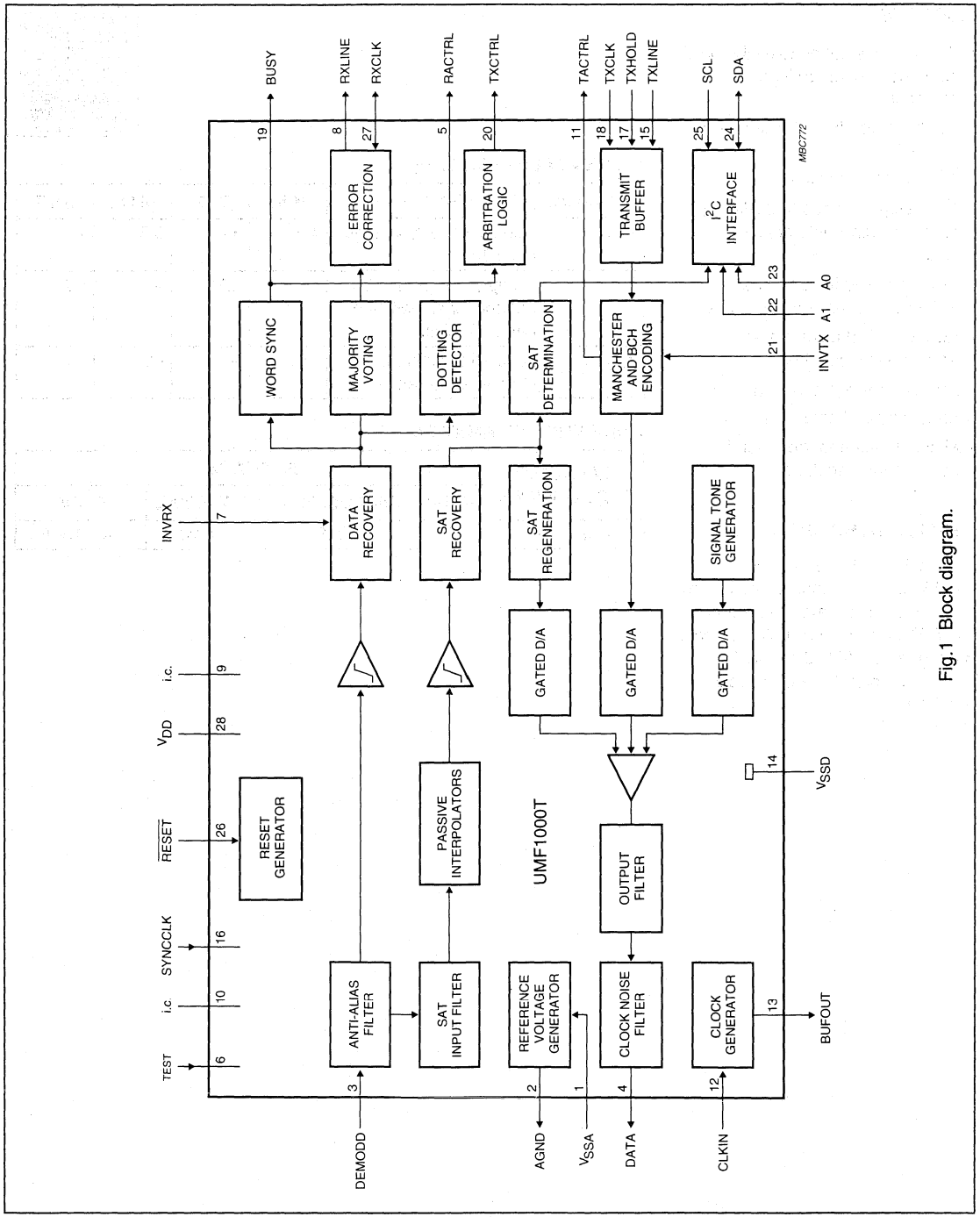


Fig.1 Block diagram.

Data processor for cellular radio (DPROC)

UMF1000T

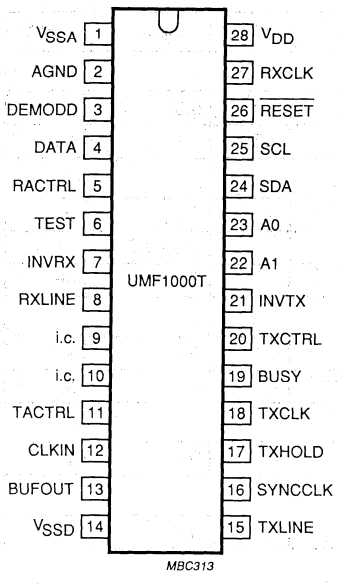


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA}	1	analog negative supply (0 V)
AGND	2	$(V_{DD} - V_{SSA})/2$ analog reference ground
DEMODD	3	received data signal input
DATA	4	transmitted data signal output
RACTRL	5	received audio control output
TEST	6	SCAN control input – used for power-on reset
INVRX	7	inverts sense of received data stream
RXLINE	8	received data signal output
i.c	9	internally connected; must be left open-circuit
i.c	10	internally connected; must be left open-circuit
TACTRL	11	transmitter audio control output
CLKIN	12	1.2 MHz external master clock input
BUFOUT	13	buffered output of internal clock oscillator
V_{SSD}	14	digital ground
TXLINE	15	transmitted data signal
SYNCCLK	16	SCAN CLOCK control input – used for power-on reset
TXHOLD	17	holds off transmission of data
TXCLK	18	transmitted data clock input
BUSY	19	reverse control channel status output
TXCTRL	20	transmitter control output
INVTX	21	inverts sense of transmitted data stream
A1	22	address input 1 – used for power-on reset (I^2C-bus)
A0	23	address input 0 (I^2C-bus)
SDA	24	serial data input/output (I^2C-bus)
SCL	25	serial clock input (I^2C-bus)
$\overline{RESET}$	26	master reset input
RXCLK	27	received data clock input
V_{DD}	28	positive supply voltage (+5 V)

CHARACTERISTICS

V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	positive supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current	normal operation; note 1	–	2.5	–	mA
Digital inputs (note 2)						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}+0.3	V
C_I	input capacitance		–	–	6	pF
Digital outputs (note 2)						
V_{OL}	LOW level output voltage	I_{sink} = 1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = 1 mA	V_{DD}–0.4	–	–	V
Open-drain outputs (note 3)						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	–	0.4	V
Open-drain SDA						
V_{OL}	LOW level output voltage	I_{sink} = 3 mA	–	–	0.4	V

Notes to the characteristics

1. 1.2 MHz clock on CLKIN, SYNCCLK HIGH, outputs unloaded analog part operating.
2. All digital inputs and outputs of DPROC are compatible with standard CMOS devices and the following general characteristics apply.
3. Open-drain outputs have no internal pull-up resistors.

FUNCTIONAL DESCRIPTION

General

The UMF1000T (DPROC) is a single-chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.

These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction, decoding and encoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation.

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels. Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticeable by the user. A data rate of 10 kbits/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig.3.

A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz), is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analogous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the 'loop'. At the base station this signal is used to ascertain the overall quality of the communication link.

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

The key requirements of a hand-held portable cellular set are:

- Small physical size
- Minimum number of interconnections (serial bus)
- Low power consumption
- Low cost.

The DPROC is a member of our Cellular Radio chip set, based on the I²C-bus, which meets these requirements. A cellular radio system schematic using the chip set is shown in Fig.4.

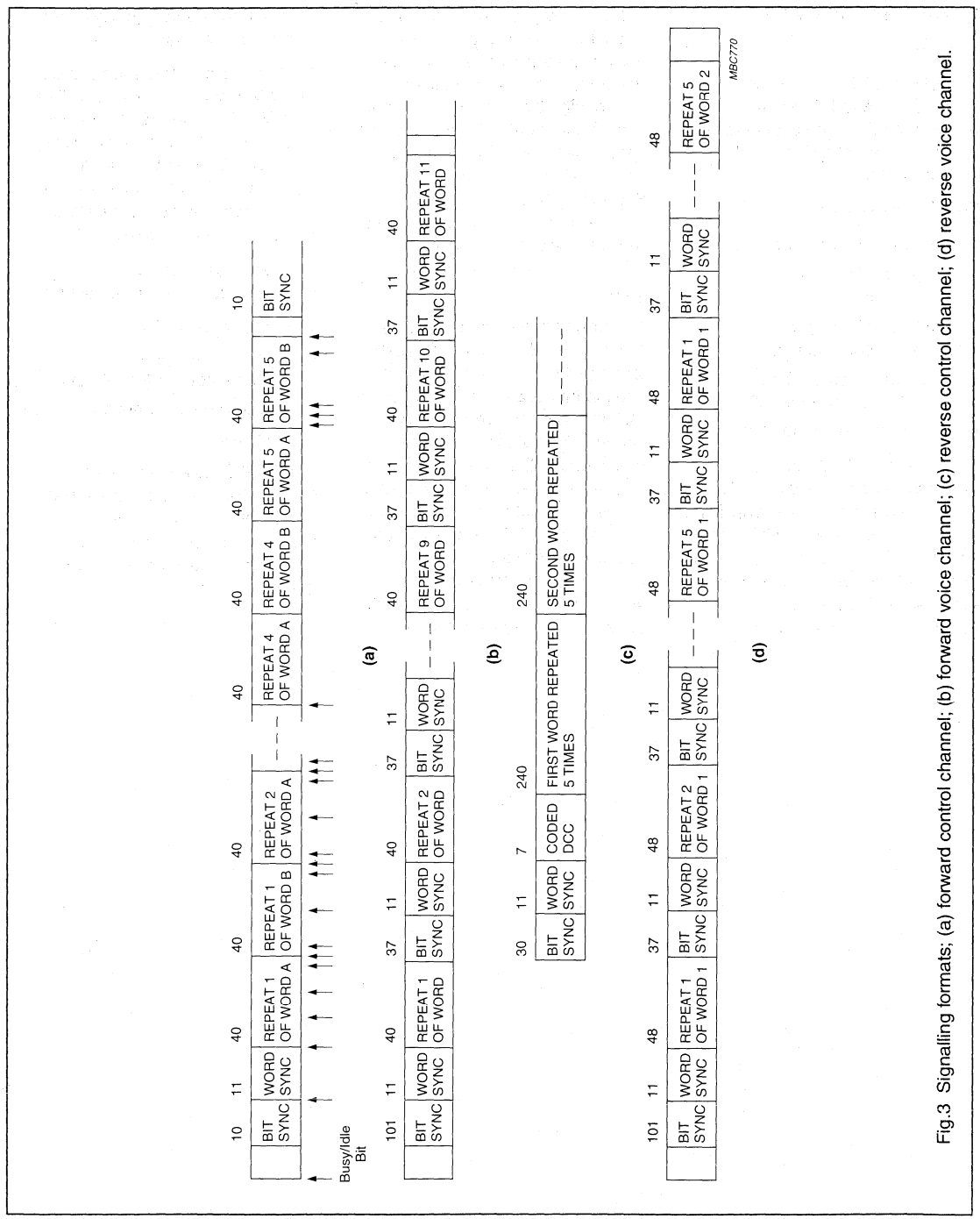


Fig.3 Signalling formats; (a) forward control channel; (b) forward voice channel; (c) reverse control channel; (d) reverse voice channel.

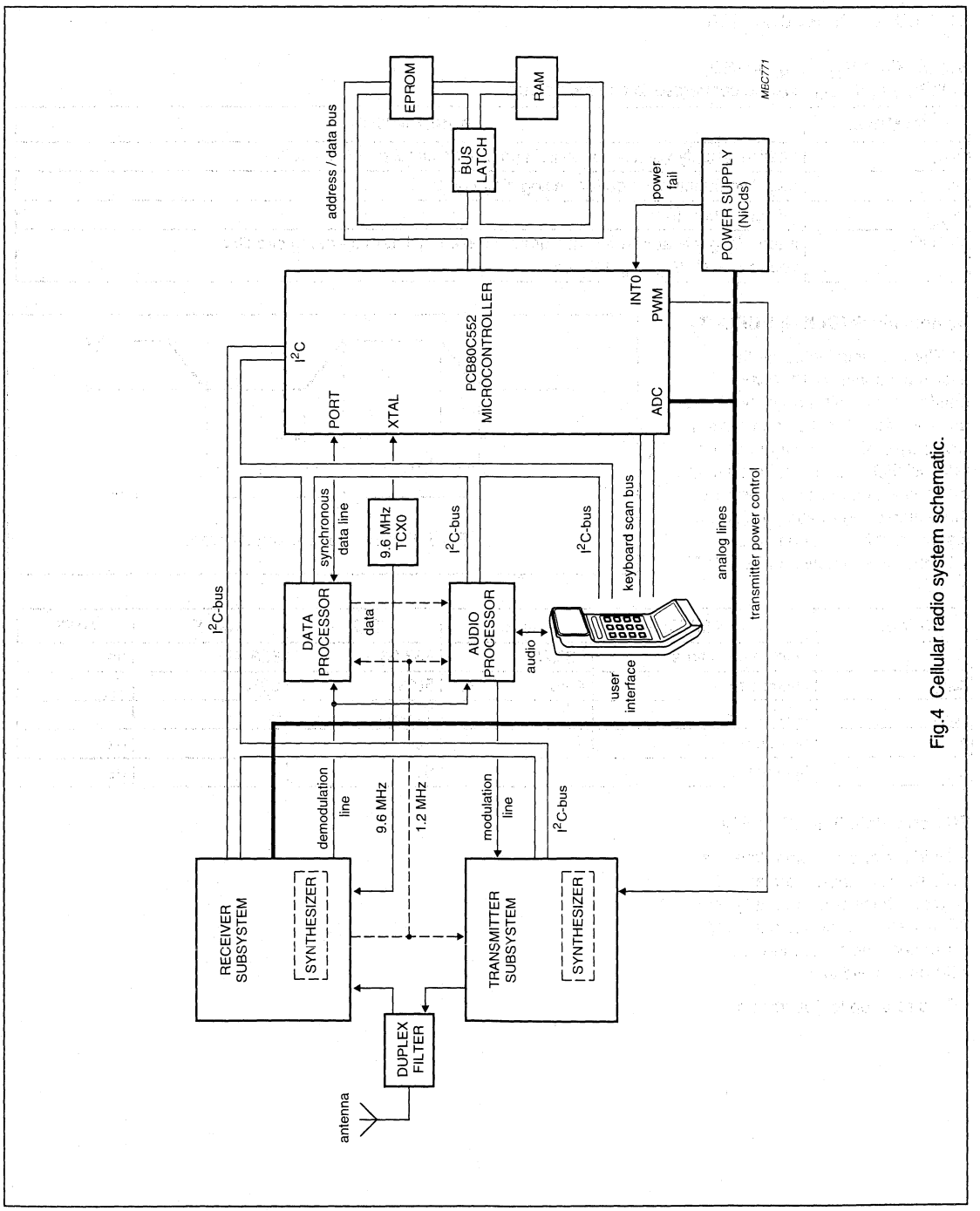


Fig.4 Cellular radio system schematic.

EXTERNAL PIN DESCRIPTION

Supply (V_{DD}; V_{SSA}; V_{SSD}; AGND)

Both V_{SSA} and V_{SSD} must be connected to common ground.

SYMBOL	DESCRIPTION
V_{DD}	positive supply voltage for digital and analog circuitry (±5 V +10%)
V_{SSA}	negative supply voltage for analog circuitry (0 V)
V_{SSD}	digital ground (0 V)
AGND	internally generated reference ground based by internal analog circuitry; voltage level $(V_{DD}-V_{SSA})/2$ ±2%

System clock (CLKIN; BUFOUT)

CLKIN is a digital input for the externally generated 1.2 MHz master clock. This signal should be accurate to 100 x 10^{-6} and have a worst case of 60 : 40 mark-space ratio. BUFOUT is the buffered output of the clock oscillator and provides the option of generating the clock signal on chip by connecting a 1.2 MHz crystal between BUFOUT and CLKIN.

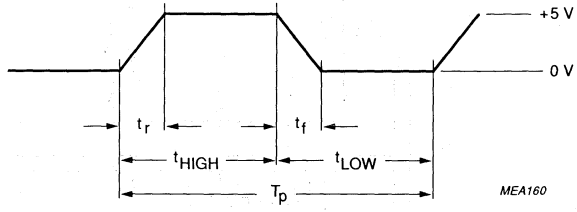


Fig.5 System clock timing diagram.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
T_p	clock period time	833.25	833.33	833.42	ns
t_{HIGH}	HIGH time	40%	50%	60%	T_p
t_{LOW}	LOW time	–	T_p-t_{HIGH}	–	
t_r	rise time	–	50	–	ns
t_f	fall time	–	50	–	ns

I²C serial data link (SDA; SCL)

SDA is the bi-directional data line; SCL the clock input from an I²C master. These constitute a typical I²C link and conform to standard characteristics as defined in the I²C-bus specification.

- Data rate: up to 100 kbits/s

Slave Address Select (A0; A1)

Selection of the device slave address is achieved by connecting A0 to either V_{SSD} or V_{DD} and connecting A1 to either pin 16 and pin 6 or to V_{DD}. The slave address is defined in accordance with the I²C specifications as shown in Fig.6.

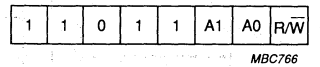


Fig.6 Device slave address.

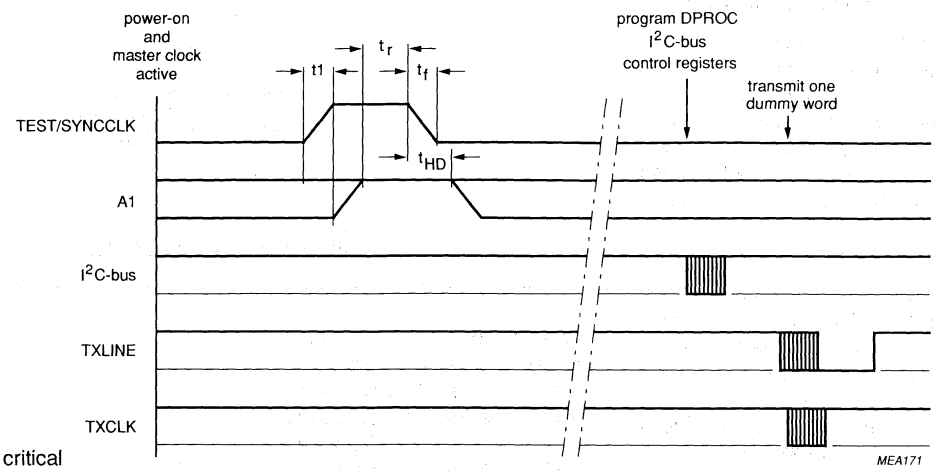
Power-up state

DPROC will not respond reliably to any inputs (including $\overline{\text{RESET}}$) until 100 µs after the power supply has settled within the specified tolerance. The analog sections of the device will have stabilized within 5 ms. No power-on reset is provided, therefore before the device can enter normal operation TEST and SYNCCLK must be pulsed HIGH. The reset pulse on these pins must have a minimum period of 250 µs and the fall time of the negative going edge must be faster than 1 µs. Pin A1 must remain HIGH during this reset period therefore if the A1 bit of the I²C address is required to be logic 0. A1 may be connected to TEST and SYNCCLK. If it is required to be at logic 1 then A1 may be permanently connected to V_{DD}. If it is required that A0 = logic 1, then a normal master reset (pin 26) sequence must follow the power-on reset sequence to get the internal registers in the defined state.

After the power-on reset a dummy transmission should be made to initiate internal DPROC counters. This transmission should be made with arbitration (ABREN) disabled and the RF transmitter stage switched OFF. Figure 7 shows the power-on reset sequence.

Master reset ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ is an asynchronous active LOW master reset input, with a minimum active pulse width of 2 µs which may be used to reset certain logic within DPROC to a predefined state as illustrated in Tables 1 and 2. Alternatively, DPROC may be set into a known initial state be setting the I²C control register as required. The internal reset sequence after a negative pulse on $\overline{\text{RESET}}$ takes 250 µs.



Where:

t1 = time not critical

t_r = reset time = 250 µs max.

t_f = pulse fall time = 1 µs max.

t_{HD} = A1 hold time = 0 µs min.

Note

The RF transmitter is OFF during reset sequence.

Fig.7 Power-on reset programming sequence.

Table 1 Predefined state of the digital output pins

OUTPUT	STATE
RXLINE	HIGH
TXCTRL	HIGH
TACTRL	HIGH
RACTRL	HIGH
BUSY	HIGH

Table 2 Predefined state of I²C registers

REGISTER	BIT							
	7	6	5	4	3	2	1	0
control	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
SATD	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
TST	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

Data Transfer Link (RXLINE; TXLINE; TXHOLD; TXCLK and RXCLK)

RXLINE, TXLINE, TXCLK and RXCLK provide a dedicated serial data link for the transfer of system data messages between DPROC and the system controller at variable rates of up to 200 kbits/s.
TXHOLD allows the system controller to preload the DPROC transmit register with one word without the data being transmitted. DPROC then starts transmitting the instant TXHOLD is driven LOW.

- RXCLK: clock input from system controller
- RXLINE: data output from DPROC to system controller
- TXCLK: clock input from system controller
- TXLINE: open drain data bi-directional line to the system controller
- TXHOLD: (HIGH) holds off transmission of data
- Data rate: up to 200 kbits/s

Note

A minimum mean data transfer rate for the received data of 2.1 kbits/s (AMPS) and 1.7 kbits/s (TACS) is required to ensure contiguity of message words.

The format for received and transmitted data words is shown in Fig.15(a) and Fig.15(b) respectively. The receive and transmit data timing is illustrated in Fig.16(a) and Fig.16(b) respectively.

Transmitter Control (TXCTRL)

TXCTRL is an open-drain output used to disable the transmitter during a Reverse Control Channel access failure.

- output level HIGH: RF enable
- output level LOW: RF disable

Transmitter Audio Enable (TACTRL)

TACTRL is an open-drain digital output signal used to blank the audio path and enable the data path to the modulator during data bursts on the Reverse Voice Channel.

- output level HIGH: audio enabled
- output level LOW: audio muted

Receiver Audio Enable (RACTRL)

RACTRL is an open-drain digital output used to blank the audio path to the earpiece when a sequence of dotting and word sync is detected.

RACTRL and TACTRL functions can be combined using one line.

- output level HIGH: audio enabled
- output level LOW: audio muted

Reverse Control Channel Status (BUSY)

BUSY is a digital output giving the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits and has the following logic levels:

- output level HIGH: channel busy
- output level LOW: channel idle

On a voice channel BUSY indicates channel idle.

Invert Receive Data (INVRX)

Enables an additional inverter in the receive data path. This allows RF demodulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC depends on the receiver local oscillator.

- input HIGH: data inverted
- input LOW: data normal

Invert Transmit Data (INVTX)

Enables an additional inverter in the transmit data path. This allows RF modulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator.

- input HIGH: data inverted
- input LOW: data normal

Transmitted Data Output (DATA)

Data is an analog output which provides Manchester encoded and filtered data signal SAT and signalling tone. This signal should normally be AC coupled into the Audio/Data summer.

- DC level: analog ground (AGND)
- signal level: 2 V (p-p) for signalling tone; signal level with filtered data signal
- signal tolerance: 2% + supply voltage variation (ΔV_{DD})
- minimum load capacitance: 10 kΩ
- maximum load capacitance: 2 nF
- maximum output impedance: 50 Ω

Received Data Input (DEMODD)

Demodd inputs analog data and SAT signals from the RF demodulator. This pin should normally be AC coupled.

- DC level: analog ground (AGND)
- maximum data level: 1 V (p-p)
- nominal data level: 250 mV (p-p)
- minimum data level: 200 mV (p-p)
- minimum SAT level: 50 mV (p-p)
- input impedance: min. 1 MΩ

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig.12.

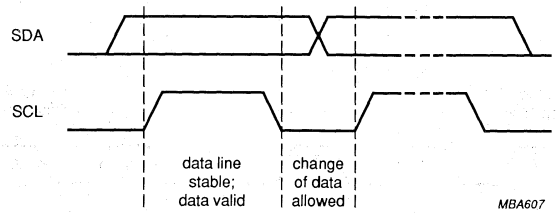


Fig.8 Bit transfer.

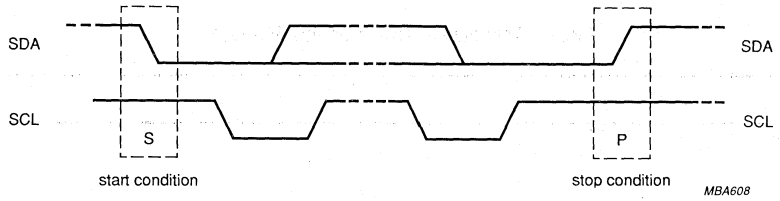


Fig.9 Definition of start and stop conditions.

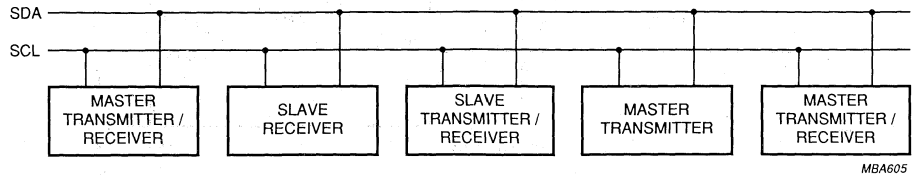


Fig.10 System configuration.

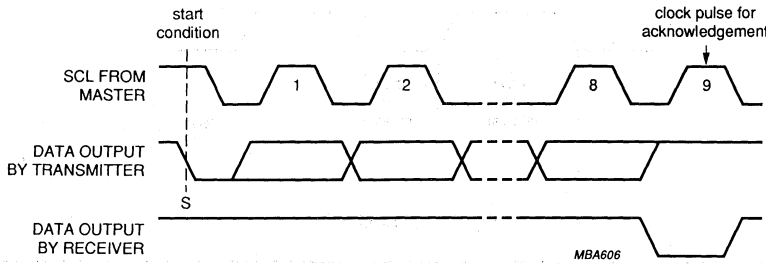


Fig.11 Acknowledgement on the I²C-bus.

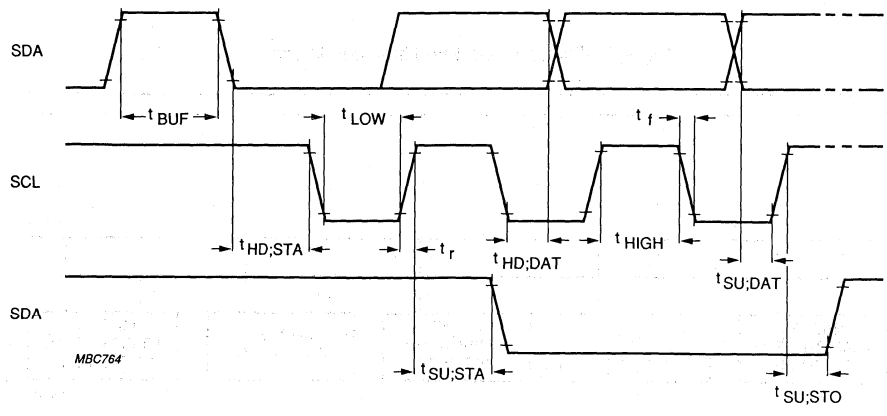
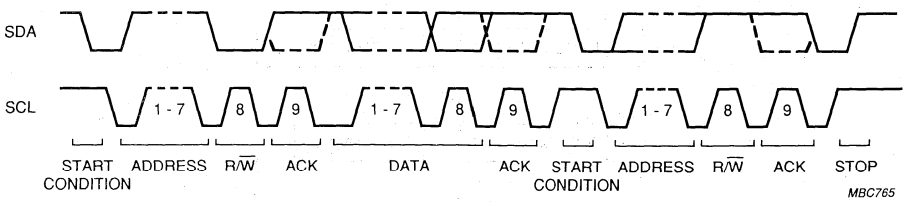


Fig.12 Timing.

Where:

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS}.

SYMBOL	TIMING	DESCRIPTION
t_{BUF}	$t \geq t_{LOW(min)}$	the minimum time the bus must be free before a new transmission can start
$t_{HD;\ STA}$	$t \geq t_{HIGH(min)}$	start condition hold time
$t_{LOW(min)}$	4.7 µs	clock LOW period
$t_{HIGH(min)}$	4 µs	clock HIGH period
$t_{SU;\ STA}$	$t \geq t_{LOW(min)}$	start condition set-up time, only valid for repeated start code
$t_{HD;\ DAT}$	$t \geq 0$ µs	data hold time
$t_{SU;\ DAT}$	$t \geq 250$ ns	data set-up time
t_r	$t \leq 1$ µs	rise time of both the SDA and SCL line
t_f	$t \leq 300$ ns	fall time of both the SDA and SCL line
$t_{SU;\ STO}$	$t \geq t_{LOW(min)}$	stop condition set-up time



Where:

Clock $t_{LOW(min)}$: 4.7 µs

Clock $t_{HIGH(min)}$: 4 µs

The dashed line is the acknowledgement of the receiver

Maximum number of bytes: unrestricted

Premature termination of transfer: allowed by generation of STOP condition

Acknowledge clock bit: must be provided by the master.

Fig.13 Complete data transfer.

I²C REGISTERS

General

The I²C register block resides internally within the I²C interface block and contains various items of status and control information which are transferred to and from DPROC via the I²C-bus. The block is organized into four 8-bit registers:

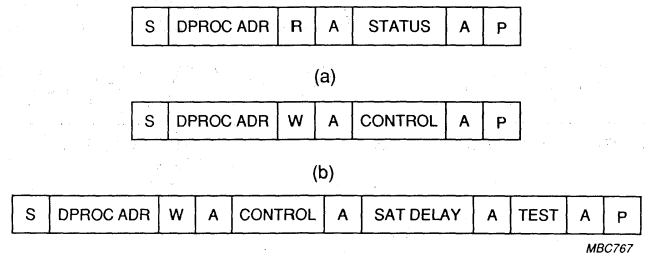
- Status Register: contain read only items
- Control Register: contain write only items
- SAT Programmable Phase Shift Register: contain write only items
- TEST Register

Note

In normal operation the SAT delay register and the TEST register require programming only after a device reset.

Table 3 Register map

REGISTER	BIT							
	7	6	5	4	3	2	1	0
status	–	–	WYNSC	BUSY	TXABRT	TXIP	MSCC1	MSCC0
control	–	SERV	STS	TXRST	ABREN	FVC	STEN	SATEN
SATD	<----------SAT delay data---------->							



Where:

S: START condition

W: read/write bit (logic 0 = write)

R: read/write bit (logic 1 = read)

A: acknowledge bit

P: STOP condition

DPROC ADR: slave address of DPROC

TEST: must be programmed to logic 0 for normal operation.

Fig.14 I²C data format; (a) read from DPROC status register; (b) write to DPROC control register; (c) write to all DPROC registers.

Status Register

This is read only register containing DPROC status information.

MEASURED SAT COLOUR CODE (MSCC1; MSCC0)

MSCC1 and MSCC0 provide information about the current measured SAT colour code in accordance with Table 4.

TRANSMISSION IN PROGRESS (TXIP)

TXIP indicates whether DPROC is currently accessing the Reverse Control or Voice Channels.

- logic 1: data transmission in progress
- logic 0: transmission not in progress

TRANSMISSION ABORT STATUS (TXABRT)

TXABRT indicates that a Reverse Control Channel Access Attempt has been aborted by DPROC without successful message transmission.

- logic 1: transmission attempt aborted
- logic 0: no access collision detected

Table 4 Measured SAT Colour Code

MSCC1	MSCC0	SAT frequency (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

REVERSE CONTROL CHANNEL STATUS (BUSY)

BUSY gives the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits on the Forward Control Channel.

- logic 1: channel busy
- logic 0: channel idle

On a voice channel the BUSY bit defaults to the set state.

Note

This signal is also routed to the BUSY output pin.

WORD SYNCHRONIZATION INDICATOR (WSYNC)

WSYNC indicates whether DPROC has acquired frame synchronization according to the Forward Control Channel format.

- logic 1: frame synchronization acquired
- logic 0: no frame synchronization

Control Register

This is a write only register containing DPROC control information.

SAT Path Enable (SATEN)

SATEN enables the SAT transponded signal to be output on external pin DATA.

- logic 1: SAT tone enabled
- logic 0: SAT tone inhibited

Signalling Tone (ST) Path Enable (STEN)

STEN enables the Signalling Tone to be output on external pin DATA.

- logic 1: ST enabled
- logic 0: ST inhibited

Channel Format Select (FVC)

FVC selects the required channel format.

- logic 1: voice channel format
- logic 0: control channel format

Transmission Abort Permission (ABREN)

ABREN indicates whether DPROC has permission to abort data transmission and disable RF on the Reverse Control Channel following the detection of a channel access attempt collision.

- logic 1: RF disable allowed
- logic 0: RF disable inhibited

Message Transmission Abort (TXRST)

TXRST terminates a message being transmitted on the reverse channel. It is a monostable signal which when activated causes a reset of the message transmission circuitry and causes TXABRT and TXIP I^2C signals to be reset.

This signal does not clear the DPROC transmit register; therefore if a word has been loaded into DPROC after a TXABRT has occured the control line TXHOLD should be held LOW to allow the word to be cleared from the DPROC input register.

- logic 1: reset active
- logic 0: reset inactive

System Type Select (STS)

STS selects required system format.

- logic 1: AMPS
- logic 0: TACS

Note

Toggling this signal also resets the receive logic in DPROC.

Serving System Select (SERV)

SERV selects which of the serving system data streams (A or B) is accepted.

- logic 1: system A selected
- logic 0: system B selected

SAT Programmable Delay Register (SATD)

SATD programs the value of phase shift which is applied to the SAT tones in the SAT Regeneration Block. This value will be determined and programmed into the System Controller during manufacture. The recovered SAT is delayed in time by approximately 0.8 µs x value in the register which corresponds to approximately 1.8 degrees x value in the register. The total phase shift is limited to 360 degrees.

The ability to adjust SAT phase angle is not necessary in current AMPS and TACS systems. Therefore this register should normally be in AMPS and TACS, this function is not necessary and should programmed to zero.

DIGITAL CIRCUIT BLOCKS

General

The majority of the digital circuitry within the DPROC device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig.1.

Data Recovery

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Strobed Comparator Block, on which it performs the following functions:

- clock recovery
- Manchester decoding
- data regeneration

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase-locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable 'bandwidth' to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1.2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output.

The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a 1 otherwise it is latched as a 0.

SAT Processing

The Supervisory Audio Tone processing consists of the following functions:

- SAT recovery
- SAT determination
- SAT regeneration

SAT RECOVERY

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.
The recovery is performed using a digital phase-locked-loop.

SAT DETERMINATION

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the I²C status registers MSCC0 and MSCC1 as shown in Table 5.

SAT REGENERATION

The SAT Regeneration Block generates a digital SAT stream from the recovered SAT stream for transponding back to the base station. The AMPS and TACS specifications require the SAT to be transponded with a maximum phase shift of 20 degrees between the point the modulated RF signal enters the mobile from the base station, and the point the modulated RF leaves the mobile. A variable phase compensation circuit is provided in DPROC to shift the recovered SAT through 0 to 360 degrees before being passed to the output summing network. The degree of phase shift is determined during manufacture of the set and the required additional phase shift is stored in non-volatile RAM and programmed via I²C at each power-on cycle. The phase correction is performed by a counter delay method using signals which are phase locked to the recovered SAT.

Dotting Detector

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of 32 bits of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL, after a Word Synchronization Block has been received, for the duration of the burst.

Table 5 Status registers MSCC0, MSCC1; decoded SAT frequencies

REGISTER		SAT frequency band (Hz ±2 Hz)	decoded SAT (Hz)
MSCC0	MSCC1		
1	1	max. 5956	not valid
0	0	5956 to 5986	5970
0	1	5986 to 6014	6000
1	0	6014 to 6046	6030
1	1	min. 6046	not valid

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

- Frame Synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11-bit Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC has achieved frame synchronization. In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode. On the Forward Voice Channel detection of the synchronization word indicates that the following 40 bits are valid data. Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

Majority Voting Block

The Majority Voting Block performs the following functions:

- identifying position and validity of frames in the received data stream
- extracting five repeats of each word from a valid frame
- performing a bit-wise majority decision on the five repeats of the data word.

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searched for and extracted by DPROC. On the forward Voice Channel DPROC will extract the first five words that occur for which a correct synchronization word is found. These words can occur in any position in the frame. A serial majority vote is performed as the fifth word is being extracted.

Error Correction Block

The Error Correction Block performs the following functions:

- extraction of a valid message from the Majority-Voted Word
- computation of the S1 and S3 syndromes
- correction of up to one error in the word
- communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$1 + X + X^6$ and $1 + X + X^2 + X^4 + X^6$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC only corrects up to one error although the code used has a Hamming distance of five. The occurence of two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

Received Data Serial Link

The Received Data Serial Link transfers data and control information from DPROC to the System Controller. The data is transferred on RXLINE under control of a clock signal RXCLK, generated by the System Controller. The system controller is informed of the arrival of a decoded data word in the DPROC output register by RXLINE being driven LOW. If the system controller chooses to ignore the received data or only partially clock the data out, the DPROC will reset the receive buffer for the next word after the period RWIN (see Fig.16).

Data Format

Each Received Data word consists of 4 bytes. The word format is shown in Fig.15(a). The sense and function of the fields is shown in Table 6.

Link Protocol

The Received Data protocol is described by the timing diagram Fig.16(a) and has the following parameters:

- maximum receive window (RWIN)
  - Control Channel (TACS) = 47 ms
  - Control Channel (AMPS) = 37 ms
- minimum clock period ($t_{CLK(min)}$) = 2 µs
- minimum clock hold-off (t_{WAIT}) = 100 µs

Transmit Data Serial Interface

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

Data Format

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig.15(b). The sense and function of the fields is shown in Table 7.

Link Protocol

Messages are normally up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. However, DPROC will transmit messages of any word length. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC to control the transfer of data words. DPROC has an on-chip buffer which can hold one complete word of a message. While new words are being loaded into DPROC, within the time period Buffer clear to end of TWIN, DPROC will maintain uninterrupted data transmission. The System Controller can abort the transmission of a message at any point activating the I²C signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 3). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig.16(b) and has the following parameters:

- maximum transmit window (TWIN)
  - voice channel (TACS) = 60 ms
  - voice channel (AMPS) = 48 ms
  - control channel (TACS) = 29 ms
  - control channel (AMPS) = 23 ms
- minimum clock period ($t_{CLK(min)}$) = 2 µs

Table 6 Received Data word

BIT	TITLE	SENSE	FUNCTION
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	LOW	if detected as HIGH indicates that a transmission error has occured on the microprocessor to DPROC serial link
0	stop	HIGH	identifies end of the word

Table 7 Transmit data word

BIT	TITLE	SENSE	FUNCTION
39	start	LOW	identifies start of word
38, 37	DCC	binary data	digital colour code
36 to 1	transmit data	binary data	transmit data word
0	stop	HIGH	identifies end of the word

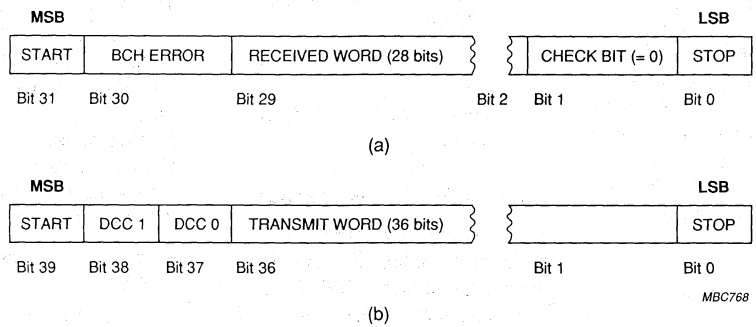
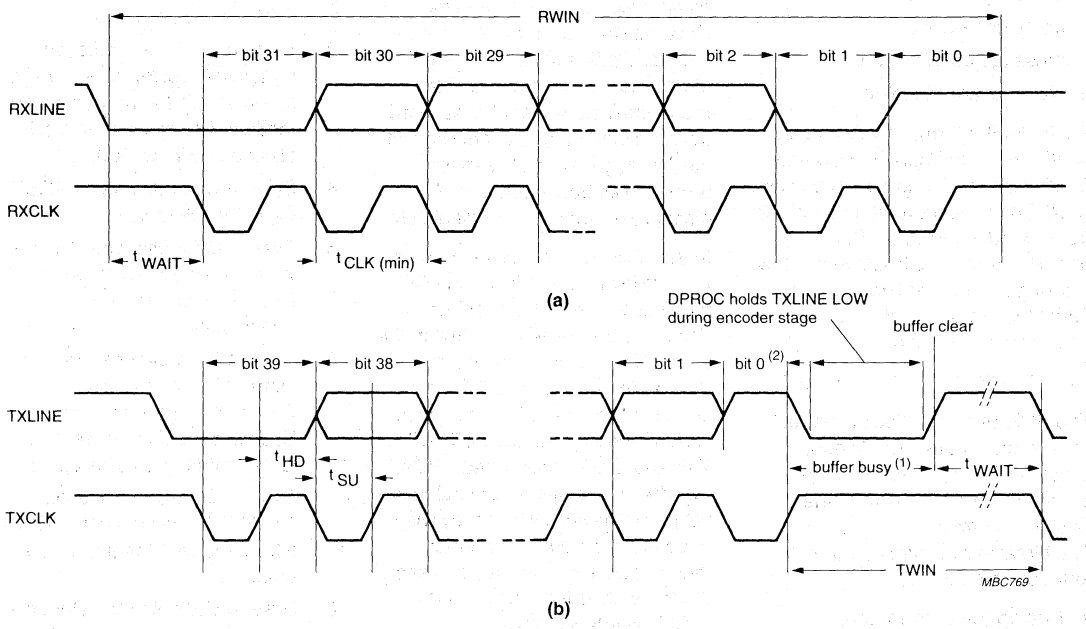


Fig.15 Data word formats; (a) received data word; (b) transmit data word.



Where:

t_{HD} = 100 ns minimum

t_{SU} = 0 ns minimum

t_{WAIT} = 0 ns minimum

(1) The buffer busy time depends on whether the first or subsequent words are being loaded.

(2) The system controller should monitor the TXLINE during bit 0, if the status of TXLINE does not change from a HIGH to a LOW on the rising edge of TXCLK, then a framing error has occured. This can be caused by glitches on the clock line or if an arbitration error occured while the DPROC transmit register was being loaded. The system controller should recover the situation by holding TXLINE HIGH and supplying clocks on TXCLK until TXLINE goes LOW. Then the situation should be treated as a normal channel arbitration failure as described in **Reverse Control Channel Access Arbitration** - Abort Procedure.

Fig.16 Data timing diagrams; (a) DPROC to microcontroller link; receive data timing; (b) microcontroller to DPROC link; transmit data timing.

BCH and Manchester Encoding Block

The functions performed by this circuit block include:

- reception of data from the System Controller
- parity generation
- message construction
- Manchester encoding

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48-bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic equation:

$$1 + X^3 + X^4 + X^5 + X^8 + X^{10} + X^{12}$$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.
The streams are formed out of the four possible field types:

- Dotting (data inversions)
- 11-bit Synchronization Word
- Digital Colour Code
- 48-bit code word

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 8.

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

Reverse Control Channel Access Arbitration

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time. This function is performed by DPROC monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ANDed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing I²C register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

INITIAL STATE

- transmitter power off via I²C
- DPROC transmit circuitry in power-up state
- TXCTRL line HIGH

ACCESS ATTEMPT PROCEDURE

1. System Controller decides to send message (see **Note to the Access Attempt Procedure**).
2. System Controller drives TXCTRL LOW directly.
3. System Controller switches transmitter power-on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).
4. System Controller sets TXRST via I²C to DPROC.
5. System Controller sets ABREN via I²C (if required) allowing DPROC to control the transmitter.
6. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.
7. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.
8. System Controller transfers the first word of the message to DPROC via serial link (see **Note to the Access Attempt Procedure**).
9. DPROC sets I²C signal TXIP and starts sending message while monitoring Busy/Idle status.
10. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.
11. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.
12. System controller loads the subsequent words of the message into DPROC when the buffer becomes clear (Fig.16b).

13. On completion of entire message DRPCO clears TXIP and 25 ms later the System Controller disables transmitter via I²C.
14. System Controller finally sends TXRST to prepare DPROC for next transmission.

Note to the Access Attempt Procedure

At stage 1 the system controller may choose to preload DPROC with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC. Figure 17 illustrates the DPROC data transmission timing.

ABORT PROCEDURE (SEE FIG.18)

1. DPROC immediately disables transmitter output by driving TXCTRL LOW.
2. DPROC sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC for next transmission.

Note to the Abort Procedure

If a message is loaded into DPROC after a TXABRT has occured this word will remain in the DPROC transmit register and will not be cleared to TXRST.
If this situation arises the method of clearing the buffer ready for a second access attempt is to leave TXHOLD LOW and then send a TXRST prior to setting up a new transmission after TXLINE goes HIGH; this will clear any residual data in the buffer.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

ANALOG CIRCUIT BLOCKS

General

The analog signal processing functions on DPROC are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by distributed RC active filters, passive interpolators and comparators.

The distributed RC sections, the Anti-Alias Filter and the Clock Noise Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolators increase the sampling rate from 300 kHz to 1.2 MHz. The sampled analog signals from the Passive Interpolators are converted to sampled 2-state digital signals by the Strobed Comparators. The Gated Digital-to-Analog converters and Analog Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROC output signals, and conversion to the sampled analog domain.

These analog section of the device are shown in Fig.1.

Reference Voltage Generator

The Reference Voltage Generator generates the analog ground reference voltage (AGND) used internally within the DPROC device. To minimize noise AGND must be externally decoupled to V_{SSA} as shown in Fig.19.

Anti-Alias Filter

The Anti-Alias Filter is placed before the SAT sampling block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Alias Filter is a continuous time-distributed RC-active low-pass filter.

Table 8 Digital Colour Code; 7-bit word

DCC1	DCC0	Coded DCC						
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1
1	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	0	0
		DCC1			DCC0		DCC1.EXOR.DCC0	

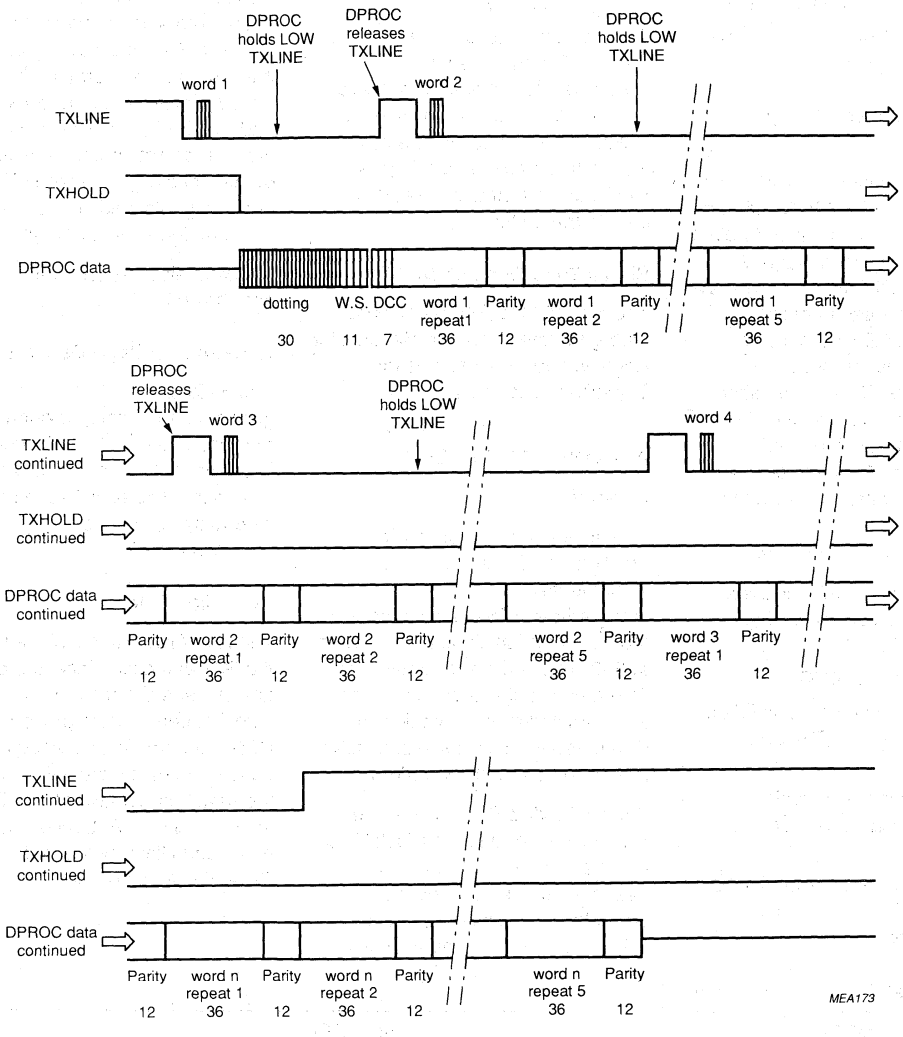


Fig.17 DPROC data transmission timing/microcontroller interface.

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the switched-capacitor filters. This reduces the coarseness of the zero-crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Strobed Comparators

The Strobed Comparators form the analog-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers which convert the filtered sampled analog signals into 2-state sampled digital signals containing only the zero-crossing information from the analog signal.

Gated Digital-to-Analog and Analog Summer

The Gated Digital-to-Analog converters and Analog Summer form the interface between the digital and analog circuitry on the transmit path of DPROC. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal.
The data streams are enabled by the I²C signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analog conversion and sub-sampling operation is performed by the Gated Digital-to-Analog converters and Analog Summer. The relative signal weights applied in the summer (with respect to the data path) are shown in Table 9.

Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC coupling from the DATA pin.

Clock Noise Filter

The filter is a non-critical continuous time-distributed RC-active low-pass filter used to remove any switching transient residues from the output signal.

Table 9 Relative signal weights

SIGNAL	RELATIVE OUTPUT LEVEL AMPS AND TACS
ST	1.0
SAT	0.25
DATA	1.0

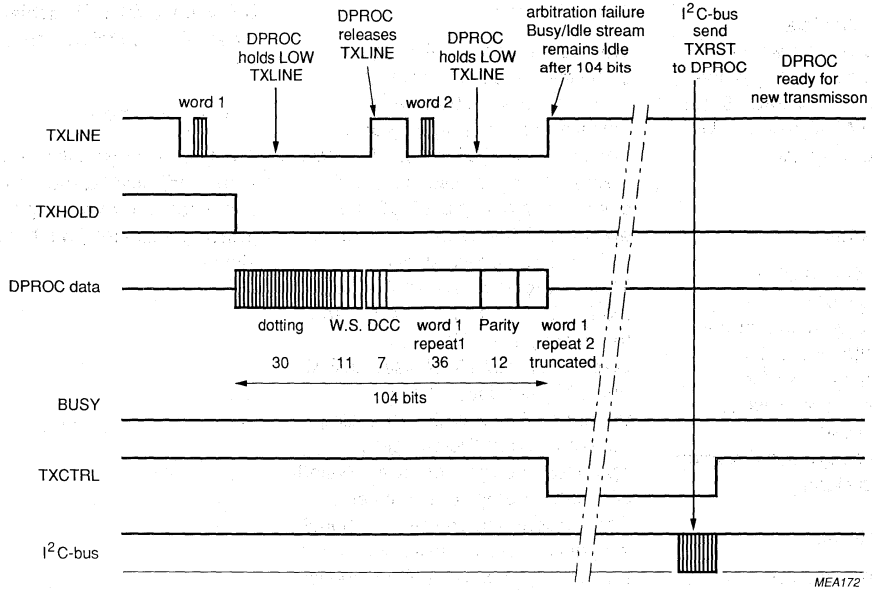


Fig.18 DPROC data transmission timing/microcontroller interface during arbitration failure.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

APPLICATION INFORMATION

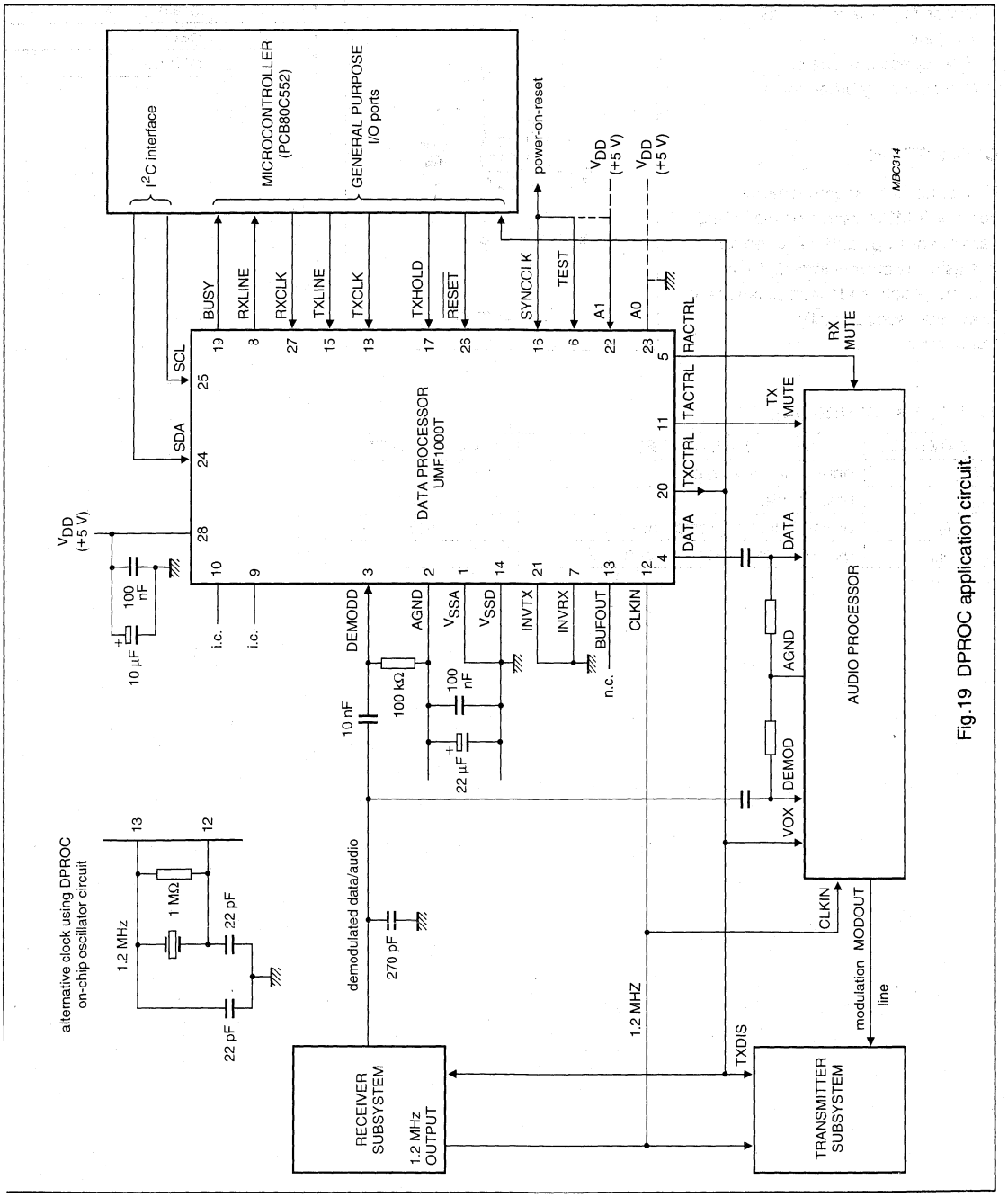


Fig.19 DPROC application circuit.

N-channel enhancement mode vertical D-MOS transistor

VN2406L

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and designed for use as a line current interrupter in telephone sets and for applications in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

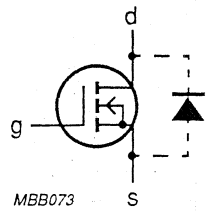


Fig.1 Symbol.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	drain current	210	mA
$R_{DS(on)}$	drain-source on-resistance	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

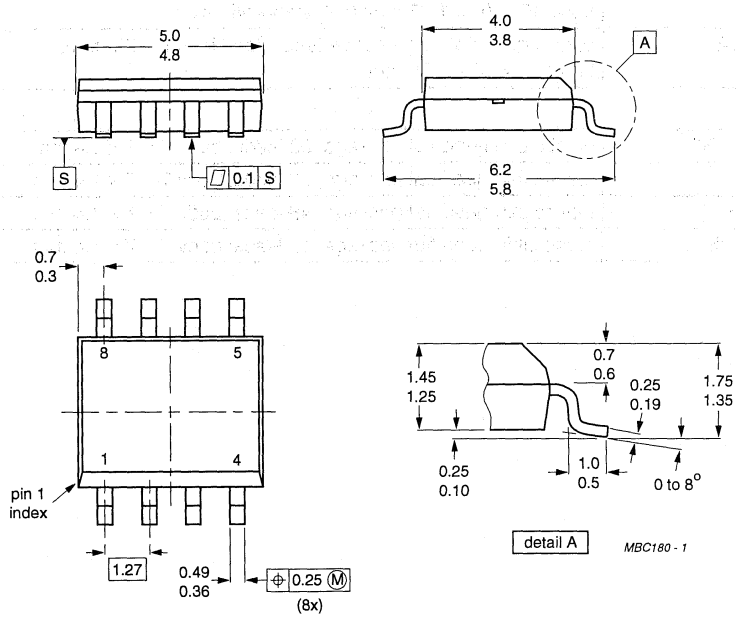
PACKAGE INFORMATION

INDEX

Package information — Package outlines

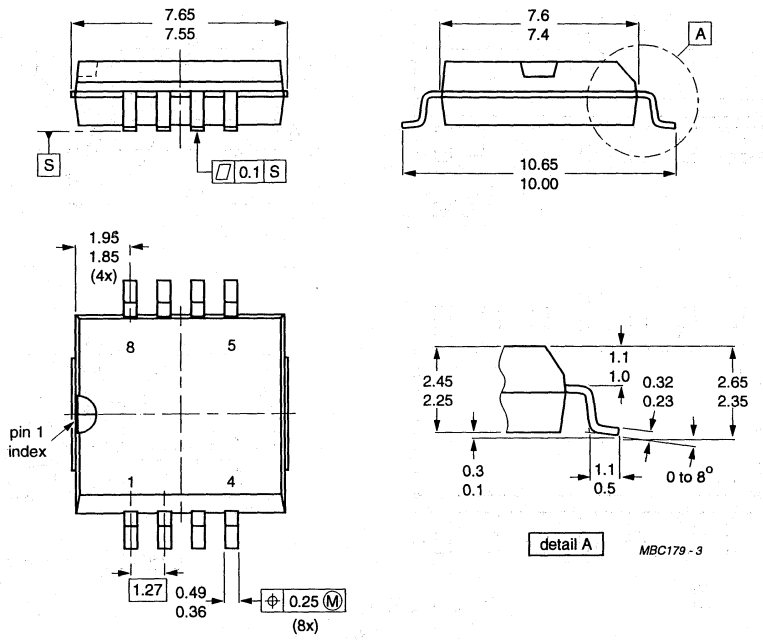
PACKAGE VERSIONS	DESCRIPTION	PAGE
QFP		
SOT205-1/SOT205AG	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	1627
SOT307-1	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm; high stand-off height	1628
SOT208-1/SOT208A	plastic quad flat package; 64 leads (lead length 2.35 mm); body 14 × 20 × 2.75 mm	1629
TQFP		
SOT358-1/SOT358BB3	plastic thin quad flat package; 32 leads; body 7 × 7 × 1.4 mm	1630
SOT358-2	plastic thin quad flat package; 32 leads; body 7 × 7 × 1.4 mm	1631
SOT313-1/1706B (BE)	plastic thin quad flat package; 48 leads; body 7 × 7 × 1.4 mm	1632
SOT313-2/1706A (BE)	plastic thin quad flat package; 48 leads; body 7 × 7 × 1.4 mm	1633

SO



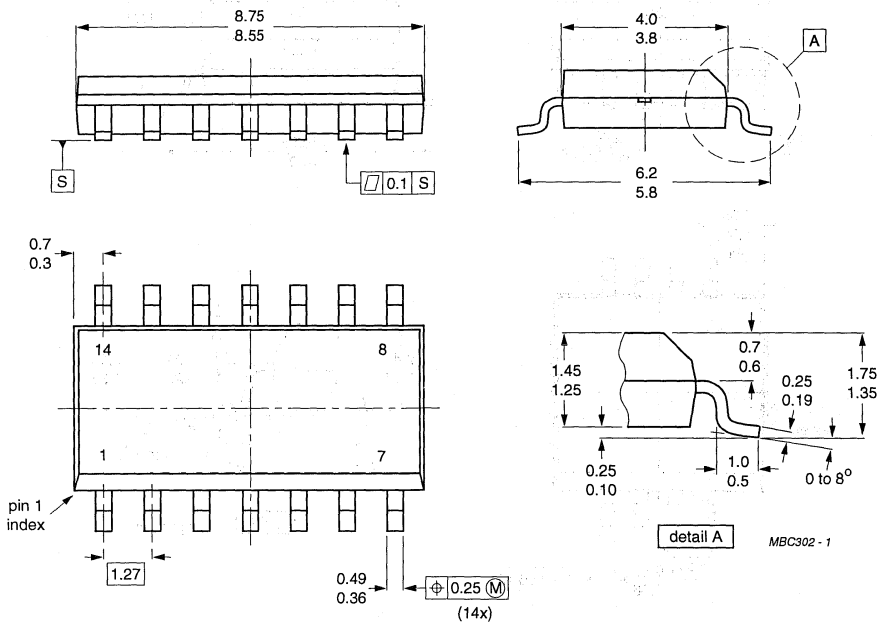
Dimensions in mm.

Fig.1 Plastic small outline package; 8 leads; body width 3.9 mm (SO8; SOT96-1).



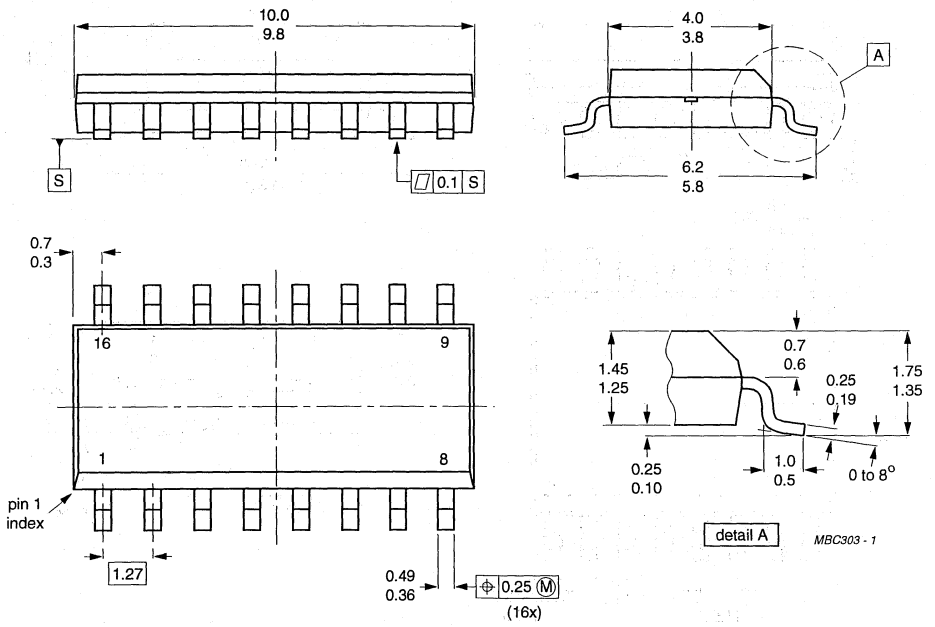
Dimensions in mm.

Fig.2 Plastic small outline package; 8 leads; body width 7.5 mm (SO8; SOT176-1).



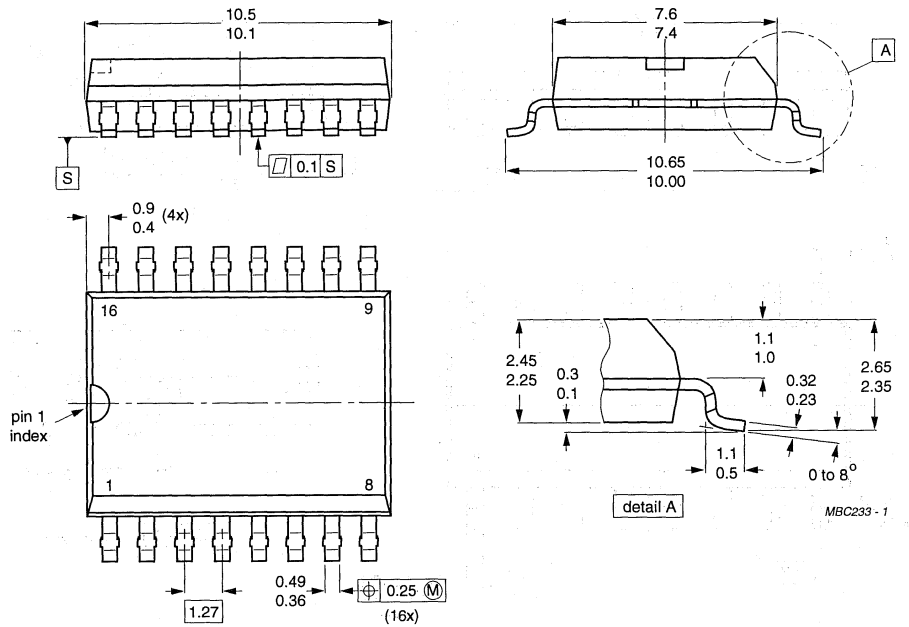
Dimensions in mm.

Fig.3 Plastic small outline package; 14 leads; body width 3.9 mm (SO14; SOT108-1).



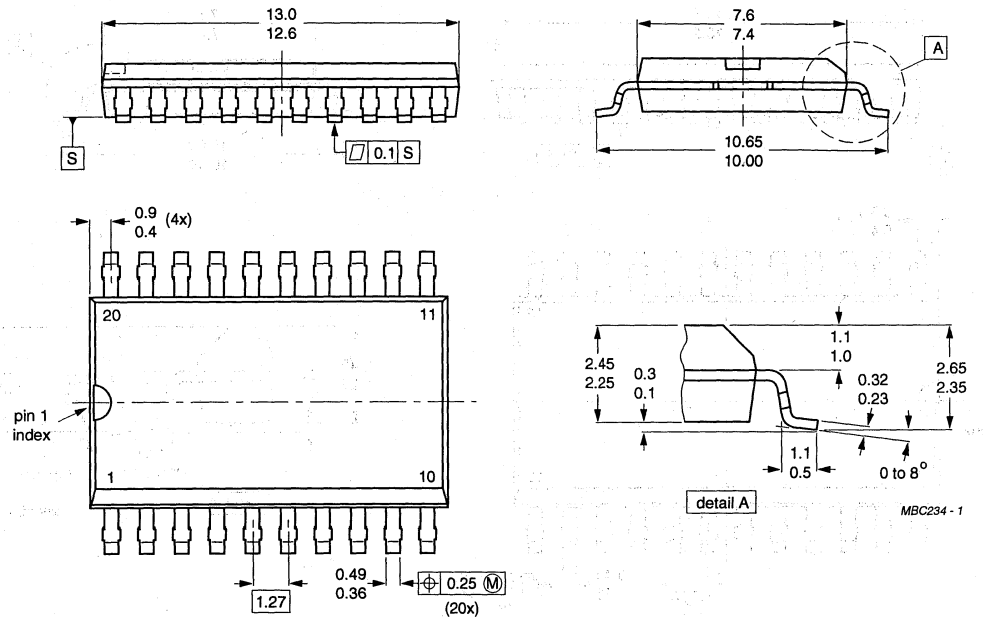
Dimensions in mm.

Fig.4 Plastic small outline package; 16 leads; body width 3.9 mm (SO16; SOT109-1).



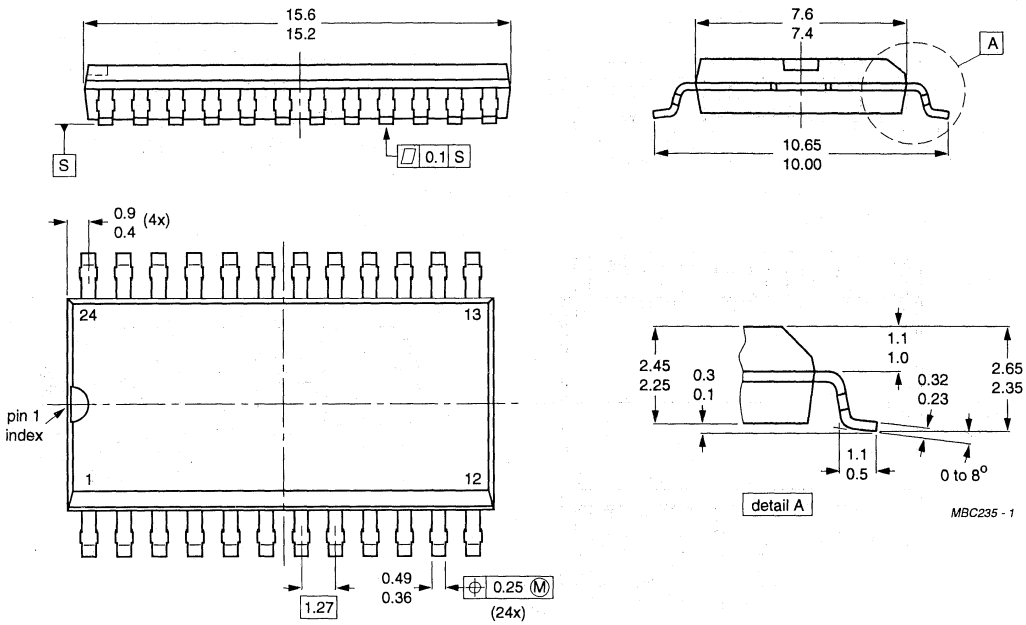
Dimensions in mm.

Fig.5 Plastic small outline package; 16 leads; body width 7.5 mm (SO16; SOT162-1).



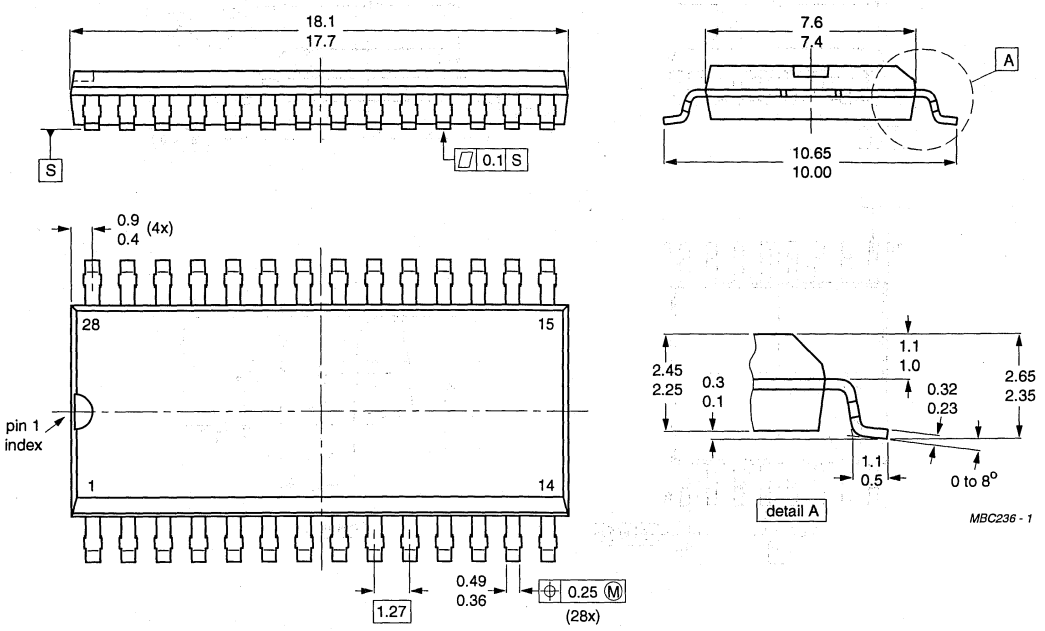
Dimensions in mm.

Fig.6 Plastic small outline package; 20 leads; body width 7.5 mm (SO20; SOT163-1).



Dimensions in mm.

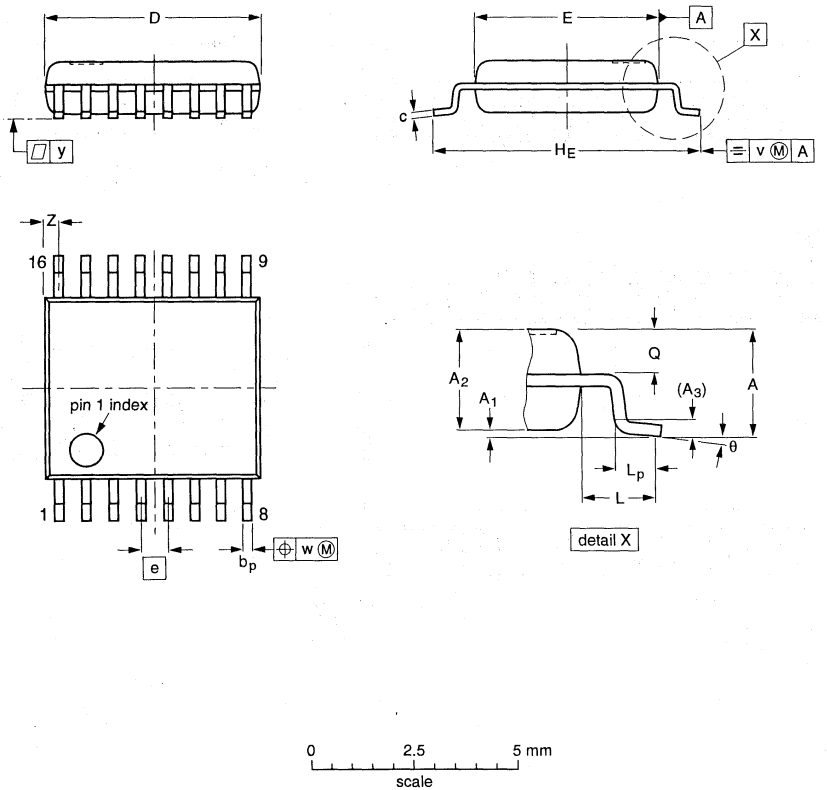
Fig.7 Plastic small outline package; 20 leads; body width 7.5 mm (SO20; SOT137-1).



Dimensions in mm.

Fig.8 Plastic small outline package; 28 leads; body width 7.5 mm (SO28; SOT136-1).

SSOP



DIMENSIONS (mm are the controlling dimensions)

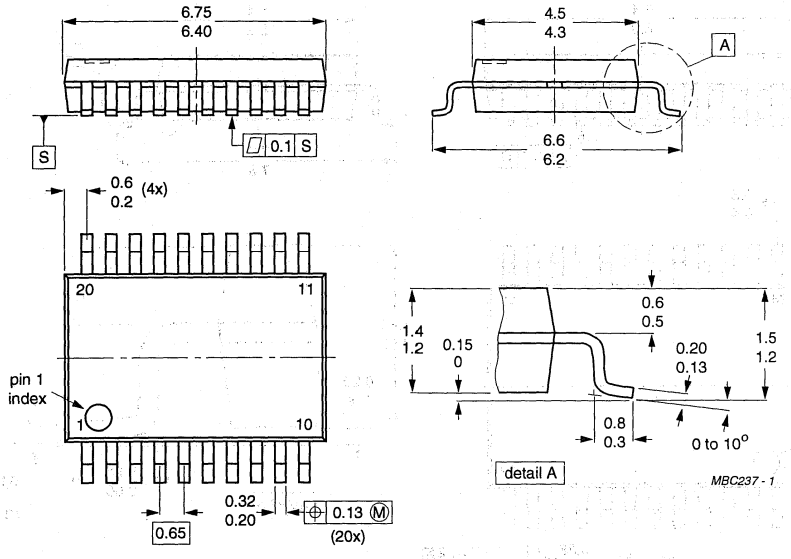
UNIT	A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5 1.2	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

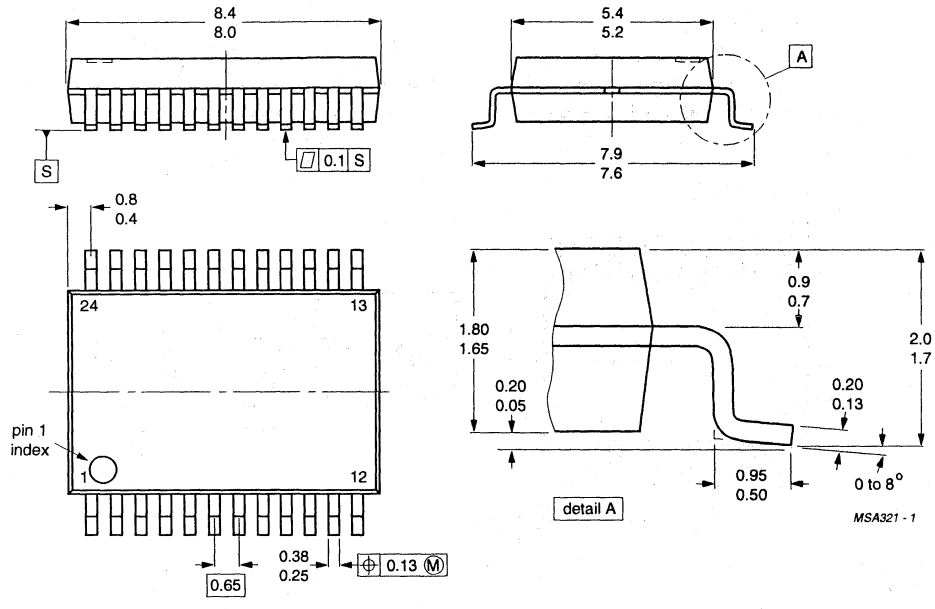
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1						~~94-04-20~~ 94-10-28

Fig.9 Plastic shrink small outline package; 16 leads; body width 4.4 mm (SSOP16; SOT369-1).



Dimensions in mm.

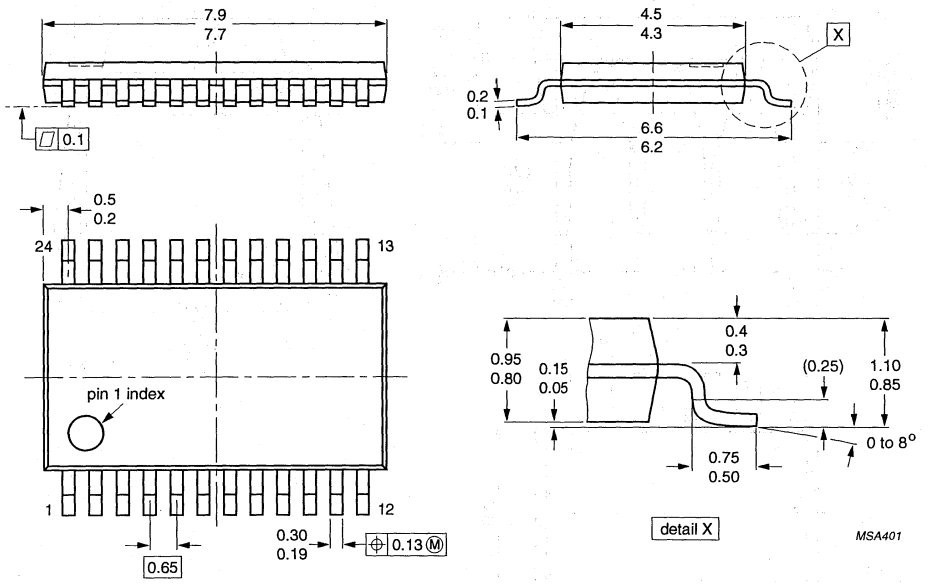
Fig.10 Plastic shrink small outline package; 20 leads; body width 4.4 mm (SSOP20; SOT266-1).



Dimensions in mm.

Fig.11 Plastic shrink small outline package; 24 leads; body width 5.3 mm (SSOP24; SOT340-1).

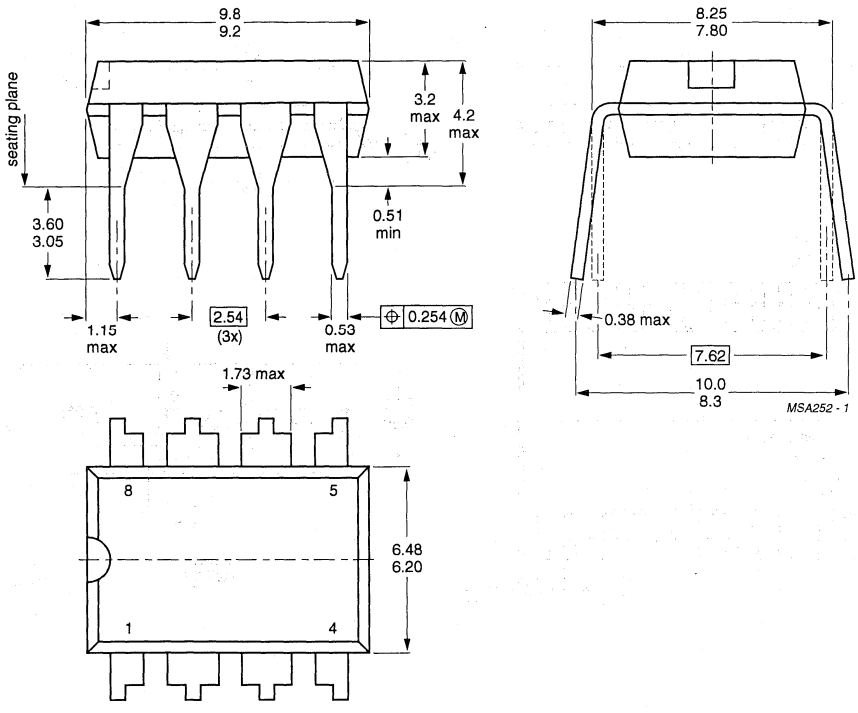
TSSOP



Also valid for SA639.
Dimensions in mm.

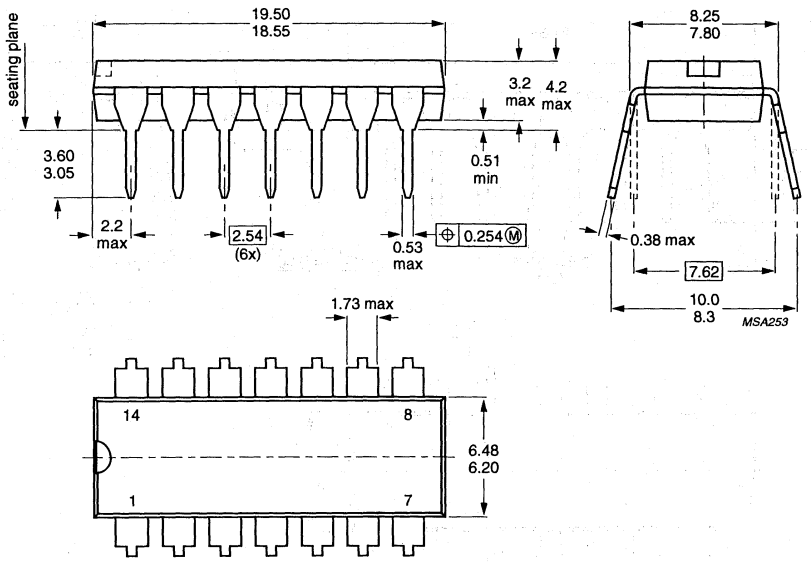
Fig.12 Plastic thin shrink small outline package; 24 leads; body width 4.4 mm (TSSOP24; SOT355-1).

DIP



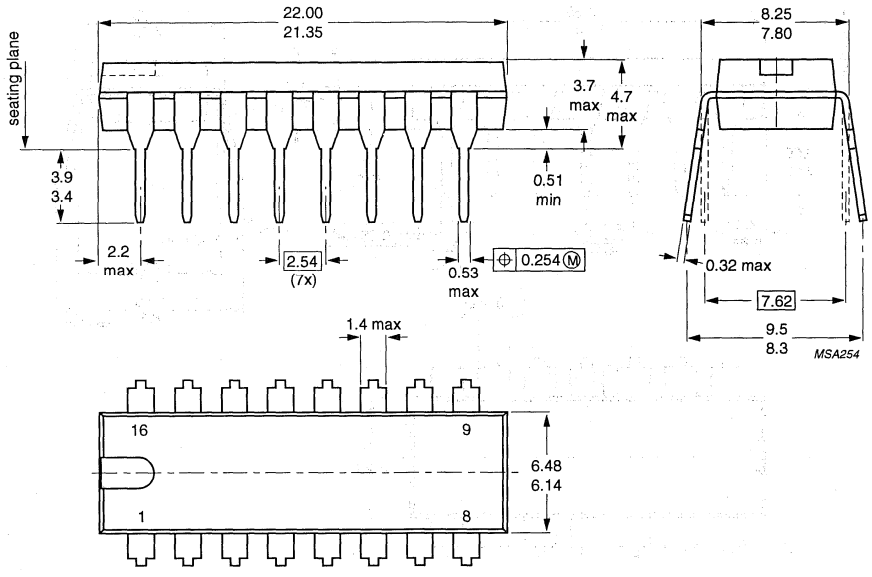
Dimensions in mm.

Fig.13 Plastic dual in-line package; 8 leads (300 mil); DIP8; SOT97-1.



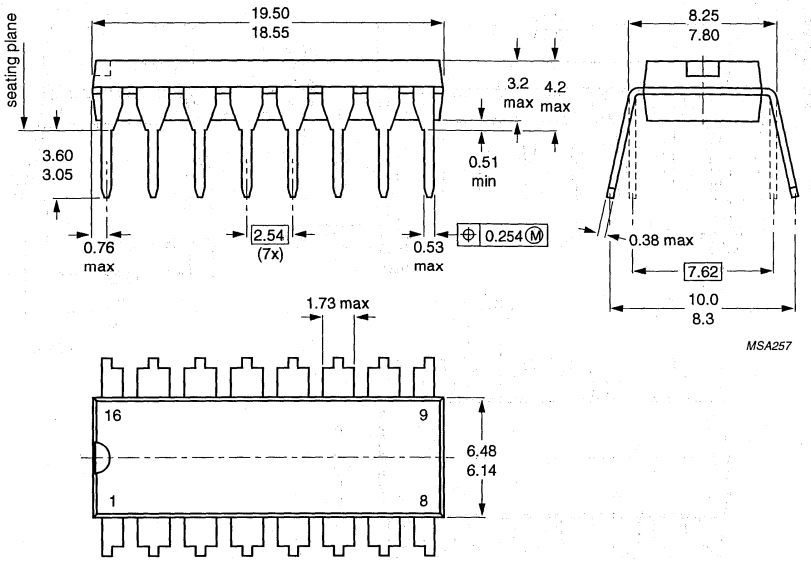
Dimensions in mm.

Fig.14 Plastic dual in-line package; 14 leads (300 mil); DIP14; SOT27-1.



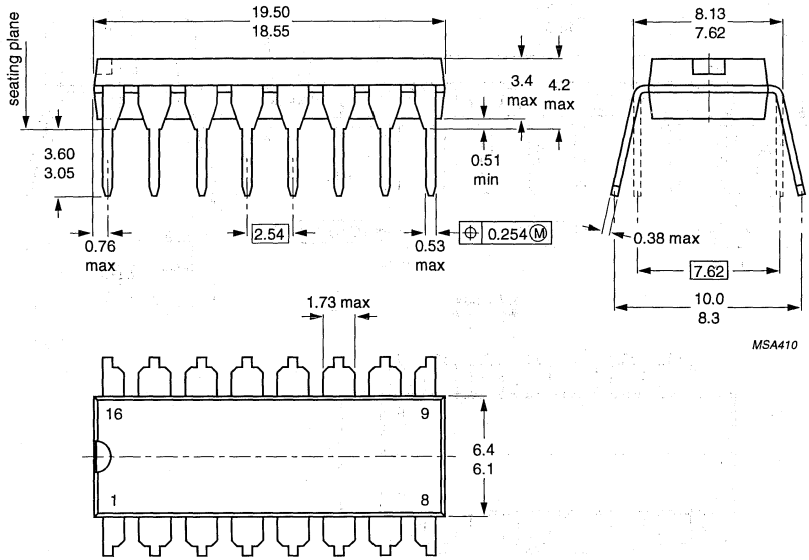
Dimensions in mm.

Fig.15 Plastic dual in-line package; 16 leads (300 mil); DIP16; SOT38-1.



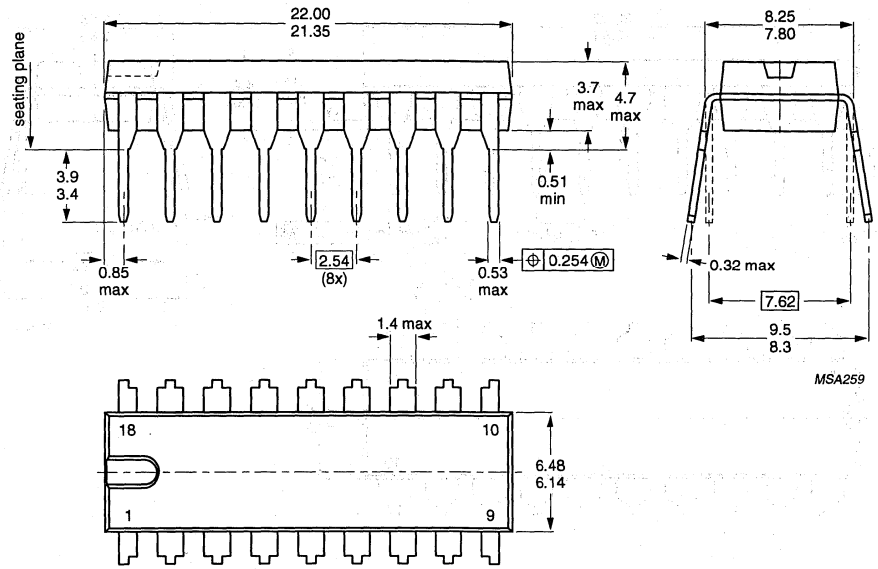
Dimensions in mm.

Fig.16 Plastic dual in-line package; 16 leads (300 mil); long body; DIP16; SOT38-4.



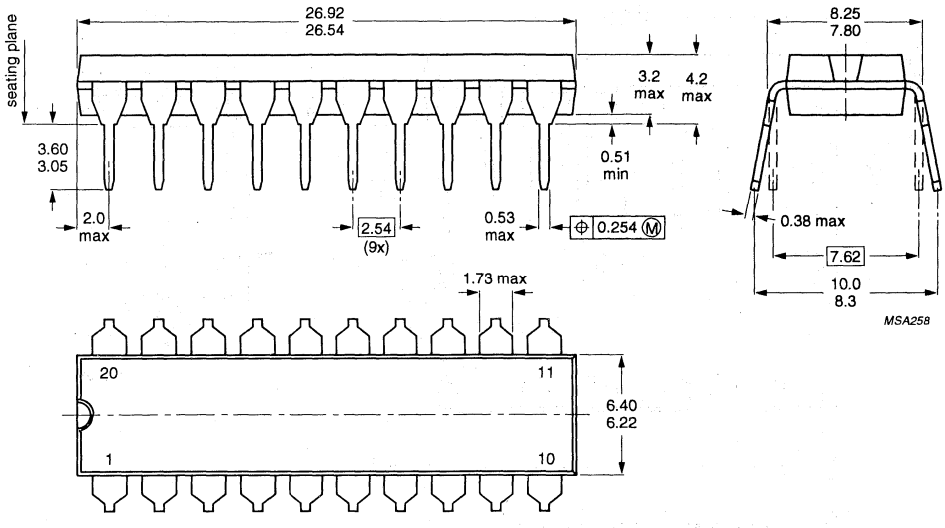
Dimensions in mm.

Fig.17 Plastic dual in-line package; 16 leads (300 mil); DIP16; SOT38-8.



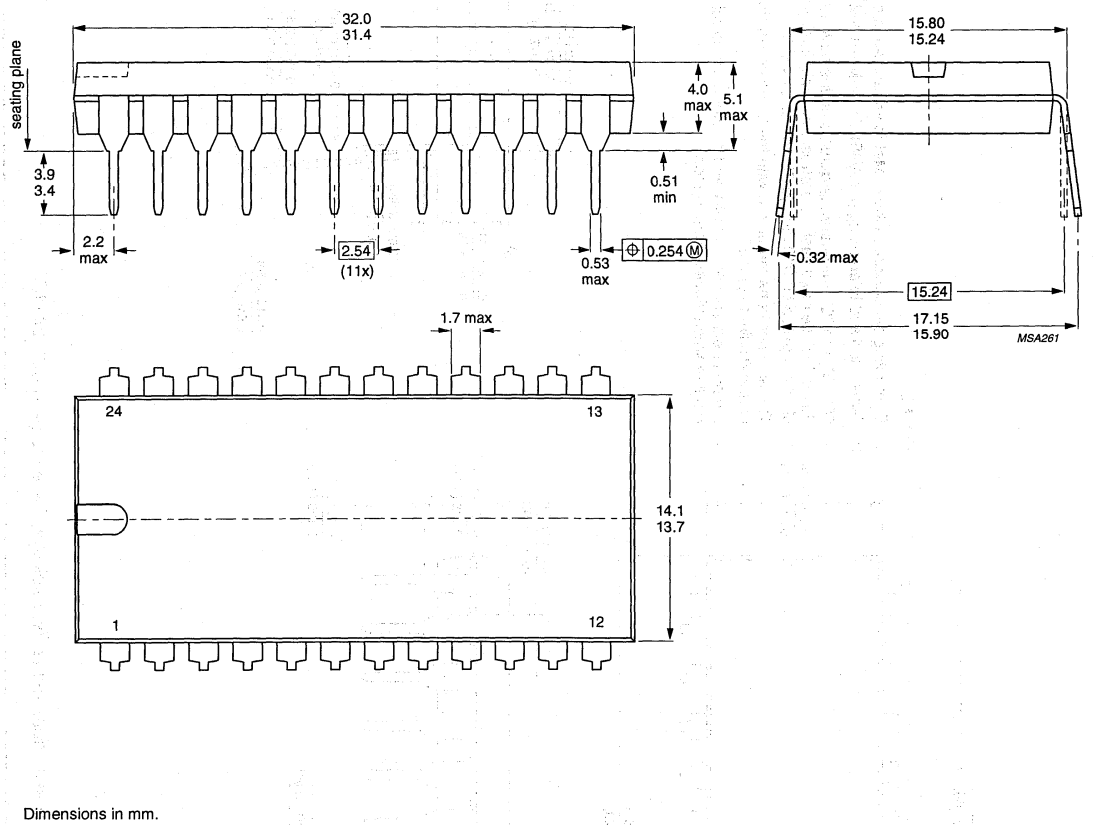
Dimensions in mm.

Fig.18 Plastic dual in-line package; 18 leads (300 mil); DIP18; SOT102-1.



Dimensions in mm.

Fig.19 Plastic dual in-line package; 20 leads (300 mil); DIP20; SOT146-1.



Dimensions in mm.

Fig.20 Plastic dual in-line package; 24 leads (600 mil); DIP24; SOT101-1.

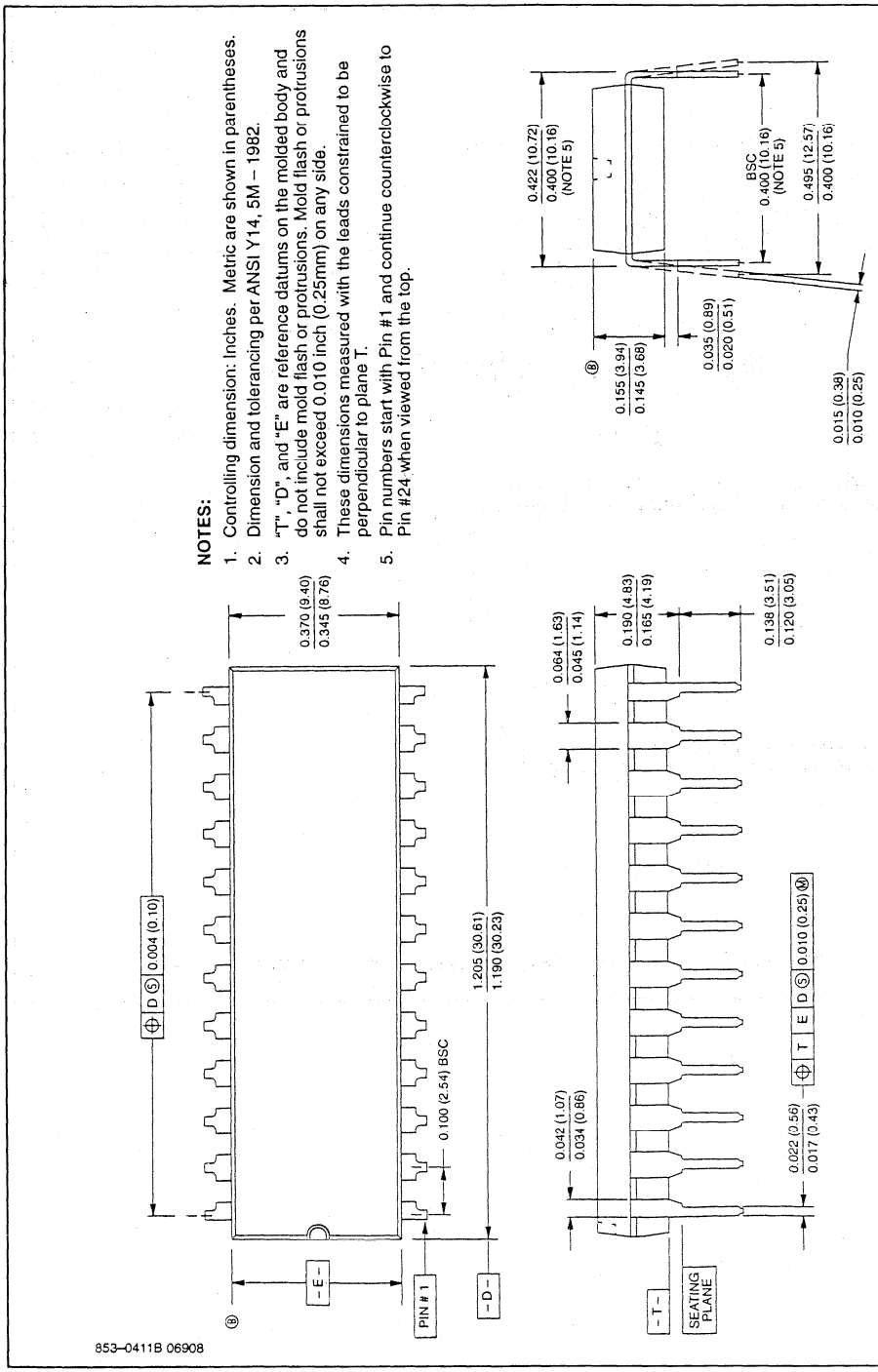
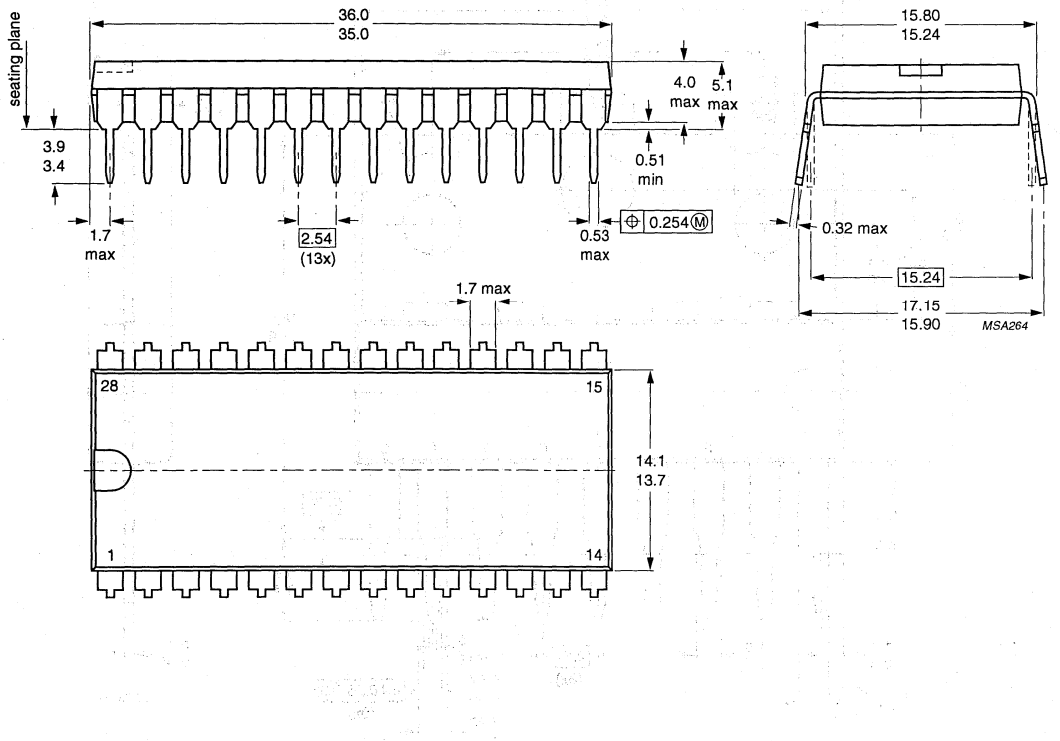


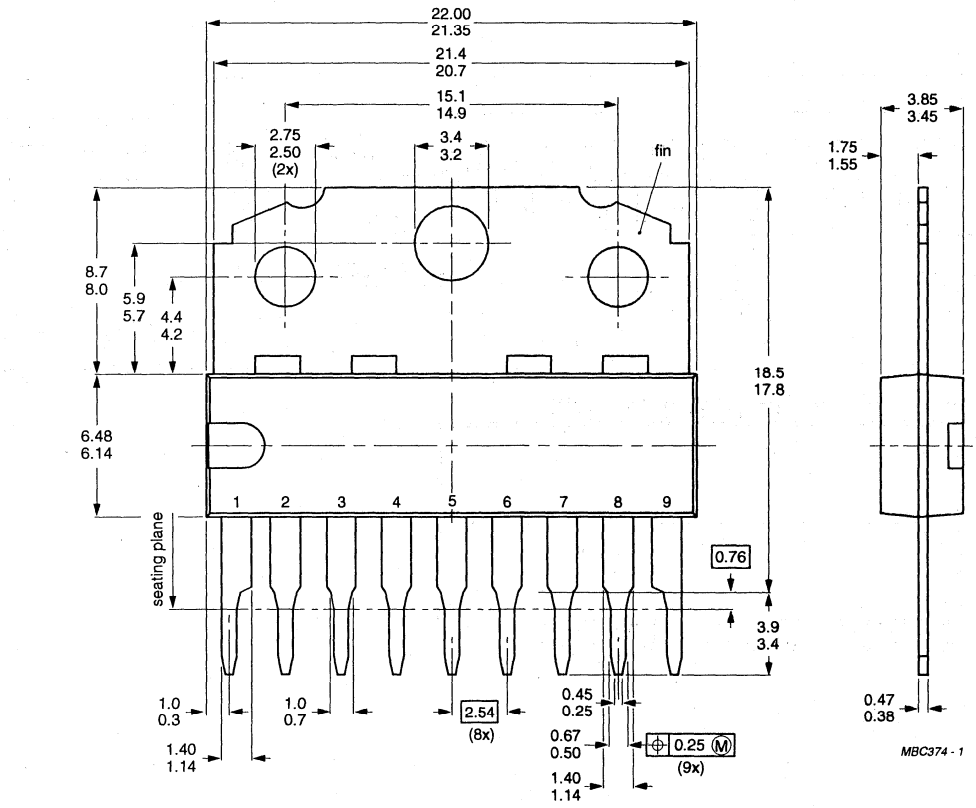
Fig.21 Plastic dual in-line (N) package; 24 leads (400 mil); 0411B.



Dimensions in mm.

Fig.22 Plastic dual in-line package; 28 leads (600 mil); DIP28; SOT117-1.

SIL



Dimensions in mm.

Fig.23 Plastic single in-line medium power package with fin; 9 leads; SIL9MPF; SOT110-1.

CERDIP

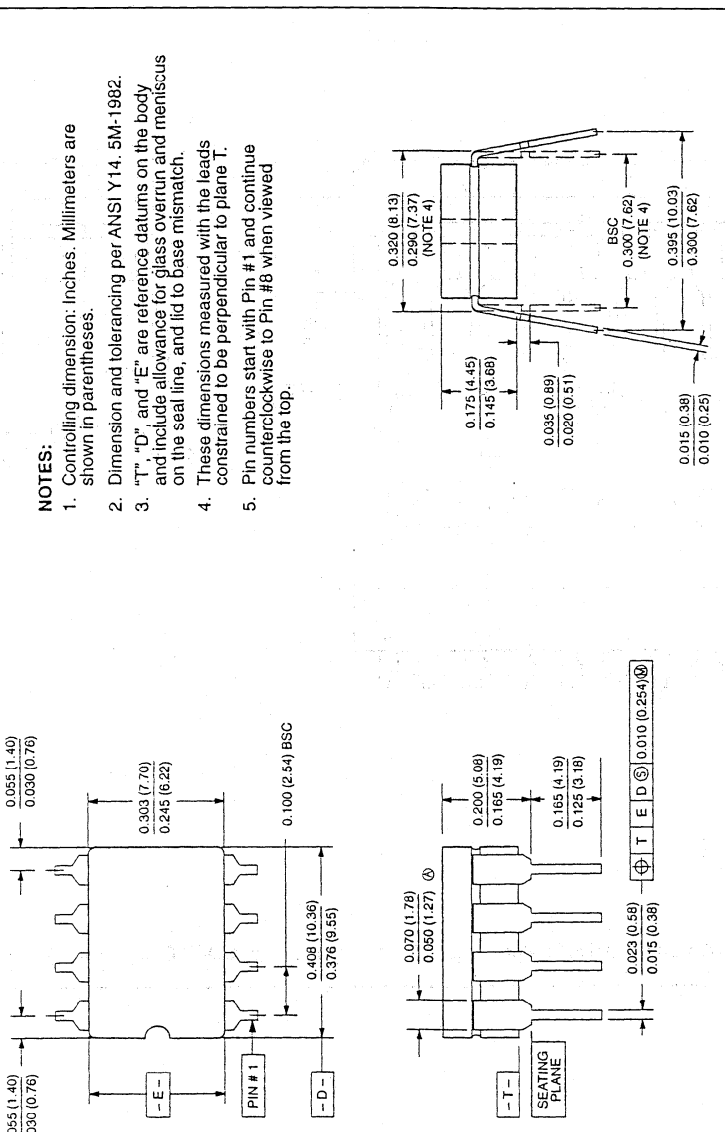
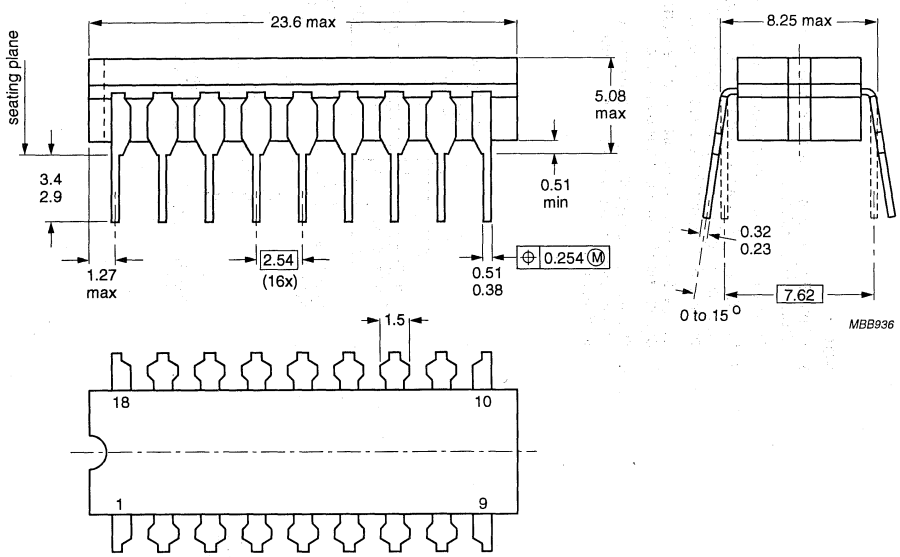


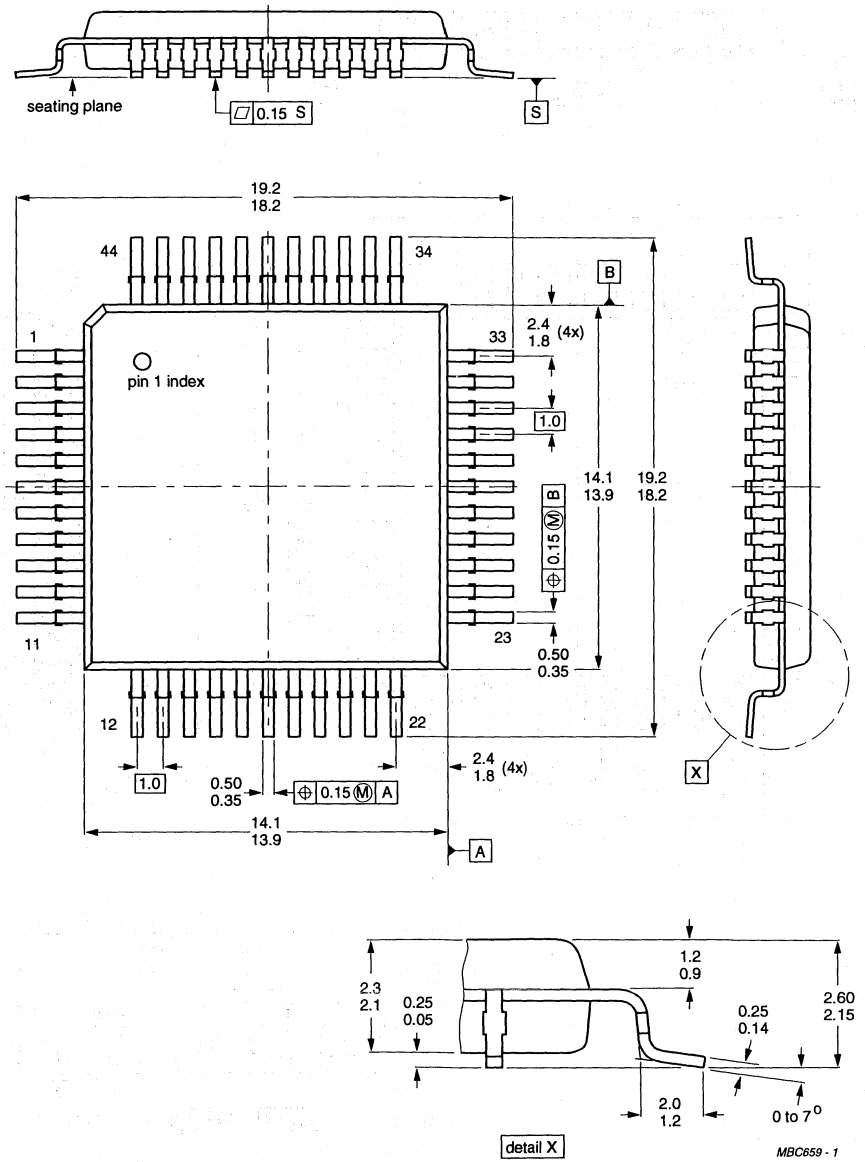
Fig.24 Ceramic dual in-line (F) package; 8 leads (300 mil); 0580A.



Dimensions in mm.

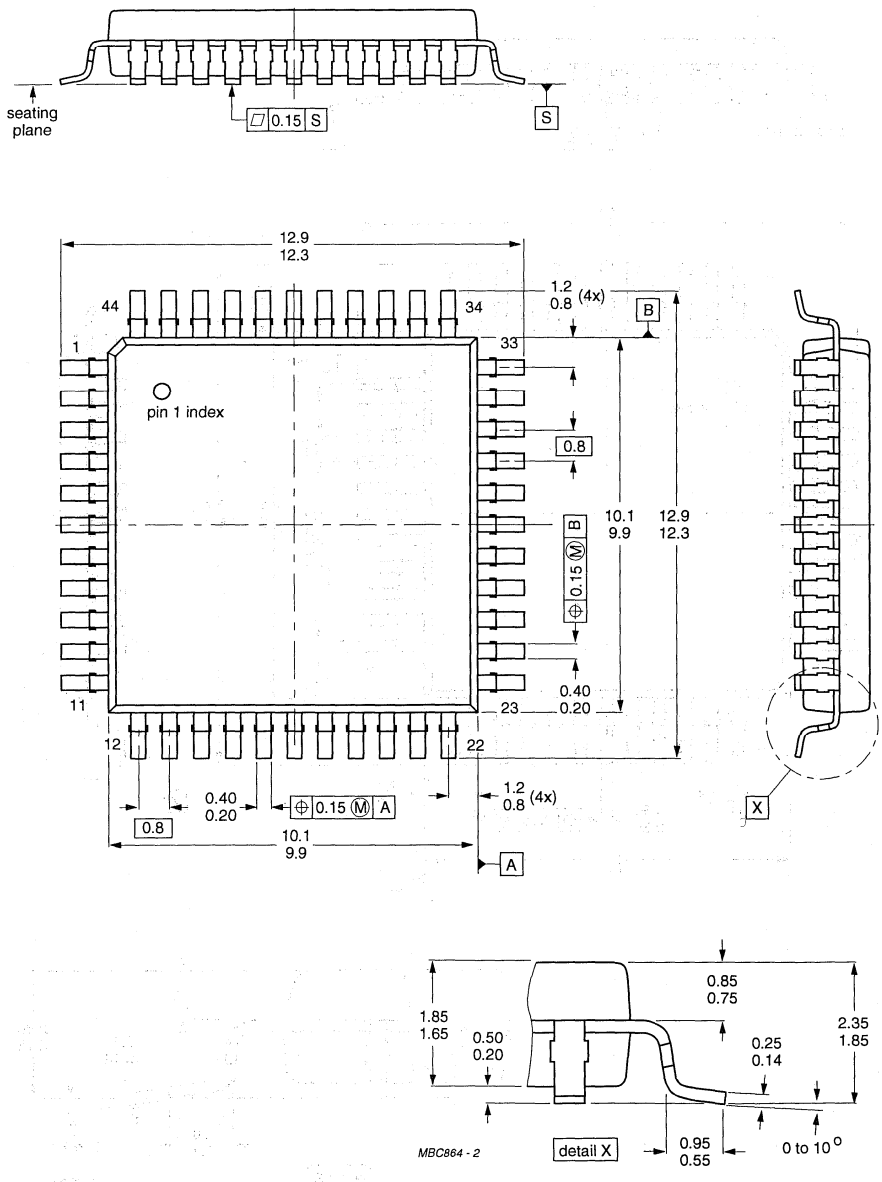
Fig.25 Ceramic dual in-line package; 18 leads; glass seal (CDIP18; SOT133-1).

QFP



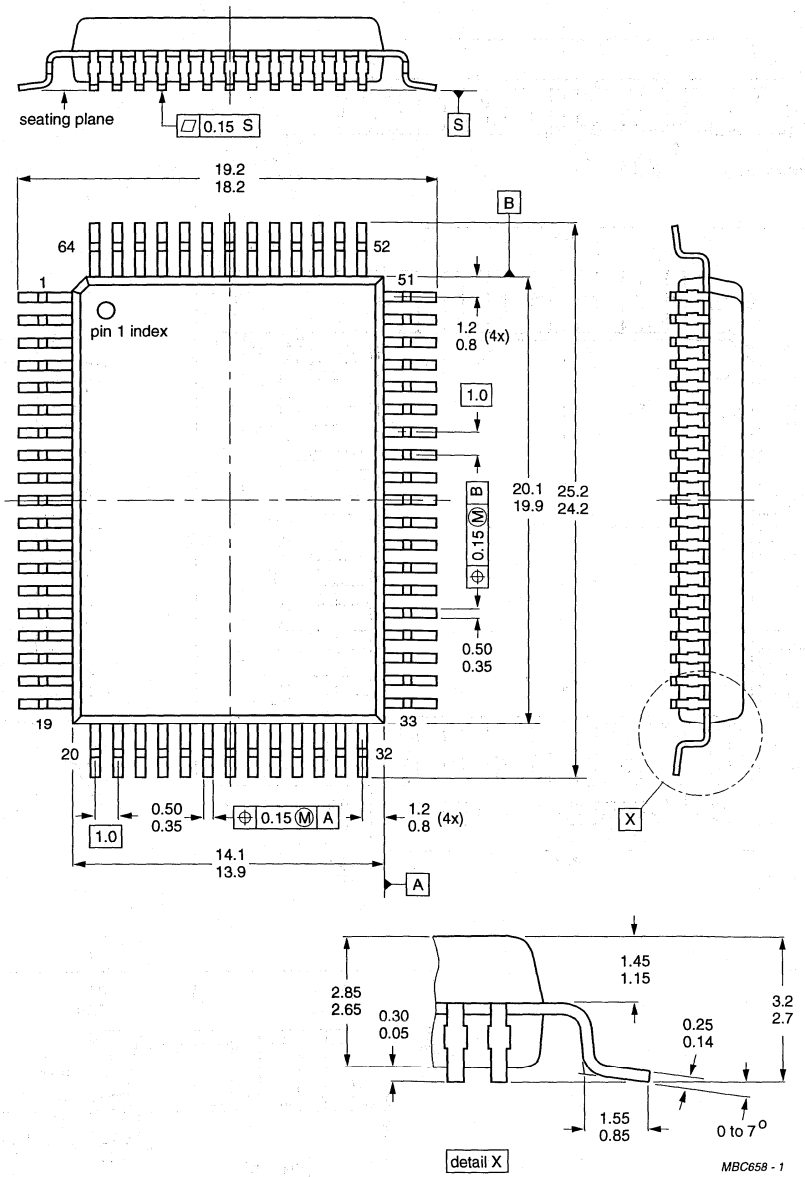
Dimensions in mm.

Fig.26 Plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm (QFP44; SOT205-1).



Dimensions in mm.

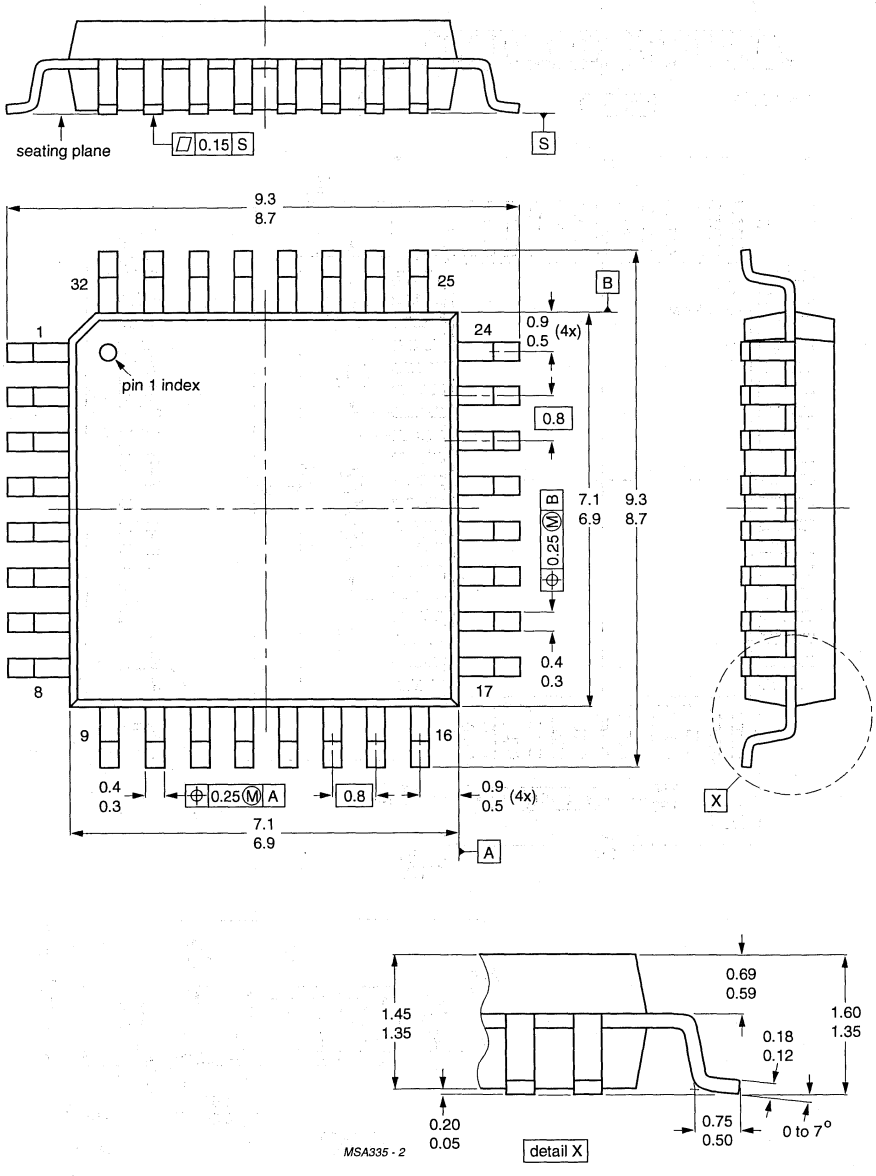
Fig.27 Plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm; high stand-off height (QFP44; SOT307-1).



Dimensions in mm.

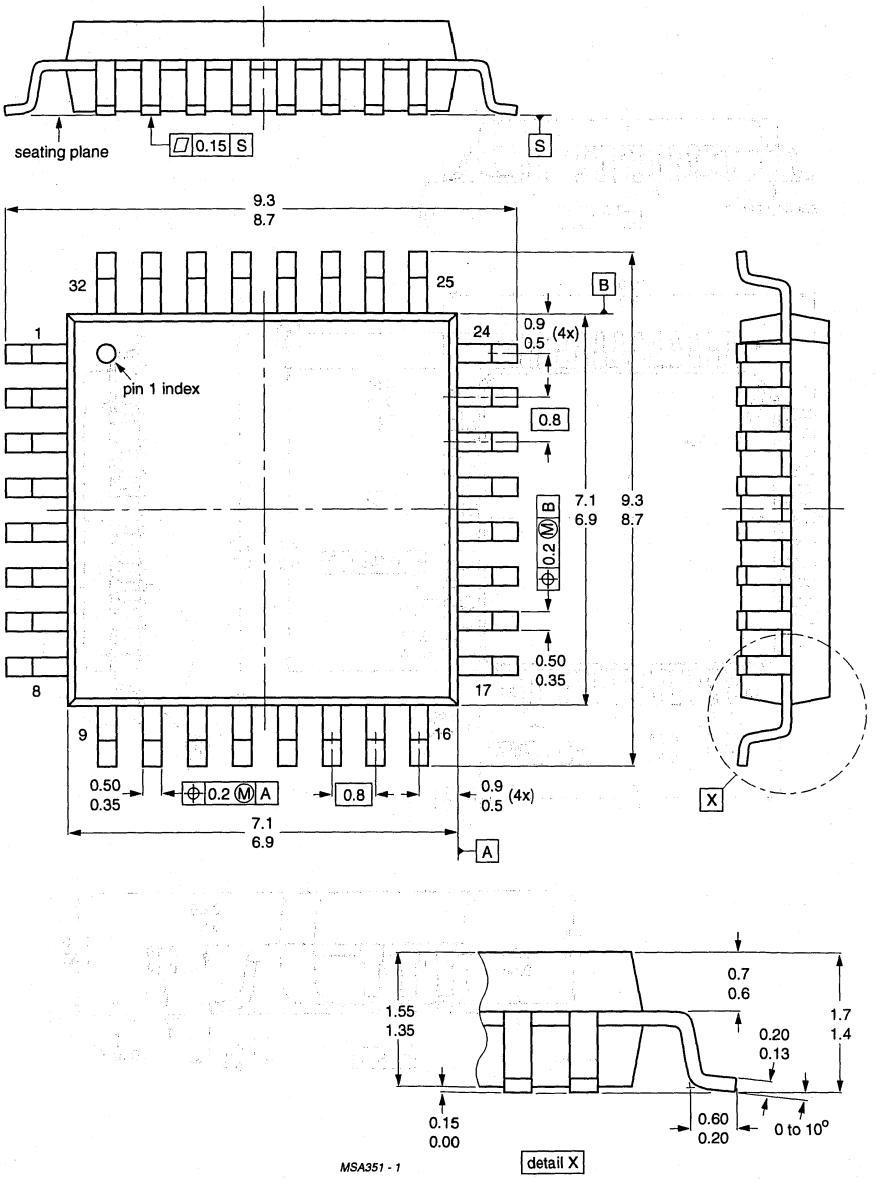
Fig.28 Plastic quad flat package; 64 leads (lead length 2.35 mm); body 14 × 20 × 2.75 mm (QFP64; SOT208-1).

TQFP



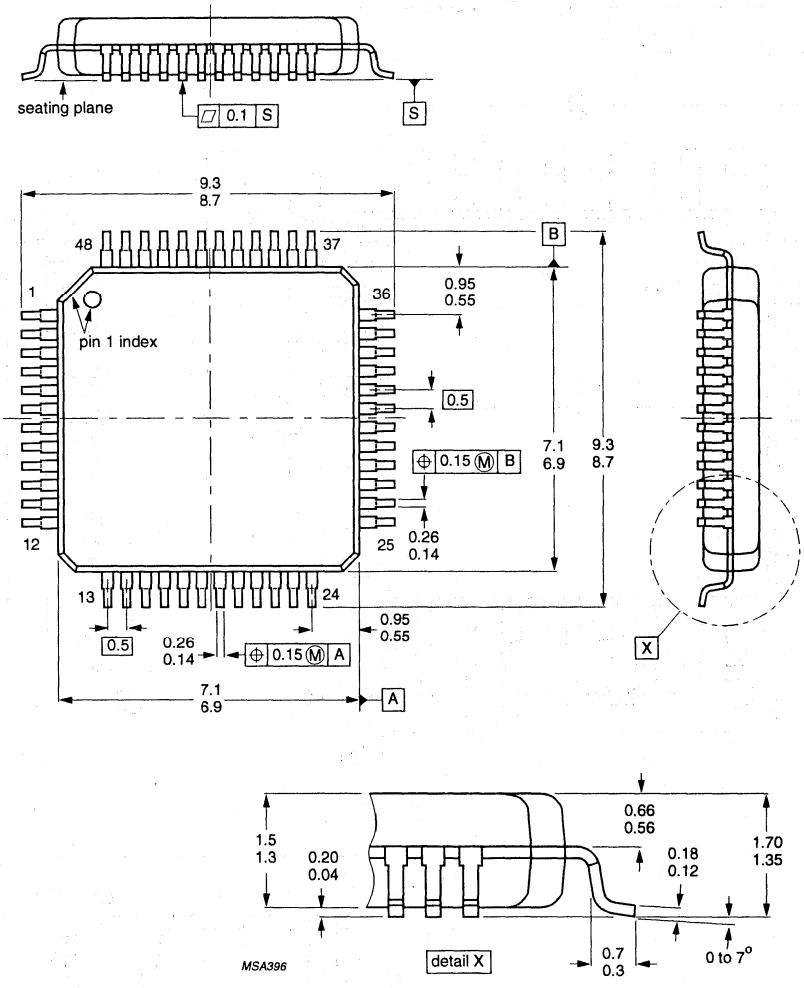
Dimensions in mm.

Fig.29 Plastic thin quad flat package; 32 leads; body 7 × 7 × 1.4 mm (TQFP32; SOT358-1).



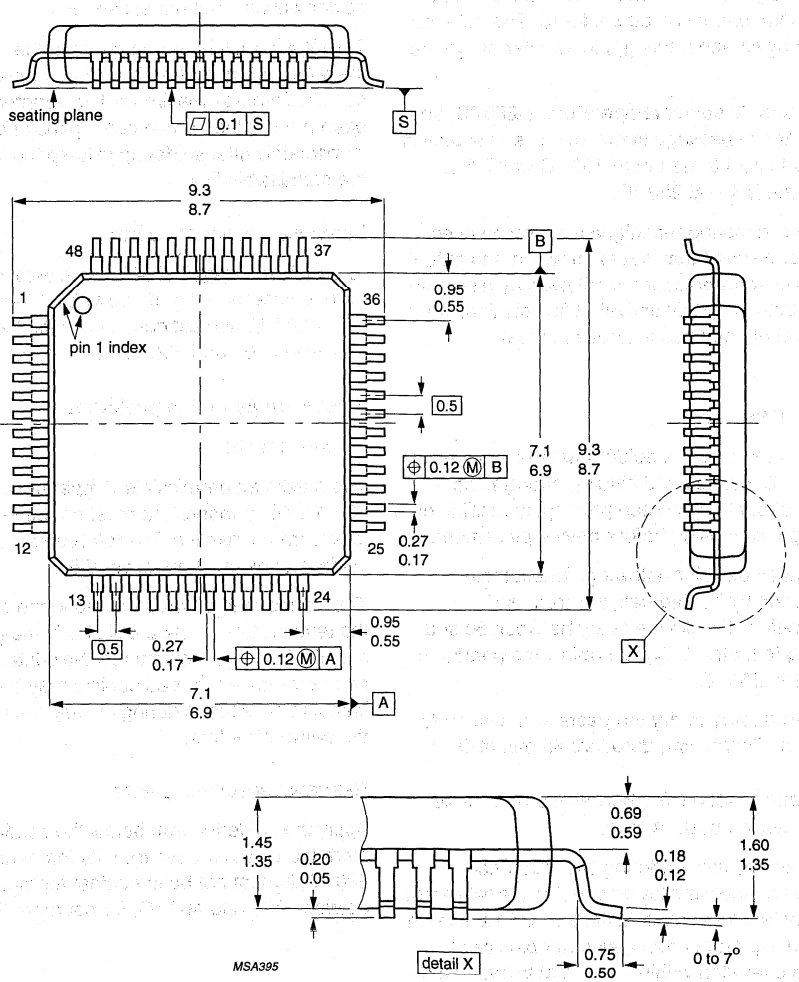
Dimensions in mm.

Fig.30 Plastic thin quad flat package; 32 leads; body 7 × 7 × 1.4 mm (TQFP32; SOT358-2).



Dimensions in mm.

Fig.31 Plastic thin quad flat package; 48 leads; body 7 × 7 × 1.4 mm (TQFP48; SOT313-1).



Dimensions in mm.

Fig.32 Plastic thin quad flat package; 48 leads; body 7 × 7 × 1.4 mm (TQFP48; SOT313-2).

SOLDERING

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic single in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

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Data handbook system

DATA HANDBOOK SYSTEM

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